

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4040B**

## **MSI**

## **12-stage binary counter**

Product specification  
File under Integrated Circuits, IC04

January 1995

# 12-stage binary counter

# HEF4040B MSI

## DESCRIPTION

The HEF4040B is a 12-stage binary ripple counter with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs ( $O_0$  to  $O_{11}$ ). The counter advances on the HIGH to LOW transition of  $\overline{CP}$ . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of  $\overline{CP}$ . Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

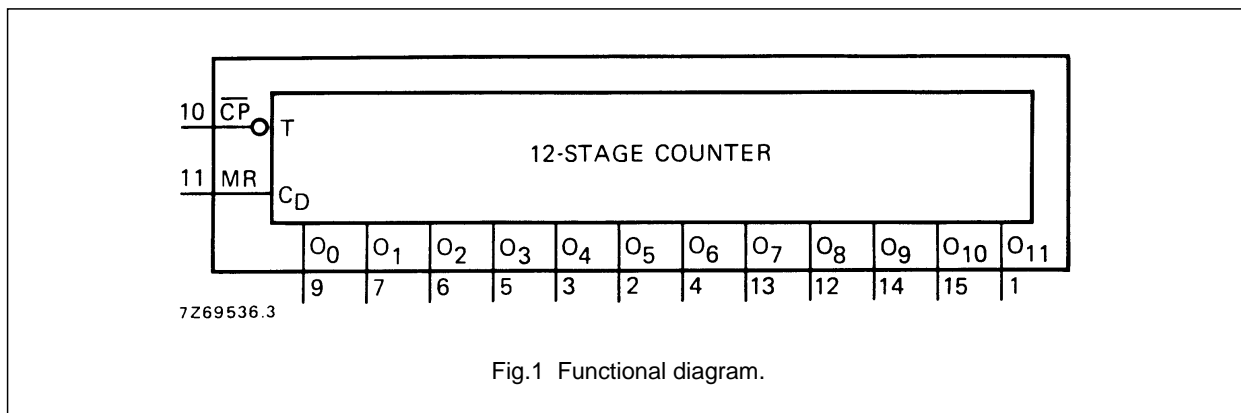


Fig.1 Functional diagram.

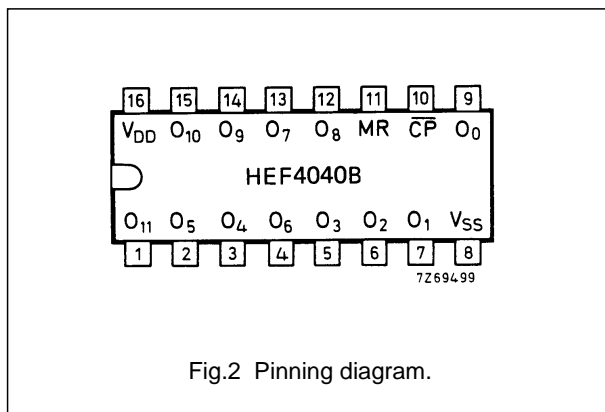


Fig.2 Pinning diagram.

## PINNING

- $\overline{CP}$  clock input (HIGH to LOW edge-triggered)
- MR master reset input (active HIGH)
- $O_0$  to  $O_{11}$  parallel outputs

## APPLICATION INFORMATION

Some examples of applications for the HEF4040B are:

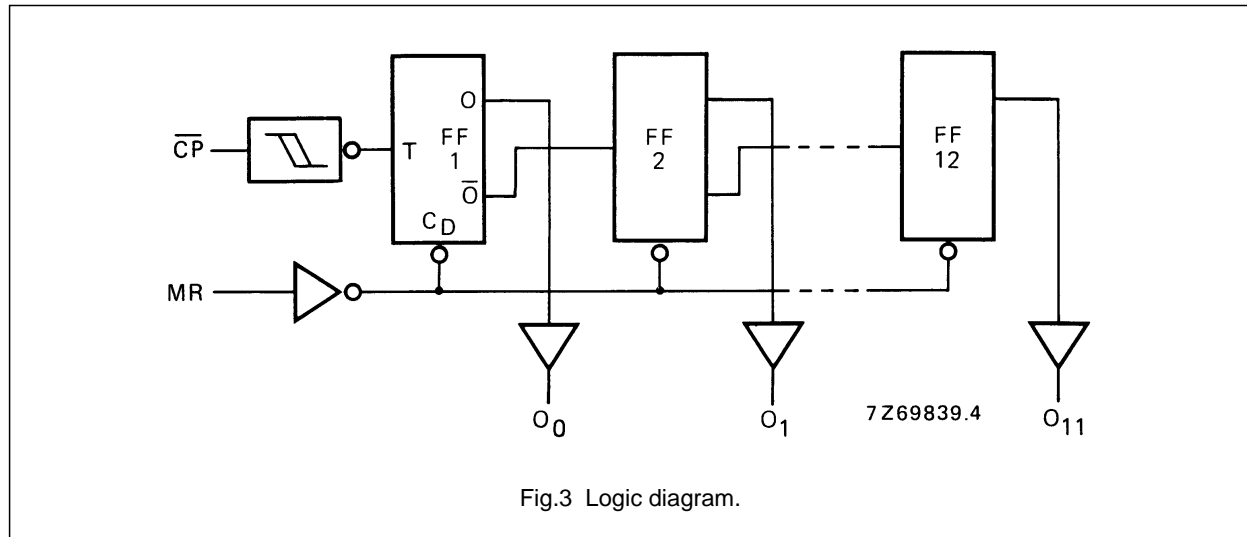
- Frequency dividing circuits
- Time delay circuits
- Control counters

## FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

- HEF4040BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4040BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4040BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

## 12-stage binary counter

HEF4040B  
MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays $\overline{CP} \rightarrow O_0$ HIGH to LOW	5	$t_{PHL}$		105	210	ns	78 ns + (0,55 ns/pF) $C_L$	
	10		45	90	ns	34 ns + (0,23 ns/pF) $C_L$		
	15		35	70	ns	27 ns + (0,16 ns/pF) $C_L$		
	LOW to HIGH	5	$t_{PLH}$		85	170	ns	58 ns + (0,55 ns/pF) $C_L$
		10		40	80	ns	29 ns + (0,23 ns/pF) $C_L$	
		15		30	60	ns	22 ns + (0,16 ns/pF) $C_L$	
	$O_n \rightarrow O_{n+1}$ HIGH to LOW	5	$t_{PHL}$		35	70	ns	note 1 (0,55 ns/pF) $C_L$
		10		15	30	ns	note 1 (0,23 ns/pF) $C_L$	
		15		10	20	ns	note 1 (0,16 ns/pF) $C_L$	
LOW to HIGH		5	$t_{PLH}$		35	70	ns	note 1 (0,55 ns/pF) $C_L$
		10		15	30	ns	note 1 (0,23 ns/pF) $C_L$	
		15		10	20	ns	note 1 (0,16 ns/pF) $C_L$	
MR $\rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		90	180	ns	63 ns + (0,55 ns/pF) $C_L$	
	10		40	80	ns	29 ns + (0,23 ns/pF) $C_L$		
	15		30	60	ns	22 ns + (0,16 ns/pF) $C_L$		
Output transition times HIGH to LOW	5	$t_{THL}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$	
	10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$		
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$		
	LOW to HIGH	5	$t_{TLH}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$
		10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$	
		15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$	

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	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum clock pulse width; HIGH	5	t <sub>WCPH</sub>	50	25	ns	see also waveforms Fig.4
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t <sub>WMRH</sub>	40	20	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t <sub>RMR</sub>	40	20	ns	
	10		30	15	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f <sub>max</sub>	10	20	MHz	
	10		15	30	MHz	
	15		25	50	MHz	

**Note**

- For other loads than 50 pF at the n<sup>th</sup> output, use the slope given.

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$400 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load cap. (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)
	10	$2\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$5\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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