

ML2340*, ML2350**

Single Supply, Programmable 8-Bit D/A Converters

GENERAL DESCRIPTION

The ML2340 and ML2350 are CMOS voltage output, 8-bit D/A converters with an internal voltage reference and a μP interface. These devices are designed to be powered by a single supply, although they can be powered from dual power supplies. The output voltage swings above zero scale (V_{ZS}) in the unipolar mode or around zero scale (V_{ZS}) in the bipolar mode, both with programmable gain. V_{ZS} can be set to any voltage from AGND to 2.25V below V_{CC} . The digital and analog grounds, DGND and AGND, are totally independent of each other. DGND can be set to any voltage from AGND to 4.5V below V_{CC} for easy interfacing to standard TTL and CMOS logic families.

The high level of integration and versatility of the ML2340 and ML2350 makes them ideal for a wide range of applications in hard disk drives, automotive, telecom, and a variety of general purpose industrial uses. One specific intended application is controlling a hard disk voice coil.

The internal reference of the ML2340 provides a 2.25V or 4.50V output for use with A/D converters that use a single 5V $\pm 10\%$ power supply, while the ML2350 provide a 2.50V or 5.00V reference output.

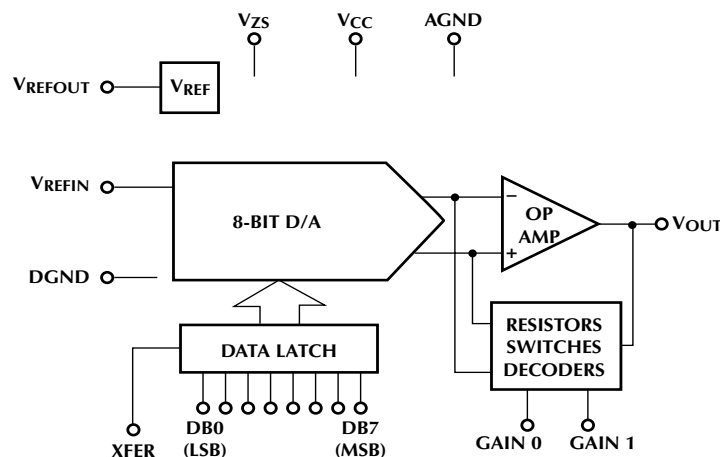
FEATURES

- Programmable output voltage gain settings of 2, 1, $\frac{1}{2}$, $\frac{1}{4}$ provide 8-, 9-, 10-, or 11-bit effective resolution around zero
- AGND to V_{CC} output voltage swing
- Bipolar or unipolar output voltage
- 4.5V to 13.2V single supply or $\pm 2.25\text{V}$ to $\pm 6.5\text{V}$ dual-supply operation
- Transparent latch allows microprocessor interface with 30ns setup time
- Data flow-through mode
- Voltage reference output

ML2340	2.25V or 4.50V
ML2350	2.50V or 5.00V
- Nonlinearity $\pm \frac{1}{4}$ LSB or $\pm \frac{1}{2}$ LSB
- Output voltage settling time over temperature and supply voltage tolerance

Within 1V of V_{CC} and AGND	2.5 μs max
Within 100mV of V_{CC} and AGND	5 μs max
- TTL and CMOS compatible digital inputs
- Low supply current (5V supply) 5mA max
- 18-pin DIP or surface mount SOIC

BLOCK DIAGRAM

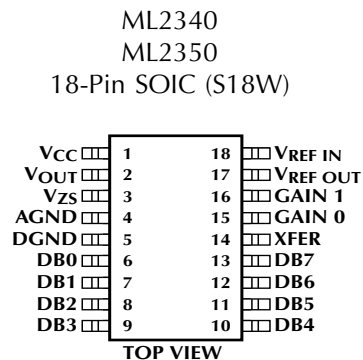
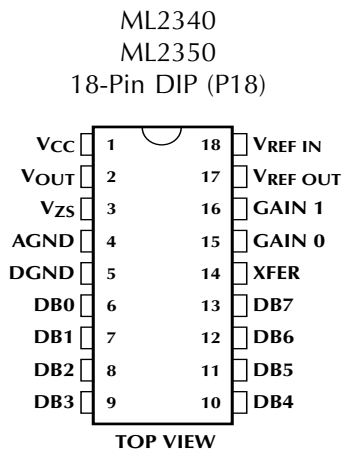


* This Part Is Obsolete

** This Part Is End Of Life As Of August 1, 2000

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PIN CONNECTIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	V _{CC}	Positive supply.	8	DB2	Data input — Bit 2.
2	V _{OUT}	Voltage output of the D/A converter. V _{OUT} is referenced to V _{ZS} .	9	DB3	Data input — Bit 3.
3	V _{ZS}	Zero Scale Voltage. V _{OUT} is referenced to V _{ZS} . V _{ZS} is normally tied to AGND in the unipolar mode or to mid-supply in the bipolar mode. When the device is operated from a single power supply, V _{ZS} has a maximum current requirement of -300µA in the bipolar mode.	10	DB4	Data input — Bit 4.
4	AGND	Analog ground.	11	DB5	Data input — Bit 5.
5	DGND	Digital ground. This is the ground reference level for all digital inputs. The range is AGND - DGND - V _{CC} - 4.5V. DGND is normally tied to system ground.	12	DB6	Data input — Bit 6.
6	DB0	Data input — Bit 0 (LSB).	13	DB7	Data input — Bit 7 (MSB).
7	DB1	Data input — Bit 1.	14	XFER	Transfer enable input. The data is transferred into the transparent latch at the high level of XFER.
			15	GAIN 0	Digital gain setting input 0.
			16	GAIN 1	Digital gain setting input 1.
			17	V _{REF OUT}	Voltage reference output. V _{REF OUT} is referenced to AGND. V _{REF OUT} is set to 2.5V and 5.0V in a low-voltage and high-voltage operation, respectively for the ML2350; 2.25V and 4.5V for the ML2340.
			18	V _{REF IN}	Voltage reference input. V _{REF IN} is referenced to AGND.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage V_{CC} with Respect to AGND	14.2V
DGND	-0.3V to $V_{CC} + 0.3V$
V_{ZS} , $V_{REF IN}$	-0.3V to $V_{CC} + 0.3V$
Logic Inputs	-0.3V to $V_{CC} + 0.3V$
Input Current per Pin	$\pm 25mA$
Storage Temperature	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ C$ (Board Mount)	875mW
Lead Temperature (Soldering 10 sec.)	
Dual-In-Line Package (Molded)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Small Outline IC Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC}	4.5V _{DC} to 13.2V _{DC}
Temperature Range	
ML2350BIJ	-40°C to +85°C
ML2340BCP, ML2340CCP	
ML2350BCP, ML2350CCP	
ML2340BCS, ML2340CCS	
ML2350BCS, ML2350CCS	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating temperature range, $V_{CC} - AGND = 5V \pm 10\%$ and $12V \pm 10\%$, $V_{REF IN}$ for ML2340 = 2.25V and 4.50V, for ML2350 $V_{REF IN} = 2.50V$ and $5.00V$, V_{OUT} load is $R_L = 1k\Omega$ and $C_L = 100pF$, V_{REF} load is $R_L = 1k\Omega$ and $C_L = 100pF$ and input control signals with $t_R = t_F - 20ns$. (Note 1)

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX			ML2350XIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Converter and Programmable Gain Amplifier									
Converter Resolution			8			8			Bits
Integral Linearity Error ML2340BXX, ML2350BXX ML2340CXX, ML2350CXX		GAIN = 2, 1, 1/2, or 1/4			$\pm 1/4$ $\pm 1/2$			$\pm 1/4$ $\pm 1/2$	LSB LSB
Differential Linearity Error ML2340BXX, ML2350BXX ML2340CXX, ML2350CXX		GAIN = 2, 1, 1/2, or 1/4			$\pm 1/4$ $\pm 1/2$			$\pm 1/4$ $\pm 1/2$	LSB LSB
Mode Select Unipolar Output Bipolar Output		V_{ZS} with respect to AGND	0 1.50		1.0 $V_{CC}-2.25$	0 1.50		1.0 $V_{CC}-2.25$	V V
Offset Error Unipolar Mode		Figure 1 GAIN = 1/4, 1/2, 1 GAIN = 2			± 10 ± 20			± 12 ± 24	mV mV
Bipolar Mode		Figure 1 GAIN = 1/4, 1/2, 1, 2			± 10 plus $\pm 2 1/2$ LSB			± 10 plus $\pm 2 1/2$ LSB	mV
Gain Error Unipolar Mode		Figure 1 GAIN = 1/4, 1/2, 1, 2		± 0.5	± 2		± 0.5	± 2.5	%FS
Bipolar Mode		GAIN = 1/4, 1/2, 1, 2		± 0.5	± 2		± 0.5	± 2.5	%FS

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ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX			ML2350XIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reference									
V _{REF OUT} Voltage ML2340BXX		V _{CC} - 7.0V T _A = 25°C T _{MIN} to T _{MAX}	2.23	2.25	2.27	2.23	2.25	2.27	V
			2.22		2.28	2.18		2.32	V
ML2340CXX		V _{CC} • 8.0V T _A = 25°C T _{MIN} to T _{MAX}	4.48	4.50	4.52	4.48	4.50	4.52	V
			4.46		4.54	4.43		4.57	V
ML2350BXX		V _{CC} - 7.0V T _A = 25°C T _{MIN} to T _{MAX}	2.22	2.25	2.29	2.22	2.25	2.28	V
			2.20		2.30	2.18		2.32	V
ML2350CXX		V _{CC} • 8.0V T _A = 25°C T _{MIN} to T _{MAX}	4.45	4.50	4.55	4.45	4.50	4.55	V
			4.40		4.60	4.35		4.65	V
ML2350BXX		V _{CC} - 7.0V T _A = 25°C T _{MIN} to T _{MAX}	2.48	2.50	2.52	2.48	2.50	2.52	V
			2.47		2.53	2.43		2.57	V
ML2350CXX		V _{CC} • 8.0V T _A = 25°C T _{MIN} to T _{MAX}	4.98	5.00	5.02	4.98	5.00	5.02	V
			4.96		5.04	4.90		5.10	V
ML2350CXX		V _{CC} - 7.0V T _A = 25°C T _{MIN} to T _{MAX}	2.45	2.50	2.55	2.46	2.50	2.55	V
			2.44		2.58	2.42		2.59	V
ML2350CXX		V _{CC} • 8.0V T _A = 25°C T _{MIN} to T _{MAX}	4.95	5.00	5.05	4.95	5.00	5.05	V
			4.90		5.10	4.85		5.15	V
Temperature Coefficient V _{REF OUT}				50			50	ppm/°C	
V _{REF} Output Current			0.75		5	0.75		5	mA
V _{REF OUT} Power Supply Rejection Ratio		100mV _{P-P} , 1kHz Sinewave on V _{CC}	-40	-60		-40	-60		dB
V _{REF IN} and V _{ZS}									
V _{REF IN} Input Range		V _{CC} - 8.75V V _{CC} • 8.75V	AGND+2		V _{CC} -1.75	AGND+2	V _{CC} -1.75	V	
			AGND+2		AGND+7	AGND+2	AGND+7	V	
V _{REF IN} DC Input Resistance			10			10		M Ω	
V _{ZS} Voltage Range	2	V _{CC} - 7.0V	AGND		V _{CC} -2.25	AGND		V _{CC} -2.25	V
Analog Output									
V _{OUT} Output Swing Unipolar Mode	2	R _L = 100kΩ	AGND+0.01		V _{CC} -0.5	AGND+0.01		V _{CC} -0.5	V
			AGND+1.0		V _{CC} -1.0	AGND+1.0		V _{CC} -1.0	V
Bipolar Mode		R _L = 100kΩ	AGND+0.1		V _{CC} -0.1	AGND+0.1		V _{CC} -0.1	V
			AGND+1.0		V _{CC} -1.0	AGND+1.0		V _{CC} -1.0	V
V _{OUT} Output Current		AGND+1V < V _{OUT} < V _{CC} -1V	-10		+10	-10		+10	mA
Power Supply Rejection Ratio		100mV _{P-P} , 1kHz sinewave on V _{CC}		-60			-60		dB

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	NOTES	CONDITIONS	ML2340XCX, ML2350XCX			ML2350XIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Digital and DC									
$V_{IN(0)}$ Logical "0" Input Voltage					0.8			0.8	V
$V_{IN(1)}$ Logical "1" Input Voltage			2.0				2.0		V
$I_{IN(0)}$ Logical "0" Input Current		$V_{IN} = \text{DGND}$	-1				-1		μA
$I_{IN(1)}$ Logical "1" Input Current		$V_{IN} = V_{CC}$			1			1	μA
Supply Current, Bipolar Mode I_{CC} , V_{CC} Current I_{AGND} , Analog Ground Current I_{VZS} , V_{ZS} Current		$V_{CC} = 5\text{V} \pm 10\%$			5.3			5.3	mA
				-90	-5.0 -300		-90	-5.0 -300	mA μA
I_{CC} , V_{CC} Current I_{AGND} , Analog Ground Current I_{VZS} , V_{ZS} Current		$V_{CC} = 12\text{V} \pm 10\%$			9.3			9.3	mA
				-90	-9.0 -300		-90	-9.0 -300	mA μA
Supply Current, Unipolar Mode I_{CC} , V_{CC} Current I_{AGND} , Analog Ground Current I_{VZS} , V_{ZS} Current	3	$V_{CC} = 5\text{V} \pm 10\%$			6.0			6.0	mA
					-4.3 -1.7			-4.3 -1.7	mA mA
I_{CC} , V_{CC} Current I_{AGND} , Analog Ground Current I_{VZS} , V_{ZS} Current	3	$V_{CC} = 12\text{V} \pm 10\%$			11.0			11.0	mA
					-7.3 -3.7			-7.3 -3.7	mA mA
AC Performance									
Settling Time t_{S1}		Figure 2, Output Step of AGND + 1V to $V_{CC} - 1\text{V}$, $R_L = 1\text{k}\Omega$		1.2	2.5		1.2	3.0	μs
		Output Step of AGND + 100mV to $V_{CC} - 100\text{mV}$, $R_L = 100\text{k}\Omega$		2.5	5		2.5	6	μs
		Output Step of $\pm 1\text{LSB}$			1			1	μs
t_{S4} , Gain Change		Change of Any Gain Setting		1.1	2.5		1.1		μs
t_{XFER} , XFER Pulse Width		Figure 3	60				60		ns
t_{DBS} , DB0-DB7 Setup Time		Figure 3	40				45		ns
t_{DBH} , DB0-DB7 Hold Time		Figure 3	0				0		ns
t_{RESET} , Power-On Reset Time					16			16	μs

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Supply current and analog ground current are specified with the digital inputs stable and no load on V_{OUT} .

Note 3: In unipolar operation with V_{ZS} and AGND tied together, digital codes that represent an analog value of less than 100mV from AGND should be avoided.

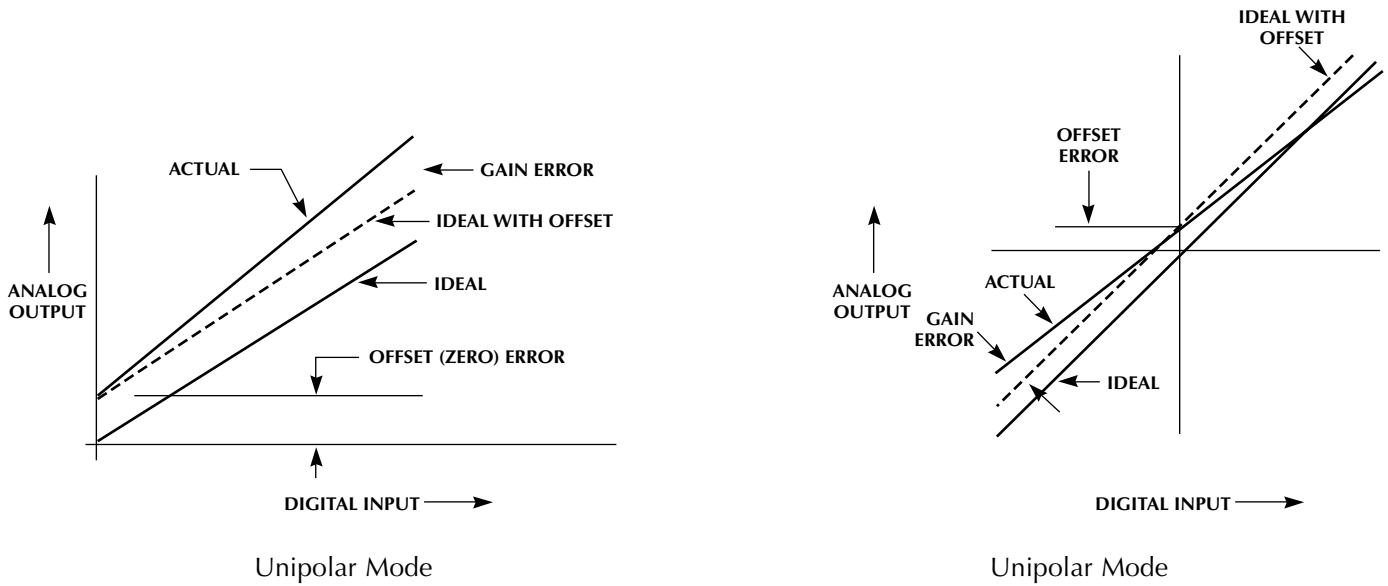


Figure 1. Gain and Offset Error

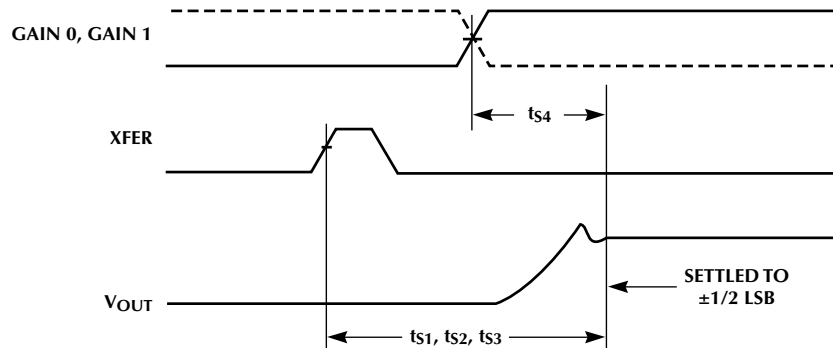


Figure 2. Settling Time

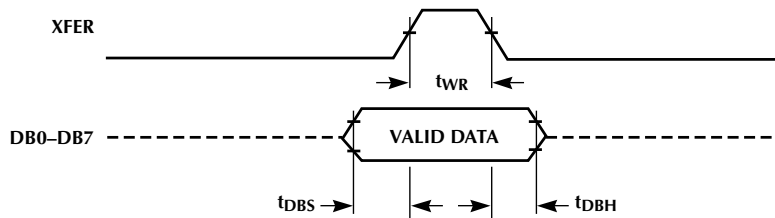


Figure 3. Single Buffered Mode

1.0 FUNCTIONAL DESCRIPTION

1.1 D/A CONVERTER

The D/A converter is implemented using an array of equal current sources that are decoded semi-linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. See Figure 4.

The input voltage reference of the D/A converter is the difference between $V_{REF\ IN}$ and AGND. This difference voltage is converted to a reference current using an internal resistor to set up the appropriate current level in

the D/A converter. The D/A converter output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

The D/A converter can be used in a multiplying mode by modulating the reference input within the specified $V_{REF\ IN}$ range.

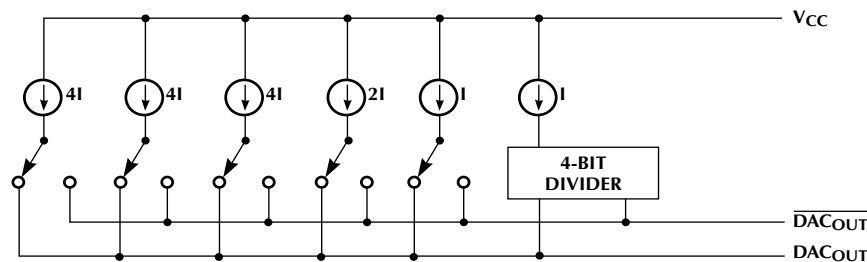


Figure 4. D/A Converter Implementation

1.2 SINGLE-SUPPLY vs. DUAL-SUPPLY OPERATION

ML2340 and ML2350 can be powered from a single supply ranging from 4.5V to 13.2V or dual supplies ranging from $\pm 2.25V$ to $\pm 6.6V$.

The internal digital and analog circuitry is powered between V_{CC} and AGND. The range of DGND is $AGND - DGND - V_{CC} - 4.5V$ with the logic thresholds set between 0.8V and 2.0V above DGND (standard TTL logic level). The range of V_{ZS} is $AGND - V_{ZS} - (V_{CC} - 2.25V)$.

1.3 UNIPOLAR AND BIPOLAR OUTPUT VOLTAGE SWING

ML2340 and ML2350 can operate in either unipolar or bipolar output voltage mode. Unipolar/bipolar mode selection is determined by comparing the zero scale voltage (V_{ZS}) of these devices to a precise internal reference that is referred to AGND. V_{ZS} is ideally the voltage that will be produced at the DAC voltage output when the digital input data is set to all "0's". Unipolar mode is selected when V_{ZS} is lower than 1.00 volt, and bipolar mode is selected when V_{ZS} is greater than 1.50 volts.

1.3.1 Unipolar Output Mode

In the unipolar mode, V_{OUT} swings above V_{ZS} . Ideally the 00000000 code results in an output voltage of V_{ZS} , and the 11111111 code results in an output voltage of $V_{FS} \times 255/256$, where V_{FS} is the full-scale voltage determined by $V_{REF\ IN}$ and the gain setting.

1.3.2 Bipolar Output Mode

In the bipolar mode, V_{OUT} swings around V_{ZS} . The input data is in 2's complement binary format. Ideally, the 00000000 code results in an output voltage of V_{ZS} ; the 10000000 code results in an output voltage of $(V_{ZS} - V_{FS})$; and the 01111111 results in an output voltage of $(V_{ZS} + V_{FS} \cdot 127/128)$, where V_{FS} is the full scale output voltage determined by $V_{REF\ IN}$ and the gain setting.

1.4 OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the D/A output current to a voltage output using a resistive network with proper gain setting determined by the GAIN 0 and GAIN 1 inputs. There are four possible gain settings for unipolar output voltage mode and bipolar output voltage mode as listed below:

Unipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output Swing Relative to V_{ZS}
0	0	$1/4$	$V_{REF\ IN} \infty 1/4$
0	1	$1/2$	$V_{REF\ IN} \infty 1/2$
1	0	1	$V_{REF\ IN} \infty 1$
1	1	2	$V_{REF\ IN} \infty 2$

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Bipolar Output Voltage Mode

GAIN 1	GAIN 0	GAIN	Voltage Output _{p,p}
0	0	1/4	$V_{REF IN} \infty 1/8$
0	1	1/2	$V_{REF IN} \infty 1/4$
1	0	1	$V_{REF IN} \infty 1/2$
1	1	2	$V_{REF IN} \infty 1$

The output buffer can source or sink as much as 10mA of current with an output voltage of at least 1V from either V_{CC} or AGND. As the output voltage approaches V_{CC} or AGND the current sourcing/sinking capability of the output buffer is reduced. The output buffer can still swing down to within 10mV of AGND and up to within 40mV of V_{CC} with a 100k Ω load at V_{OUT} to AGND in the unipolar operation. In the bipolar operation, the output buffer swing is limited to about 100mV from either rails.

1.5 VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2340 and ML2350. Two reference voltages can be produced by each device. An internal comparator monitors the power supply voltage to determine the selection of the reference voltage. A reference voltage of 2.25 volts on the ML2340 and 2.50 volts on the ML2350 is selected when the supply voltage is less than approximately 7.50 volts. Otherwise, a reference voltage of 4.50 volts and 5.00 volts is selected. To prevent the comparator from oscillating between the two selections, avoid operation with a power supply between 7.0 and 8.0 volts.

The bandgap reference is trimmed for zero Temperature Coefficient (TC) at 35°C to minimize output voltage drift over the specified operating temperature range.

The internal reference is buffered for use by the DAC and external circuits. The reference buffer will source more than 5mA of current and sink more than 1mA of current. With $V_{REF IN}$ connected to $V_{REF OUT}$, the following output voltage ranges of the DAC are obtained:

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Gain Setting	$V_{REF} = 2.25V$ with $V_{CC} - 7.0V$		$V_{REF} = 4.5V$ with $V_{CC} \bullet 8.0V$	
	Unipolar	Bipolar	Unipolar	Bipolar
1/4	0 to 0.562V	-0.281V to +0.281V	0 to 1.125V	-0.562V to +0.562V
1/2	0 to 1.125V	-0.562V to +0.562V	0 to 2.250V	-1.125V to +1.125V
1	0 to 2.250V	-1.125V to +1.125V	0 to 4.500V	-2.250V to +2.250V
2	0 to 4.500V	-2.250V to +2.250V	0 to 9.000V	-4.500V to +4.500V

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Gain Setting	$V_{REF} = 2.50V$ with $V_{CC} - 7.0V$		$V_{REF} = 5.0V$ with $V_{CC} \bullet 8.0V$	
	Unipolar	Bipolar	Unipolar	Bipolar
1/4	0 to 0.625V	-0.3125V to +0.3125V	0 to 1.25V	-0.625V to +0.625V
1/2	0 to 1.250V	-0.6250V to +0.6250V	0 to 2.50V	-1.250V to +1.250V
1	0 to 2.500V	-1.2500V to +1.2500V	0 to 5.00V	-2.500V to +2.500V
2	0 to 5.000V	-2.5000V to +2.5000V	0 to 10.00V	-5.000V to +5.000V

An external reference can alternatively be used on $V_{REF IN}$ to set the desired full scale voltage. The linearity of the D/A converter depends on the reference used, however. To insure integral linearity at an 8-bit level, a reference voltage of no less than 2V and no more than 7V (2.75V for operation with a low-voltage power supply) should be used.

1.6 DIGITAL INTERFACE

The digital interface of the ML2340 and ML2350 consist of a transfer input (XFER) and eight data inputs, DB0 through DB7. The digital interface operates in one of the two modes:

1.6.1 Single-Buffered Mode

Digital input data on DB0–DB7 is passed through an 8-bit transparent input latch on the rising edge of XFER. Because the outputs of the latch are connected directly to the inputs of the internal DAC, changes on the digital data while the XFER input is still active will cause an immediate change in the DAC output voltage. To hold the input data on the latch, the XFER input needs deactivated while the data is still stable.

1.6.2 Flow-Through Mode

In the flow-through mode, the input latch is bypassed. When XFER is set to logic "1", a change of data inputs, DB0–DB7, results in an immediate update of the output voltage.

1.7 POWER-ON-RESET

The ML2340 and ML2350 have an internal power-on-reset circuit to initialize the device when power is first applied to the device. The power-on-reset interval of typically 8 μ s begins when the supply voltage, V_{CC} reaches approximately 2.0V. During the power-on-reset interval, the transparent latch is reset to all "0's".

2.0 TYPICAL APPLICATIONS

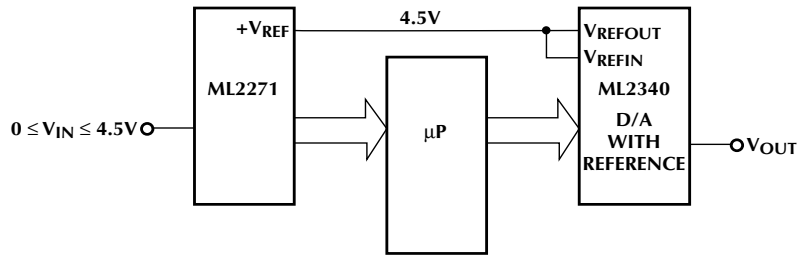


Figure 5. Using 4.50V Reference of D/A for Reference of A/D Using Single 5V $V_{CC} \pm 10\%$

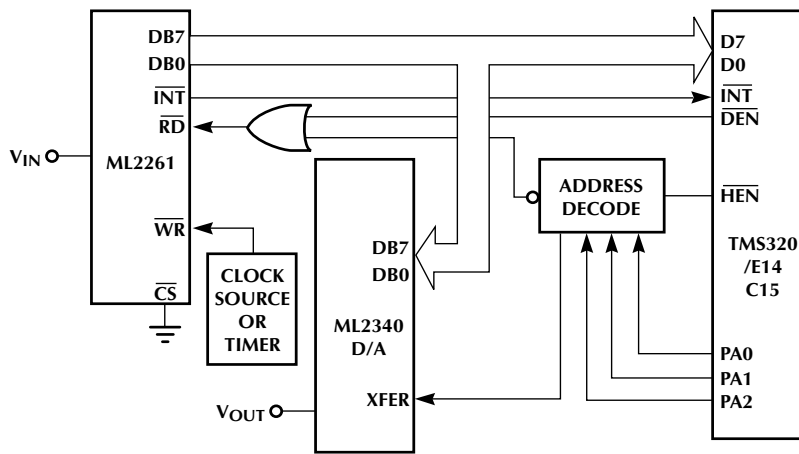


Figure 6. TMS320 Interface

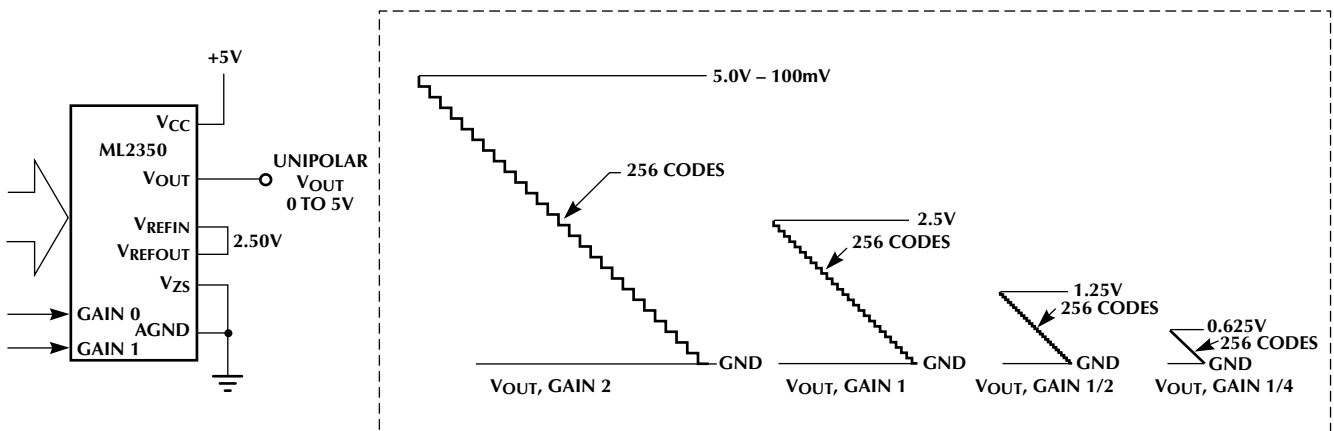


Figure 7. Single 5V Supply Unipolar V_{OUT}

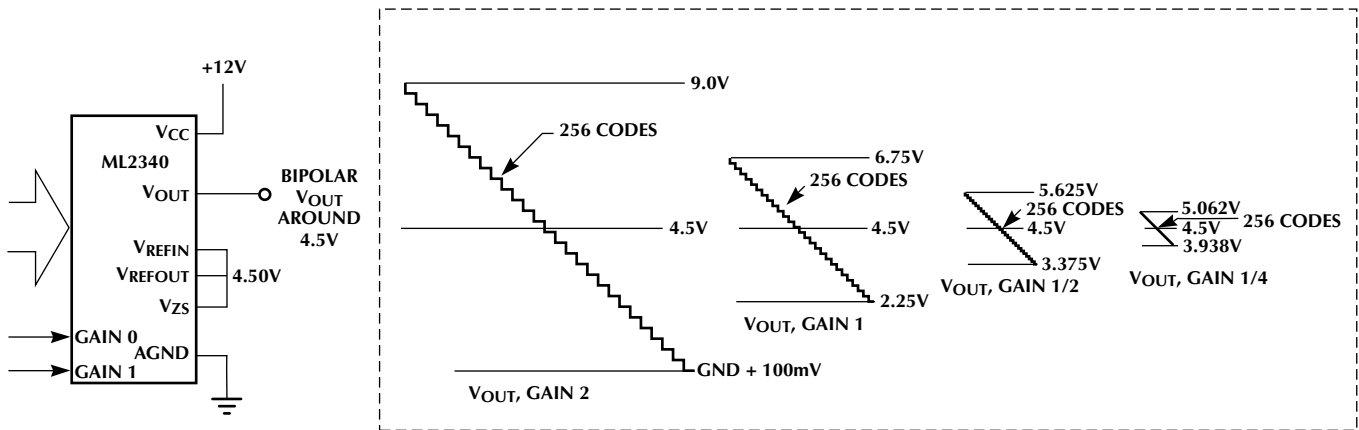


Figure 8. Single 12V Supply, Bipolar V_{OUT} with 11-Bits Resolution Around 4.5V

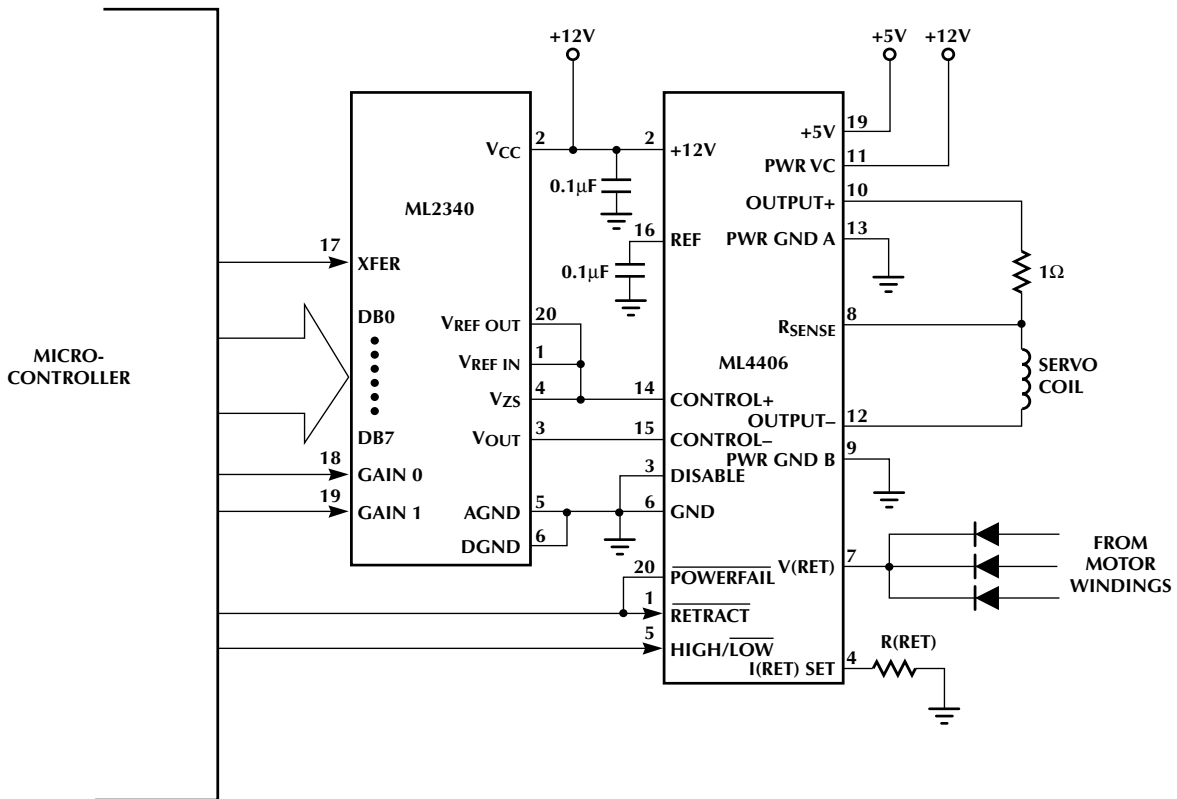
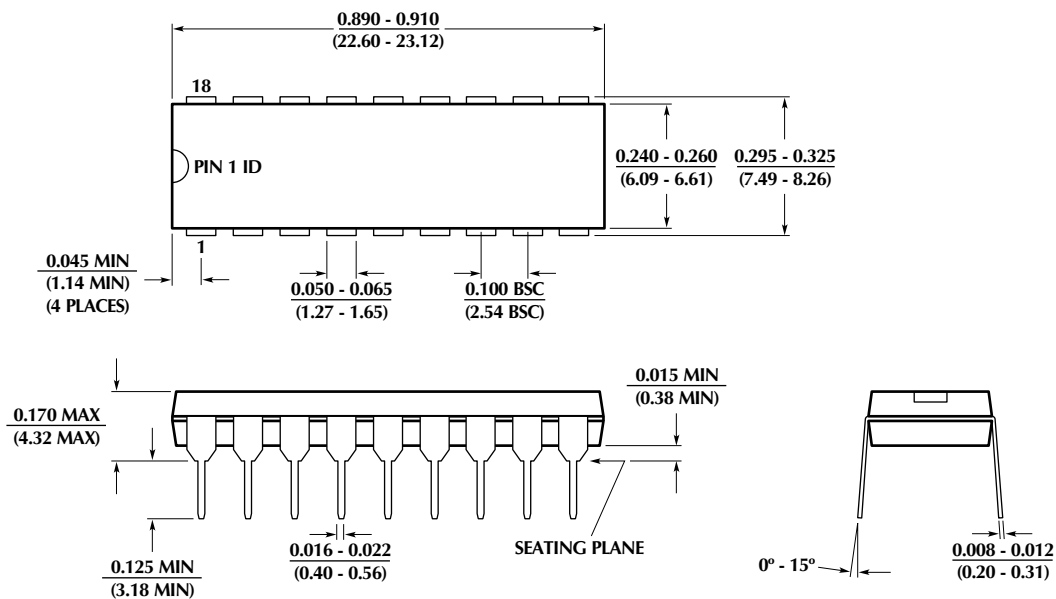


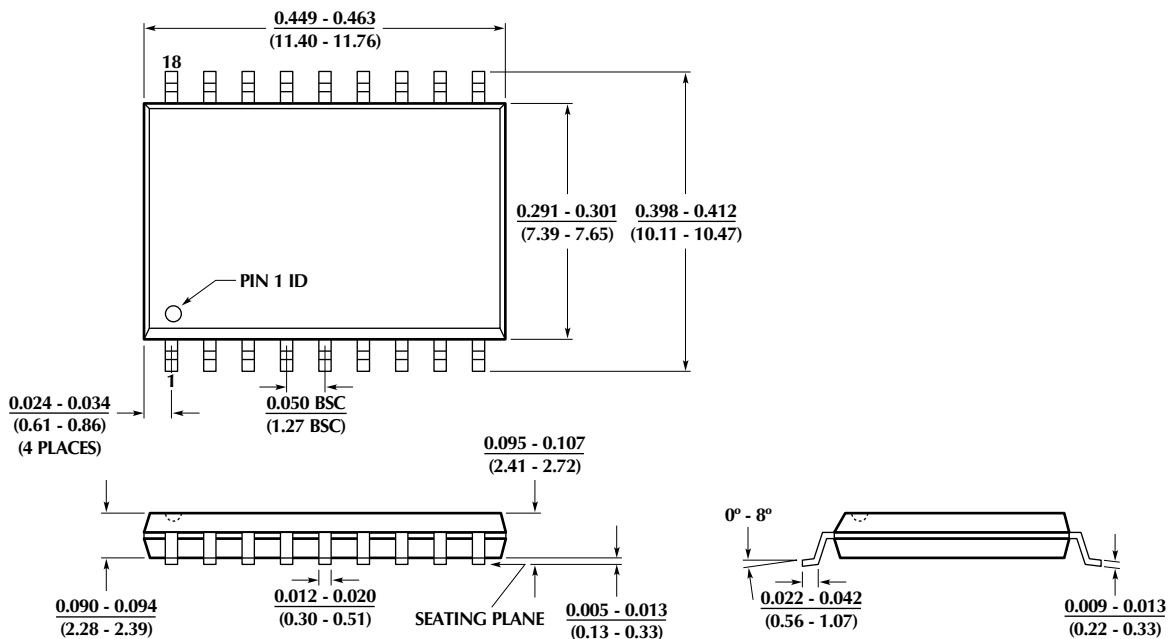
Figure 9. Hard Disc Drive Servo Coil Driver Providing 13-Bit Effective Resolution

PHYSICAL DIMENSIONS inches (millimeters)

**Package: P18
18-Pin PDIP**




**Package: S18
18-Pin SOIC**



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ORDERING INFORMATION

PART NUMBER	INTEGRAL & DIFFERENTIAL NON-LINEARITY	TEMPERATURE RANGE	PACKAGE
$V_{REF\ OUT} = 2.25V$ with $V_{CC} = 5V$			
ML2340CCP/5 (OBS) ML2340CCS/5 (OBS)	$\pm 1/2$ LSB	0°C to 70°C 0°C to 70°C	Molded DIP (P18) Molded SOIC (S18)
$V_{REF\ OUT} = 2.50V$ with $V_{CC} = 5V$			
ML2350CCP/5 (OBS) ML2350CCS/5 (EOL) ML2350CIS/5 (EOL)	$\pm 1/2$ LSB	0°C to 70°C 0°C to 70°C -40°C to 85°C	Molded DIP (P18) Molded SOIC (S18) Molded SOIC (S18)
$V_{REF\ OUT} = 4.50V$ with $V_{CC} = 12V$			
ML2340CCP/12 (OBS) ML2340CCS/12 (OBS)	$\pm 1/2$ LSB	0°C to 70°C 0°C to 70°C	Molded DIP (P18) Molded SOIC (S18)
$V_{REF\ OUT} = 5.00V$ with $V_{CC} = 12V$			
ML2350CCP/12 (OBS) ML2350CCS/12 (OBS) ML2350CIS/12 (OBS)	$\pm 1/2$ LSB	0°C to 70°C 0°C to 70°C -40°C to 85°C	Molded DIP (P18) Molded SOIC (S18) Molded SOIC (S18)

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Products described in this document may be covered by one or more of the following patents, U.S.: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; Japan: 2598946; 2619299. Other patents are pending.

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