FUJITSU

# MOS 65536-BIT DYNAMIC RANDOM ACCESS MEMORY

**MB 8264A-10**
**MB 8264A-12**
**MB 8264A-15**

## 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

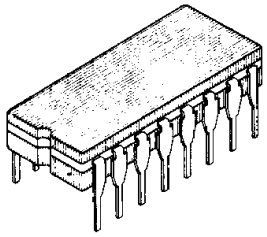
The Fujitsu MB 8264A is a fully decoded, dynamic random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8264A to be housed in a standard 16 pin DIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out.

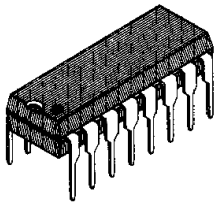
The MB 8264A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

- 65,536 x 1 RAM, 16 pin DIP/18 pad LCC
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  100 ns max (MB 8264A-10)
  120 ns max (MB 8264A-12)
  150 ns max (MB 8264A-15)
- Cycle time,
  190 ns min (MB 8264A-10)
  230 ns min (MB 8264A-12)
  260 ns min (MB 8264A-15)
- Single +5V Supply, ±10% tolerance
- Low power (active)
  275 mW max (MB 8264A-10)
  248 mW max (MB 8264A-12)
  220 mW max (MB 8264A-15)
  22 mW Standby (max)
- 2ms/128 refresh cycles
- $\overline{RAS}$-only and Hidden refresh capability
- Read-Modify-Write and Page-Mode capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- On-chip latches for Addresses and Data-in
- $t_{AR}$, $t_{WCR}$, $t_{DHR}$ are eliminated
- Standard 16-pin Ceramic (Cerdip) DIP: Surfix-Z
  Standard 16-pin Plastic DIP: Surfix-P
  Standard 18-pad Ceramic LCC: Surfix-TV



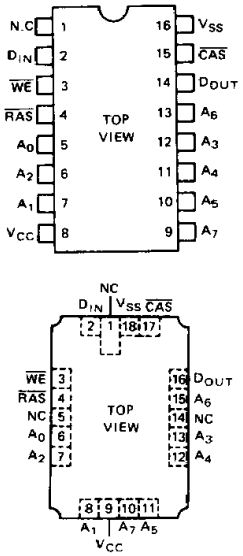
**CERAMIC PACKAGE (CERDIP) DIP-16C-C04**



**PLASTIC PACKAGE DIP-16P-M03**

LCC-18C-F02 : See Page 1-191

**PIN ASSIGNMENT**




### ABSOLUTE MAXIMUM RATINGS (See NOTE)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | | $V_{IN}$, $V_{OUT}$ | −1 to +7 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | | $V_{CC}$ | −1 to +7 | V |
| Storage temperature | Ceramic | $T_{STG}$ | −55 to +150 | °C |
| | Pastic | | −55 to +125 | |
| Power dissipation | | $P_D$ | 1.0 | W |
| Short circuit output current | | | 50 | mA |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



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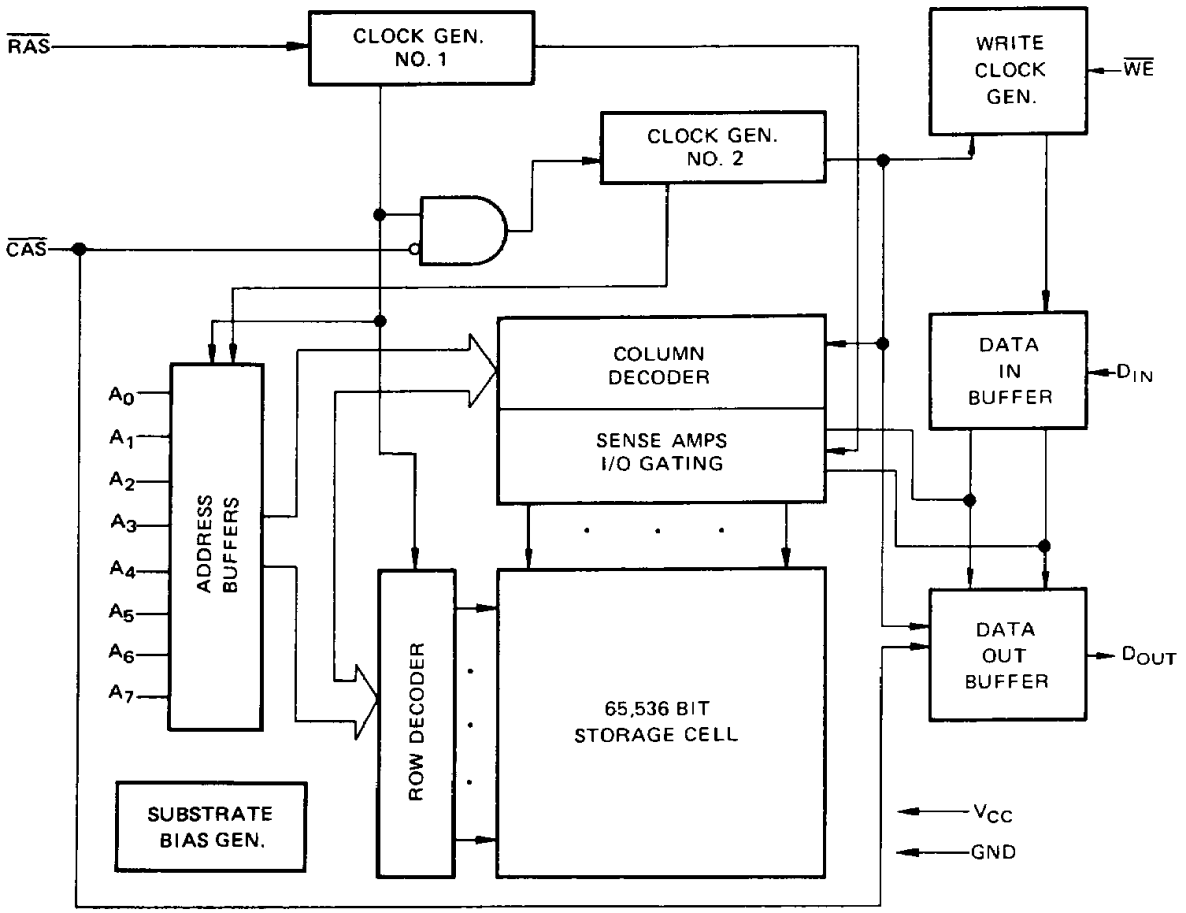
Fig. 1 – MB 8264A BLOCK DIAGRAM




## CAPACITANCE ($T_A$ = 25°C)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input Capacitance $A_0$~$A_7$, $D_{IN}$ | $C_{IN1}$ | | 5 | pF |
| Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $C_{IN2}$ | | 8 | pF |
| Output Capacitance $D_{OUT}$ | $C_{OUT}$ | | 7 | pF |



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# RECOMMENDED OPERATING CONDITIONS

(Referenced to $V_{SS}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Operating Temperature |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$<br>$V_{SS}$ | 4.5<br>0 | 5.0<br>0 | 5.5<br>0 | V<br>V | 0°C to +70°C |
| Input High Voltage, all inputs | $V_{IH}$ | 2.4 | | 6.5 | V | |
| Input Low Voltage, all inputs | $V_{IL}$* | -1.0 | | 0.8 | V | |

**Note** * : The device can withstand undershoots to the -2V level with a pulse width of 20 ns.

# DC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| OPERATING CURRENT *<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC}$ = min) | MB 8264A-10 | $I_{CC1}$ | | 50 | mA |
| | MB 8264A-12 | | | 45 | |
| | MB 8264A-15 | | | 40 | |
| STANDBY CURRENT<br>Standby Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | | $I_{CC2}$ | | 4 | mA |
| REFRESH CURRENT *<br>Average power supply current<br>($\overline{CAS}$ = $V_{IH}$, $\overline{RAS}$ cycling; $t_{RC}$ = min) | MB 8264A-10 | $I_{CC3}$ | | 38 | mA |
| | MB 8264A-12 | | | 35 | |
| | MB 8264A-15 | | | 31 | |
| PAGE MODE CURRENT*<br>Average power supply current<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ cycling; $t_{PC}$ = min) | MB 8264A-10 | $I_{CC4}$ | | 35 | mA |
| | MB 8264A-12 | | | 32 | |
| | MB 8264A-15 | | | 28 | |
| INPUT LEAKAGE CURRENT<br>Input leakage current, any input<br>(0V≦$V_{IN}$≦5.5V, $V_{CC}$=5.5V, $V_{SS}$=0V, all other pins not test=0V) | | $I_{I(L)}$ | -10 | 10 | μA |
| OUTPUT LEAKAGE CURRENT<br>(Data out is disabled, 0V≦$V_{OUT}$≦5.5) | | $I_{O(L)}$ | -10 | 10 | μA |
| OUTPUT LEVELS<br>Output high voltage ($I_{OH}$ = -5mA)<br>Output low voltage ($I_{OL}$ = 4.2mA) | | $V_{OH}$<br>$V_{OL}$ | 2.4 | <br>0.4 | V<br>V |

**Note** * : $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with the output open.



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# AC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)** NOTES 1, 2, 3

| Parameter | NOTES | Symbol | MB 8264A-10 | | MB 8264A-12 | | MB 8264A-15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Time between Refresh | | $t_{REF}$ | | 2 | | 2 | | 2 | ms |
| Random Read/Write Cycle Time | | $t_{RC}$ | 190 | | 230 | | 260 | | ns |
| Read-Write Cycle Time | | $t_{RWC}$ | 230 | | 265 | | 280 | | ns |
| Page Mode Cycle Time | | $t_{PC}$ | 105 | | 120 | | 145 | | ns |
| Page Mode Read-Write Cycle Time | | $t_{PRWC}$ | 135 | | 155 | | 180 | | ns |
| Access Time from $\overline{RAS}$ | 4, 6 | $t_{RAC}$ | | 100 | | 120 | | 150 | ns |
| Access Time from $\overline{CAS}$ | 5, 6 | $t_{CAC}$ | | 50 | | 60 | | 75 | ns |
| Output Buffer Turn Off Delay | | $t_{OFF}$ | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Transition Time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns |
| $\overline{RAS}$ Precharge Tim | | $t_{RP}$ | 80 | | 100 | | 100 | | ns |
| $\overline{RAS}$ Pulse Width | | $t_{RAS}$ | 100 | 10000 | 120 | 10000 | 150 | 10000 | ns |
| $\overline{RAS}$ Hold Time | | $t_{RSH}$ | 50 | | 60 | | 75 | | ns |
| $\overline{CAS}$ Precharge Time (Page mode only) | | $t_{CP}$ | 45 | | 50 | | 60 | | ns |
| $\overline{CAS}$ Precharge Time (All cycles except page mode) | | $t_{CPN}$ | 20 | | 20 | | 25 | | ns |
| $\overline{CAS}$ Pulse Width | | $t_{CAS}$ | 50 | 10000 | 60 | 10000 | 75 | 10000 | ns |
| $\overline{CAS}$ Hold Time | | $t_{CSH}$ | 100 | | 120 | | 150 | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Tim | 7, 8 | $t_{RCD}$ | 20 | 50 | 20 | 60 | 25 | 75 | ns |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | | $t_{CRP}$ | 0 | | 0 | | 0 | | ns |
| Row Address Set Up Time | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| Row Address Hold Time | | $t_{RAH}$ | 10 | | 10 | | 15 | | ns |
| Column Address Set Up Time | | $t_{ASC}$ | 0 | | 0 | | 0 | | ns |
| Column Address Hold Time | | $t_{CAH}$ | 15 | | 15 | | 20 | | ns |
| Read Command Set Up Time | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| Read Command Hold Time Referenced to $\overline{CAS}$ | 10 | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| Read Command Hold Time Referenced to $\overline{RAS}$ | 10 | $t_{RRH}$ | 20 | | 20 | | 20 | | ns |
| Write Command Set Up Time | 9 | $t_{WCS}$ | 0 | | 0 | | 0 | | ns |
| Write Command Hold Time | | $t_{WCH}$ | 20 | | 25 | | 30 | | ns |
| Write Command Pulse Width | | $t_{WP}$ | 20 | | 25 | | 30 | | ns |
| Write Command to $\overline{RAS}$ Lead Time | | $t_{RWL}$ | 35 | | 40 | | 45 | | ns |
| Write Command to $\overline{CAS}$ Lead Time | | $t_{CWL}$ | 35 | | 40 | | 45 | | ns |
| Data In Set Up Time | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| Data In Hold Time | | $t_{DH}$ | 20 | | 25 | | 30 | | ns |
| $\overline{CAS}$ to $\overline{WE}$ Delay | 9 | $t_{CWD}$ | 40 | | 50 | | 60 | | ns |
| $\overline{RAS}$ to $\overline{WE}$ Delay | 9 | $t_{RWD}$ | 90 | | 110 | | 120 | | ns |
| $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time ($\overline{RAS}$-only refresh) | | $t_{RPC}$ | 20 | | 20 | | 20 | | ns |



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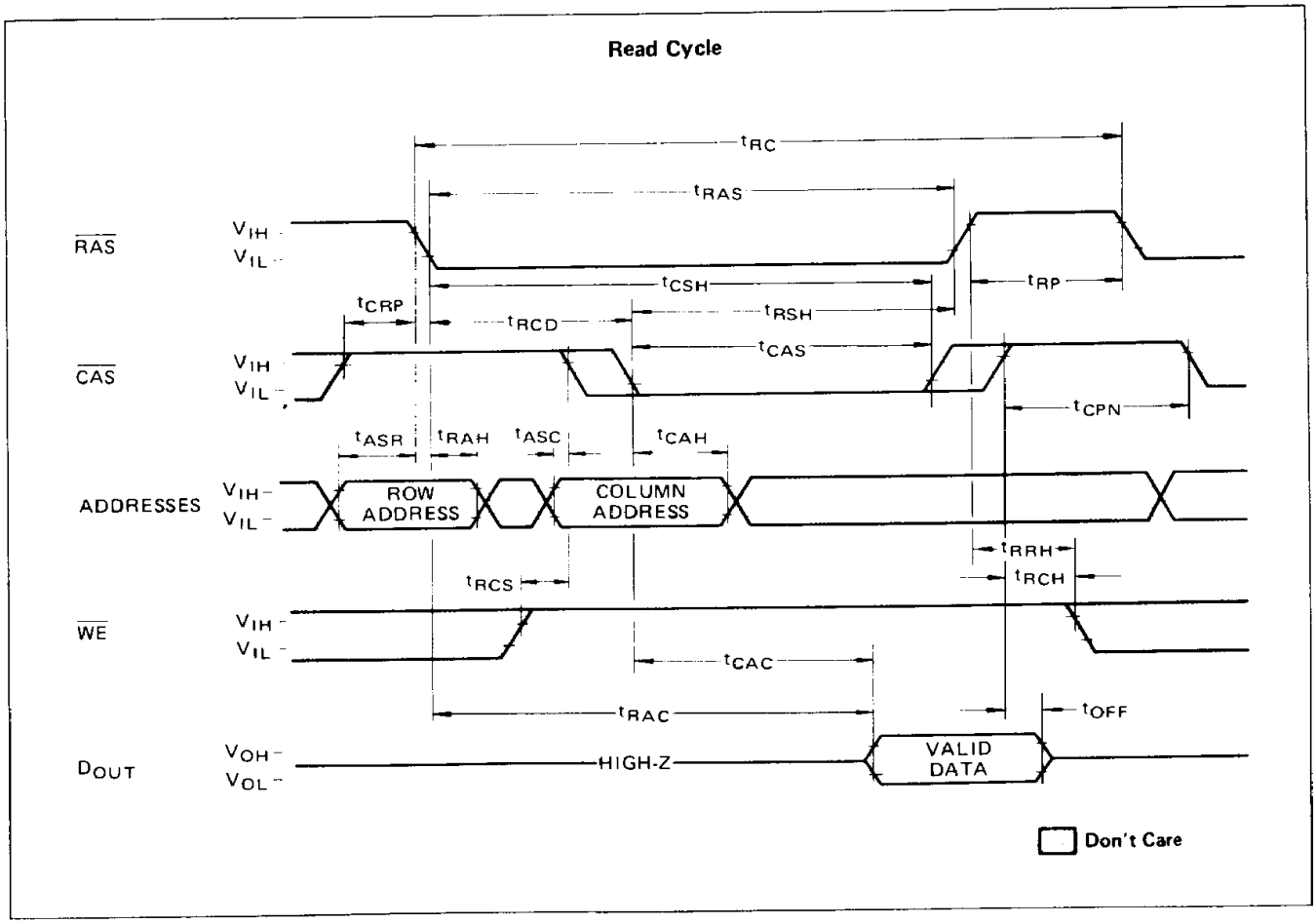
**Notes:**

1. An initial pause of 200 $\mu$s is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. AC characteristics assume $t_T$ = 5ns.
3. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
8. $t_{RCD}$ (min) = $t_{RAH}$ (min) + 2$t_T$ ($t_T$=5ns) + $t_{ASC}$ (min)
9. $t_{WCS}$, $t_{CWD}$ and $t_{RWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.

**Read Cycle**



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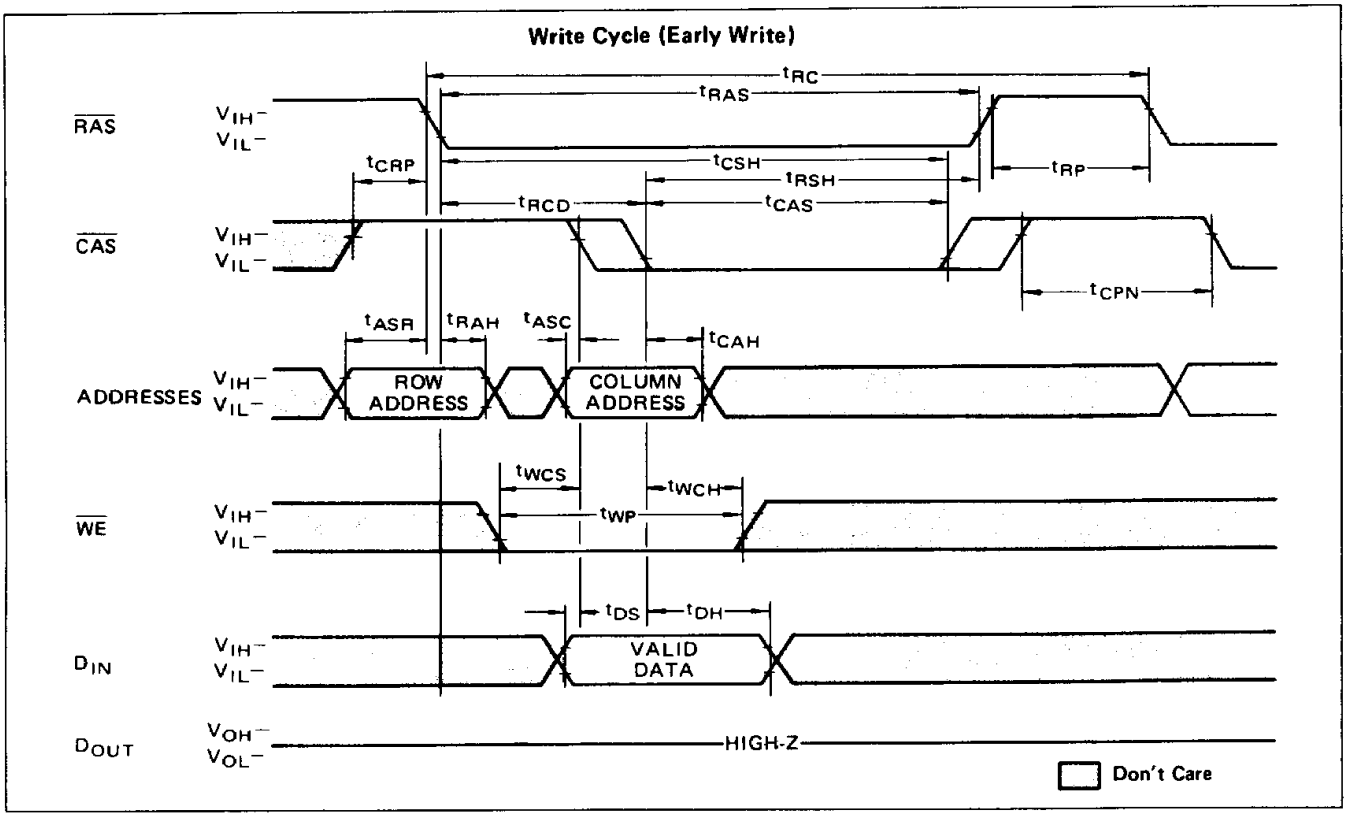
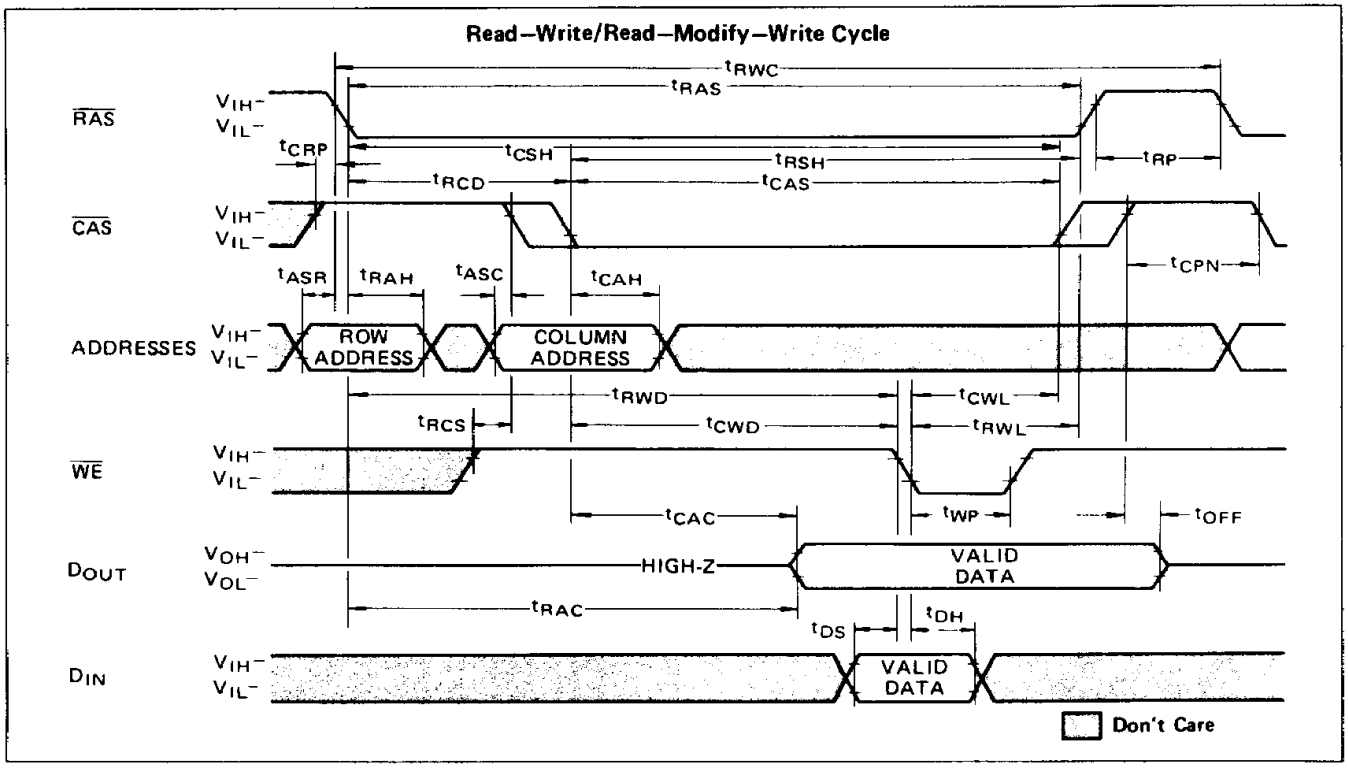
## Write Cycle (Early Write)




## Read–Write/Read–Modify–Write Cycle



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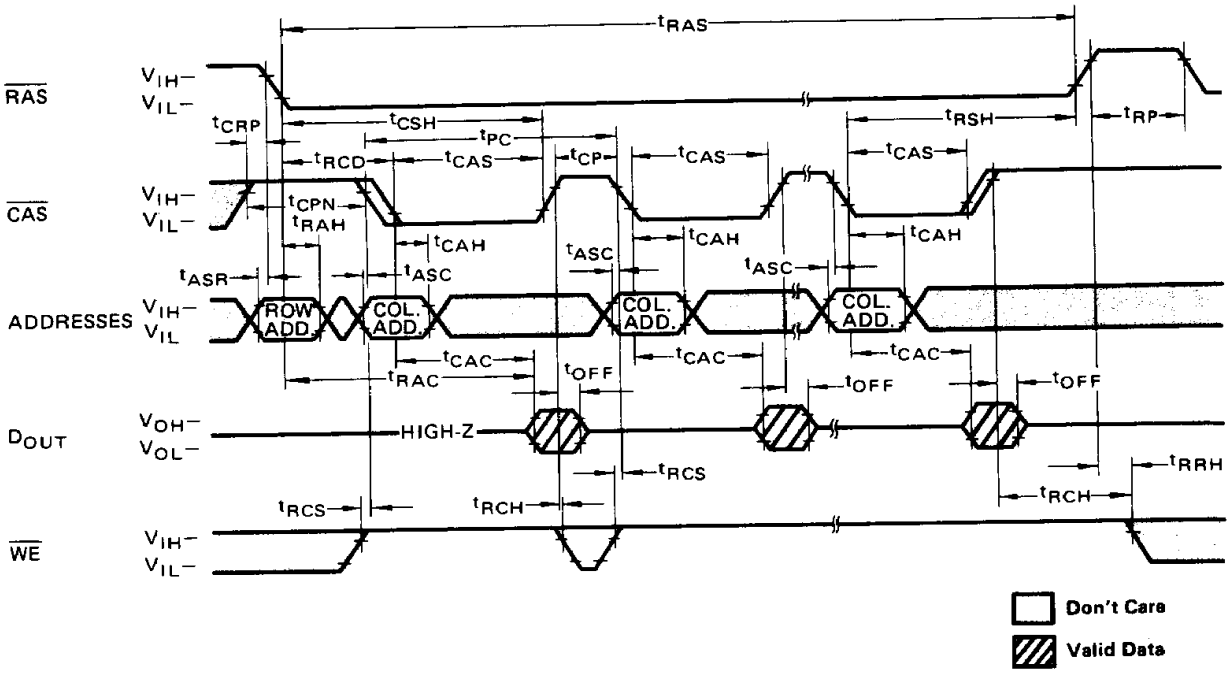
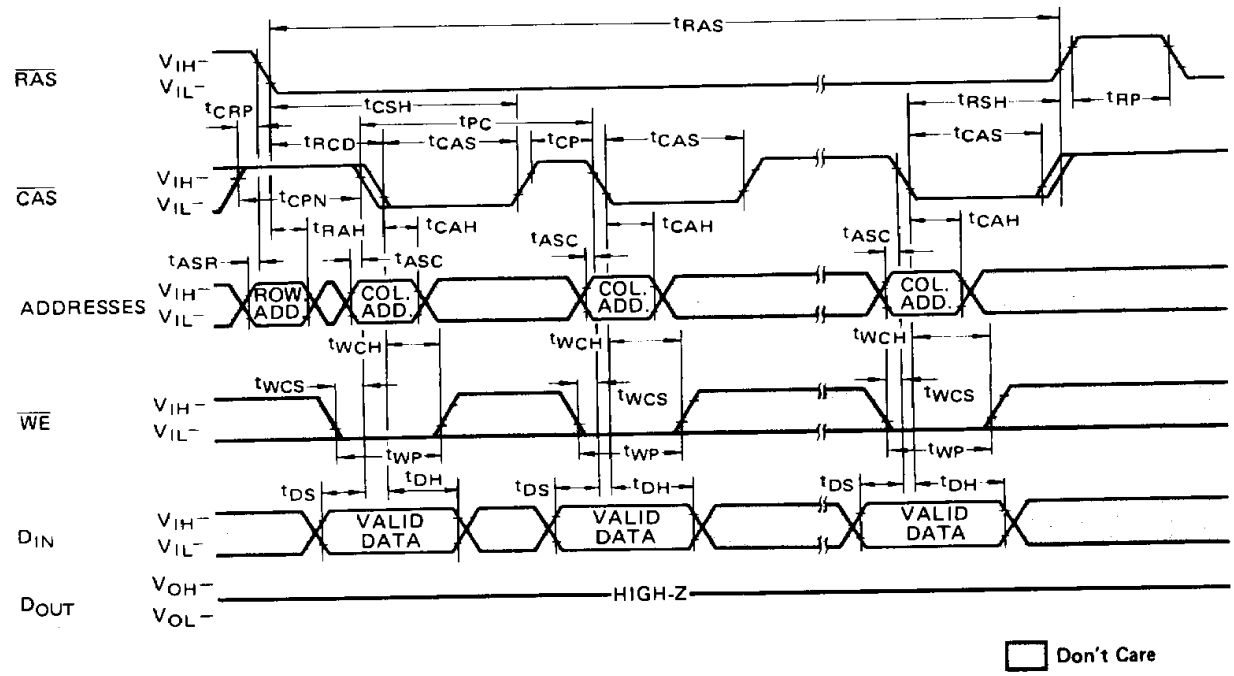
## Page Mode Read Cycle




## Page Mode Write Cycle



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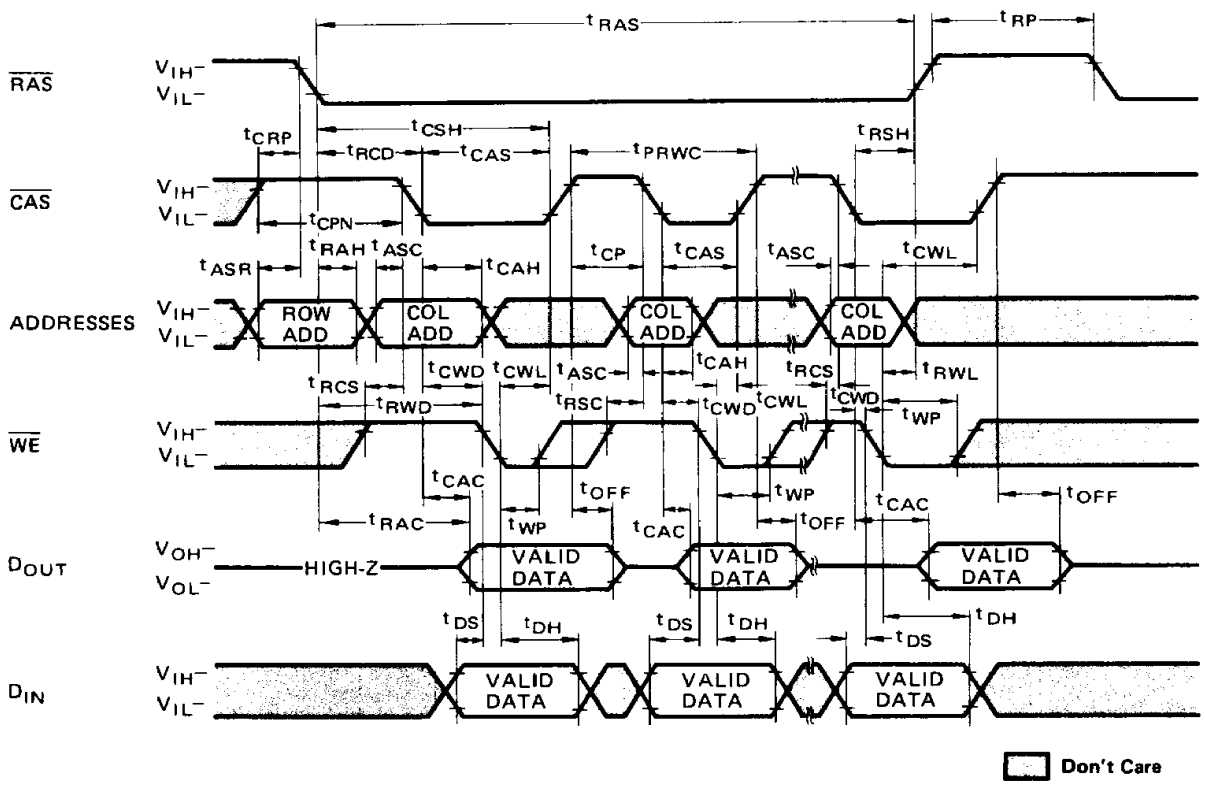
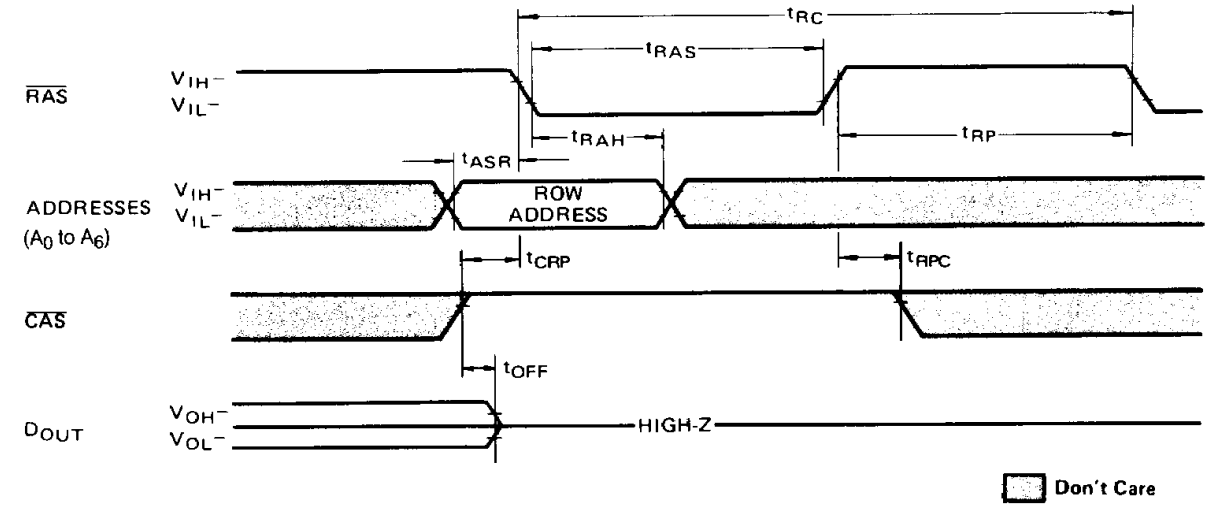
## Page Mode Read-Write Cycle




## RAS-only Refresh Cycle

**Note:** $\overline{WE}$, $D_{IN}$ = Don't care, $A_7$ = $V_{IH}$ or $V_{IL}$



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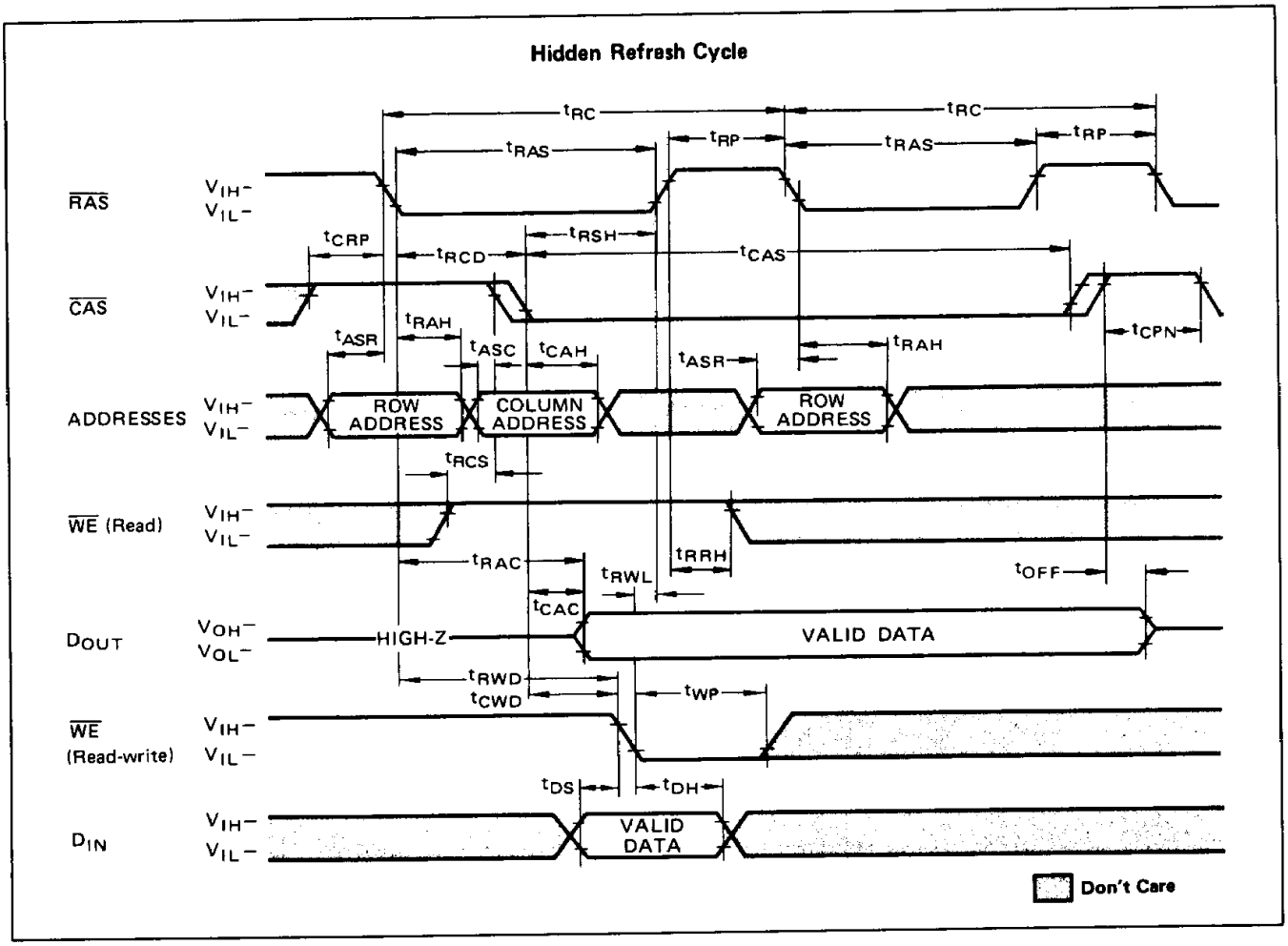


# DESCRIPTION

**Address Inputs:**
A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB 8264A. Eight row-address bits are established on the input pins ($A_0$ through $A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permite triggering of $\overline{CAS}$ as soon as the Row Address Hold Time ($t_{RAH}$) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

**Write Enable:**
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode and low selects write mode. Data input is disabled when read mode is selected.

**Data Input:**
Data is written into the MB 8264A during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In ($D_{IN}$) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, $D_{IN}$ is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be low after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time ($t_{CWD}$) has been satisfied. Thus $D_{IN}$ is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

**Data Output:**
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a



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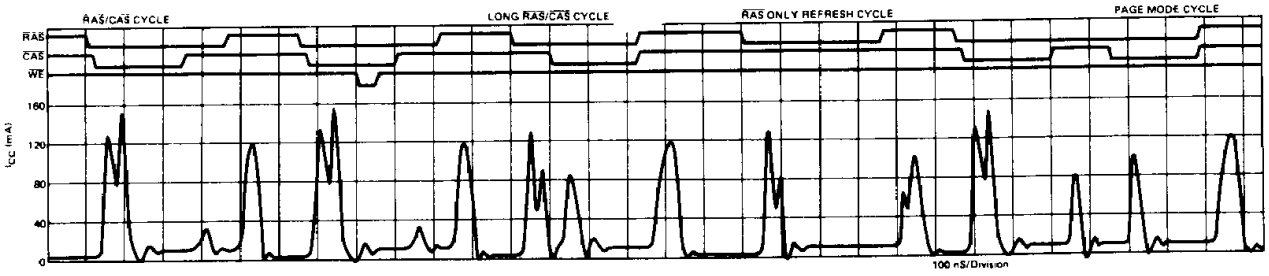
high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after $t_{RAC}$ from the falling edge of $\overline{RAS}$ when $t_{RCD}$ (max) is satisfied, or after $t_{CAC}$ from the falling edge of $\overline{CAS}$ when the transition occurs after $t_{RCD}$ (max). Data remains valid until $\overline{CAS}$ is returned to a high. In a write cycle the indentical sequence occurs, but data is not valid.

**Page Mode:**
Page-mode operation permits strobing the row-address into the MB 8264A while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row addresses don't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row addresses are eliminated.

**$\overline{RAS}$-only Refresh**
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either $V_{IL}$ or $V_{IH}$ is permitted for $A_7$. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in a high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

**Hidden Refresh:**
$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ as $V_{IL}$ from a previous memory read cycle.

Fig. 2 – CURRENT WAVE FORM ($V_{CC}$ = 5.5V, $T_A$ = 25°C)



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# TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

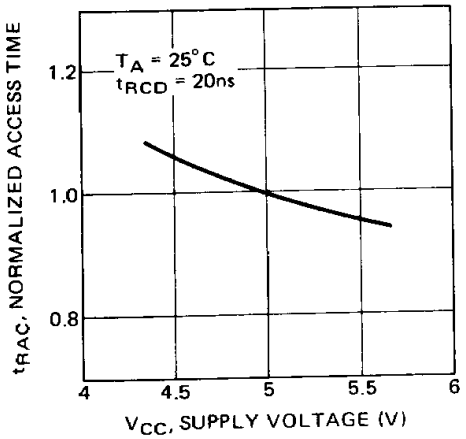


Fig. 4 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

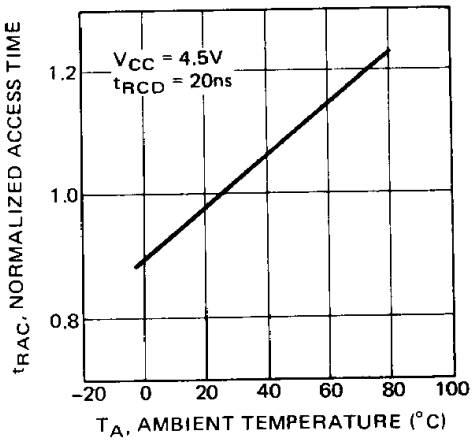


Fig. 5 – OPERATING CURRENT vs CYCLE RATE

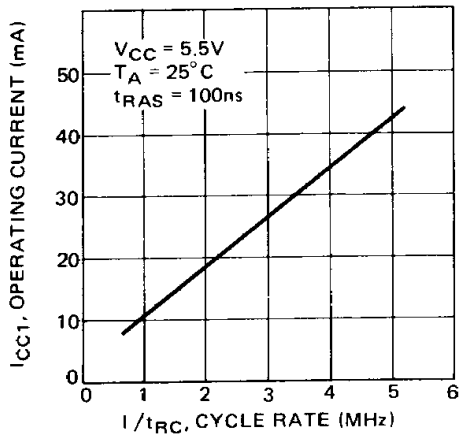


Fig. 6 – OPERATING CURRENT vs SUPPLY VOLTAGE

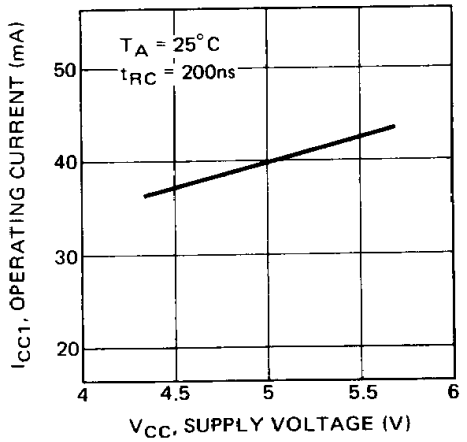


Fig. 7 – OPERATING CURRENT vs AMBIENT TEMPERATURE

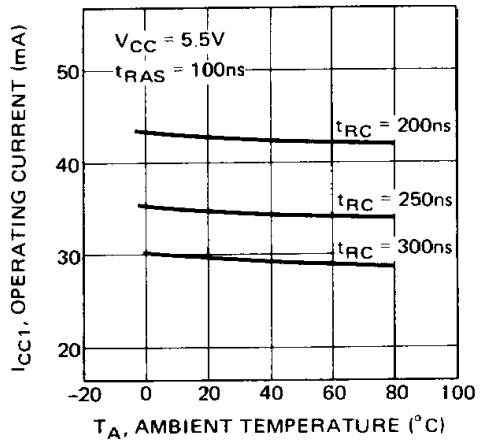


Fig. 8 – STANDBY CURRENT vs SUPPLY VOLTAGE

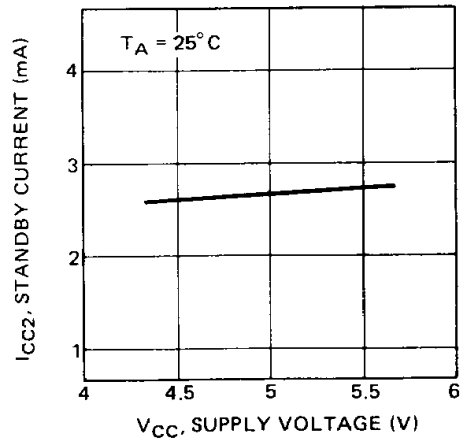




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**Fig. 9 – STANDBY CURRENT vs AMBIENT TEMPERATURE**

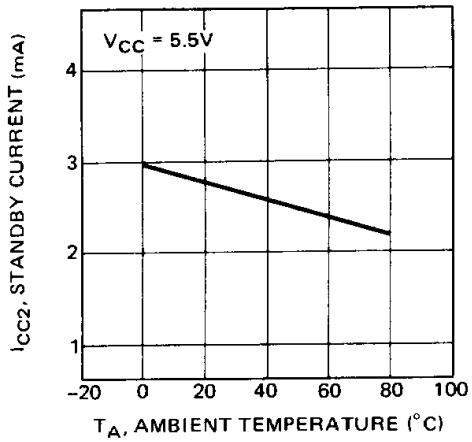


**Fig. 10 – REFRESH CURRENT vs CYCLE RATE**

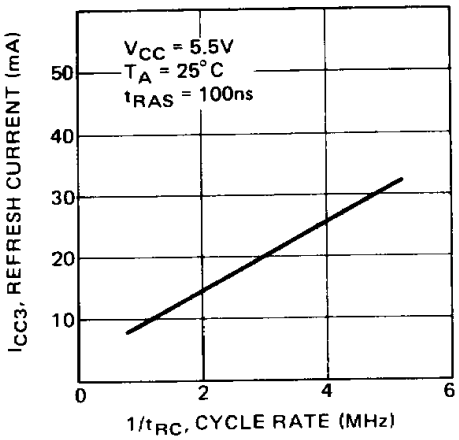


**Fig. 11 – REFRESH CURRENT vs SUPPLY VOLTAGE**

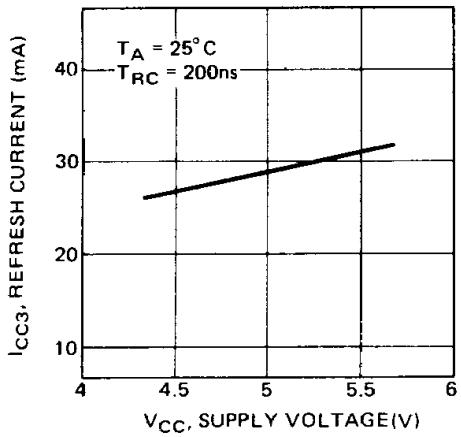


**Fig. 12 – REFRESH CURRENT vs AMBIENT TEMPERATURE**

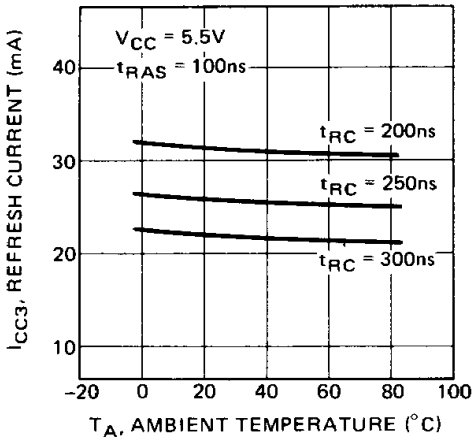


**Fig. 13 – PAGE MODE CURRENT vs CYCLE RATE**

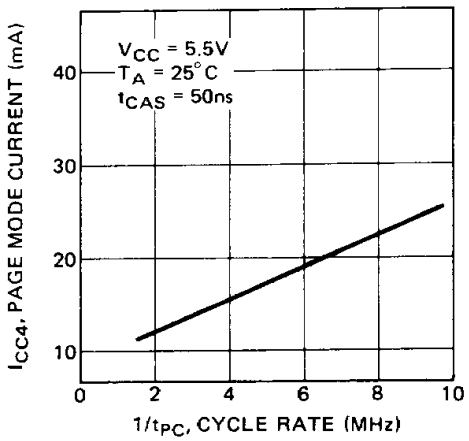


**Fig. 14 – PAGE MODE CURRENT vs SUPPLY VOLTAGE**

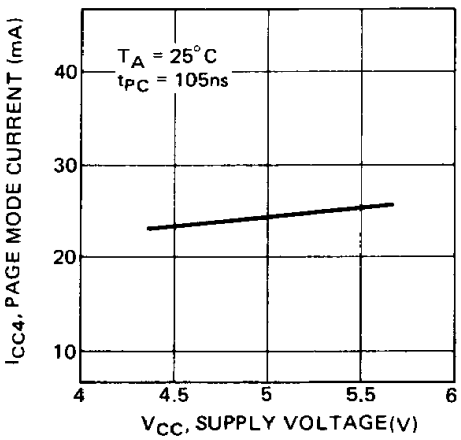




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**Fig. 15 – PAGE MODE CURRENT vs AMBIENT TEMPERATURE**

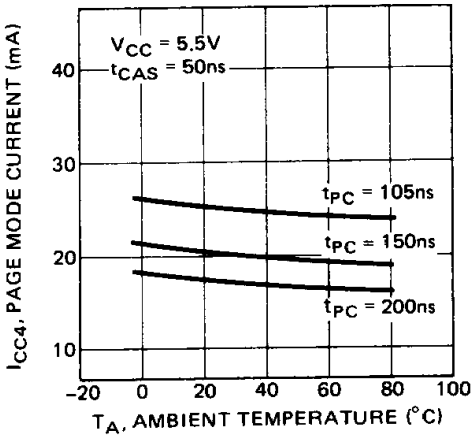


**Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE**

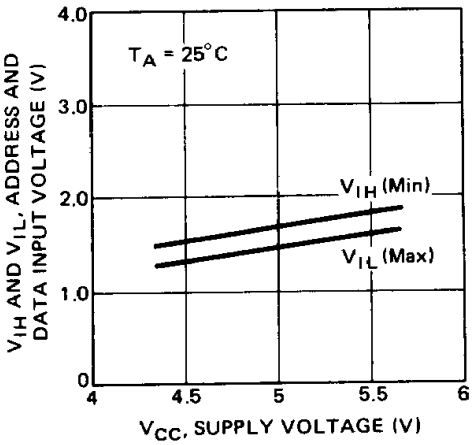


**Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE**

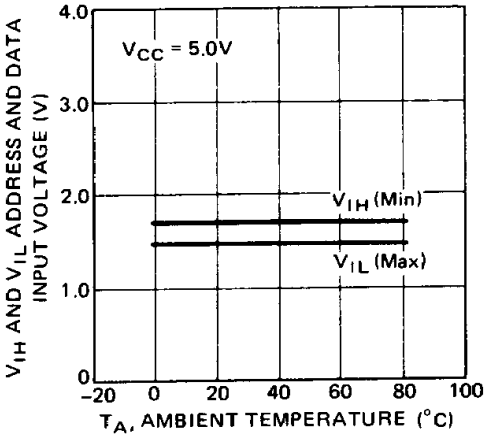


**Fig. 18 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE**

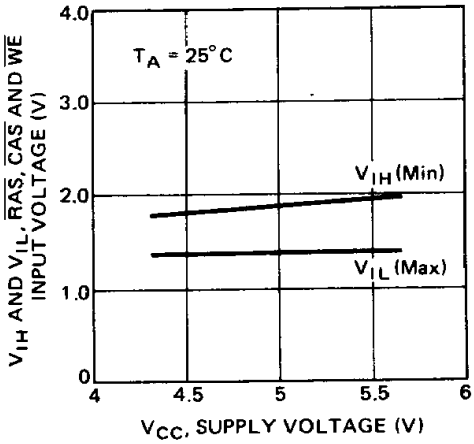


**Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ VOLTAGE vs AMBIENT TEMPERATURE**

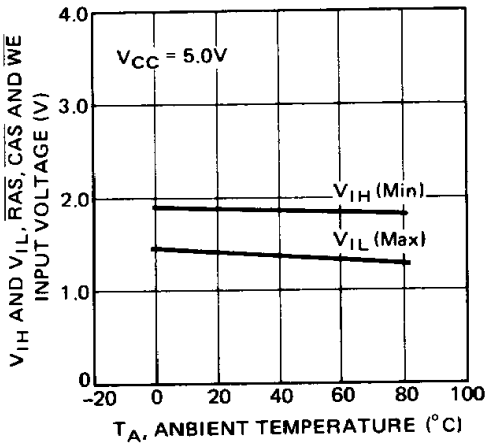




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Fig. 20 — CURRENT WAVE FORM DURING POWER UP

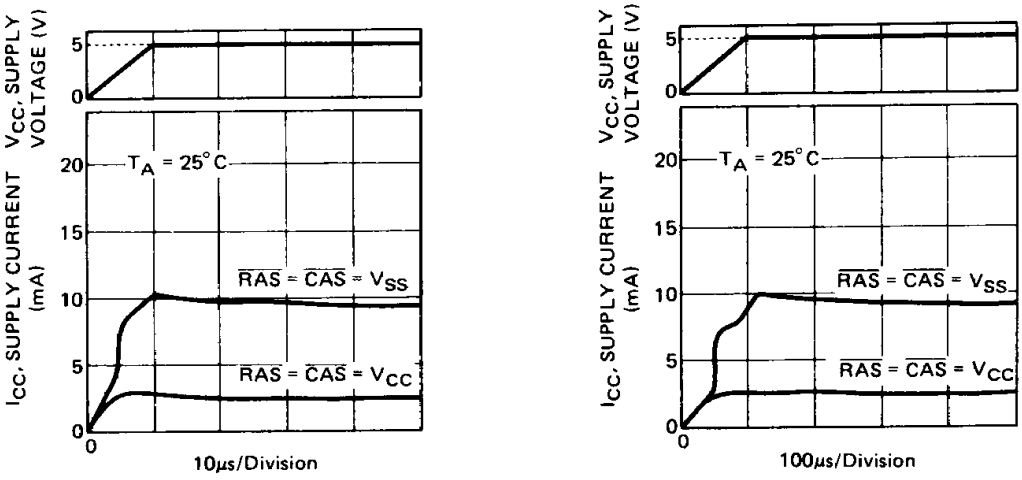



Fig. 21 — CURRENT WAVE FORM DURING POWER UP (ON MEMORY BOARD)

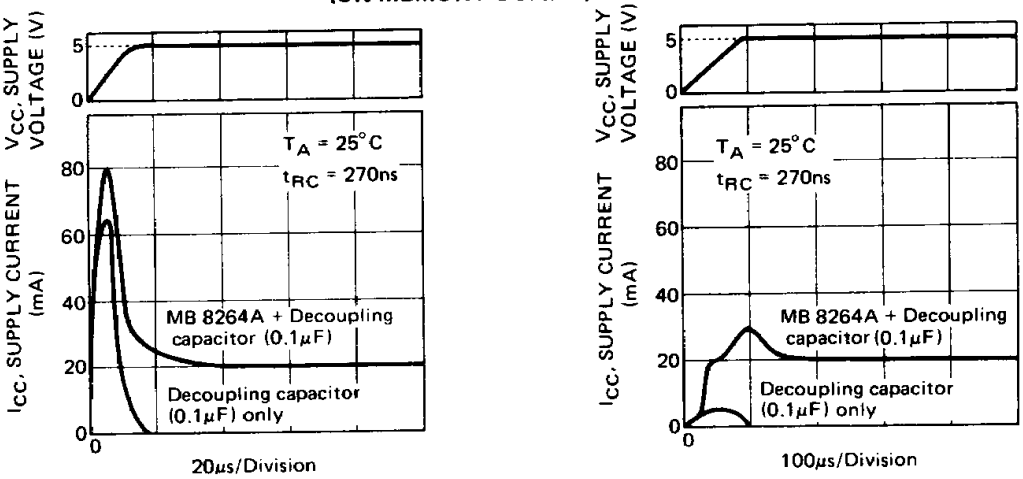
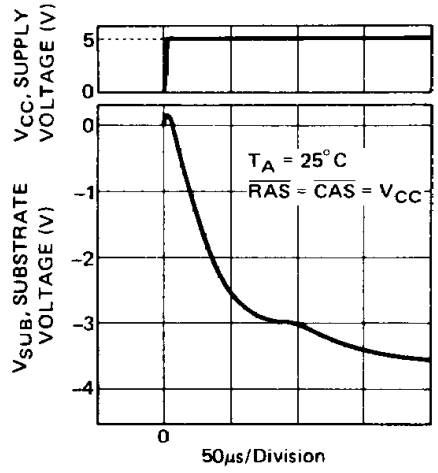



Fig. 22 — SUBSTRATE VOLTATE vs SUPPLY VOLTAGE (DURING POWER UP)



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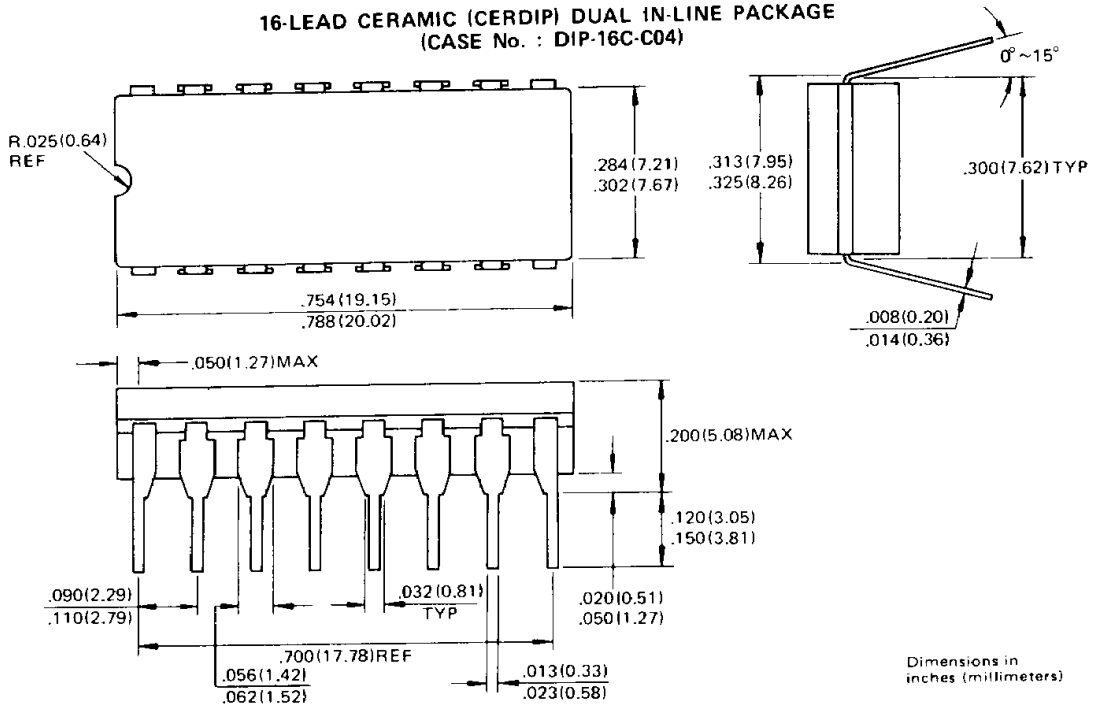
# PACKAGE DIMENSIONS

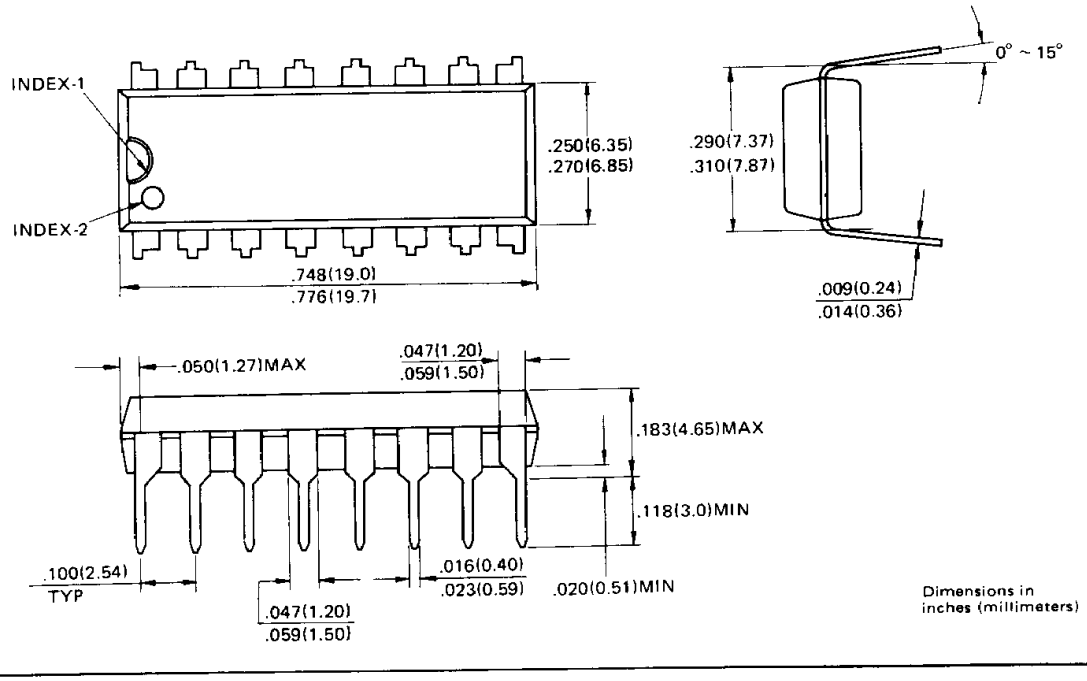
**Standard 16-pin Ceramic DIP (Surfix : -Z)**

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C04)




**Standard 16-pin Plastic DIP (Surfix : -P)**

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



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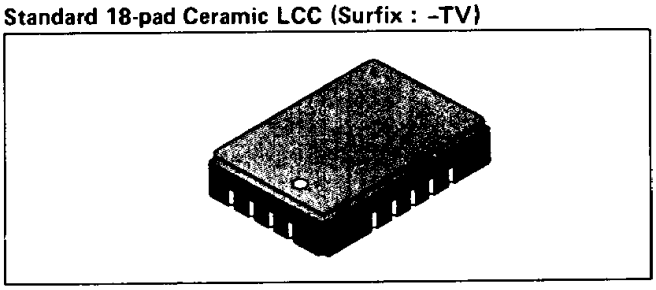
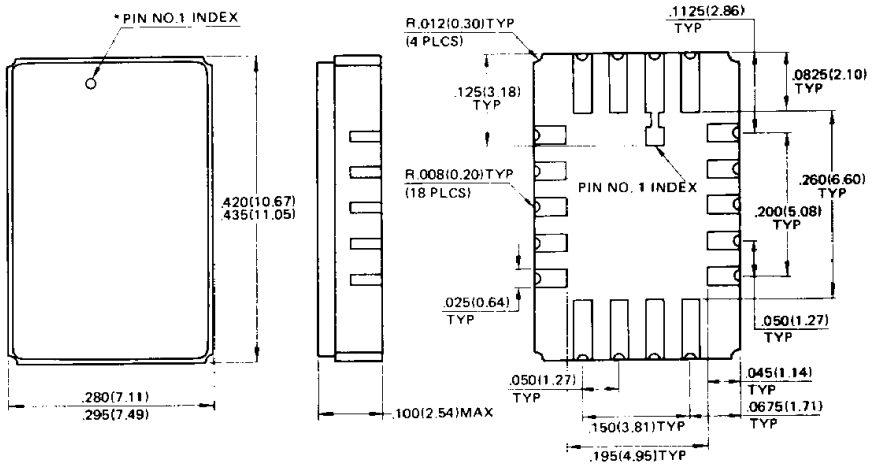
# PACKAGE DIMENSIONS

**Standard 18-pad Ceramic LCC (Surfix : -TV)**



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)




*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)



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