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SP1648

ECL OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of an inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

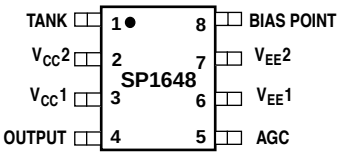
The SP1648 may be operated from a +5.0V dc supply or a -5.2V dc supply, depending upon system requirements.

Operating temperature range: 0°C to +75°C (Plastic)

Supply voltage	GND PINS	SUPPLY PINS
+5.0V dc	6,7	2,3
-5.2V dc	2,3	6,7

ORDERING INFORMATION

SP1648 MP (Industrial - Miniature Plastic Package)



MP8

Fig.1 Pin connections (not to scale) - top view

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V_{CC} - V_{EE} +8.0V
Output source current<40mA
AGC input V_{CC} to V_{EE}
Storage temperature range-55°C to +150°C (Plastic)
Operating junction temperature MP<150°C

ELECTRICAL CHARACTERISTICS

Supply Voltage: +5.0V

Characteristic	Symbol	Pin under test	SP1648 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Max.	V_{CC}	I_L	V_{EE} (Gnd)
Power supply drain current	I_E	7	-	-	-	40	-	-	mAdc	-	-	2,3	-	6,7
Logic '1' output voltage	V_{OH}	4	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	-	1	2,3	3	6,7
Logic'0' output voltage	V_{OL}	4	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	1	-	2,3	3	6,7
Bias voltage	V_{bias}*	8	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	-	-	2,3	-	6,7
			Min.	Typ. Max.	Min.	Typ. Max.	Min	Typ. Max.						
Peak-to-peak tank voltage	V_{p-p}	1	-	- -	-	500 -	-	- -	mV	see Fig.4	-	2,3	3	6,7
Output duty cycle	V_{DC}	4	-	- -	-	50 -	-	- -	%	see Fig.4	-	2,3	3	6,7
Oscillation frequency	f_{max}	-	-	- -	200	225 -	-	- -	MHz	see Fig.4	-	2,3	3	6,7

Test temp.	V_{IH} Max.	V_{IL} Min.	V_{CC}	I_L
-30°C	+1.960	+1.410	5.0	5.0
+25°C	+1.800	+1.300	5.0	5.0
+85°C	+1.680	+1.180	5.0	5.0

Thermal Characteristics:

MP8 Θ_{JA} = 163°C/W
Θ_{JC} = 57°C/W

Supply Voltage: -5.2V

Characteristic	Symbol	Pin under test	SP1648 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Max.	V_{CC}	I_L	V_{EE} (Gnd)
Power supply drain current	I_E	7	-	-	-	41	-	-	mAdc	-	-	6,7	-	2,3
Logic '1' output voltage	V_{OH}	4	1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	-	1	6,7	3	2,3
Logic'0' output voltage	V_{OL}	4	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	1	-	6,7	3	2,3
Bias voltage	V_{bias}*	8	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	-	-	6,7	-	2,3
			Min.	Typ. Max.	Min.	Typ. Max.	Min	Typ. Max.						
Peak-to-peak tank voltage	V_{p-p}	1	-	- -	-	500 -	-	- -	mV	see Fig.4	-	6,7	3	2,3
Output duty cycle	V_{DC}	4	-	- -	-	50 -	-	- -	%	see Fig.4	-	6,7	3	2,3
Oscillation frequency	f_{max}	-	-	- -	200	225 -	-	- -	MHz	see Fig.4	-	6,7	3	2,3

Test temp.	V_{IH} Max.	V_{IL} Min.	V_{CC}	I_L
-30°C	-3.240	-3.790	5.2	5.0
+25°C	-3.400	-3.900	5.2	5.0
+85°C	-3.520	-4.020	5.2	5.0

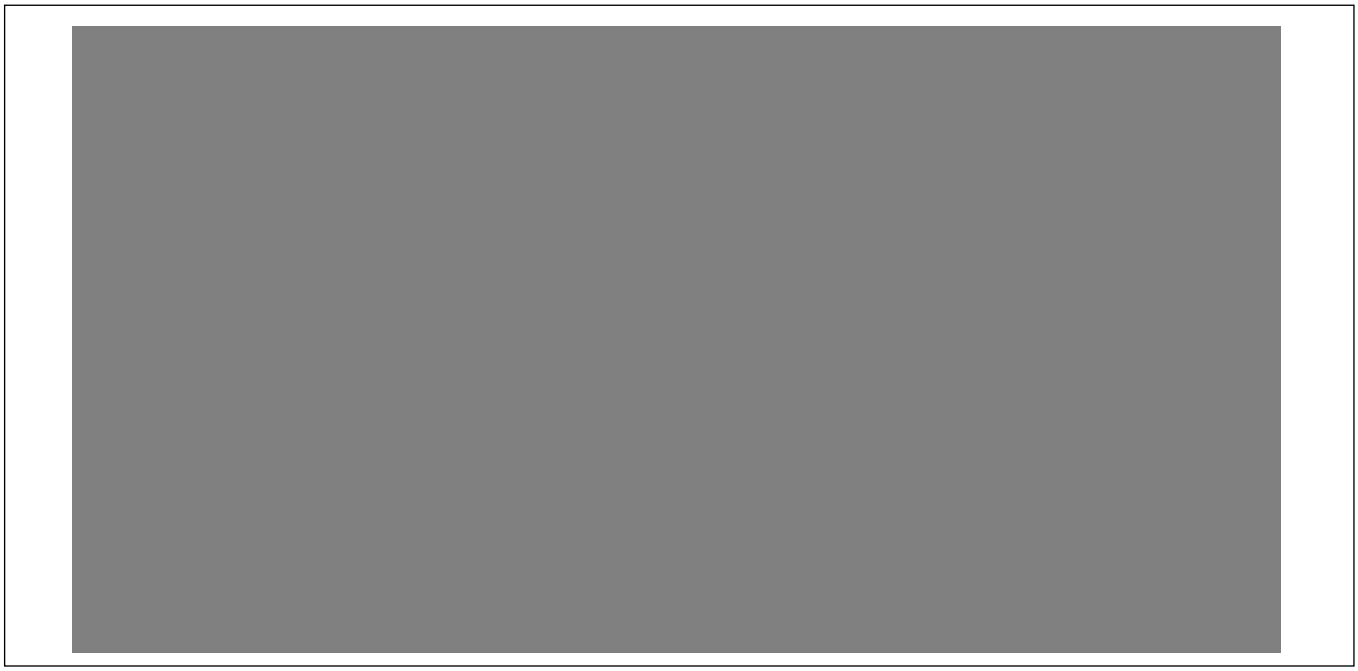


Fig.3 Spectral purity of signal at output

OPERATING CHARACTERISTICS

Fig.2 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 through TR14 provide this bias drive for the oscillator and output buffer. Fig.3 indicates the high spectral purity of the oscillator output.

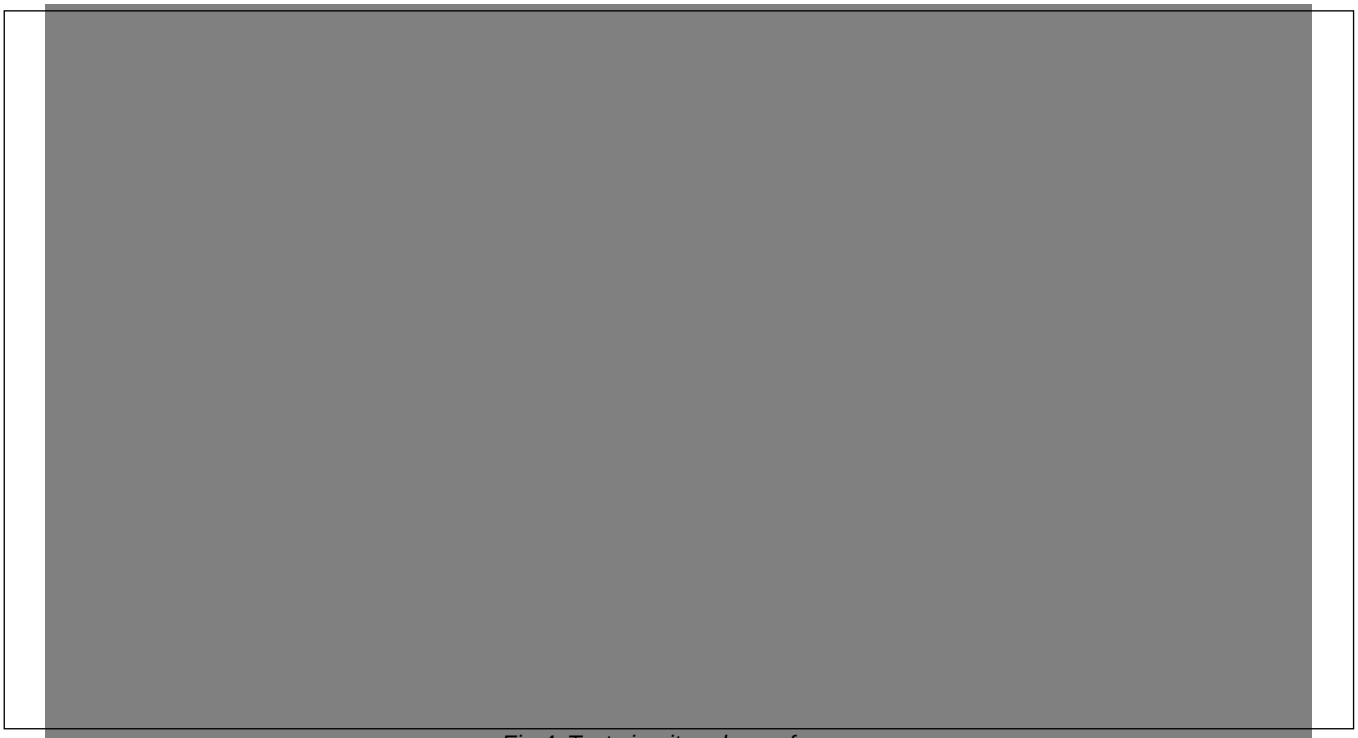


Fig.4 Test circuit and waveforms

When operating the oscillator in the voltage controlled mode (Fig.5), it should be noted that the cathode of the varactor diode, (D) should be biased at least $2V_{BE}$ above V_{EE} (≈1.4v for positive supply operation).

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Fig.6.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figs.7, 8 and 9. Figs.7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6pF typical). Fig.8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1kΩ resistor in Figs.7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51kΩ) in Fig.9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\,(max) + C_S}}{\sqrt{C_D\,(min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L(C_D\,(max) + C_S)}}$

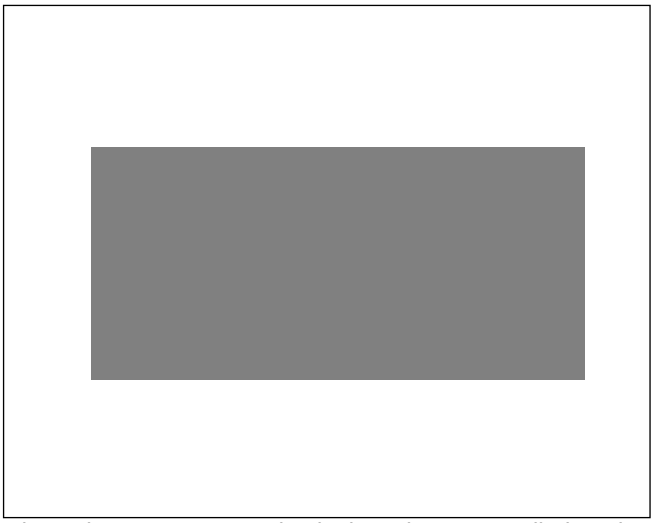


Fig.5 The SP1648 operating in the voltage-controlled mode

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Fig.3).

Capacitors (C1 and C2 of Fig.5) should be used to by-pass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

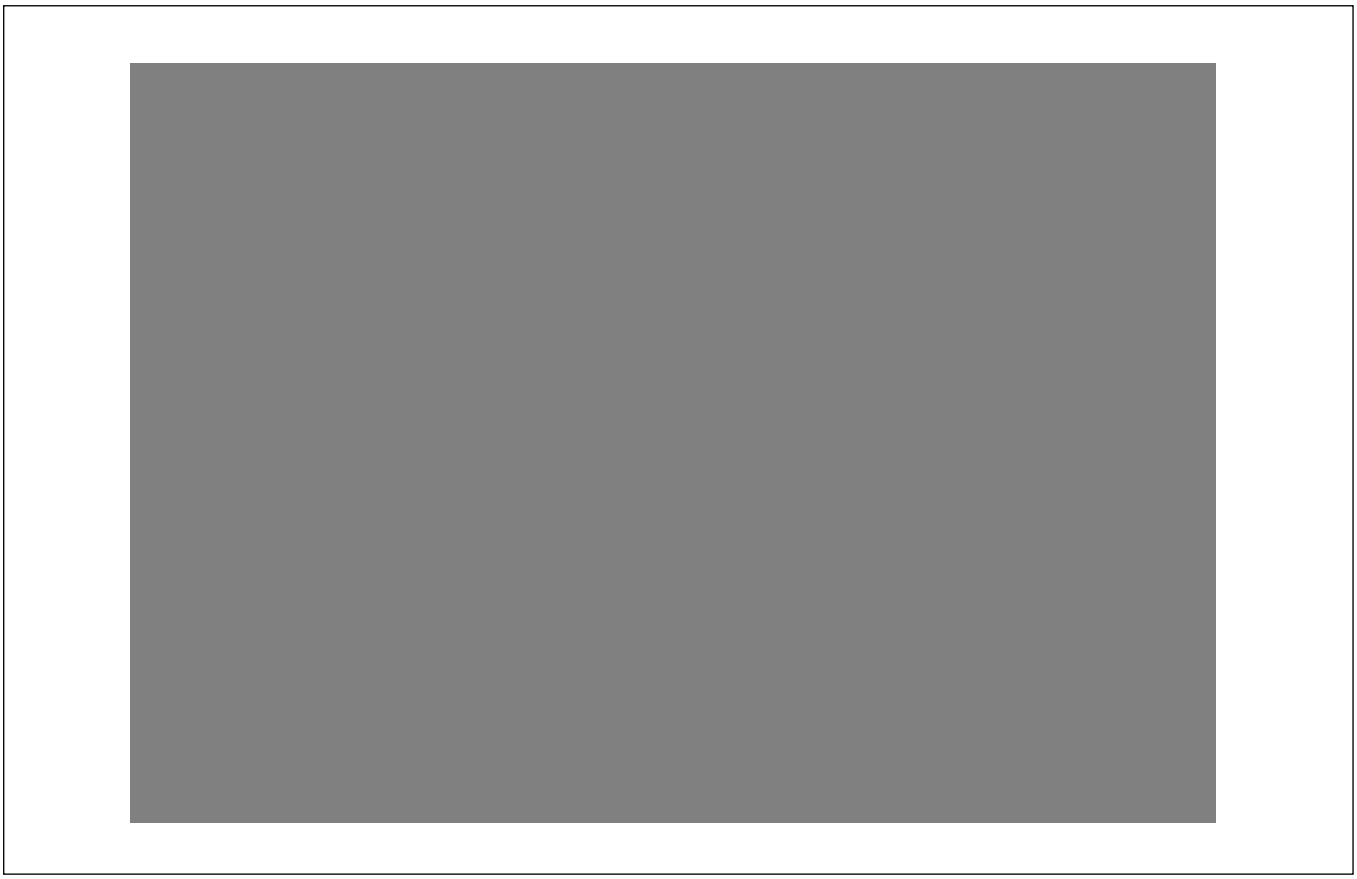


Fig.6 Frequency deviation test circuit

Fig.7

Fig.8

Fig.9

For output frequency operation between 1MHz and 50MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All by-passing should be as close to the package pins as possible to minimise unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0V supply is used, -5.2V if a negative supply is used).

At frequencies above 100MHz typ. it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by attaching a series resistor (1kΩ minimum) from the AGC to the most positive power potential (+5.0V if a +5.0V supply is used, ground if a -5.2V supply is used).

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