CONTROL CIRCUIT FOR SMPS

GENERAL DESCRIPTION

The TDA1060 is a bipolar integrated circuit intended for the control of a switched-mode power supply. It incorporates all the control functions likely to be required in switched-mode power supplies for professional equipment.

Features

- Suitability for a wide range of supply voltages
- Built-in stabilized power supply for external circuitry
- Built-in temperature-compensated voltage reference
- Adjustable frequency
- Adjustable control loop sensitivity
- Adjustable pulse width
- Adjustable maximum duty factor
- Adjustable overcurrent protection limit
- Low supply voltage protection with hysteresis
- Loop fault protection
- Slow-start facility
- Feed-forward facility
- Core saturation protection facility
- Overvoltage protection facility
- Remote ON/OFF switching facility

QUICK REFERENCE DATA

Supply voltage (voltage source)	V_{CC}	max.	18 V
Supply current (current source)	I_{CC}	max.	30 mA
Output current	$-I_{14}; I_{15}$	max.	40 mA
Stabilized voltage	V_Z	typ.	8,4 V
Reference voltage	V_{ref}	typ.	3,72 V
Output pulse repetition frequency range	f_o	50 Hz to 100	kHz
Operating ambient temperature range			
TDA1060; T	T_{amb}	−25 to + 125	°C
TDA1060A	T_{amb}	0 to + 70	°C
TDA1060B	T_{amb}	−55 to + 150	°C

PACKAGE OUTLINES

TDA1060, TDA1060A: 16-lead DIL; plastic (SOT38).
TDA1060B: 16-lead DIL ceramic (cerdip) (SOT74).
TDA1060T: 16-lead mini-pack; plastic (SO16; SOT109A).

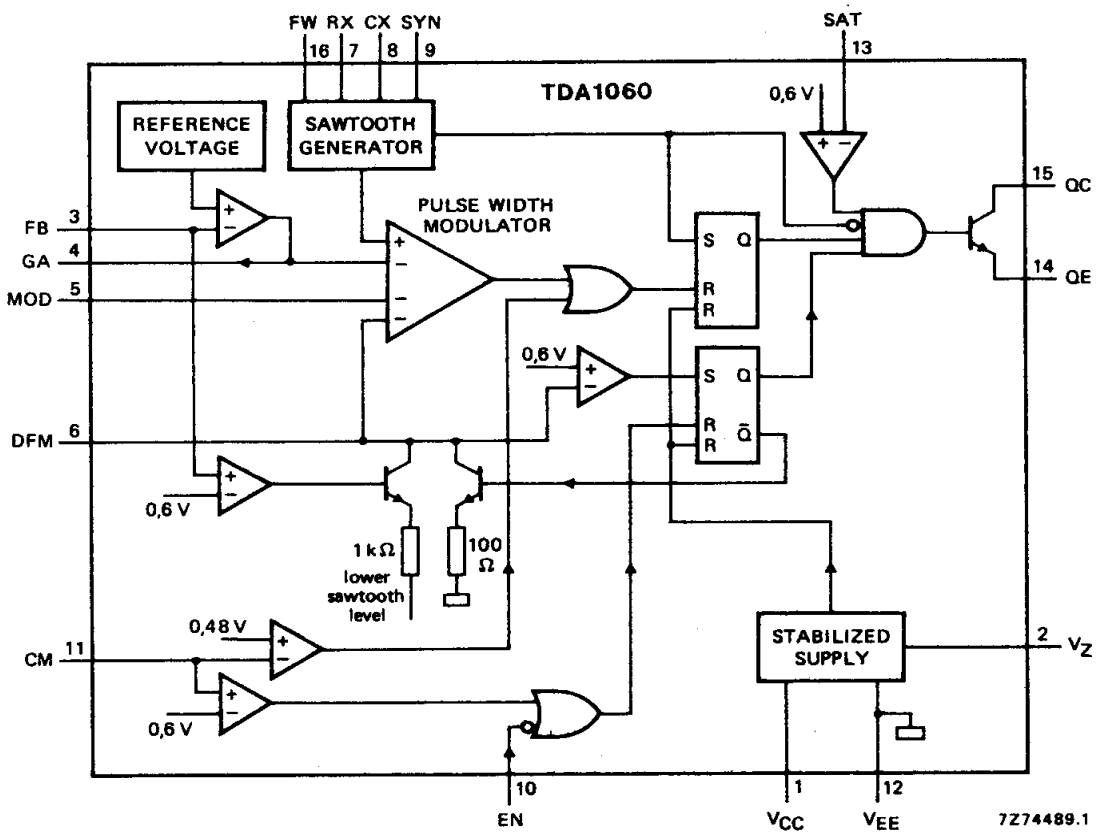

Fig. 1 Block diagram.

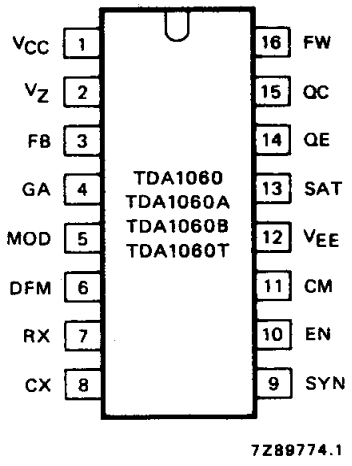

Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply connection
2	V_Z	stabilized voltage output
3	FB	feedback input
4	GA	gain adjustment output
5	MOD	modulation input
6	DFM	maximum duty factor input
7	RX	external resistor connection
8	CX	external capacitor connection
9	SYN	synchronization input
10	EN	ENABLE input
11	CM	overcurrent protection input
12	V_{EE}	common
13	SAT	core saturation and overvoltage protection input
14	QE	emitter output
15	Q_C	collector output
16	FW	feed-forward input

FUNCTIONAL DESCRIPTION

The TDA1060 contains the control loop for a fixed-frequency pulse-duration regulated SMPS. The device works as follows. The output voltage V_O of the SMPS is sensed via a feedback network and compared with an internal reference voltage V_{ref}. Any difference between V_O and V_{ref} is amplified and fed to a pulse-width modulator (PWM), where it is compared with the instantaneous level of a ramp waveform (sawtooth) from an oscillator. The output from the PWM is a rectangular waveform synchronized with the oscillator waveform; its duty factor depends on the difference between V_O and V_{ref}. This signal drives the base of the SMPS power switching transistor so that its conduction period and hence the amount of energy transferred from the input to the output of the SMPS is controlled, resulting in a constant output voltage.

Stabilized power supply: V_{CC} and V_Z (pins 1 and 2)

The circuit contains a voltage/current regulator and may be supplied either by a current source (e.g. a series resistor connected to the high voltage input of the SMPS), or a voltage source (e.g. a 12 V battery).

The stabilized voltage, typically 8,4 V, is also available at V_Z, pin 2 for supplying external circuitry, e.g. a potentiometer to adjust the maximum duty factor. This supply output is protected against short-circuits. The current drawn from this output increases the total IC supply current by the same amount.

When the supply voltage V_{CC} becomes too low, i.e. $V_{CC} < V_Z + 0{,}2$ V, the circuit is automatically switched off. As soon as the supply voltage exceeds this threshold value by more than 0,2 V the circuit starts the SMPS via the slow start procedure.

Operating frequency: RX and CX (pins 7 and 8)

The frequency of the sawtooth generator, and hence of the output pulses, is set by an external resistor R7 at RX, pin 7, and an external capacitor C8 at CX, pin 8 (see Fig. 7). The frequency may be set between 50 Hz and 100 kHz and is virtually independent of the supply voltage.

Maximum duty factor and slow start: DFM (pin 6)

The maximum duty factor is set by the voltage on the duty factor input DFM (see Fig. 4). This voltage usually is derived from the stabilized power supply V_Z, pin 2, by an external voltage divider, see Fig. 8. As the upper and lower levels of the sawtooth waveform are set by an internal voltage divider, the accuracy of the maximum duty factor setting is determined by resistor ratios rather than by absolute values.

In case of a short-circuited feedback loop ($V_{3\text{-}12}$ less than typ. 600 mV) the duty factor input is internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ. The maximum duty factor permitted in that case sets a maximum limit to the impedance level of the external voltage divider at pin 6.

During the flyback of the sawtooth the output pulse is inhibited. For a 1 nF capacitor C8 at pin 8 this flyback time is 1 μs. This sets a natural limit to the duty factor.

The time constant for the slow start is determined by an external capacitor connected between the maximum duty factor input DFM and V_{EE}, pin 12, together with the impedance of the voltage divider at pin 6. This capacitor also determines the dead time before the slow start procedure for remote ON/OFF or when the current sensing voltage has exceeded 600 mV, see below.

If the DFM input is note used it should be connected to V_Z via a resistor of 5 kΩ.

FUNCTIONAL DESCRIPTION (continued)

Control loop sensitivity, stability, and feedback loop fault protection, FB and GA (pins 3 and 4)

The device contains a control loop error amplifier, i.e. a differential amplifier that compares the voltage on the feedback input FB, pin 3, with the internal reference voltage. This reference voltage is a temperature-compensated voltage source based on the band-gap energy of silicon.

The control loop sensitivity is determined by the closed-loop gain A_f of the error amplifier. Normally the output from the SMPS is connected to the feedback input FB via a voltage divider and a series resistor. The closed-loop gain of the error amplifier is set by applying feedback from the gain adjustment output GA, pin 4, to the feedback input FB by a resistor R3-4, see Fig. 8.

To avoid instability a capacitor should be connected between the gain output GA and V_{EE}, pin 12. A 22 nF capacitor will cause the frequency response to fall off above 600 Hz.

The feedback input FB is internally biased to the HIGH level, this gives a protection against a feedback loop fault: an open feedback loop will make the duty factor zero.

A shorted feedback loop (feedback voltage less than typ. 600 mV) causes the maximum duty factor input DFM to be internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ, thus substantially reducing the maximum duty factor. This duty factor will then be determined by the impedance of the external voltage divider at DFM, pin 6, and the internal biasing resistor.

Overcurrent protection input CM (pin 11)

There are two current limits, corresponding with voltages on the overcurrent protection input CM of typ. 480 mV and 600 mV. As soon as the voltage on this input exceeds 480 mV, the running output pulse is immediately terminated; the next pulse starts normally at the next period. If the voltage exceeds 600 mV, the output pulses are inhibited for a certain dead time, during which the slow start capacitor at pin 6 is unloaded. After this the circuit starts again with the slow start procedure.

If the overcurrent protection input CM is not used, it should be connected to V_{EE}, pin 12.

Feed-forward input FW (pin 16)

The feed-forward input FW can be connected to an external voltage divider from the input voltage of the SMPS, see Fig. 8. It has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on the feed-forward input increases, the upper level of the sawtooth is also increased. Since neither the voltage level that sets the maximum duty factor nor the feedback voltage are influenced by the feed-forward, the duty factor reduces (see Fig. 6). This can therefore compensate for mains voltage variations.

If feed-forward is not required the feed-forward input FW should be connected to V_{EE}, pin 12.

Synchronization input SYN (pin 9)

The frequency of the sawtooth waveform, and hence of the output pulses, can be synchronized via the TTL compatible synchronization input SYN. The synchronizing frequency must be lower than the oscillator free-running frequency. When the synchronization input is LOW the sawtooth generator is stopped; it starts again when the input goes HIGH. Synchronization pulses do not influence the slope of the sawtooth, and hence not the width of the output pulses, they only change their separation in time.

For free-running operation it is advisable to connect the synchronization input SYN to V_Z, pin 2.

Core saturation and overvoltage protection input SAT (pin 13)

To obtain a protection against core saturation, especially during transient conditions, the output transformer of the SMPS has to be fitted with a winding serving as a current sensor. Its output voltage is rectified and fed to the SAT input.

This core saturation protection may be combined with an overvoltage protection. To this end a portion of the SMPS output voltage is also fed to the SAT input either via a voltage divider or via a suitable regulator diode (zener diode). The output pulses are inhibited as long as the voltage on this input exceeds the threshold voltage, typ. 600 mV.

The voltage at the SAT input does not influence the frequency of the sawtooth generator and hence not of the output pulses.

If none of these protection facilities are used, the SAT input should be connected to V_{EE}, pin 12.

Remote ON/OFF switching: ENABLE input EN (pin 10)

The output pulses can be switched on and off by applying logic levels to the TTL compatible ENABLE input. A LOW level causes immediate inhibition of the output pulses, a subsequent HIGH level switches the circuit on with the slow-start procedure.

If this facility is not required, EN should be connected to V_Z, pin 2.

Modulation input MOD (pin 5)

The duty factor of the output pulses may be reduced below the value resulting from the voltages on the maximum duty factor input DFM and the gain adjust output GA by applying a lower voltage to the modulation input MOD. This input may be used with an external control loop, e.g. for constant-current control, or to obtain a fold-back characteristic.

If the modulation input is not used, it should be connected to V_Z, pin 2.

Output QC and QE (pins 13 and 14)

To avoid double pulses that might occur at an excessively low mains voltage or an excessively high output current the output is preceded by a latch. The two outputs offer a choice of output current polarity, QC giving a positive current, i.e. a current flowing into the output, and QE giving a negative current, a current flowing out of the output. The two connections have the additional advantage that the relatively large output currents do not flow through the V_{CC} and V_{EE} connections, where they could induce noise.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (voltage source)	V_{CC}	−0,5 to + 18	V
Supply current (current source)	I_{CC}	max. 30	mA
Feed-forward input voltage range			
$V_{CC} < 24$ V	$V_{16\text{-}12}$	0 to V_{CC}	V
$V_{CC} > 24$ V	$V_{16\text{-}12}$	0 to 24	V
Input voltage range (all other inputs)	V_I	0 to V_Z	V
Emitter output voltage range	$V_{14\text{-}12}$	0 to 5	V
Collector output voltage range	$V_{15\text{-}12}$	0 to V_{CC}	V
Output current			
d.c. (see Figs 3a, c and e)	$-I_{14}$; I_{15}	max. 40	mA
peak; t = max. 1 μs; duty factor d < 10%	$-I_{14}$; I_{15}	max. 200	mA
Storage temperature range			
TDA1060; T	T_{stg}	−55 to + 150	°C
TDA1060A	T_{stg}	−55 to + 150	°C
TDA1060B	T_{stg}	−55 to + 150	°C
Operating ambient temperature range			
TDA1060; T	T_{amb}	−25 to + 125	°C
TDA1060A	T_{amb}	0 to + 70	°C
TDA1060B	T_{amb}	−55 to + 150	°C
Power dissipation (see Figs 3b, d and f)	P_{tot}	max. 1	W

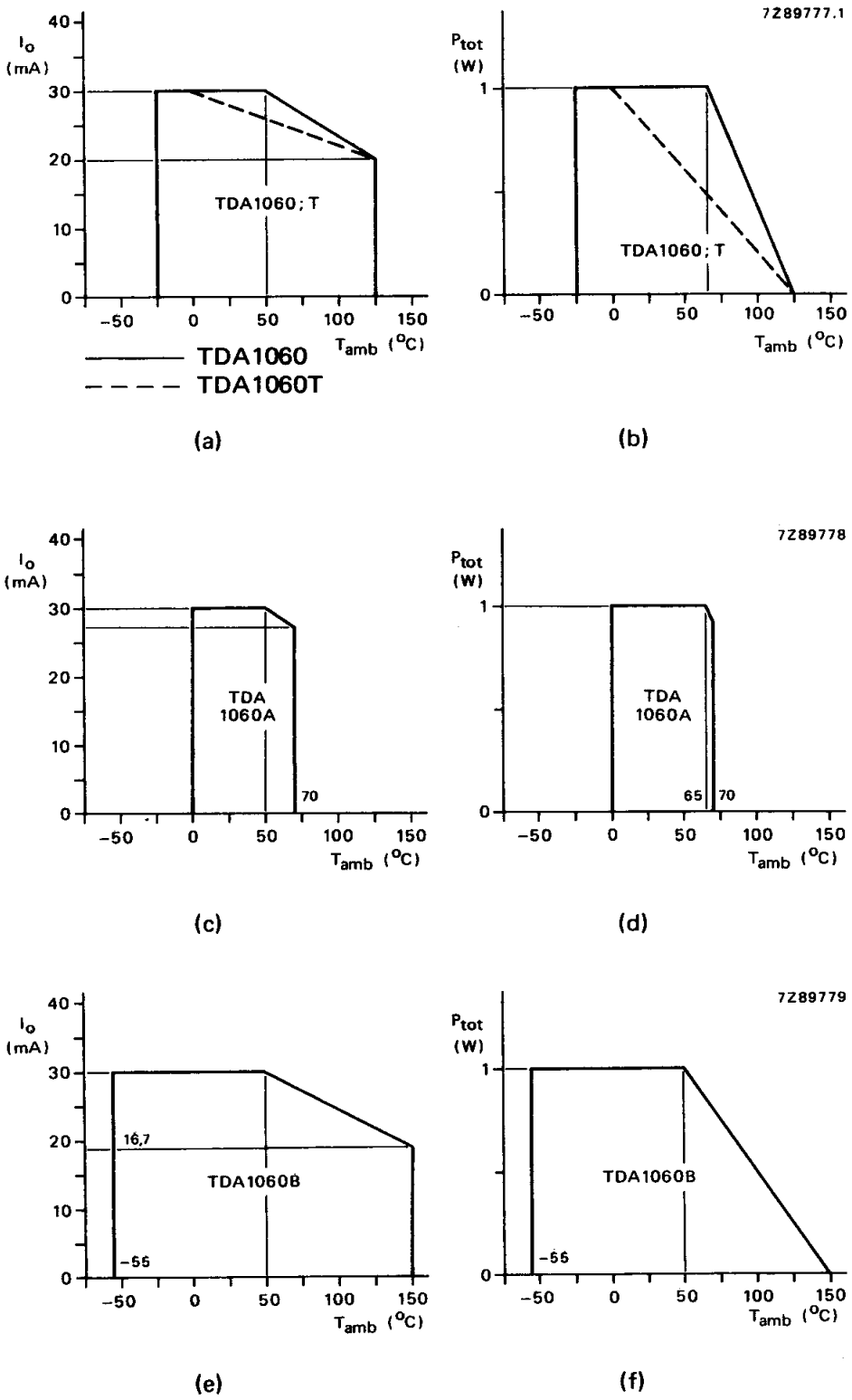

Fig. 3 Output current and power dissipation derating curves.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = operating ambient temperature range, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating ambient temperature range					
TDA1060; T	T_{amb}	−25	–	125	°C
TDA1060A	T_{amb}	0	–	70	°C
TDA1060B	T_{amb}	−55	–	150	°C
Supply V_{CC} (pin 1)					
Supply voltage at I_{CC} = 15 mA					
TDA1060; T	V_{CC}	18,5	23	27	V
TDA1060A	V_{CC}	18,5	23	27	V
TDA1060B	V_{CC}	18	23	27,5	V
at I_{CC} = 30 mA					
TDA1060; T	V_{CC}	19,5	24	29	V
TDA1060A	V_{CC}	19,5	24	29	V
TDA1060B	V_{CC}	19	24	29,5	V
Supply current; R7 = 25 kΩ; duty factor δ = 50%; I_Z = 0; at T_{amb} = 25 °C	I_{CC}	2,5	–	10	mA
over ambient temperature range	I_{CC}	2,5	–	15	mA
Threshold voltage of low supply voltage protection at T_{amb} = 25 °C	V_{CC}	8,85	–	10,8	V
Variation with temperature	$-\Delta V_{CC}/\Delta T$	–	7,5	–	mV/K
Hysteresis of low supply voltage protection	ΔV_{CC}	–	500	–	mV
Stabilized supply output V_Z (pin 2)					
Output voltage at T_{amb} = 25 °C	V_Z	7,5	8,4	9	V
Variation with temperature	$\Delta V_Z/\Delta T$	−1,5	–	+ 1,5	mV/K
Output current	$-I_Z$	–	–	5	mA
Feedback input FB (pin 3)					
Input voltage, feedback operation	$V_{3\text{-}12}$	2	–	V_Z-1	V
Input current at $V_{3\text{-}12}$ = 2 V	$-I_3$	1,5	12	35	μA
Internal reference voltage, measured at pin 3; pins 3 and 4 interconnected and grounded via a 100 nF capacitor; T_{amb} = 25 °C	V_{ref}	3,42	3,72	4,03	V
Variation with temperature	$\frac{\Delta V_{ref}/V_{ref}}{\Delta T}$	–	0,01	–	%/K
Variation with supply voltage	$\frac{\Delta V_{ref}}{\Delta V_{CC}}$	–	0,8	–	mV/V

parameter	symbol	min.	typ.	max.	unit
Long-term variation with time	$\pm \Delta V_{ref}/\Delta t$	–	2	–	μV/h
Threshold voltage of feedback loop short-circuit protection at $T_{amb} = 25\,^{o}C$	V_{3-12}	470	600	720	mV
Variation with temperature	$\frac{\Delta V_{3-12}/V_{3-12}}{\Delta T}$	–	0,01	–	%/K
Gain adjustment output GA (pin 4)					
Open-loop gain, pin 3 to pin 4	A_o	–	60	–	dB
External feedback resistance	R_{3-4}	10	–	–	kΩ
Modulator input MOD (pin 5)					
Input current at $V_{5-12} = 2$ V; $V_{4;6-12} > 2$ V	$-I_5$	–	–	5	μA
Maximum duty factor input DFM (pin 6)					
Input voltage for limiting the duty factor to 50%; f_o = 20 to 50 kHz; $V_{16-12} = 0$ V	V_{6-12}	–	$0{,}42V_Z$	–	V
Input current at $V_{6-12} = 2$ V	$-I_6$	–	–	6	μA
Capacitor discharge current during fault condition	I_6	2,5	–	–	mA
Minimum output OFF time at C7 = 1,8 nF	t_{off}	–	1	–	μs
Variation of max. duty factor with temperature at f_o = 20 kHz and δ_{max} = 50%	$\Delta\delta_{max}/\Delta T$	–	0,02	–	%/K
Internal biasing resistor to V_{EE} at $V_{3-12} = 0$ V	R_{6-12}	0,75	1	1,25	kΩ
Synchronization input SYN (pin 9)					
Input voltage, sawtooth ON	V_{IH}	2	–	V_Z	V
sawtooth OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{9-12} = 0$ V	$-I_{IL}$	20	–	120	μA
External resistor connection RX (pin 7)					
External frequency adjustment resistor	R7	5	–	40	kΩ
External capacitor connection CX (pin 8)					
Sawtooth, upper level at $V_{16-12} = 0$ V	V_{8-12}	–	5,7	–	V
lower level	V_{8-12}	–	1,3	–	V
Oscillator frequency R7 = 6,4 kΩ, C8 = 6,4 nF	f_{osc}	–	30,5	–	kHz
Output pulse repetition frequency range	f_o	0,05	–	100	kHz
Variation with temperature	$\frac{\Delta f_o/f_o}{\Delta T}$	–	0,03	–	%/K

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Feed-forward input FW (pin 16)					
Input voltage					
for $V_{CC} < 24$ V	V_{16-12}	0	–	V_{CC}	V
for $V_{CC} > 24$ V	V_{16-12}	0	–	24	V
Input current at $V_{16-12} = 16$ V; $V_{CC} = 18$ V; $T_{amb} = 25$ °C	I_{16}	–	–	5	μA
Frequency variation with input voltage at $V_{16-12} > 8$ V	$\frac{\Delta f_o/f_o}{\Delta V_{16-12}}$	–	1	–	%/V
Overcurrent protection input CM (pin 11)					
Input voltage	V_{11-12}	0	–	V_Z	V
Input threshold voltage for single pulse inhibit (current limit mode); $T_{amb} = 25$ °C	V_{T1}	400	–	500	mV
Ratio of threshold voltages for shot down/ slow start and for single pulse inhibit	V_{T2}/V_{T1}	–	1,25	–	
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{11-12} = 250$ mV	$-I_{11}$	–	–	10	μA
Turn-off delay, $I_{15} = 40$ mA; $V_{11-12} = 1{,}2 \times V_{T1}$	t_d	–	–	1,0	μs
Core saturation and overvoltage protection input SAT (pin 13)					
Input voltage	V_{13-12}	0	–	V_Z	V
Input threshold voltage at $T_{amb} = 25$ °C	V_{13-12}	470	600	720	mV
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{13-12} = 250$ mV	$-I_{13}$	–	–	7	μA
ENABLE input EN (pin 10)					
Input voltage					
ON	V_{IN}	2	–	V_Z	V
OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{10-12} = 0$ V	$-I_{IL}$	20	–	120	μA
Outputs QC and QE (pins 14 and 15)					
Output current	$-I_{14}; I_{15}$	40	–	–	mA
Emitter output voltage	V_{14-12}	–	–	5	V
Collector output voltage at $V_{14-12} = 0$ V; $I_{15} = 40$ mA	V_{15-14}	–	–	500	mV

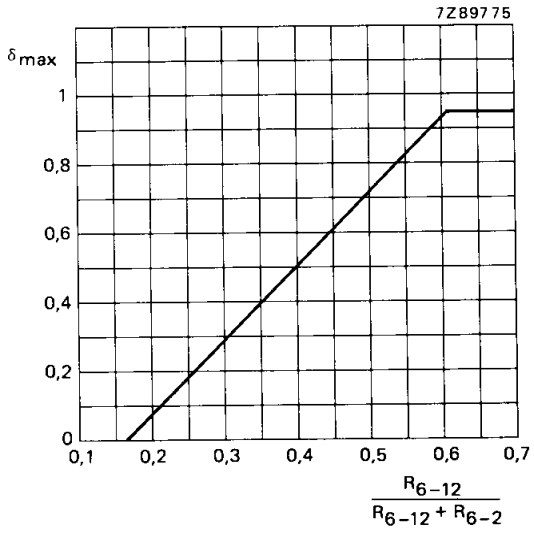

Fig. 4 Maximum duty factor δ_{max} as a function of the voltage divider ratio at the duty factor input DFM.

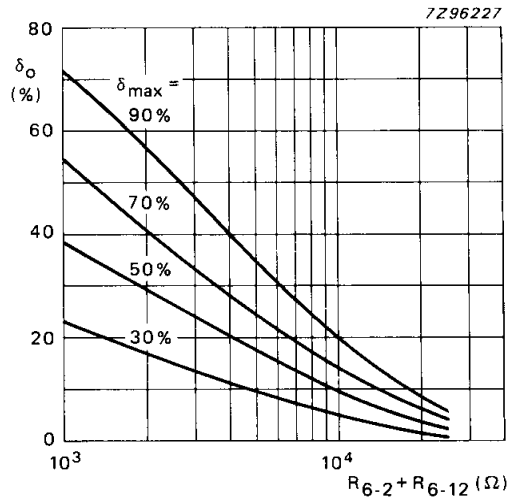

Fig. 5 Soft-start minimum duty factor (δ_o) as a function of R_{6-2} and R_{6-12}.

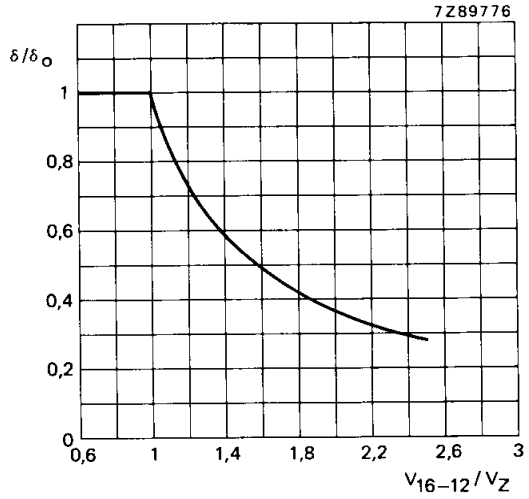

Fig. 6 Feed-forward regulation characteristic. Duty factor δ as a function of the voltage V_{16-12} on the feed-forward input FW. δ_o is the duty factor for $V_{16-12} \leqslant V_Z$.

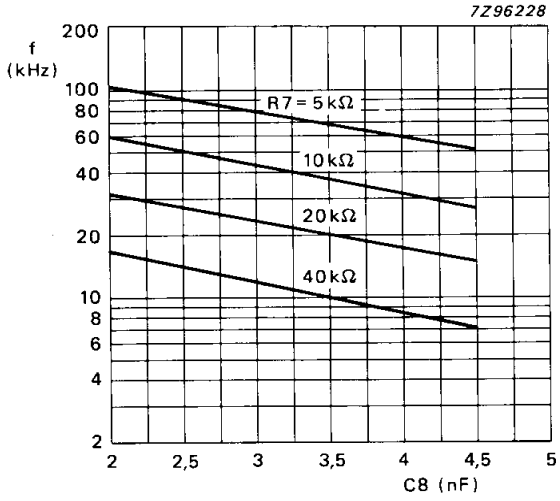

Fig. 7 Typical frequency as a function of C8 (R7 as parameter).

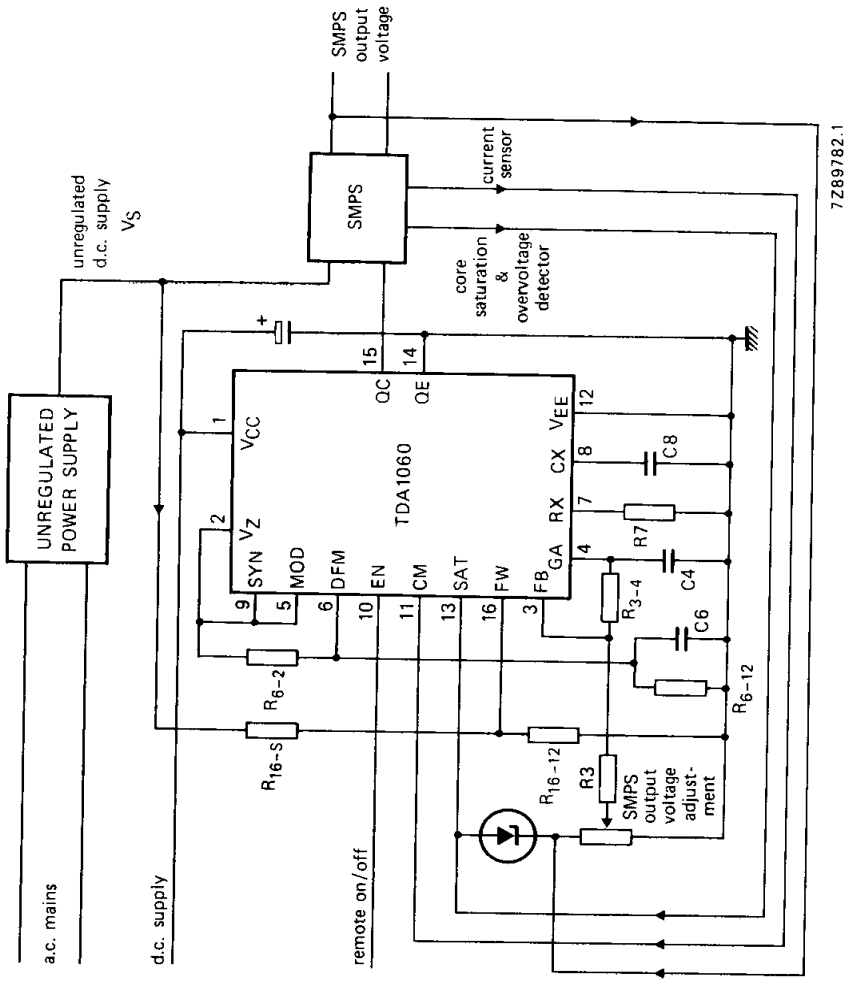

Fig. 8 Connections to the TDA1060 in a switched-mode power supply.

APPLICATION INFORMATION

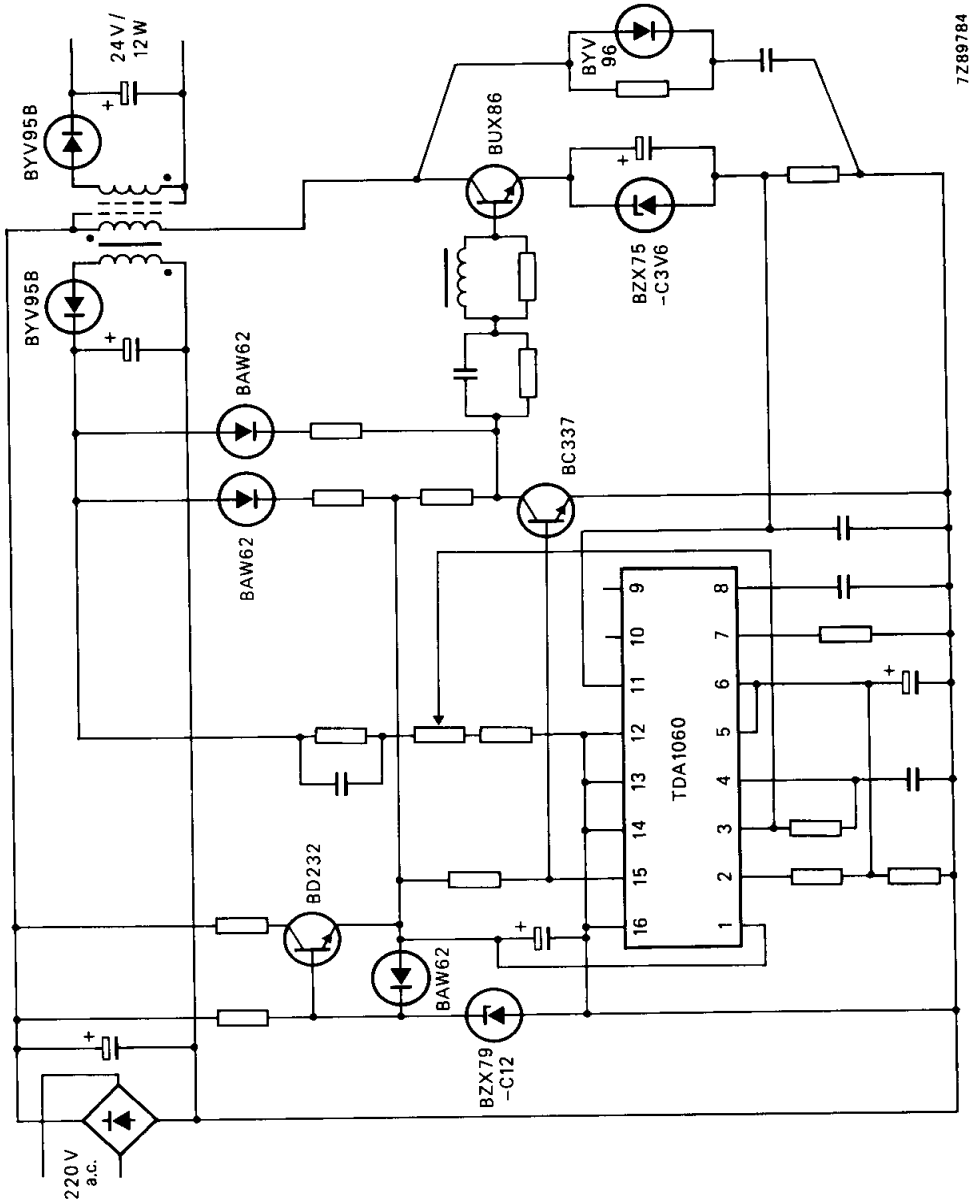

Fig. 9 Application of the TDA1060 in a 24 V, 12 W SMPS with flyback converter.

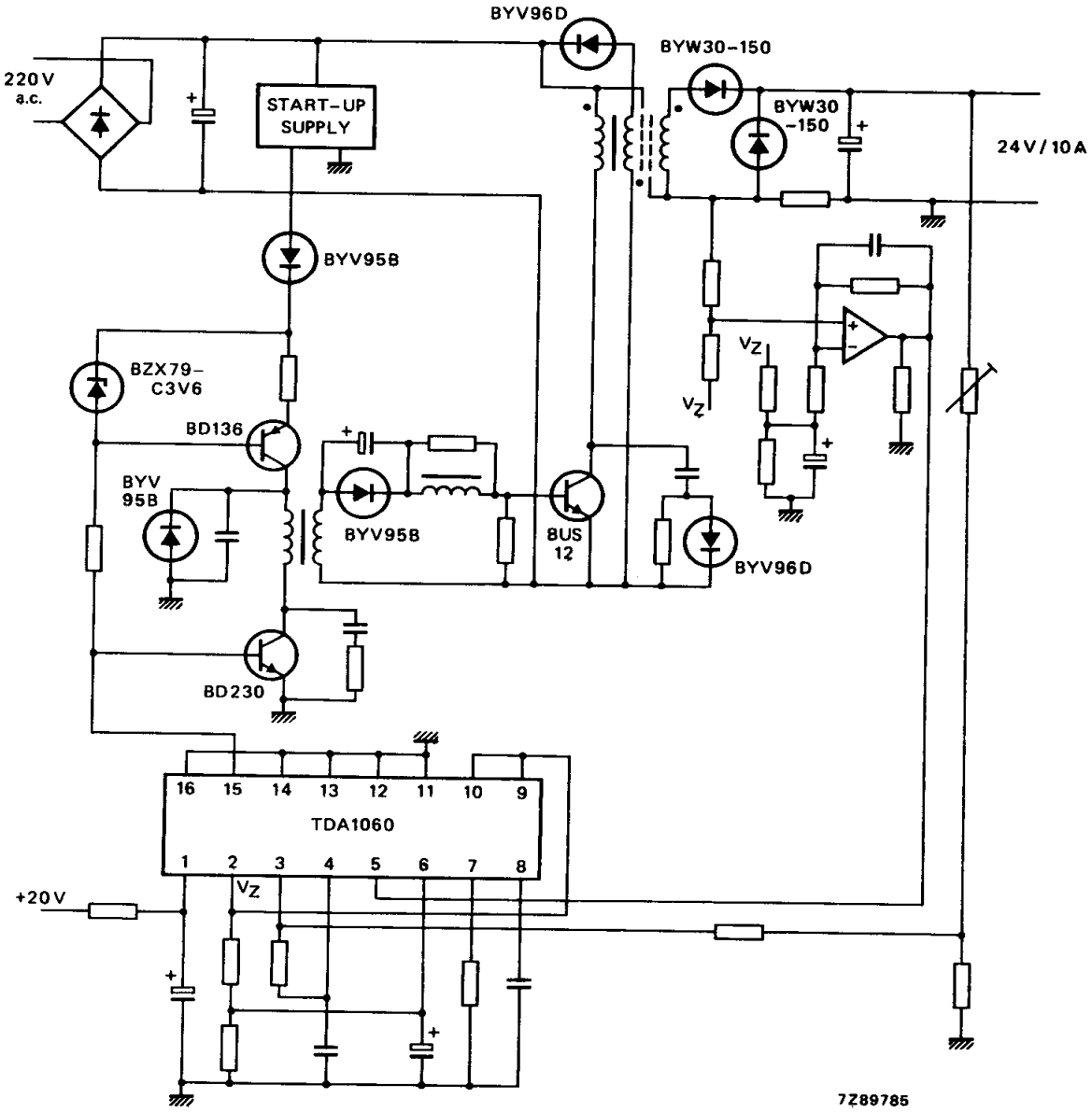

Fig. 10 Application of the TDA1060 in a 24 V, 240 W SMPS with forward converter.

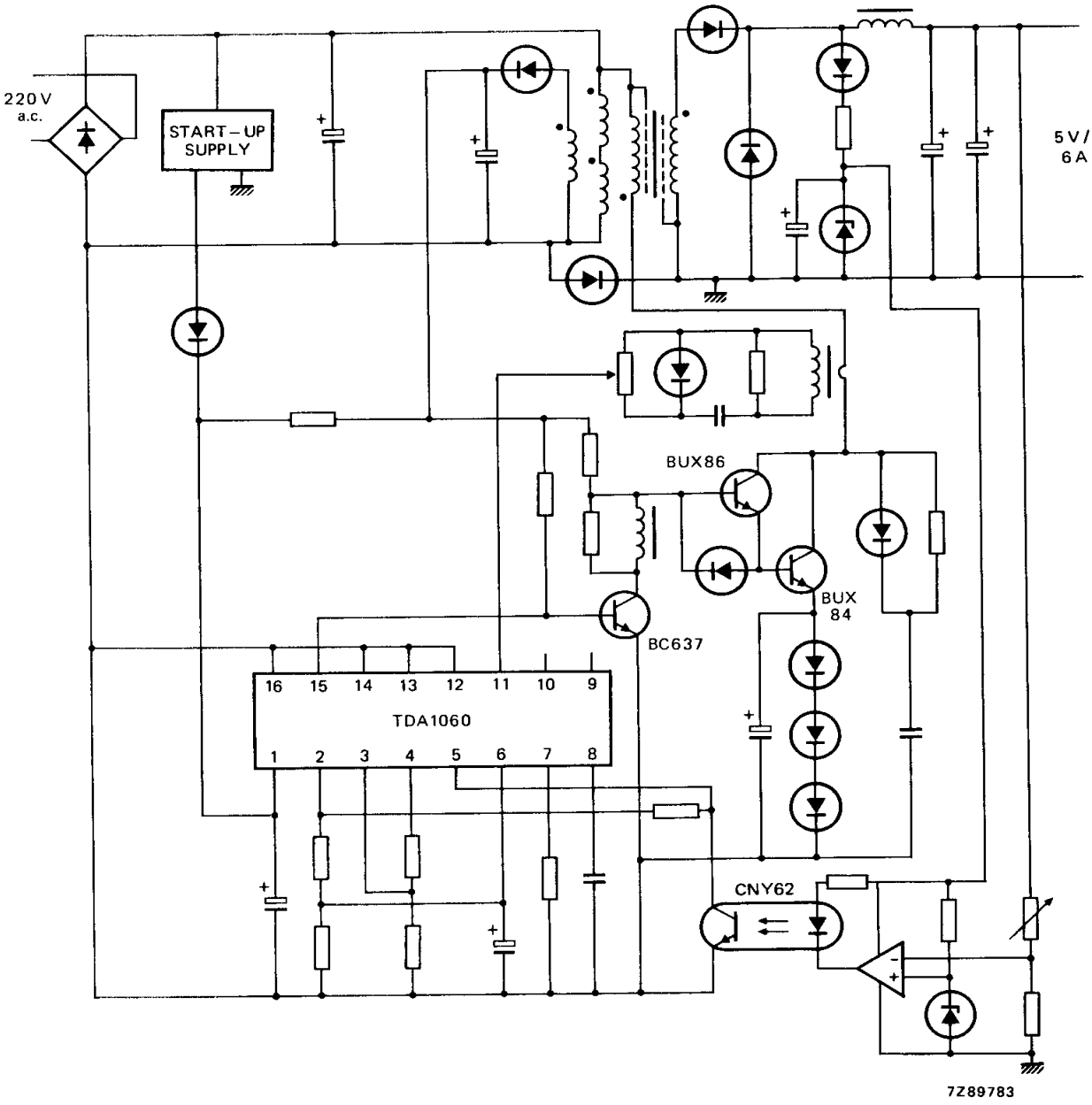

Fig. 11 Application of the TDA1060 in a 5 V, 30 W SMPS with forward converter and with an optocoupler CNY62 for voltage separation.

APPLICATION INFORMATION SUPPLIED UPON REQUEST.