

## 4-Mbit (512K x 8) Static RAM

### Features

- **High Speed: 70 ns**
- **4.5V–5.5V operation**
- **Low active power**
  - Typical active current: 2.5 mA @ f = 1 MHz
  - Typical active current: 12.5 mA @ f = f<sub>max</sub>(70 ns)
- **Low standby current**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **CMOS for optimum speed/power**
- **Available in standard 32-lead (450-mil) SOIC, 32-lead TSOP II and 32-lead Reverse TSOP II packages**

### Functional Description

The CY62148B is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion

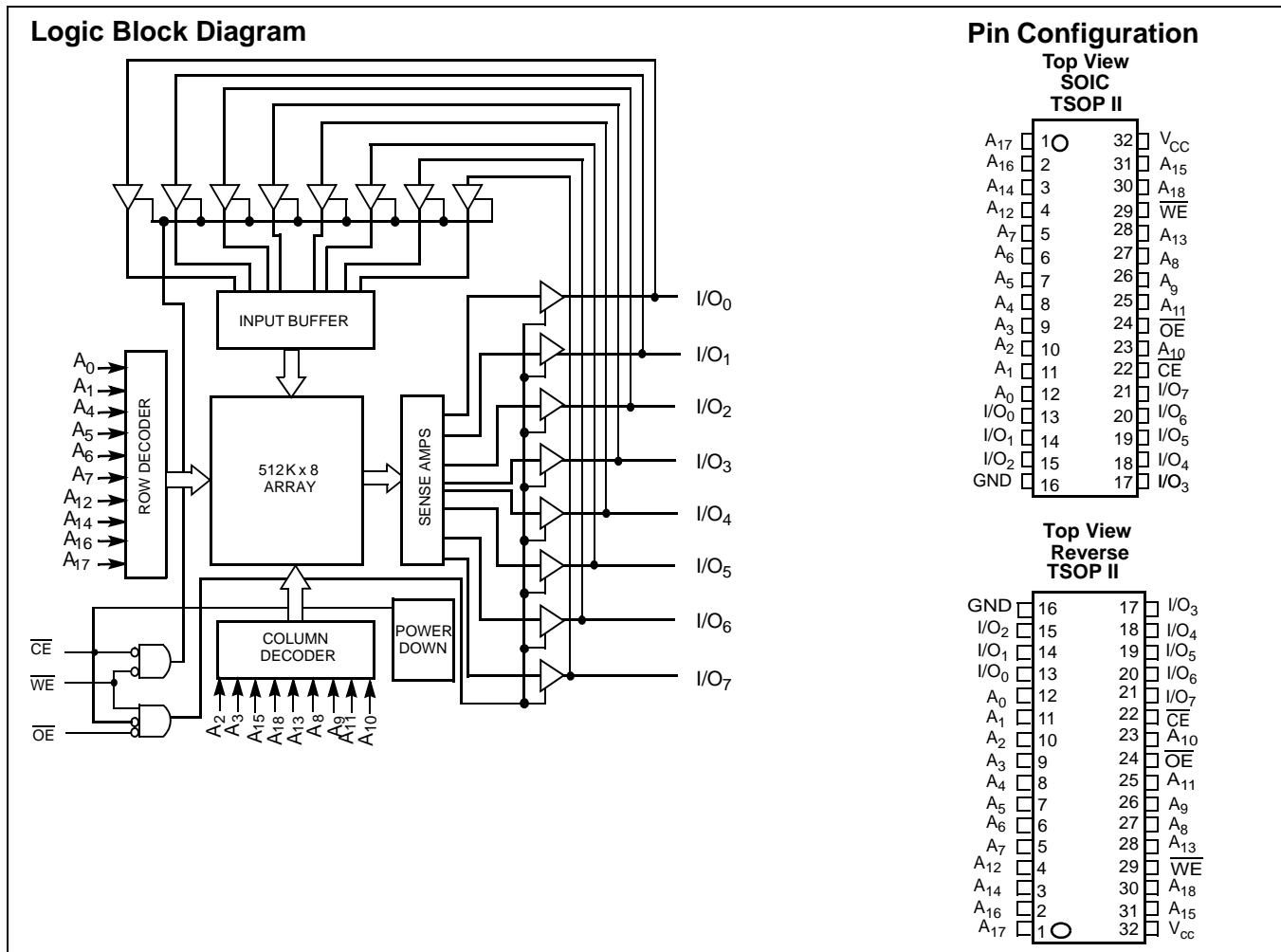
is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 99% when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY62148B is available in a standard 32-pin 450-mil-wide body width SOIC, 32-pin TSOP II, and 32-pin Reverse TSOP II packages.



**Product Portfolio**

Product	V <sub>CC</sub> Range			Speed	Temp.	Power Dissipation			
						Operating, I <sub>CC</sub>		Standby (I <sub>SB2</sub> )	
	f = f <sub>max</sub>					Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
	Min.	Typ.	Max.						
CY62148BLL	4.5 V	5.0V	5.5V	70 ns	Com'l	12.5 mA	20 mA	4 μA	20 μA
					Ind'l				

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V  
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V

Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... 2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	4.5V–5.5V
Industrial	-40°C to +85°C	

**Electrical Characteristics** Over the Operating Range

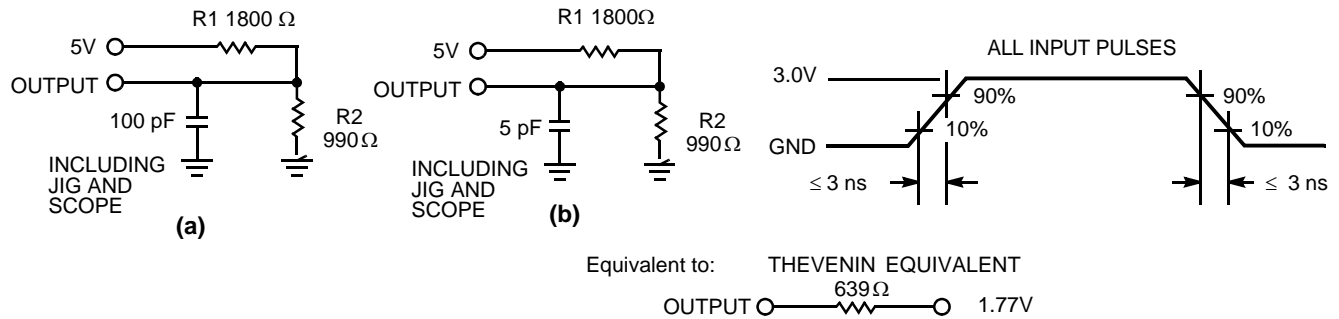
Parameter	Description	Test Conditions	CY62148B-70			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1 mA	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		12.5	20	mA
		f = 1 MHz	Com/Ind'l I <sub>OUT</sub> = 0 mA V <sub>CC</sub> = Max.,	2.5		mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>			1.5	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		4	20	μA

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "Instant On" case temperature.
- Typical values are measured at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, and are included for reference only and are not tested or guaranteed.

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	6	pF
$C_{OUT}$	Output Capacitance		8	pF

**AC Test Loads and Waveforms**

**Note:**

- Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics<sup>[5]</sup> Over the Operating Range**

Parameter	Description	62148BLL-70		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	70		ns
$t_{AA}$	Address to Data Valid		70	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		70	ns
<b>WRITE CYCLE<sup>[8]</sup></b>				
$t_{WC}$	Write Cycle Time	70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	60		ns
$t_{AW}$	Address Set-Up to Write End	60		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	55		ns
$t_{SD}$	Data Set-Up to Write End	30		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		25	ns

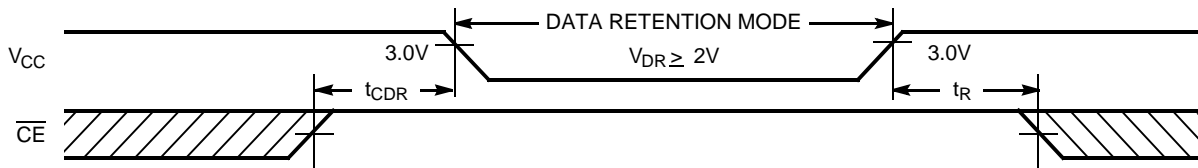
**Notes:**

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
6. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
7.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

**Data Retention Characteristics** (Over the Operating Range)

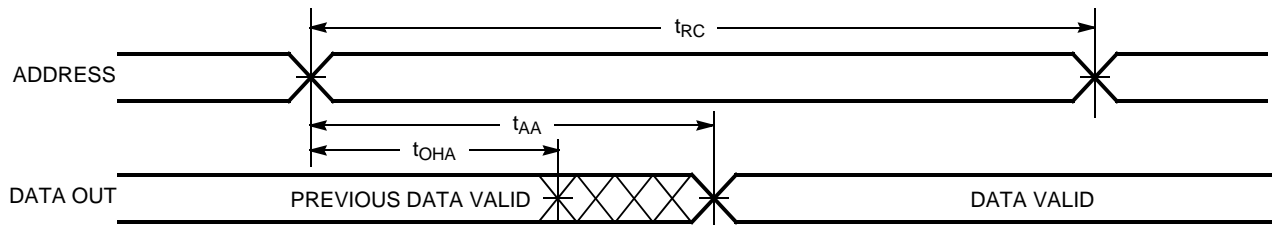
Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0			V
$I_{CCDR}$	Data Retention Current	Com'l LL			20	$\mu A$
		Ind'l LL	No input may exceed $V_{CC} + 0.3V$ $V_{CC} = V_{DR} = 3.0V$ $CE > V_{CC} - 0.3V$		20	$\mu A$
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time	$V_{IN} > V_{CC} - 0.3V$ or $V_{IN} < 0.3V$	0			ns
$t_R^{[9]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform**

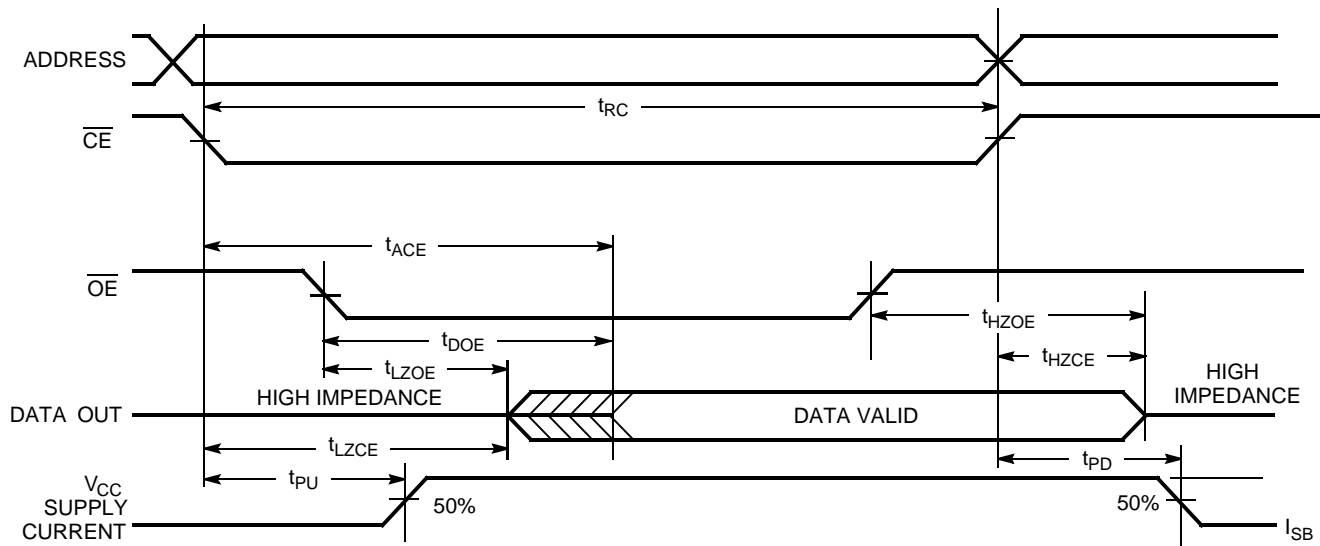


**Switching Waveforms**

**Read Cycle No.1<sup>[10, 11]</sup>**



**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>**

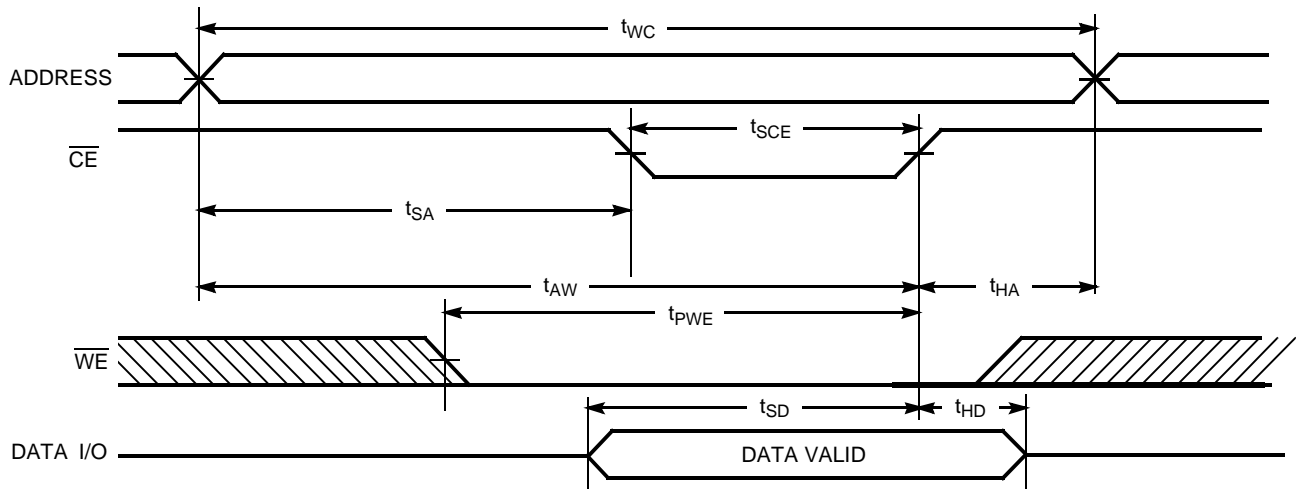


**Notes:**

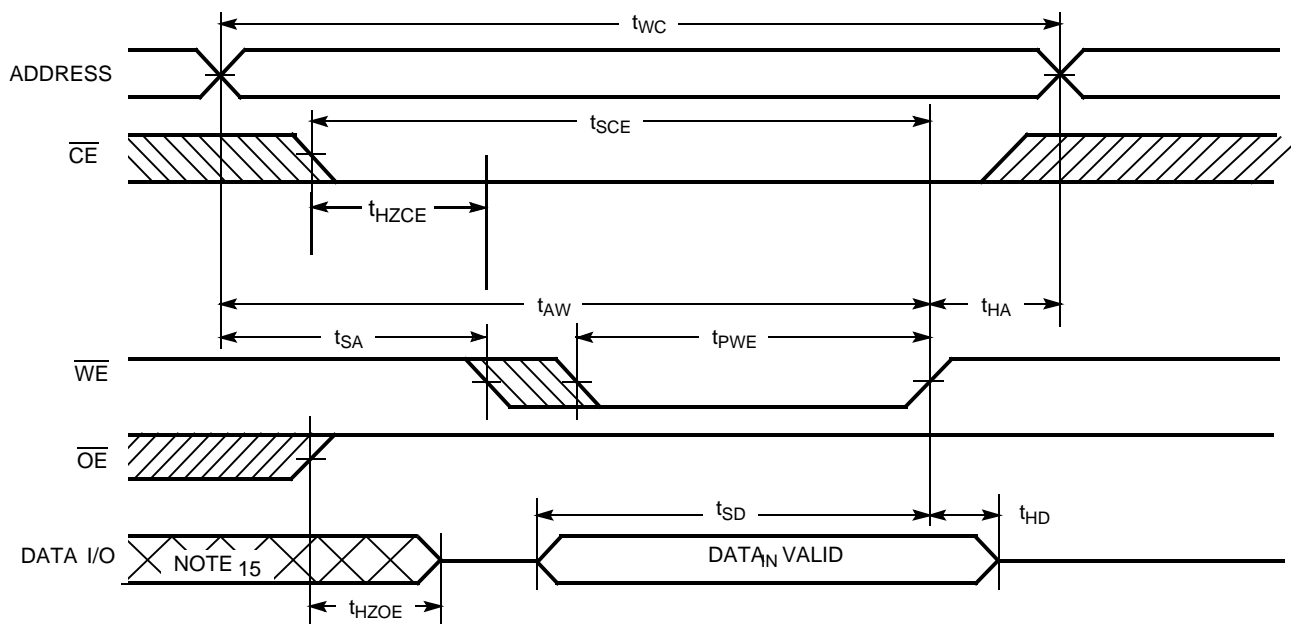
9. Full Device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu s$  or stable at  $V_{CC(min)} \geq 100 \mu s$ .
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**

**Write Cycle No. 1 (CE Controlled)<sup>[13]</sup>**



**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>**

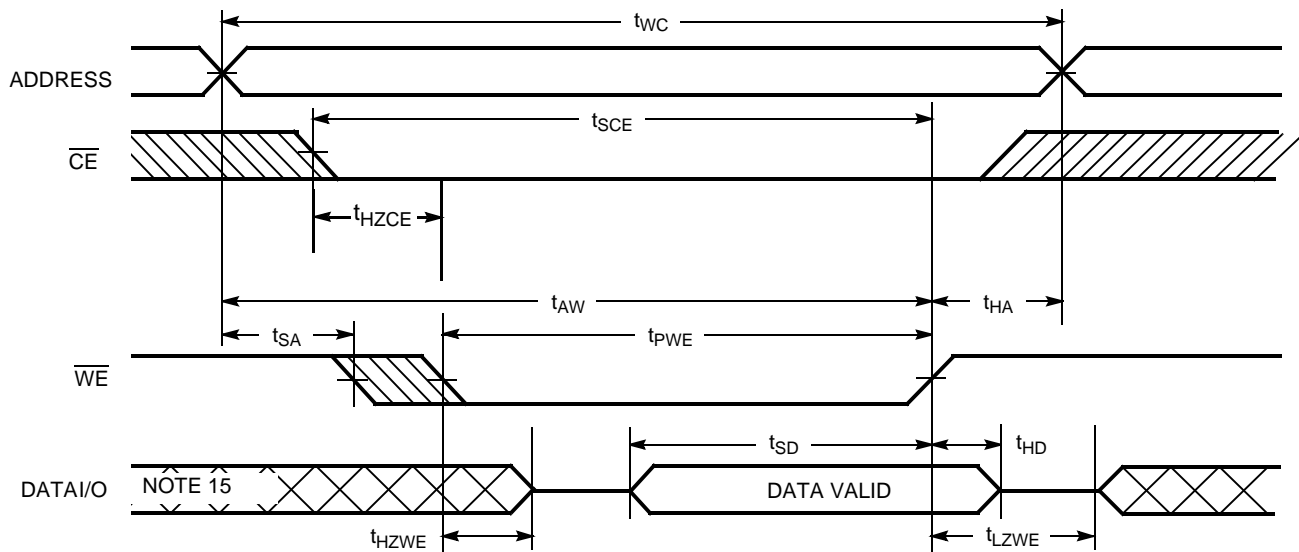


**Notes:**

13. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

14. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .

15. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[13, 14]</sup>**

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> – I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

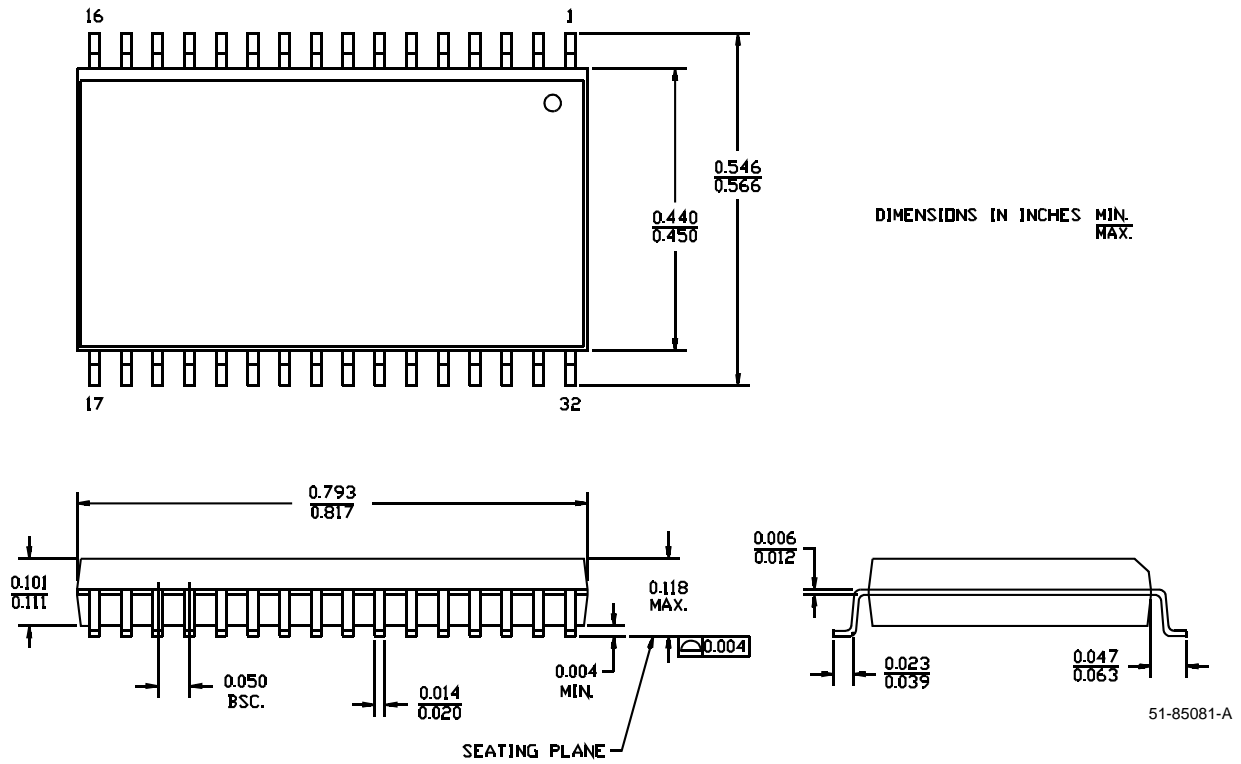
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62148BLL-70SC	51-85081	32-lead (450-Mil) Molded SOIC	Commercial
	CY62148BLL-70ZC	51-85095	32-lead TSOP II	
	CY62148BLL-70ZRC	51-85138	32-lead RTSOP II	
	CY62148BLL-70SI	51-85081	32-lead (450-Mil) Molded SOIC	Industrial
	CY62148BLL-70ZI	51-85095	32-lead TSOP II	
	CY62148BLL-70ZRI	51-85138	32-lead RTSOP II	

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

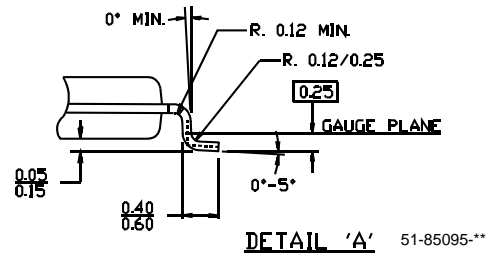
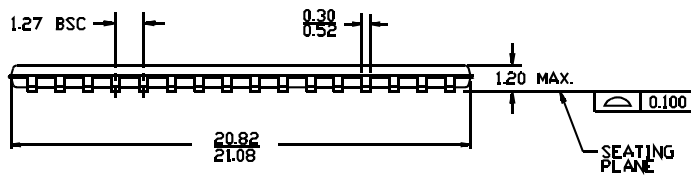
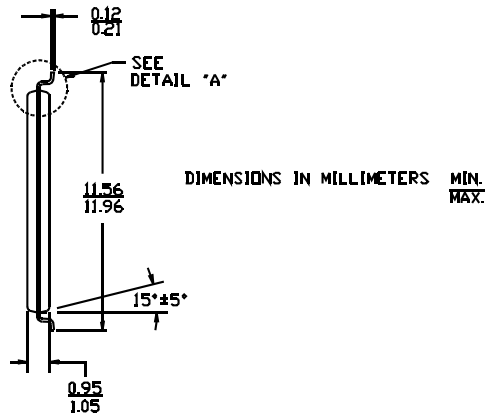
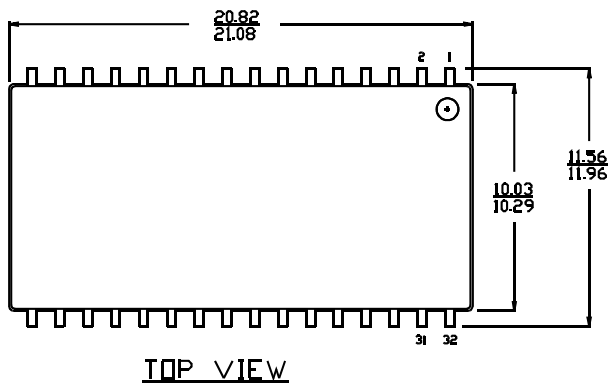
32-lead (450 MIL) Molded SOIC (51-85081)





Package Diagrams (continued)

32-lead Thin Small Outline Package Type II (51-85095)

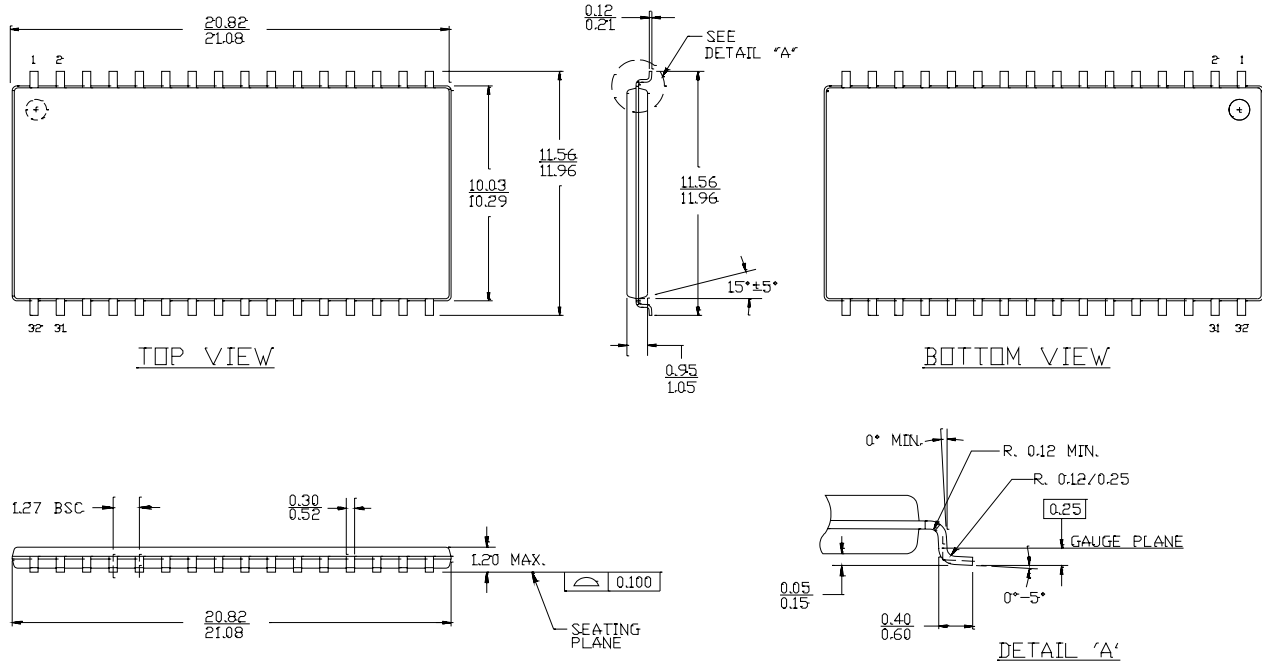


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Package Diagrams (continued)

32-lead Reverse Thin Small Outline Package Type II (51-85138)

DIMENSIONS IN MILLIMETERS MIN. MAX.



51-85138-\*\*

**Document History Page**

Document Title: CY62148B 4-Mbit (512K x 8) Static RAM Document Number: 38-05039				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106833	05/01/01	SZV	Change from Spec number 38-01104 to 38-05039
*A	106970	07/16/01	GAV	Modified annotations on Pin Configurations; $t_{SD} = 30$ ns
*B	109766	10/09/01	MGN	Remove 55-ns devices
*C	485639	See ECN	VKN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Corrected the typo in the Array size in the Logic Block Diagram on page# 1 Renamed Package Name column with Package Diagram in the Ordering Information Table