SIEMENS

FM Sound IF for Television Applications with I²C Bus and SCART

TBA 130-2

Preliminary Data

Bipolar IC

Features

- I²C bus control for the functions volume, muting, voice/music switching, as well as SCART recording/playback switching
- Integrated deemphasis resistor
- Low harmonic distortion factor

FM IF amplifier, comprising a limiter amplifier with an FM demodulator.

The AF section includes an SCART recording/playback switch, a voice/music switch, as well as a digital/analog converter to set the volume for the AF output. Control of volume, SCART recording/playback switch, and voice/music switch is achieved via an I²C bus serial interface.

The component is used in mono television sets with internal I²C bus control.

Type	Ordering Code	Package
TBA 130-2	Q67000-A8054	P-DIP-18

Circuit Description

In its FM section, the component contains an eight-stage, symmetrical limiter amplifier with subsequent coincidence demodulator. The AF section contains a mute circuit, an analog switch for the SCART recording/playback function, as well as a 6-bit D/A converter to set the volume for the AF output, and a voice/music switch. Control of the D/A converter, the switch function for record/playback and voice/music is achieved via an I²C bus serial interface (ref. diagrams).

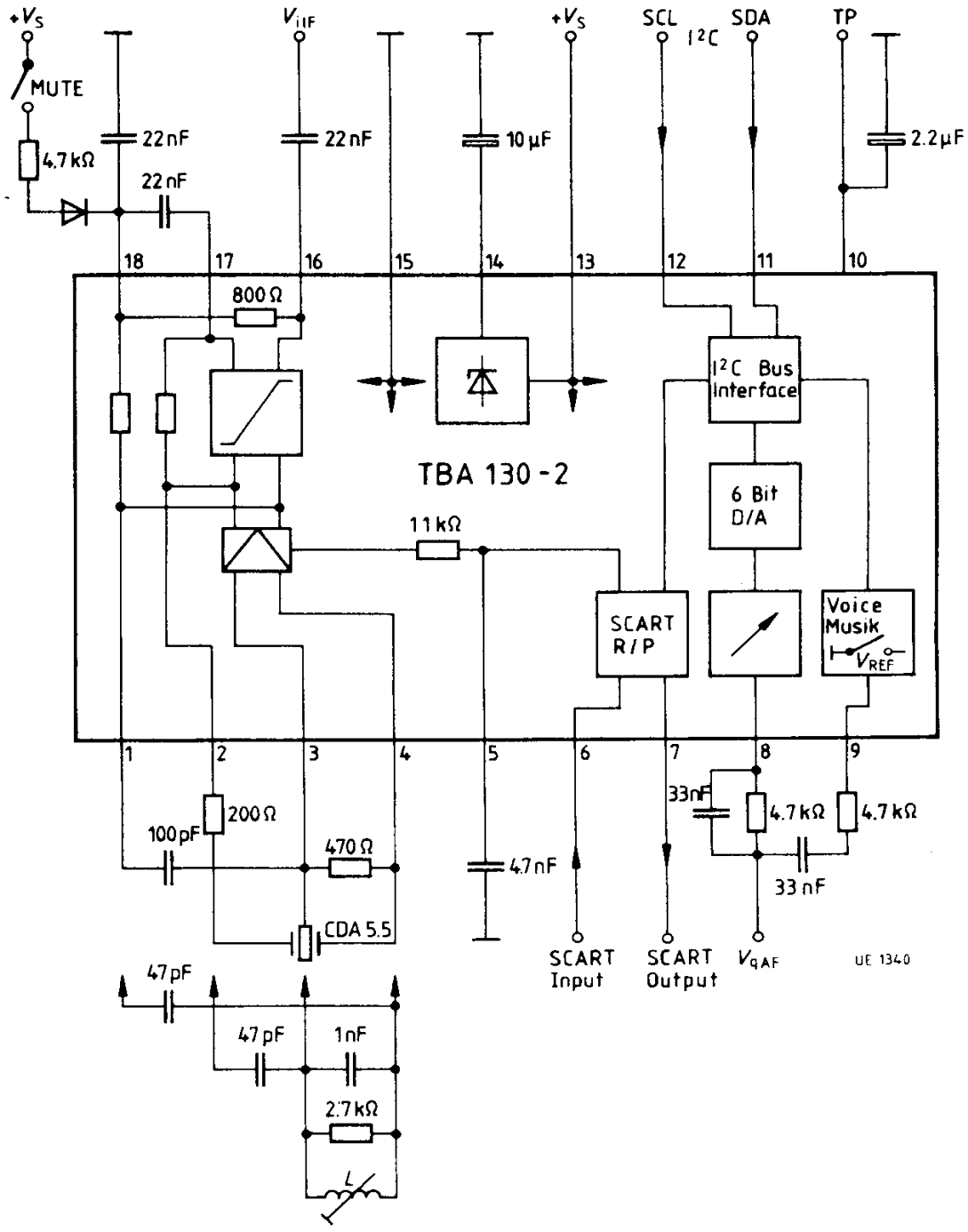
Data from the processor passes through an I²C bus control and is stored in registers according to its function (latch 1-3). If the bus is free, both lines will be in the mark state (SDA, SCL high). Each message begins with the start conditions: SDA goes L, while SCL remains H.

Any additional information transfer takes place while SCL = L, data is accepted by the control with the positive clock edge. If SDA goes H while the clock is H, the circuit recognizes a stop condition and thus, an end of the message.

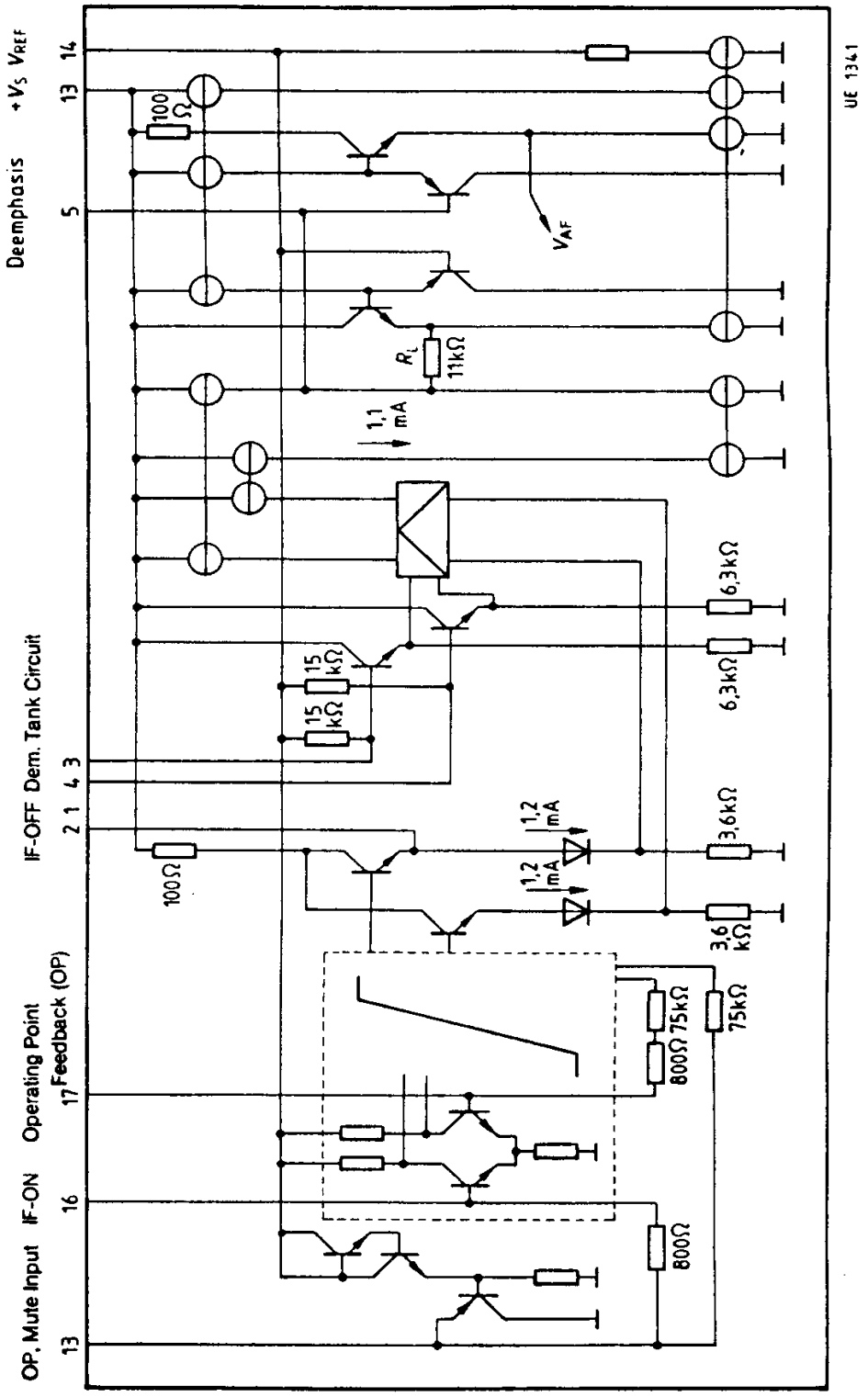
The logic operates according to the table shown on page 375. All messages are transmitted byte-by-byte, followed by a ninth clock pulse, while the control returns the SDA line to L (acknowledge condition). The first byte consists of 7 address bits, with which the processor selects the TBA 130-2 from among several peripheral components (chip select). The eighth bit determines the direction of the subsequent data traffic (in this case read mode only).

The first and the second bit of the data bytes determine which latch will be called (sub-address). The volume information is contained in 6 bits (64 steps). For reasons of compatibility with the TDA 6200, a second bit with the same sub-address but with random contents must be transmitted for setting the volume.

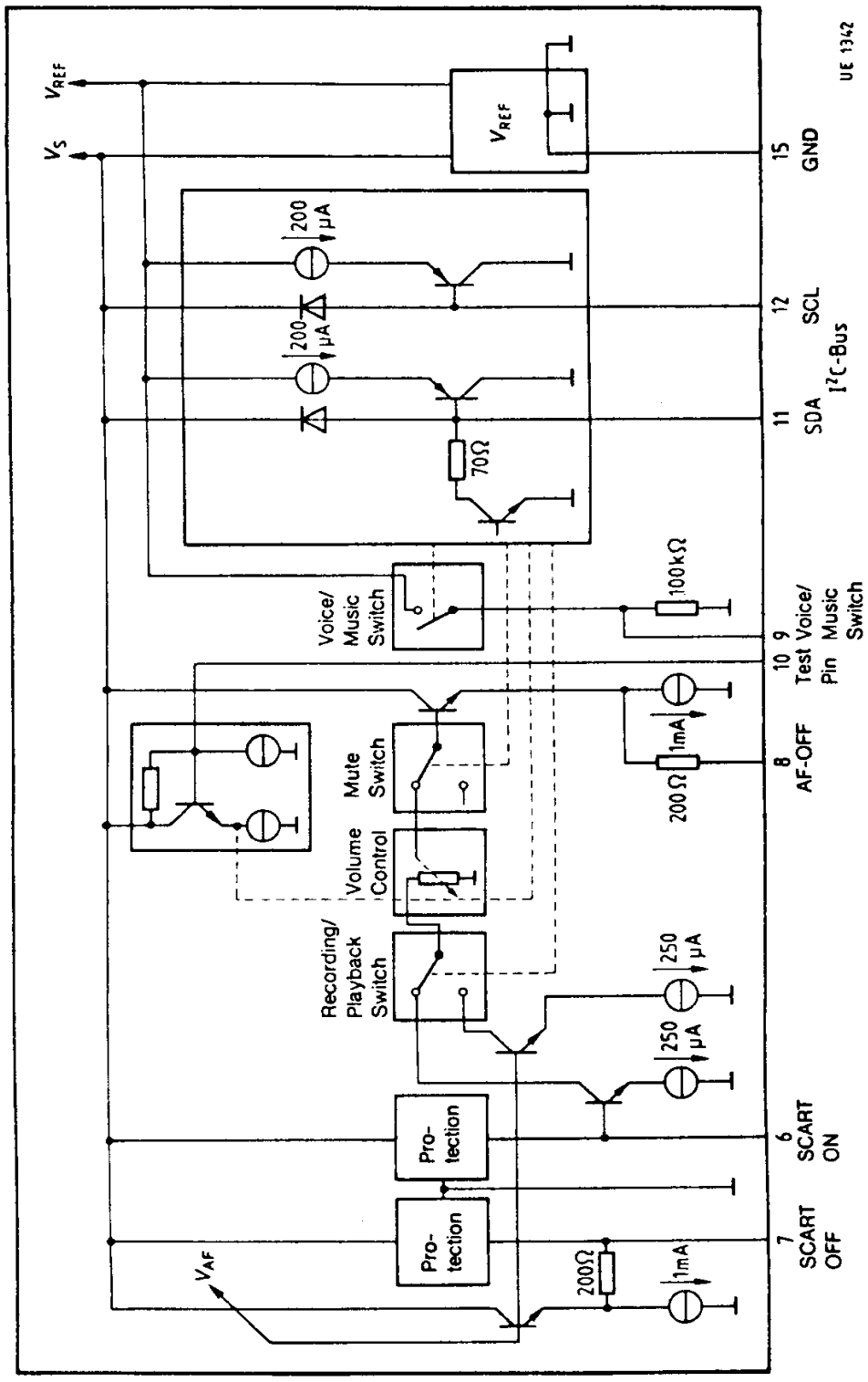
Block Diagram



Expanded Block Diagram Part 1



Expanded Block Diagram Part 2



Pin Functions

Pin No.	Function
1, 2	IF amplifier output (emitter follower)
3, 4	Demodulator tank circuit connection (high impedance input – slope of S curve determined by external resistor between pins 3 and 4)
5	Connection for deemphasis capacitor (a series resistor of 11 kΩ is integrated)
6	AF input of SCART interface
7	AF output of SCART interface (emitter follower)
8	AF output (emitter follower)
9	Voice/music switch (open collector; max. 1 mA!)
10	Test pin (access to volume control)
11	Data input/output of the I^2C bus control
12	Clock frequency input of the I^2C (inter IC) bus control
13	Supply voltage
14	Internal reference voltage (6 V typ.)
15	GND
16	IF input (limiter amplifier input; internal resistor between pins 16 and 18 is 800 Ω typ.)
17	Limiter amplifier operating point feedback (RF decoupling of IF amplifier with appropriate capacitors if required)
18	Limiter amplifier operating point and low end; MUTE input (RF decoupling of IF amplifier with appropriate capacitors if required)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	0	16	V
Reference current	I_{REF}	0	2	mA
IF input voltage	$V_{i\ 16\ rms}$	0	600	mV
DC voltage	$V_{3, 4, 6}$	0	V_S	V
DC voltage	$V_{11, 12}$	0	V_S	V
DC voltage	$V_{16, 17, 18}$	0	V_{REF}	V
DC current	$I_{1, 2}$	0	2	mA
DC current	$I_{5, 7, 8}$	– 1	2	mA
DC current	I_9	0	2	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		80	K/W

Operating Range

Supply voltage	V_S	10.5	15.75	V
Frequency	f	0.1	12	MHz
Ambient temperature	T_A	0	70	°C

Characteristics

V_S = 12 V; T_A = 25 °C; $f_{I\,14}$ = 5.5 MHz; Δf = ± 30 kHz; f_{mod} = 1 kHz

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	I_S	24	36	48	mA
Reference voltage	V_{REF}	5.4	6	6.6	V
Input voltage for limiter threshold $V_{Q\,7,8}$ = – 3 dB	$V_{I\,16\,rms}$		50	100	µV
SCART output voltage $V_{I\,16\,rms}$ = 10 mV	$V_{Q\,7}$	450	650	850	mV
AF output voltage L byte = BF	$V_{Q\,8}$	450	650	850	mV
DC voltage portion $V_{I\,16\,rms}$ = 10 mV; Δf = 0; $THD = THD_{min}$	$V_{Q\,7}$; $V_{Q\,8}$		6		V
Total harmonic distortion $V_{I\,16\,rms}$ = 10 mV L byte = BF	THD_7; THD_8			1	%
AM suppression[1] $V_{I\,16\,rms}$ = 500 µV; m = 30%	$\alpha_{AM\,7,8}$	50	60		dB
Volume control L byte = 80-BF	ΔV_8	80			dB
Max. input voltage SCART $THD_8 \leq 1\%$	$V_{I\,6\,rms}$	2			V
Gain between SCART input (pin 6) and AF output (pin 8) L byte = BF	G_{SC}		0		dB

Switching Voltage Muting

ON (AF OFF)	V_{18} =	8		V_S	V
OFF	V_{18} =	0		3	V

Voice / Music Switch ($I_{Q\,9}$ = 1 mA)

V/M = 0 = high-ohmic R_{OFF} Pin 14 V_{REF}		75	100		kΩ
V/M = 1 = low-ohmic R_{ON} DC voltage at pin 9 ($I_{Q\,9}$ = 0)	V_9 =	5.4	6	800 6.6	Ω V

[1] Test conditions for the reference point
$f_{I\,14}$ = 5.5 MHz; $V_{I\,14\,rms}$ = 10 mV; Δf = ± 30 kHz; f_{mod} = 1 kHz

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C; $f_{i\,14}$ = 5.5 MHz

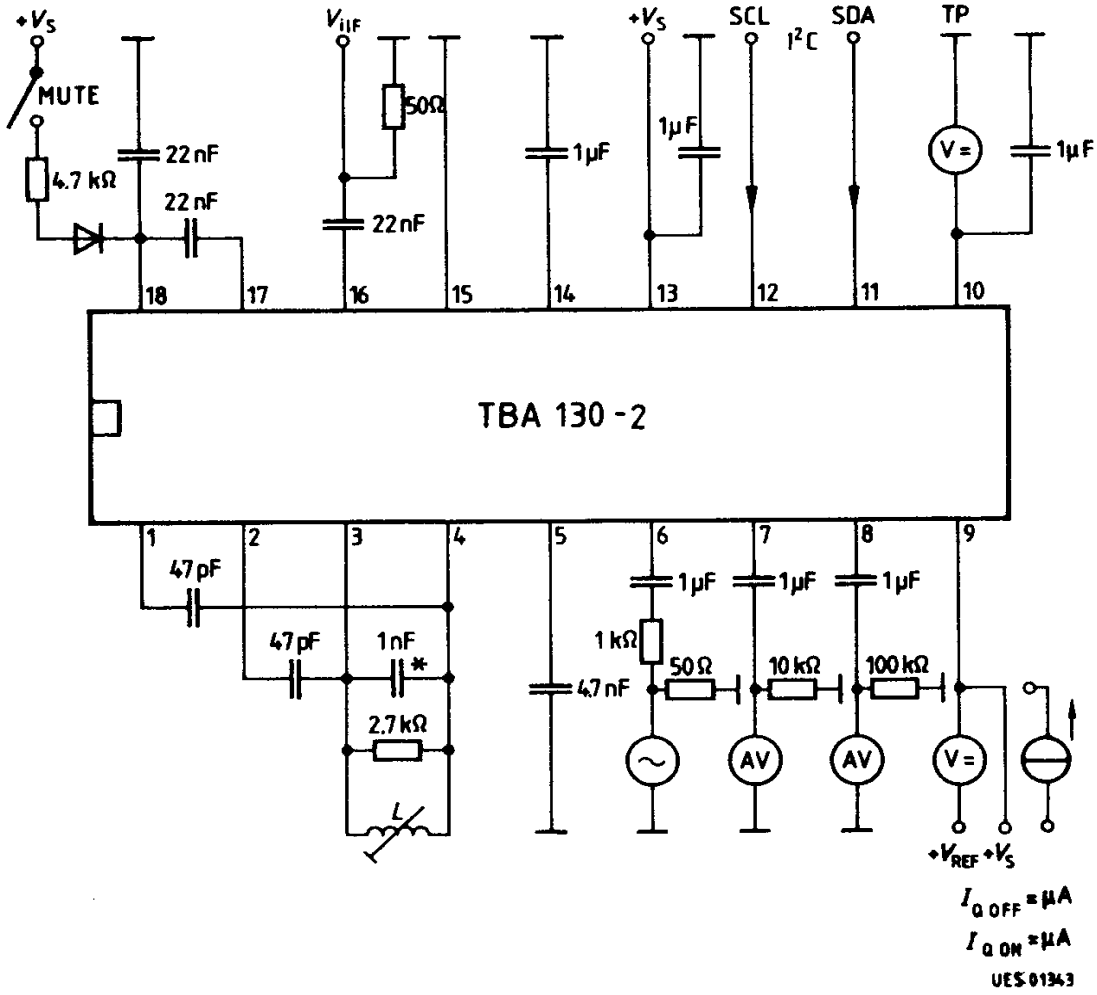
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C Bus (SCL, SDA)					
Edges SCL, SDA					
Rise time	t_r			1	µs
Fall time	t_f			0.3	µs
Shift Clock SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_{HIGH}	4			µs
L- pulse width	t_{LOW}	4			µs
Start					
Set-up time	t_{SUSTA}	4			µs
Hold time	t_{HDSTA}	4			µs
Stop					
Set-up time	t_{SUSTO}	4			µs
Bus free	t_{BUF}	4			µs
Data Change					
Set-up time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Input SCL, SDA					
Input voltage	V_{IH} V_{IH}	2.4 0.3		5.5 1	V V
Input current	I_{IH} I_{IH}			50 100	µA µA

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C; $f_{I\,14}$ = 5.5 MHz

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Output SDA (open collector)					
Output voltage R_L = 2.5 kΩ I_{QL} = 2 mA	V_{QH} V_{QL}			5.5 0.4	V V
Design-Related Characteristics					
Input resistance	$R_{I\,3,4}$	20			kΩ
Output resistance	$R_{Q\,7,8}$			200	Ω
Input resistance	$R_{I\,6}$	20			kΩ
Input impedance	$Z_{I\,16}$		800		Ω
IF residual voltage $\Delta V_{S\,rms}$ = 500 mV; f_S = 100 Hz	$V_{Q\,7,8}$		10		mV
Hum suppression $V_S/V_{Q\,7,8}$ (without deemphasis C) $\Delta V_{S\,rms}$ = 500 mV; f_S = 100 Hz	α_{hum}		30		dB
Crosstalk rejection[1] $V_{6\,rms}$ = 2 V; SC = 0	$\alpha_{6\text{-}8}$	60			dB

[1] Test conditions for the reference point
$f_{I\,14}$ = 5.5 MHz; $V_{I\,14\,rms}$ = 10 mV; Δf = ± 30 kHz; f_{mod} = 1 kHz

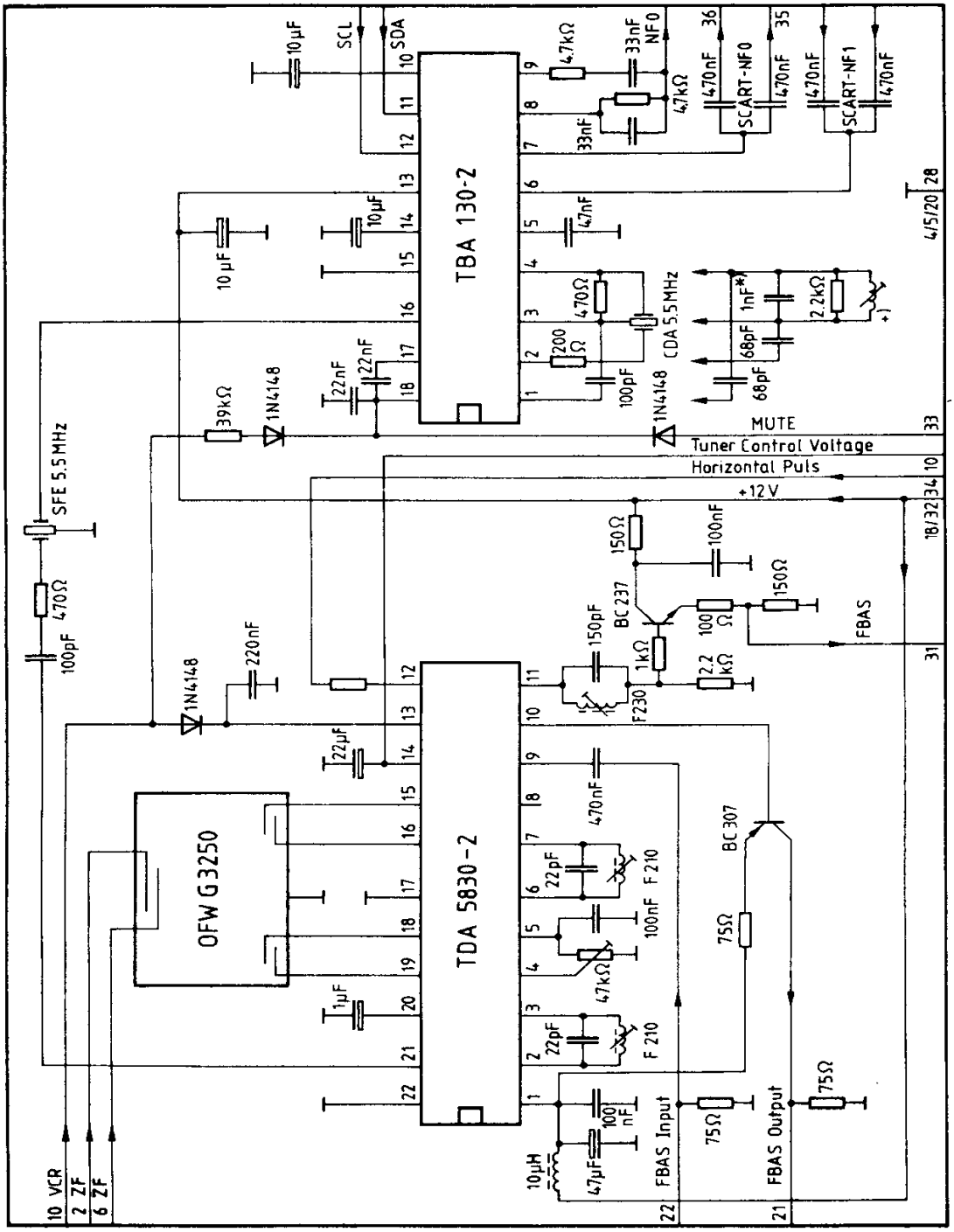
Test Circuit



L: 10 turns, 0.2 CuL; Q_B approx. 25
e.g. Vogt Coil Assembly 517 12 000 00

* STYROFLEX Capacitor

Application Circuit



L: 10 turns, 0.2 CuL; Q_B approx. 25
e.g. Vogt Coil Assembly 517 12 000 00

* STYROFLEX Capacitor

Software Definition

The following data format is used:

1) **Chip Address**

MSB							LSB	
1	0	0	0	0	0	0	0	acknowledge

MSB is transmitted first

2) **Data Bytes with Sub-Addresses**

a) volume

MSB							LSB
1	0	V_{05}	V_{04}	V_{03}	V_{02}	V_{01}	V_{00}
1	0	X	X	X	X	X	X

The second byte has to be included in the transfer

V_{X5} = MSB
V_{X0} = LSB

1	0	0	0	0	0	0	0	min. volume
1	0	1	1	1	1	1	1	max. volume

b) SCART control byte

MSB							LSB
1	SC	X	X	X	X	X	0

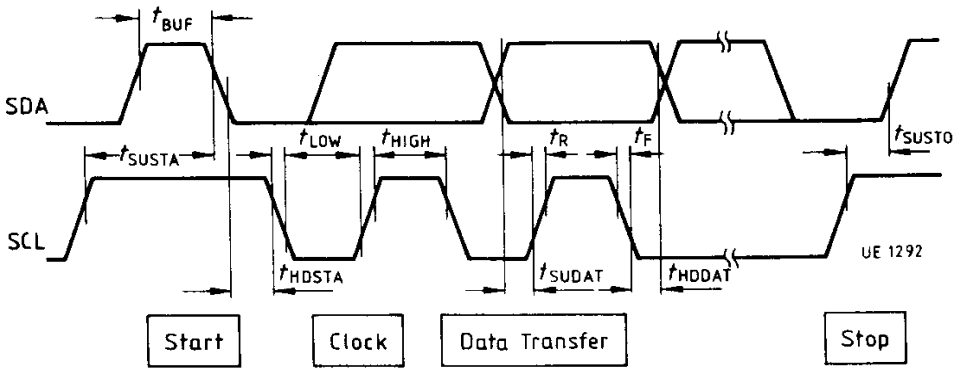
SC = 1 SCART playback; SCART input is connected with AF output
SC = 0 standard operating mode

c) AF control byte

MSB							LSB
0	0	M	X	V/M	X	X	X

V/M = 0 pin 9 high-impedance
V/M = 1 pin 9 low-impedance
M = 1 muting for AF output
M = 0 AF ON

I²C Bus Timing Diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	H- pulse width (clock)
t_{LOW}	L- pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free
t_F	Fall time
t_R	Rise time

Above times are referenced to V_{IH} and V_{IL} values.