MITSUBISHI LSIs

M5L8279P-5

T-52-33-15

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

The M5L8279P-5 is a programmable keyboard and display interface device that is designed to be used in combination with an 8-bit/16-bit microprocessor. This device is fabricated with N-channel silicon-gate ED-MOS process technology and is packed in a 40-pin DIL package. It needs only single 5V power supply.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Keyboard mode
- Sensor matrix mode
- Strobed mode
- Internally provided key bounce protection circuit
- Programmable debounce time
- 2-key lockout/N-key rollover
- 8-character keyboard FIFO
- Internally contained 16 × 8-bit display RAM
- Programmable right and left entry

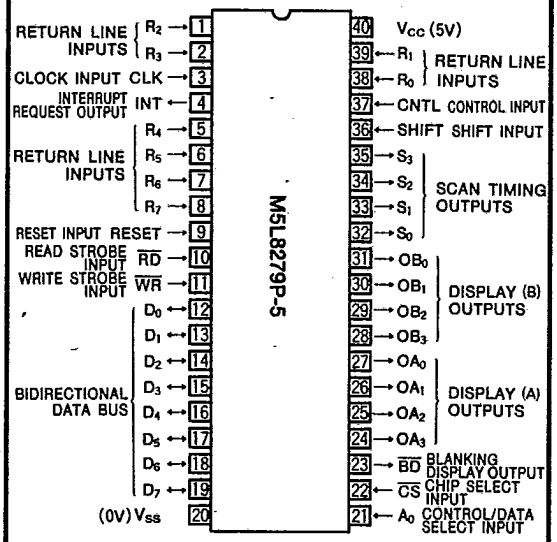
APPLICATION

Microcomputer I/O device

64 contact key input device for such items as electronic cash registers

Dual 8- or single 16-alphanumeric display

PIN CONFIGURATION (TOP VIEW)

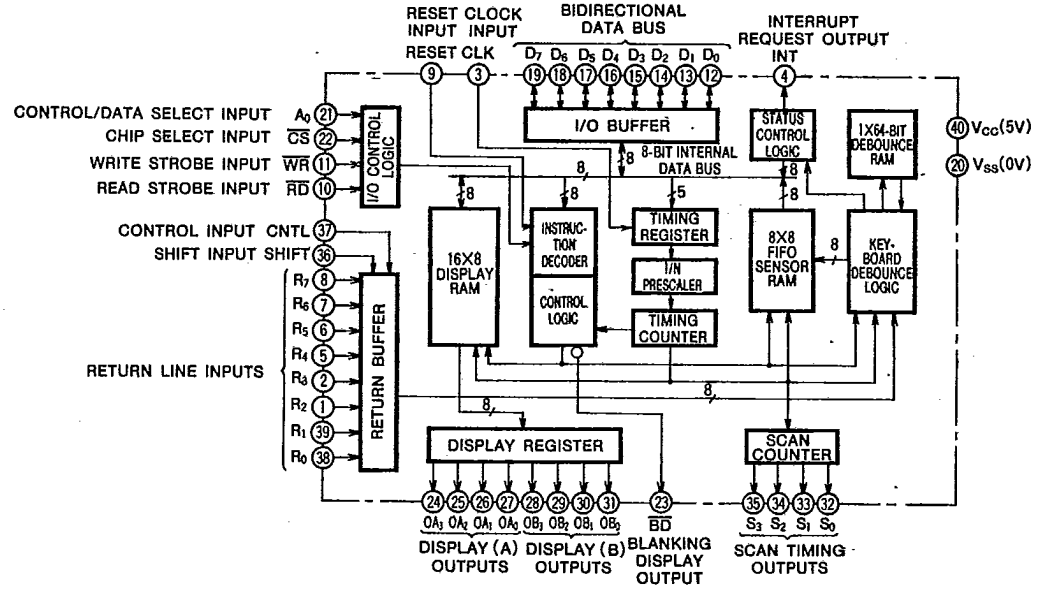


Outline 40P4

FUNCTION

The total chip, consisting of a keyboard interface and a display interface, can be programmed by eight 8-bit commands. The keyboard portion is provided with a 64-bit key debounce buffer and an 8 × 8-bit FIFO/SENSOR RAM. It operates in any one of the scanned keyboard mode, scanned sensor matrix mode or strobed entry mode. The display portion is provided with a 16 × 8-bit display RAM that can be organized into a dual 16× 4 configuration. Also, an 8-digit display configuration is possible by means of programming.

BLOCK DIAGRAM



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PIN DISCRIPTION

pin	Name	Input or output	Functions
R_0~R_7	Return line inputs	In	These are the return lines which are connected with the scan lines through the keys or sensor switches, and are used for 8-bit input in the strobed entry mode. They are provided with internal pullups to maintain them high-level until a switch closure pulls one low-level. They become active at low-level.
CLK	Clock input	In	Clock signal from the system which is used to generate internal timing.
INT	Interrupt request output	Out	When there is any data in the FIFO during the keyboard mode or the strobed mode, this signal turns high-level so as to request interrupt to the CPU. It turns low-level each time data is read, but if any data remains in the FIFO it will turn high-level again and request interrupt to the CPU. End interrupt command resets INT signal.
RESET	Reset input	In	Resets the chip when this signal is high-level. After the reset it assumes 16-digit, left-entry, encode display and 2-key lockout mode, and the prescale value of the clock becomes 31. The display RAM, however, is not cleared.
$\overline{RD}$	Read strobe input	In	Functions to control data transfer to the data bus.
$\overline{WR}$	Write strobe input	In	Functions to control command/data transfer from the data bus.
D_0~D_7	Bidirectional data bus	In/out	All data and commands between the CPU and the chip are transferred through these lines.
A_0	Control/data select input	In	When this signal is high-level, it indicates that the signals in and out are either command (in) or status (out). When low-level, it indicates they are data (in/out).
$\overline{CS}$	Chip select input	In	Chip select is enabled when this signal is low-level.
$\overline{BD}$	Blanking display output	Out	This signal is used in preventing overlapped display during digit swiching. It also may be brought to low-level by display blanking command.
OA_0~OA_3 OB_0~OB_3	Display (A) and (B) outputs	Out	These output ports can be used either as a dual 4-bit port or a single 8-bit port depending on an application, and the contents of the display RAM are output synchronizing with the scan timing signals. These two 4-bit ports may be blanked independently. Blanking may be activated with either high- or low-level signal by means of clear command.
S_0~S_3	Scan timing outputs	Out	These signals are used to scan the key switch, the sensor matrix or the display digit. They can be either decoded or encoded, but it requres an external decoder in the encode mode. Signals S_0~S_3 are all turned to low-level when RESET is high-level.
SHIFT	Shift input	In	In the keyboard mode, the shift input becomes the second highest bit of the key input information and is stored in the FIFO. This input is ignored in the other modes. It is constantly kept at high-level by an internal pull resistor. The signal is active at high-level.
CNTL	Control input	In	In the keyboard mode, the control input becomes the most significant bit of the key input information and is stored in the FIFO. The signal is active at high-level. In the strobed entry mode, it becomes the strobe signal and stores the return input data in the FIFO at the rising edge of the input. It affects nothing internal in the sensor mode. It is constantly kept at high-level by an internal pullup resistor.

OPERATION

One of the three operating modes, the keyboard mode is the most common, and allows programmed 2-key lockout and N-key rollover. Encoded timing signals corresponding with key input are stored in the FIFO through the keydebounce logic, and the debouncing time of the key is also programmable. In the sensor mode, the contents of the 8 × 8 key contacts are constantly stored in the FIFO/sensor RAM, generating an interrupt signal to the CPU each time there is a change in the contents. In the strobed entry mode, the CNTL input signal is used as a strobe for storing the 8 return line inputs to the FIFO/sensor RAM.

The display portion is provided with a 16 × 8-bit display RAM that can be organized into a dual 16 × 4-bit configuration. Also, an 8-digit display configuration is possible by means of programming. Input to the register can be performed by either left or right entry modes. In the auto increment mode, read and write can be carried out after designating the starting address only.

Both the keyboard and display sections are scanned by common scan timing signals that are derived from the basic clock pulse. This frequency-dividing ratio is changeable by means of programming. There are decode and encode modes for the scanning mode; timing signals that are decoded from the lower 2 bits of the scan counter are output in the decode mode, while the 4-bit binary output from the scan counter is decoded externally in the encode mode.

COMMAND DESCRIPTION

There are eight commands provided for programming the operating modes of the M5L8279P-5. These commands are sent on the data bus with the signal $\overline{CS}$ in low-level and the signal A_0 in 1 and are stored in the M5L8279P-5 at the rising edge of the signal $\overline{WR}$. The order of the command execution is arbitrary.

1. Mode Set Command

	MSB							LSB
Code :	0	0	0	D	D	K	K	K

DD (Display mode set command)

0 0 8—8-bit character display—left entry
0 1 16—8-bit character display—left entry (Note1)
1 0 8—8-bit character display—right entry
1 1 16—8-bit character display—right entry

KKK (Keyboard mode set command)

0 0 0 Encoded display keyboard mode — 2-key lockout (Note1)
0 0 1 Decoded display keyboard mode — 2-key lockout
0 1 0 Encoded display keyboard mode — N-key rollover
0 1 1 Decoded display keyboard mode — N-key rollover
1 0 0 Encoded display, sensor mode
1 0 1 Decoded display, sensor mode
1 1 0 Encoded display, strobed entry mode
1 1 1 Decoded display, strobed entry mode

Note 1 : Default after reset.

2. Program Clock Command

	MSB							LSB
Code :	0	0	1	P	P	P	P	P

The external clock is divided by the prescaler value PPPPP designated by this command to obtain the basic internal frequency.
When the internal clock is set to 100kHz, it will give a 5.1ms keyboard scan time and a 10.3ms debounce time. The prescale value that can be specified by PPPPP is from 2 to 31. In case PPPPP is 00000 or 00001, the prescale is set to 2. Default after a reset pulse is 31, but the prescale value is not cleared by the clear command.

3. Read FIFO Command

	MSB							LSB	
Code :	0	1	0	AI	X	A	A	A	X = Don't care

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the FIFO. As long as data is to be read from the FIFO, no additional commands are necessary.
AI and AAA are used only in the sensor mode. AAA designates the address of the FIFO to be read, and AI is the auto-increment flag. Turning AI to 1 makes the address automatically incremented after the second read operation. This auto-increment bit does not affect the auto-increment of the display RAM.

4. Read Display RAM Command

	MSB							LSB
Code :	0	1	1	AI	A	A	A	A

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the display RAM. As long as data is to be read from the display RAM, no additional commands are necessary.
The data AAAA is the value with which the display RAM read/write counter is set, and it specifies the address of the display RAM to be read or written next.
AI is the auto-increment flag. Turning AI to 1 makes the address automatically incremented after the second read/write operation. This auto-increment bit does not affect the auto-increment of FIFO readout in the sensor mode.

5. Write Display RAM Command

	MSB							LSB
Code :	1	0	0	AI	A	A	A	A

With this command, following display RAM read/write addressing is achieved without changing the data readout source (FIFO or display RAM). Meaning of AI and AAAA are identical with read display RAM command.

6. Display Write Inhibit/Blanking Command

	MSB							LSB	
Code :	1	0	1	X	IW A	IW B	BL A	BL B	X = Don't care

The IW is a write inhibit bit to the display RAM that corresponds with the output A or B. Inhibit is activated by turning the IW 1.
The BL is used in blanking the out A or B. Blanking is activated by turning the BL 1. Setting both BL flags makes the signal $\overline{BD}$ low-level so that it can be used in 8-bit display mode.
Resetting the flags makes all IW and BL turn 0.

7. Clear Command

	MBS							LSB
Code :	1	1	0	C_D	C_D	C_D	C_F	C_A

C_D: Clears the display RAM.

C_D	C_D	C_D	
0	X	X	No specific performance
1	0	X	Entire contents of the display RAM are turned 0.
1	1	0	The contents of the display RAM are turned 20H (00100000 = $0A_30A_20A_10A_0$ $0B_30B_20B_10B_0$).
1	1	1	Entire contents of the display RAM are turned 1.

C_F : Clears the status word and resets the interrupt signal (INT).

C_A : Clears the display RAM and the status word and resets the interrupt signal (INT).

Clearing condition of the display RAM is determined by the lower 2 bits of the C_D.

Clearing the display RAM needs some time (~ 160 μ second) and causes the display-unavailable status (DU) in the status word to be 1. The display RAM is not accessible for the duration of this time, even if the display mode was in 8-digit display mode or a decoded mode.

As both C_F and C_A function to reset the internal keydebounce counter, the key input under counting is ignored, and the internal FIFO counter is reset to make the interrupt signal low-level.

C_A resets the internal timing counter, forcing $S_0 \sim S_3$ to start from $S_3S_2S_1S_0 = 0000$ after the execution of the command.

8. End Interrupt/Error Mode Set Command

	MSB							LSB	
Code :	1	1	1	E	X	X	X	X	X = Don't care

In the sensor matrix mode, an interrupt signal is generated at the beginning of the next key scan time to inhibit further writing to the FIFO when there is a change in the sensor switch. The interrupt request output INT is reset when the sensor RAM is read with the Auto-increment flag 0, or the execution of this command.

When E is kept in 0, depression of any sensor makes the second highest bit of the status word 1. When E is kept in 1, the status is kept 0 all the time.

When E is programmed to 1 in the N-key rollover mode, the execution of this command makes the chip operate in special error mode, during which time depression of more than two keys in a key debounce time causes an error and sets the second highest bit of the status word 1.

STATUS WORD

MSB							LSB
DU	S/E	O	U	F	N	N	N

NNN: Indicates the number of characters in the FIFO during the keyboard and strobed entry modes.

F: Indicates that the FIFO is filled up with 8 characters. The number of characters existing in the FIFO (0 ~ 8 characters) can be known by means of the bits NNN and F (FNNN = 0000~FNNN = 1000).

U: Underrun error flag
This flag is set when a master CPU tries to read an empty FIFO.

O: Overrun error flag
This flag is set when another character is strobed into a full FIFO.
The bits U and O cannot be cleared by status read. They will be cleared by the clear command.

S/E: Sensor closure/multiple error flag
When 111EXXXX is executed by turning E = 0 , the bit S/E in the status word is set when there is at least one sensor closure.
When 111EXXXX is executed by turning E = 1 (special error mode), the bit S/E is set when there are more than two key depressions made in a key scan time.

DU: Display unavailable
This flag is set when a clear display command is executed, and announces that the display RAM is not accessible.

CPU INTERFACE

1. Command Write

A command is written on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ low-level and A_0 1.

2. Data Write

Data is written to the display RAM on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ low-level and A_0 0.

The address of the display RAM is also incremented on the rising edge of the signal $\overline{WR}$ if AI is set for the display RAM.

3. Status Read

The status word is read when $\overline{CS}$ and $\overline{RD}$ are low-level and A_0 is 1. The status word appears on the data bus as long as the signal $\overline{RD}$ is low-level.

4. Data Read

Data is read from either the FIFO or the display RAM with $\overline{CS}$ and $\overline{RD}$ are low-level and A_0 is 0. The source of the data (FIFO or display RAM) is decided by the latest command (read display or read FIFO). The data read appears on the data bus as long as the signal $\overline{RD}$ is low-level.

The trailing edge of the signal $\overline{RD}$ increments the address of the FIFO or the display RAM when AI is set. After the reset, data will be read from the FIFO, however.

A_0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Operation
1	L	H	L	Command write
0	L	H	L	Data write
1	L	L	H	Status read
0	L	L	H	Data read
X	H	X	X	No operation

KEYBOARD INTERFACE

Keyboard interface is done by the scan timing signals (S_0~S_3), the return line inputs (R_0~R_7), the SHIFT and the CNTRL inputs.

In the decoded mode, the low-order of 2 bits of the internal scan counter are decoded and come out on the timing pins (S_0~S_3). In the encoded mode, the four binary bits of the scan counter are directly output on the timing pins, thus a 3-to-8 decoder must be employed to generate keyboard scan timing.

The return line inputs (R_0~R_7), the SHIFT and the CNTL inputs are pulled up high-level by internal pullup transistors until a switch closure pulls one low.

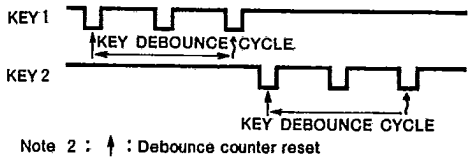
The internal key debounce logic works for a 64-key matrix that is obtained by combining the return line inputs with the scan timing.

For the keyboard interface, M5L8279P-5 has four distinctive modes that allow various kinds of applications. In the following explanation, a "key scan cycle" is the time needed to scan a 64-key matrix, and a "key debounce cycle" needs a duration of two "key scan" cycles. (In the decoded mode 32 keys, unlike 64 keys in the encoded mode, can be employed for a maximum key matrix due to the limit of timing signals. However, both the key scan cycle and the key debounce cycle are the same as in the encoded mode.)

1. 2-Key Lockout (Scanned Keyboard Mode)

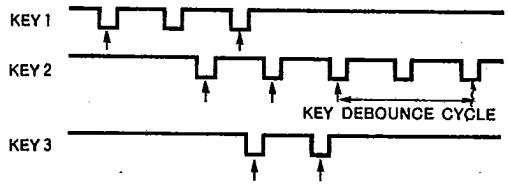
The detection of a new key closure resets the internal debounce counter and starts counting. At the end of a key debounce cycle, the key is checked and entered into the FIFO if it is still down. An entry in the FIFO sets the INT output high. If any other keys are depressed in a key debounce cycle, the internal key debounce counter is reset each time it encounters a new key. Thus only a single-key depression within a key debounce duration is accepted, but all keys are ignored when more than two keys are depressed at the same time.

Example 1 : Accepting two successive key depressions



Note 2 : ↑ : Debounce counter reset
↑ : Key input

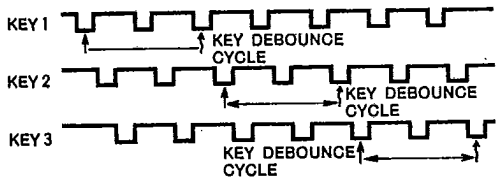
Example 2 : Overlapped depression of three keys



Note 3 : Only key 2 is acceptable

2. N-Key Rollover (Scanned Keyboard Mode)

Each key depression is treated independently from all others so as to allow overlapped key depression. Detection of a new key depression makes the internal key debounce counter reset and start to count in a same manner as in the case of 2-key lockout. But, in N-key rollover, other key closures are entirely ignored within a key debounce cycle so that depression of any other keys would not reset the key debounce counter. In this way, overlapped key depression is allowed so as to enable the following key input:

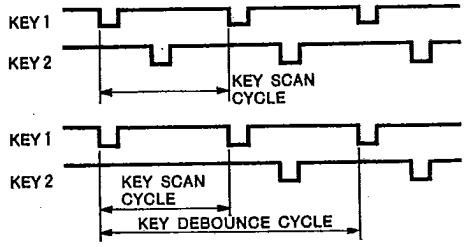


The scanned key input signal does not always reflect the actual key depressing action, as the key matrix is scanned by the timing signal.

With N-key rollover, there is a mode provided with which error is caused when there are more than 2 key inputs in a key debounce cycle, which can be programmed by using the end interrupt/error mode set command. In this mode (special error mode), recognition of the above error sets the INT signal to high-level and sets the bit S/E in the status word.

In case 2 key entries are made separately in more than a debounce cycle, there would be no problem, as key depression is clearly identified. And no problem exists for 2-key lockout, as the both keys are recognized invalid.

Example of error (Special error mode)



3. Sensor Matrix Mode

The key debounce logic is disabled in this mode. As the image of the sensor switch is kept in the FIFO, any change in this status is reported to the CPU by means of the interrupt signal INT. Although a debounce circuit is not used in this mode, it has an advantage in that the CPU is able to know how long and when the sensor was depressed.

In the sensor matrix mode with the bit E = 0 of the end interrupt/error mode set command, the second most significant bit of the status word (S/E bit) is set to 1 when any sensor switch is depressed.

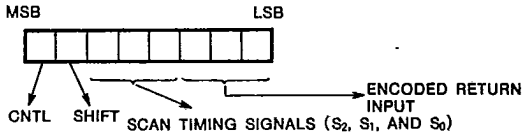
Any sensor change detected by the M5L8279P-5 in one key scan cycle causes only once INT generation at the first timing of the next scan cycle.

4. Strobe Mode

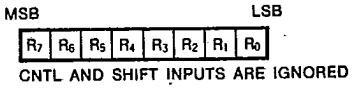
The data is entered into the FIFO from the return lines (R_0~R_7) at the rising edge of a CNTL pulse. The INT goes high while any data exists in the FIFO, in the same manner as in the keyboard mode. The key debounce circuit will not operate.

Formats of data entered into the FIFO in each of the above modes are described in the following:

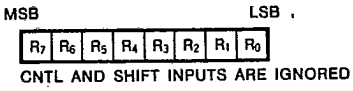
Keyboard matrix



Sensor matrix mode



Storobe mode



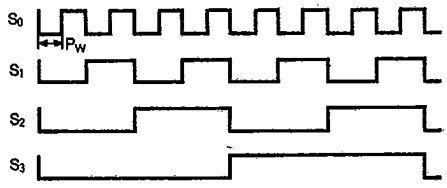
DISPLAY INTERFACE

The display interface is done by 8 display outputs (OA_0~OA_3, OB_0~OB_3), a blanking signal ($\overline{BD}$), and scan timing outputs (S_0~S_3).
The relation between the data bus and the display outputs is as shown below:

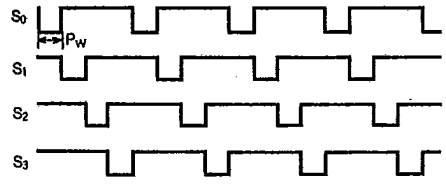
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
↓	↓	↓	↓	↓	↓	↓	↓
OA_3	OA_2	OA_1	OA_0	OB_3	OB_2	OB_1	OB_0

Clearing the display RAM is not achieved by the reset signal (9-pin) but requires the execution of the clear command.
The timing diagrams for both the encoded and decoded modes are shown below.
For the encoded mode, a 3-to-8 or 4-to-16 decoder is required, according to whether eight or sixteen digit display used.

(1) Encoded mode

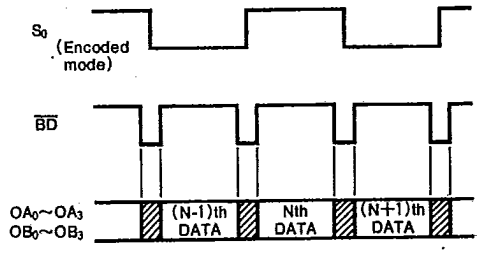


(2) Decoded mode



Note 4 : Here P_W is 640μs if the internal clock frequency is set to 100kHz.

Timing relations of S_0, $\overline{BD}$, and display outputs (OA_0~OA_3, OB_0~OB_3) are shown below.



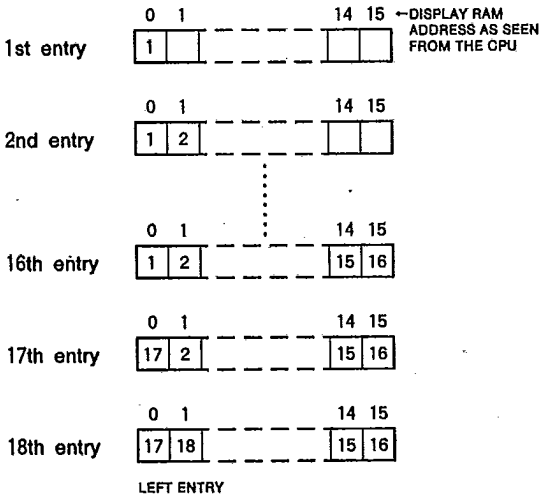
Note 5 : Values of the output data shown in the slanted line areas are decided upon the clear command executed last to become the value of the display RAM after the reset. The values in the slanted areas after reset will go low-level. In the same manner, the values OA_0~OA_3, OB_0~OB_3 are dependent on the clear command executed last. When the both A and B are blanked, the signal $\overline{BD}$ will be in low-level.

KEY ENTRY METHODS

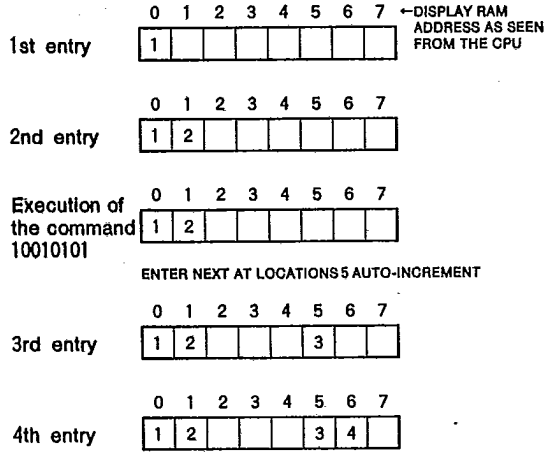
1. Left Entry

Address 0 in the display RAM corresponds to the leftmost position ($S_3S_2S_1S_0 = 0000$) of a display and address 15 (or address 7 in 8-character display) to the rightmost position ($S_3S_2S_1S_0 = 1111$ or $S_2S_1S_0 = 111$). The 17th (9th) character is entered back into the leftmost position.

Auto-increment mode



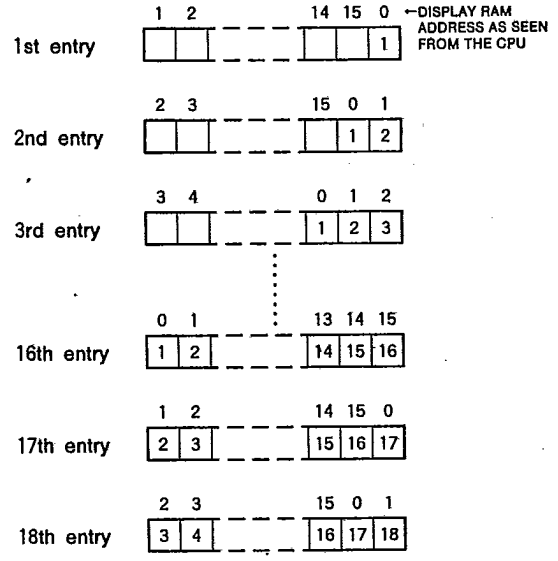
Auto-increment mode



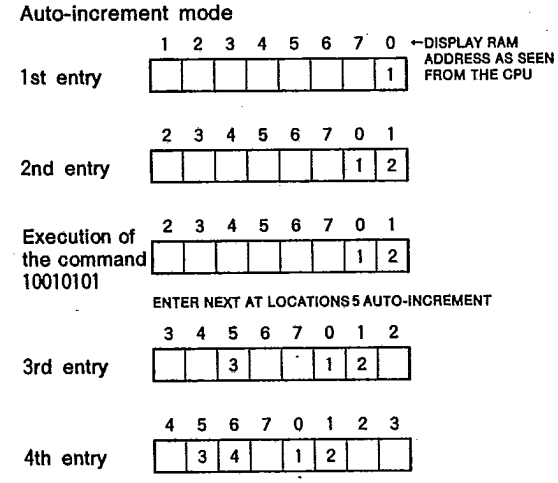
2. Right Entry

The first data is entered in the rightmost position of a display. From the next entry, the display is shifted left one character and the new data is placed in the rightmost position. A display position and a register address as viewed from the CPU change each time and do not correspond.

Auto-increment mode



Auto-increment mode



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Maximum power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−60~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{IH(RL)}$	High-level input voltage, for return line inputs		2.2			V
V_{IH}	High-level input voltage, all others		2.0			V
$V_{IL(RL)}$	Low-level input voltage, for return line inputs		V_{SS}-0.5		1.4	V
V_{IL}	Low-level input voltage, all others		V_{SS}-0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
$V_{OH(INT)}$	High-level output voltage, interrupt request output	I_{OH}=−400μA	3.5			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}				120	mA
$I_{I(RL)}$	Input current, return line inputs, shift input and control input	V_I=V_{CC}			10	μA
		V_I=0V	−100			
I_I	Input current, all others	V_I=0V, V_{CC}	−10		10	μA
I_{OZ}	Off-state output current	V_O=0V~V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_I=V_{CC}	5		10	pF
C_O	Output terminal capacitance	V_O=V_{CC}	10		20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(R)}$	Read cycle time		1000			ns
$t_{W(R)}$	Read pulse width		250			ns
$t_{SU(A-R)}$	Address setup time befor RD		0			ns
$t_{h(R-A)}$	Address setup time after RD		0			ns

Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(W)}$	Write cycle time		1000			ns
$t_{W(W)}$	Write pulse width		250			ns
$t_{SU(A-W)}$	Address setup time before WR		0			ns
$t_{h(W-A)}$	Address hold time after WR		0			ns
$t_{SU(DQ-W)}$	Data input setup time before WR		150			ns
$t_{h(W-DQ)}$	Data input hold time after WR		0			ns

Other Timing

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(\phi)}$	Clock cycle time		320		DC	ns
$t_{W(\phi)}$	Clock pulse width		120			ns

For an internal clock frequency of 100kHz

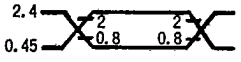
- Key scan cycle time: ~ 5.1ms
- Key debounce cycle time: ~10.3ms
- Single-key scan time: 80μs
- Display scan time: ~10.3ms
- Single digit display time: 490μs
- Blanking time: 150μs
- Internal clock cycle: 10μs

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output enable time after read	C_L=150pF			150	ns
$t_{PZV(A-DQ)}$	Output enabl time after address				250	ns
$t_{PVZ(R-DQ)}$	Output disable time after read		10		100	ns

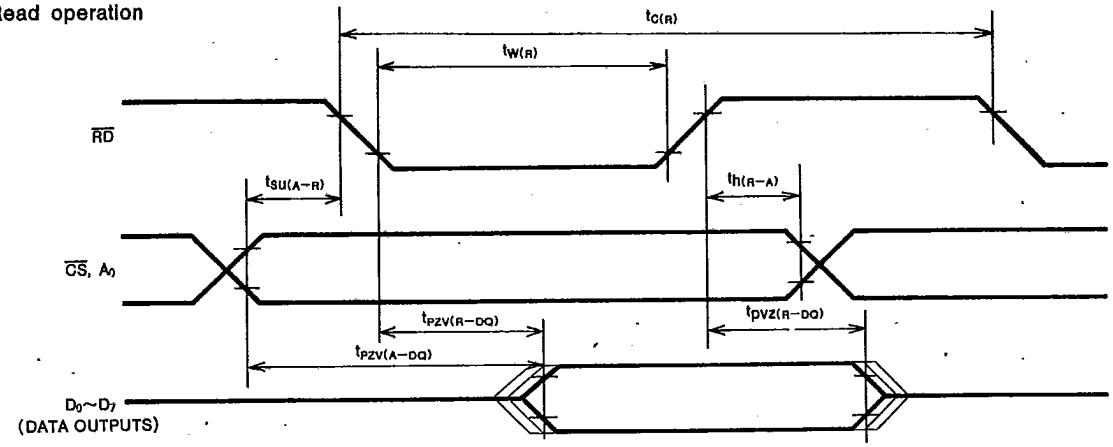
Note 6 : A. C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Referens level Input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

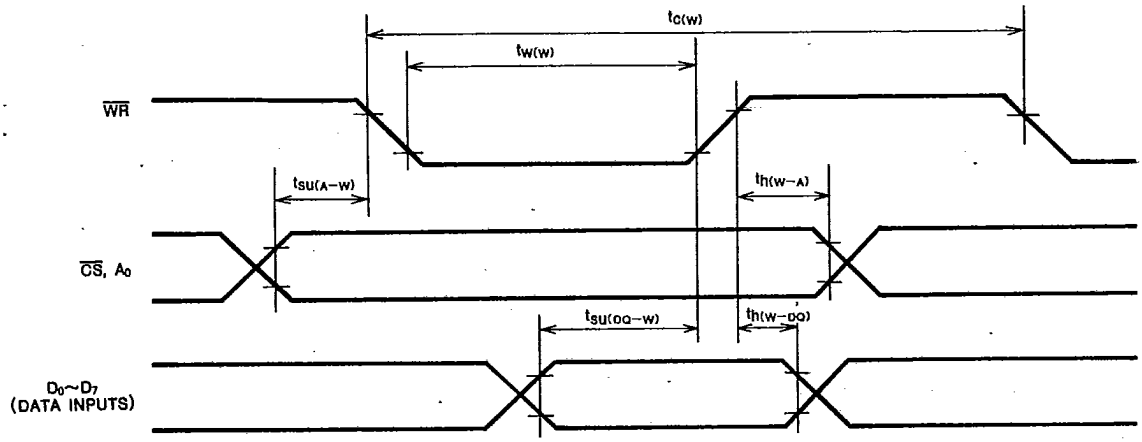


TIMING DIAGRAM

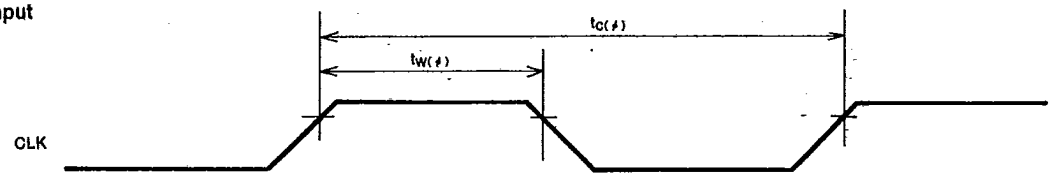
Read operation



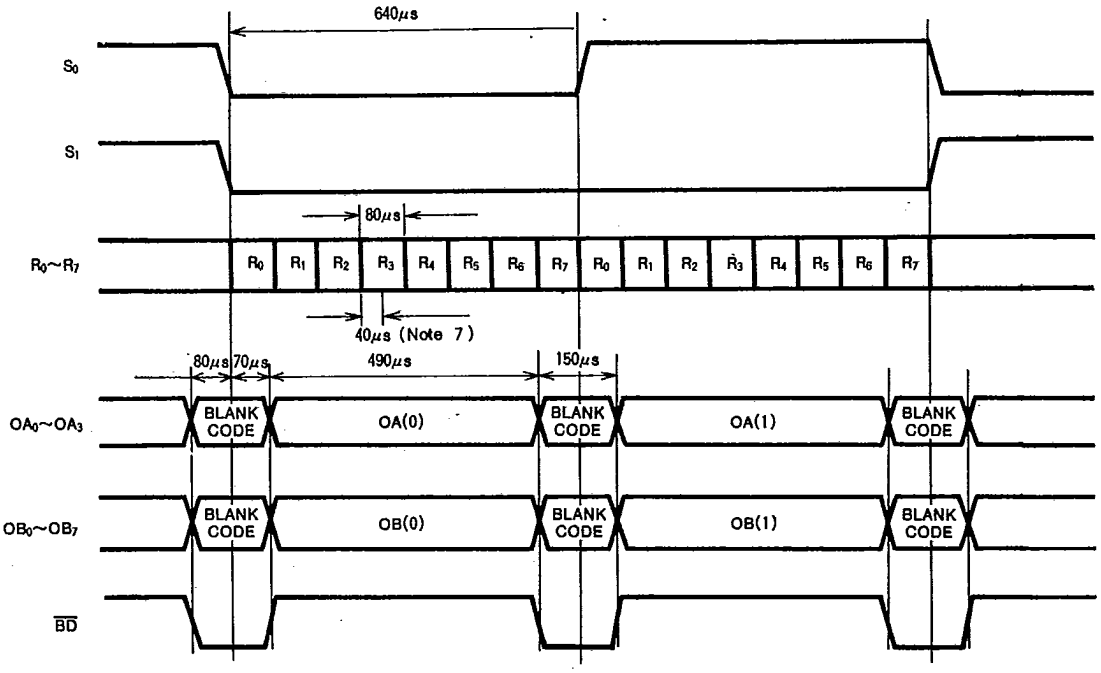
Write operation



Clock Input

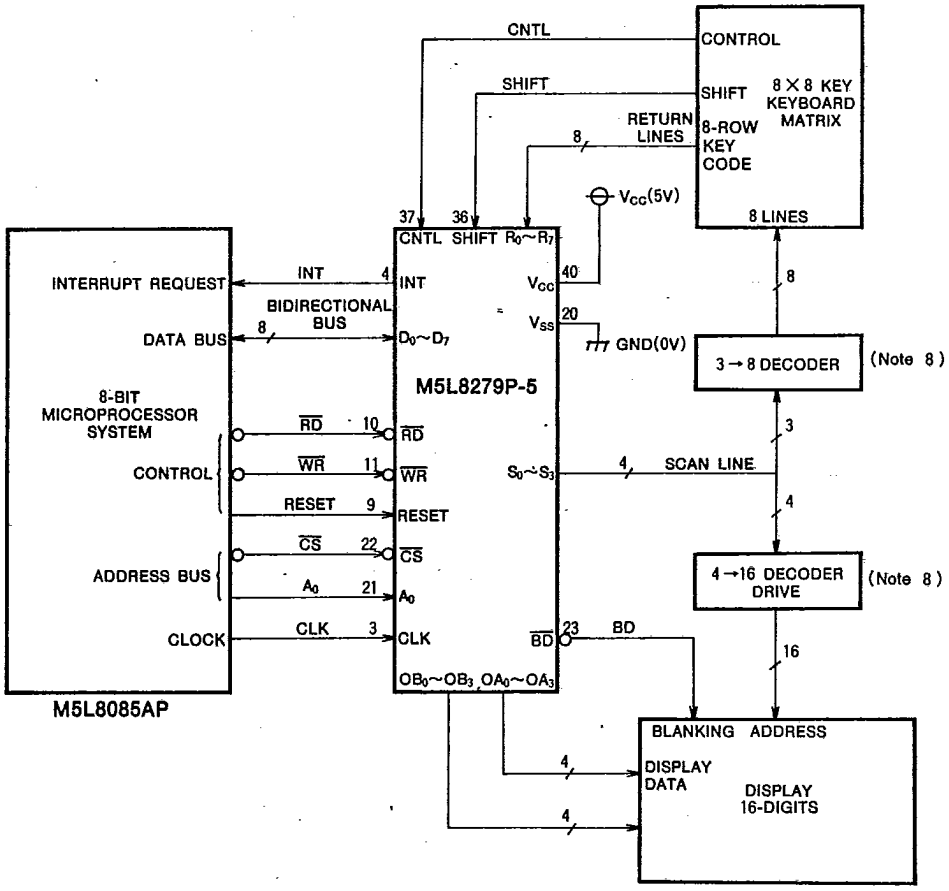


DISPLAY (This example is encoded display, left entry mode with internal clock cycle 10μsec. Scan timing output S_2, S_3 are not shown.)



Note 7 : The scanned data on the return line is sampled serialy from R_0 to R_7. Each data is latched in the middle of the each sampling period.

APPLICATION EXAMPLE



Note 8 : When using an 8-bit character display of more than 9 digits for the decoder display, it is necessary to provide two decoders for example 4 → 10 decoder, 4 → 16 decoder and key scan 3 → 8 decoder.
Only S_0, S_1 and S_2 may be used as inputs to the key scan 3 → 8 decoder.
(Don't drive the keyboard decoder with the MSB of the scan line.)