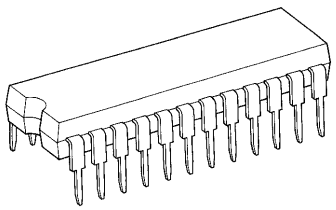
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA1300AN

A DEFLECTION PROCESSOR IC FOR MULTI POINT FREQUENCIES SCANNING CTV

TA1300AN is a deflection processor for multi frequencies scanning TV.
TA1300AN provides sync and deflection processing of horizontal and vertical sync for HDTV format signal and double scanning signal of PAL / NTSC.
These functions are integrated in a 24 pin dual-in-line shrink-type plastic package.
TA1300AN provides I^2C bus interface, so various functions and controls are adjustable via the bus.



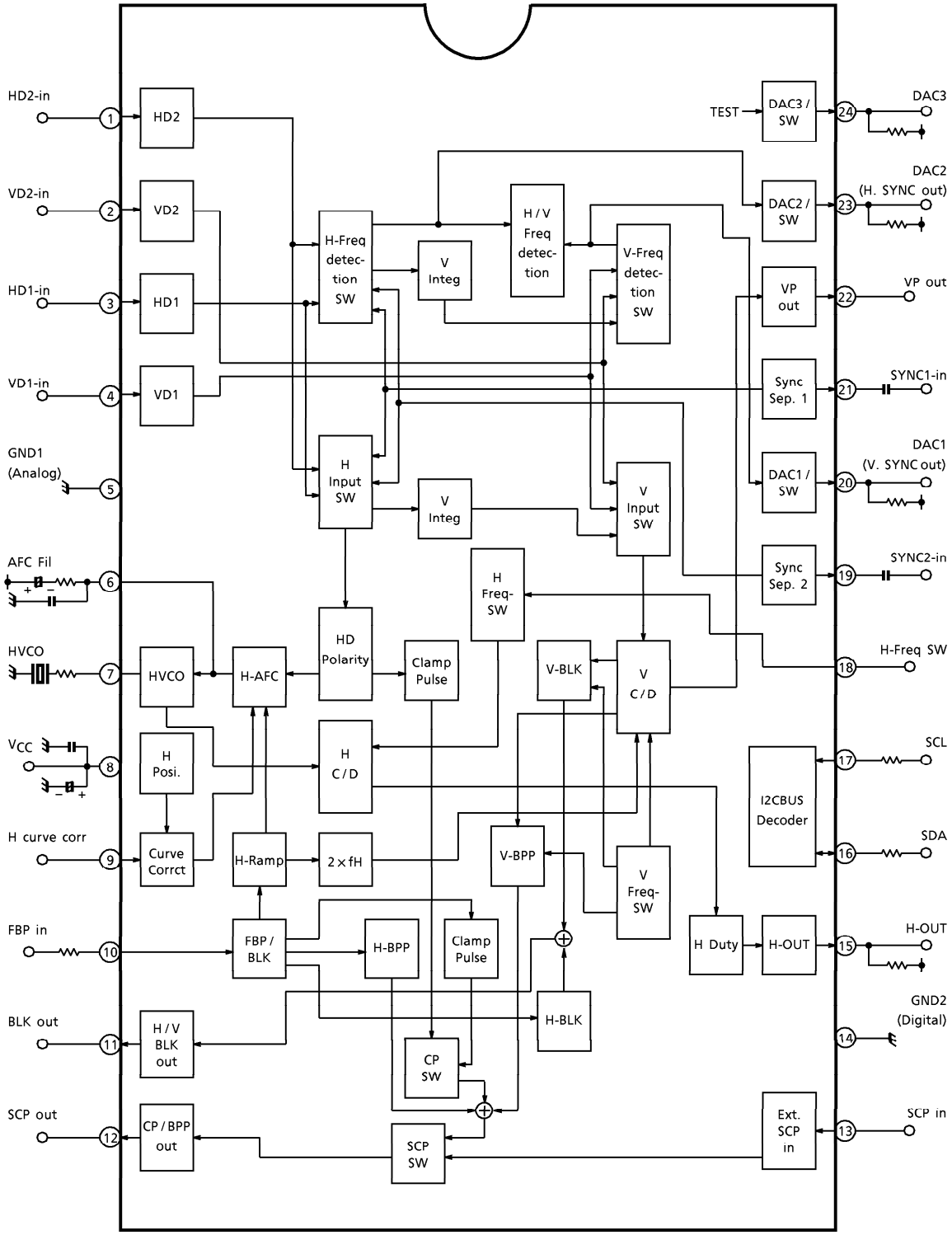
SDIP24-P-300-1.78

Weight : 1.22 g (Typ.)

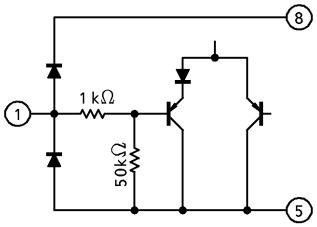
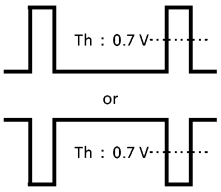
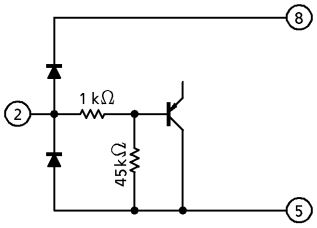
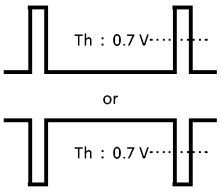
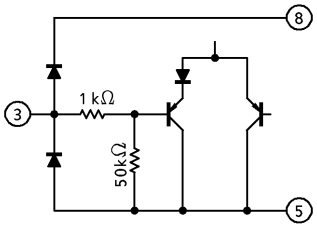
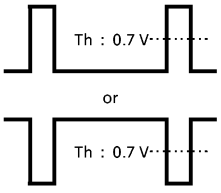
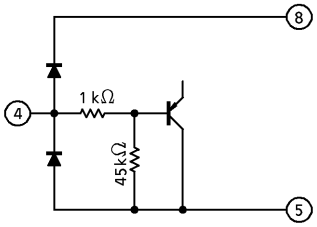
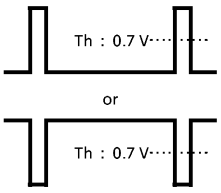
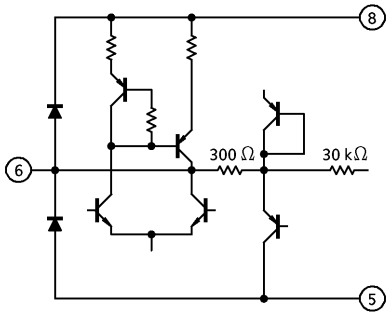
FEATURES

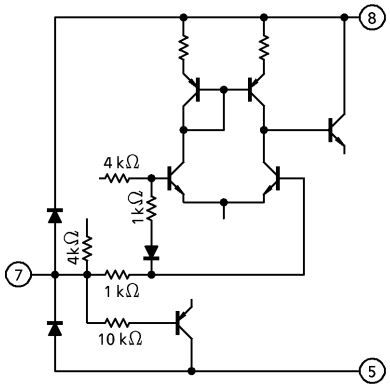
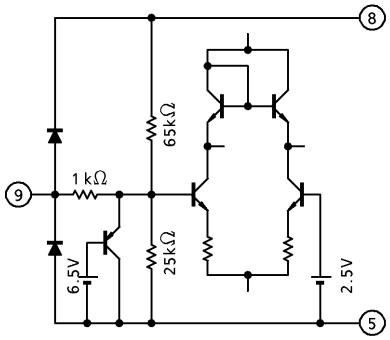
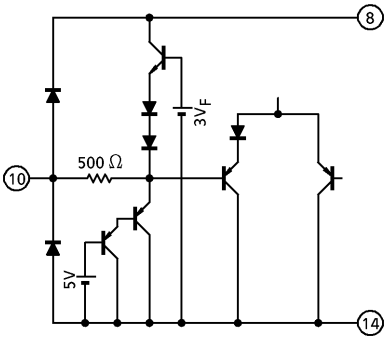
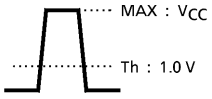
- Horizontal frequency detection circuit (15.75 kHz / 31.5 kHz / 33.75 kHz)
- Vertical frequency detection circuit (480I / 480P / 1080I / 1080P / PAL 100 Hz / NTSC 120 Hz)
- Clamping pulse and black peak detection stopping pulse output circuit
- Horizontal and vertical blanking pulse output circuit
- Horizontal output circuit
- Vertical pulse output circuit (VP output)
- Accepts 3-level sync for Japan HDTV (2-input) / Accepts both negative and positive HD and VD (2-input)
- Horizontal and vertical input frequency counter circuit
- Horizontal or composite-sync output / Vertical sync output
- Mask for the copy guard signal

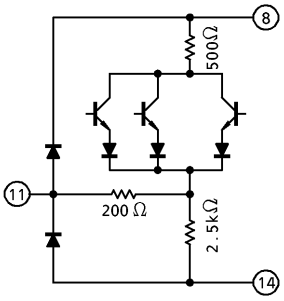
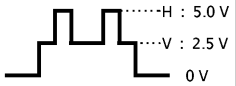
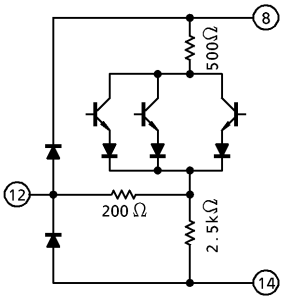
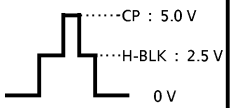
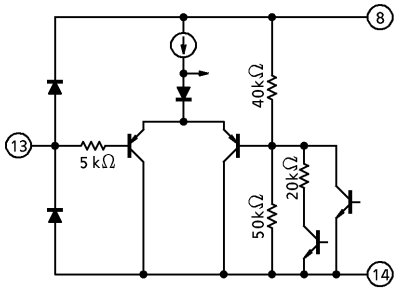
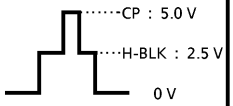
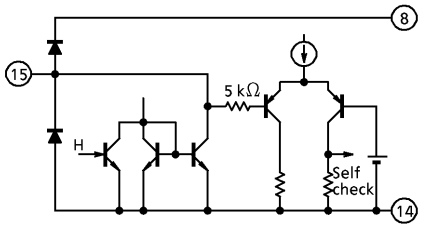
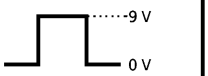
BLOCK DIAGRAM

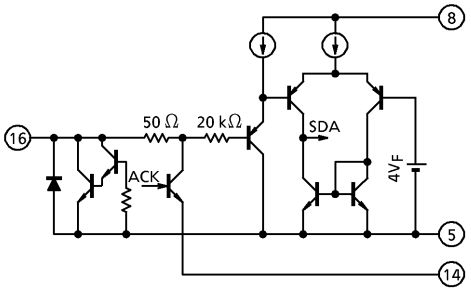
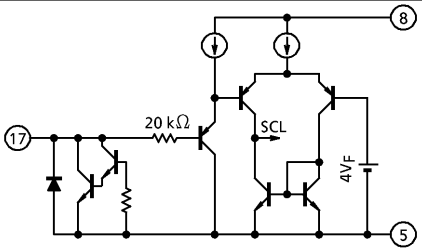
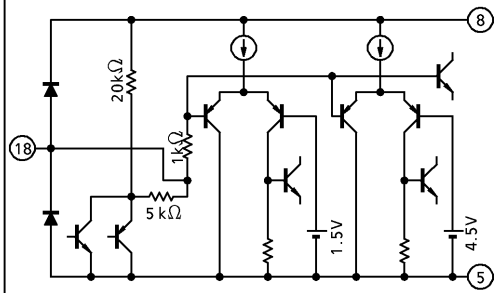
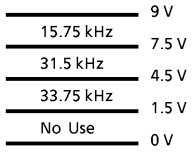
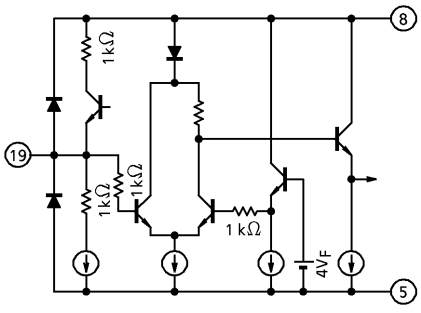
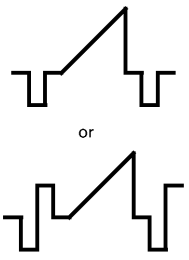


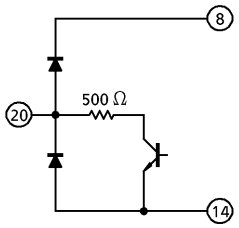
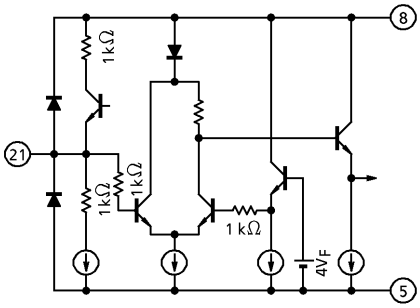
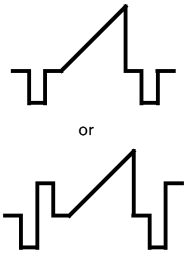
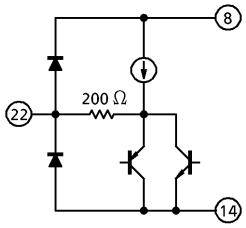
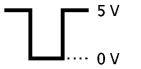
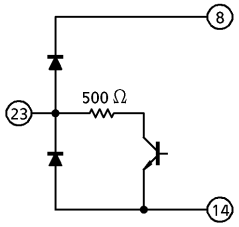
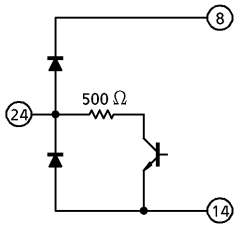
TERMINAL FUNCTIONS

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	INPUT / OUTPUT SIGNAL
1	HD2 input	Input the horizontal synchronizing signal. Its polarity correspond to both positive and negative.		
2	VD2 input	Input the vertical synchronizing signal. Its polarity correspond to both positive and negative.		
3	HD1 input	Input the horizontal synchronizing signal from UP-CONVERTER. Its polarity correspond to both positive and negative.		
4	VD1 input	Input the vertical synchronizing signal from UP-CONVERTER. Its polarity correspond to both positive and negative.		
5	GND1 (Analog)	The GND pin for Analog circuit blocks.	—	—
6	AFC filter	Connect the filter for horizontal AFC. The frequency of the horizontal output is varied by the voltage at this pin.		DC

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	INPUT / OUTPUT SIGNAL
7	HVCO	Connect the ceramic oscillator for horizontal oscillation. The oscillator to be used is CSB503F30, made by MURATA electronics.		—
8	V_{CC}	The V_{CC} pin. Connect 9 V (TYP.).	—	—
9	H curve correction	Used to correct distortion of picture in the case of high-tension fluctuation. Input the AC component of high-tension fluctuation. Not to use the distortion correction feature, connect a capacitor between this pin and GND.		DC : 2.5 V
10	FBP input	Input FBP for horizontal AFC.		

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	INPUT / OUTPUT SIGNAL
11	BLK output	Horizontal and vertical blanking pulse output pin.		
12	SCP output	SCP (Sand Castle Pulse) output pin. The output signal consists of clamp pulse, horizontal blanking pulse and vertical blanking pulse.		
13	SCP input	Input the SCP signal from UP-CONVERTER. The components are clamp, horizontal and vertical blanking pulses. If no-use, connect to GND.		
14	GND2 (Digital)	The GND pin for Logic blocks.	—	—
15	H OUT	Horizontal output pin. This pin is open-collector system.		

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	INPUT / OUTPUT SIGNAL
16	SDA	The SDA pin for I^2C BUS.		—
17	SCL	The SCL pin for I^2C BUS.		—
18	HORIZONTAL FREQUENCY SW	Switches between the horizontal frequencies. If H-freq is controlled by the BUS, open this pin. Pin-control has the priority over the BUS selection.		Output (When BUS control) ; 00 (15.75 k) : DC9 V 01 (31.5 k) : DC6 V 10 (33.75 k) : DC3 V Input (When pin control) ; 
19	SYNC2 input	Input a signal to separate sync signal. Input signal through a capacitor.		White 100% = 1 V_{p-p} 

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	INPUT / OUTPUT SIGNAL
20	DAC1 (V. SYNC output)	DAC1 or vertical synchronizing signal output pin. This pin is open-collector system.		DC or V SYNC
21	SYNC1 input	Input a signal to separate sync signal. Input signal through a capacitor.		White 100% = 1 V_{p-p}  or
22	VP output	Vertical pulse output pin.		
23	DAC2 (H. SYNC output)	DAC2, horizontal sync signal or composite sync signal output pin. This pin is open-collector system.		DC or H SYNC
24	DAC3 output	DAC3 output pin. This pin is open-collector system.		DC

BUS CONTROL MAP

WRITE MODE

SLAVE ADDRESS : 48H (01001000)

SUB-ADDRESS	D_7 MSB	D_6	D_5	D_4	D_3	D_2	D_1	D_0 LSB	Preset MSB	Preset LSB
00	H-FREQUENCY		H-DUTY	DAC1	DAC2	DAC3	TEST		1000	0000
01	HORIZONTAL POSITION							HBP-PHS	1000	0000
02	HBL-PHS	SCP-SW		CLP-PHS	FREQ DET SW		INPUT SW		0000	0000
03	V BLANKING STOP PHASE					V-FREQUENCY			1000	0000

READ MODE

SLAVE ADDRESS : 49H (01001001)

	D_7 MSB	D_6	D_5	D_4	D_3	D_2	D_1	D_0 LSB
0	PONRES	V FREQUENCY DET						
1	H-OUT	H FREQUENCY DET						

BUS CONTROL FUNCTION

WRITE MODE (* : Preset)

- H-FREQUENCY (Horizontal oscillation frequency)

  The horizontal frequency switch. The status of pin 18 has priority over the BUS selection.

  (00) ; 15.75 kHz (01) ; 31.5 kHz *(10) ; 33.75 kHz (11) ; Don't use.

- H-DUTY (H-out duty)

  H-out duty switch.

  *(0) ; 41% (1) ; 47%

- DAC1, 2, 3 (DAC control switch)

  1 bit DAC control switch (open-collector).

  *(0) ; OPEN (high) (1) ; ON (low)

- TEST (Test mode)

  Switching outputs of DAC 1 / 2 / 3 and IC test mode for the shipping.

  *(00) ; DAC outputs are active as 1 bit DAC.

  (01) ; V.SYNC from V.SYNC count SW circuit is output to DAC1.
  H.SYNC / C.SYNC from H.SYNC count SW circuit is output to DAC2.
  DAC3 is active as DAC.

  (10) ; H.SYNC / C.SYNC from H.SYNC count SW circuit is output to DAC2
  DAC1 / 3 is active as DAC.

  (11) ; IC test mode for the shipping.

- HORIZONTAL POSITION (Horizontal picture position)

  Adjust horizontal picture position. HD is output 0.5 μs later than the input FBP when the BUS data is center value.

  (0000000) ; − 10.5% (H periodically)

  *(1000000) ; 0%

  (11111111) ; + 10.5%

- HBP-PHS (Horizontal black peak detection pulse phase)
  When SCP SW data is (00), the phase of H-BPP (horizontal black peak detection stopping pulse) which is output from pin 12 can be switched.
  *(0) ; from 6.3% forward to 6.3% later of FBP
  (1) ; from 3.5% forward to 3.5% later of FBP

- HBL-PHS (Horizontal blanking start phase)
  Change the H-BLK start phase. H-BLK is output from pin 11.
  *(0) ; the phase is same as FBP (1) ; 4% forward of horizontal period from FBP phase

- SCP-SW (SCP mode switch)
  SCP output from pin 12 is switched.
  *(00) ; IC internal mode (CP + BPP)
  (01) ; IC internal mode (only CP)
  (10) ; CP is IC internal pulse (CP + external BPP)
  (11) ; External input

  Note) External input is the pulse from pin 13.

- CLP PHS (Clamp pulse phase change)
  When SCP SW data is (00), (01) or (10), the CP phase can be changed.
  If no-signal inputs, the CP will be output 1.2 μs (4.2%) later than FBP start phase and its width will be 0.8 μs (2.7%) automatically.
  *(0) ; 0.92 μs (3.1%) later than HD stop phase, 0.74 μs (2.5%) width
  (1) ; 0.24 μs (0.8%) later than HD stop phase, 0.71 μs (2.4%) width

- FREQ DET SW (switching inputs for horizontal and vertical frequency counter)
  Switching input signals for horizontal and vertical frequency counter. This SW acts independently from INPUT SW mode and the result is output as Read BUS data.
  *(00) ; SYNC1 input (01) ; HD1 / VD1 inputs (10) ; HD2 / VD2 inputs (11) ; SYNC2 input

- INPUT SW (input switch)
  Switch input signals.
  *(00) ; HD1 / VD1 inputs (01) ; HD2 / VD2 inputs (10) ; SYNC1 input (11) ; SYNC2 input

- V BLANKING STOP PHASE [V-BLK P] (vertical BLK phase switch)
  Change the V-BLK stop phase
  (00000) ; 17H *(10000) ; 33H (11110) ; 47H (11111) ; Internal V-BLK OFF
- V-FREQUENCY (Vertical free-run frequency (pull-in range))
  Set the vertical frequency pull-in range, V-STOP and Vertical black peak detection phase. It can be pulled in from 49H later than Vertical signal input.
  Vertical black peak detection stop phase is 20H later than V-BLK P. However, when this data is (010), it is 50H later than vertical signal.

	Pull-in range	V black peak detection pulse phase	V-BLK start phase	Ref. / V (H) frequency
*(000)	49~1281H	V-BLK P + 20~1100H	VP output start phase	1080P / 30 Hz (33.75 kHz)
(001)	49~849H	V-BLK P + 20~730H		720P / 60 Hz (45 kHz)
(010)	49~637H	50~545H	512H	Compression / 60 Hz (33.75 kHz)
(011)	49~637H	V-BLK P + 20~545H	VP output start phase	1080I / 60 Hz (33.75 kHz)
(100)	49~613H	V-BLK P + 20~500H		480P / 60 Hz (31.5 kHz)
(101)	49~363H	V-BLK P + 20~290H		PAL / SECAM / 100 Hz (31.5 kHz), 50 Hz (15.625 kHz)
(110)	49~307H	V-BLK P + 20~240H		NTSC / 60 Hz (15.734 kHz), 120 Hz (31.5 kHz)
(111)	VP Stop	—	—	—

READ MODE

- PONRES (POWER ON RESET)
  0 ; Status was read (on and after second data read)
  1 ; Just after power-on (first data read)
- H-OUT (H-OUT self-check result)
  H-out signal exist or not.
  0 ; No-signal 1 ; Exist
- V FREQ DET (Vertical frequency of SYNC or VD input which is selected by FREQ DET SW)
  000000~0001100 ; No-VD signal
  0001101 ; nearly 162 Hz
  1111111 ; 16.5 Hz

  How to calculate the vertical frequency (X) ;
  Decimalize V-FREQ DET READ data and the result is called Y.
  If H-FREQUENCY is 15.75 kHz or 31.5 kHz, Z = 476.2 μs.
  If H-FREQUENCY is 33.75 kHz or 45 kHz, Z = 474.1 μs.
  $$\text{Vertical frequency (X)} = 1 \div (Y \times Z)\ [\text{Hz}]$$
  The error of Y is from +1 to −0. When the vertical frequency is more than approximate 162 Hz, it is not able to be measured exactly.
  The time constant to separate V.SYNC from integrated C.SYNC is 9 μs. (error : ±1 μs)

- H FREQ DET (Horizontal frequency of SYNC or HD input which is selected by FREQ DET SW)
  0000000 ; No-signal 1111111 ; more than 53 kHz

  How to calculate the horizontal frequency (X) ;

  X, Y and Z are defined in the same way as the case of vertical frequency.

  Horizontal frequency (X) = Y ÷ (5 × Z) [kHz]

  The error of Y is from +1 to −0. When the horizontal frequency is more than approximate 53 kHz, it is not able to be measured exactly.

  When V-SYNC or VD does not input, the horizontal frequency is not measured and the DATA became 0000000.

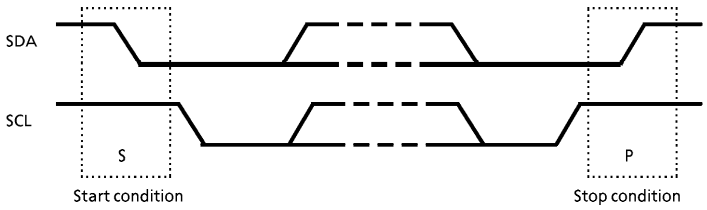
  Note) The start trigger for frequency counting is ACK of 2nd byte in BUS read mode.
  The counting period is between first V-sync (VD) and second V-sync (VD) after the trigger. we recommend that the BUS reading interval is more than 3 V because the BUS read data is stable.

DATA TRANSFER FORMAT VIA I²C BUS

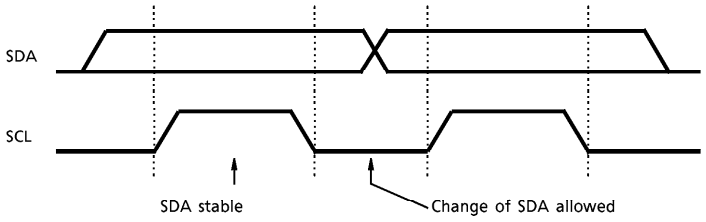
SLAVE ADDRESS : 48H (01001000)

A6	A5	A4	A3	A2	A1	A0	W / R
0	1	0	0	1	0	0	0 / 1

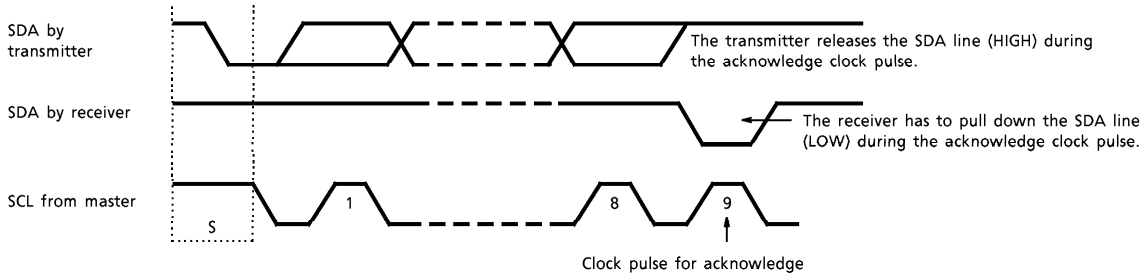
Start and stop condition



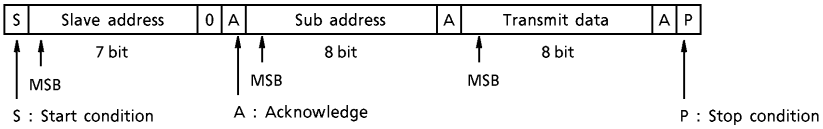
Bit transfer



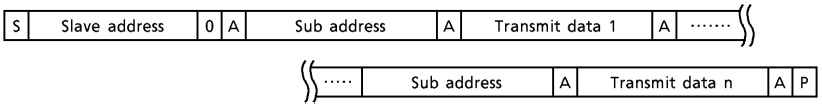
Acknowledge



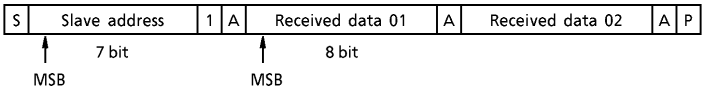
Data transmit format 1



Data transmit format 2



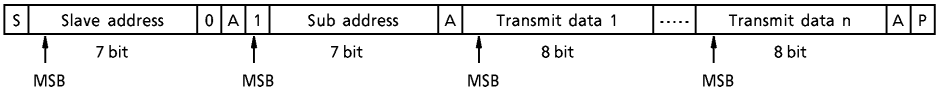
Data receive format



At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave.

The Stop condition is generated by the master.

Optional data transmit format : Automatic increment mode



In this transmission method, data is set on automatically incremented sub-address from the specified sub-address.

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
SUPPLY VOLTAGE	V_{CCmax}	12	V
MAXIMUM INPUT VOLTAGE	einmax	9	V_{p-p}
POWER CONSUMPTION	P_D (*1)	1250	mW
POWER CONSUMPTION REDUCTION RATIO (*1)	1 / Qja	– 10	mW / °C
OPERATING TEMPERATURE	T_{opr}	– 20~65	°C
STORAGE TEMPERATURE	T_{stg}	– 55~150	°C

(*1) : Refer to the figure below.

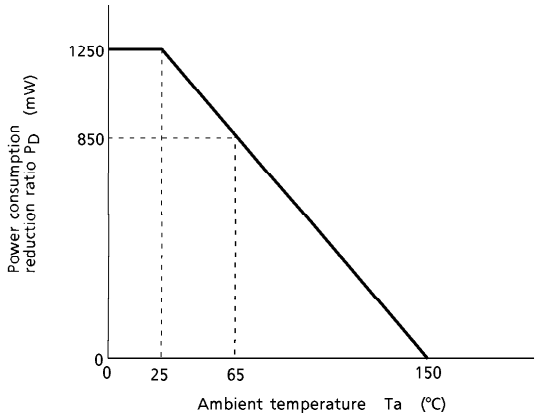


Fig. P_D-Ta curve

RECOMMENDED OPERATING CONDITION

CHARACTERISTICS	CONTENT	MIN.	TYP.	MAX.	UNIT
POWER SUPPLY VOLTAGE (V_{CC})	Pin 8	8.7	9.0	9.3	V
HD1, HD2 Input Level	Pin 3, 1	2.0	5.0	—	V_{p-p}
VD1, VD2 Input Level	Pin 4, 2	2.0	5.0	—	
SYNC1, SYNC2 Input Level	Pin 21, 2, White 100% : include Sync (Negative Sync)	0.9	1.0	1.1	
FBP Input Current	Pin 10	—	1.0	2.0	mA
DAC1, DAC2, DAC3	Pin 19, 23, 24	—	0.5	1.0	
H-OUT Input Current	Pin 15	—	8	15	

CURRENT CONSUMPTION

(V_{CC} = 9 V and Ta = 25°C, unless otherwise specified)

Pin NAME	SYMBOL	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT
V_{CC}	I_{CC}	—	35	42	49	mA

PIN VOLTAGE

No.	CHARACTERISTICS	SYMBOL	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT
1	HD2 Input	V1	—	0.00	0.05	0.20	V
2	VD2 Input	V2	—	0.00	0.05	0.20	
3	HD1 Input	V3	—	0.00	0.05	0.20	
4	VD2 Input	V4	—	0.00	0.05	0.20	
7	HVCO	V7	—	4.70	5.00	5.30	
9	H Curve Correction	V9	—	2.30	2.50	2.70	
13	SCP Input	V13	—	0.00	0.40	0.80	
19	SYNC2 Input	V19	—	1.80	2.00	2.20	
21	SYNC1 Input	V21	—	1.80	2.00	2.20	

AC CHARACTERISTICS

HORIZONTAL BLOCK

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Sync1 / 2 input horizontal sync phase	$S_{1PH\,/\,2PH}$	(Note HA01)	0.55	0.65	0.75	μs
HD1 / 2 input horizontal sync phase	$HD_{1PH\,/\,2PH}$	(Note HA02)	0.58	0.68	0.78	
Polarity distinction active range	HD_{DUTY1}	(Note HA03)	—	0.5	2.0	%
	HD_{DUTY2}		62	67	72	
	HD_{DUTY3}		—	99.5	98	
	HD_{DUTY4}		47.5	52.5	57.5	
Sync1 / 2 input threshold amplitude	$V_{thS1\,/\,2}$	(Note HA04)	0.04	0.07	0.1	V_{p-p}
HD1 / 2 input threshold voltage	$V_{thHD1\,/\,2}$	(Note HA05)	0.7	0.8	0.9	
Horizontal phase adjustment variable range	$\Delta H_{SFT\,-}$	(Note HA06)	9.5	10.5	11.5	%
	$\Delta H_{SFT\,+}$		9.5	10.5	11.5	
H curve correction variable range	ΔH#9	(Note HA07)	2.9	3.4	3.9	
Clamp pulse phase / width / level	CP_{S0}	(Note HA08)	2.4	3.1	3.8	%
	CP_{W0}		2.0	2.5	3.0	
	CP_{V0}		4.7	5.0	5.3	V
	CP_{S1}		0	0.8	1.5	%
	CP_{W1}		1.9	2.4	2.9	
	CP_{V1}		4.7	5.0	5.3	V
	CP_{S2}		3.2	4.2	5.2	%
	CP_{W2}		2.2	2.7	3.2	
	CP_{V2}		4.7	5.0	5.3	V
Black peak detection pulse phase / level	HBP_{S0a}	(Note HA09)	4.3	6.3	8.3	%
	HBP_{W0b}		4.3	6.3	8.3	
	HBP_{V0}		2.2	2.5	2.8	V
	HBP_{S1a}		1.5	3.5	5.5	%
	HBP_{W1b}		1.5	3.5	5.5	
	HBP_{V1}		2.2	2.5	2.8	V

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Horizontal blanking pulse phase / width / level	$HBLK_{S0a}$	(Note HA10)	0	0	0.3	%
	$HBLK_{S0b}$		0	0.1	0.3	
	$HBLK_{V0}$		4.7	5.0	5.3	V
	$HBLK_{S1a}$		2	4	6	%
	$HBLK_{S1b}$		0	0.1	0.3	
	$HBLK_{V1}$		4.7	5.0	5.3	V
FBP input threshold	V_{thFBP}	(Note HA11)	0.8	1.0	1.2	
Delayed HD pulse width	W_{dHD}	(Note HA12)	0.9	1.1	1.3	μs
AFC phase detection current	ID1 / 2	(Note HB01)	310	385	460	μA
	ID3 / 4		520	650	780	
HVCO oscillation start voltage	V_{VCO}	Monitor pin 7, V_{CC} voltage	3.9	4.2	4.5	V
H-OUT start voltage	V_{HON}	Monitor pin 15, V_{CC} voltage	5.3	5.6	5.9	
H-OUT pulse duty	TH_{00A}	(Note HB02)	39	41	43	%
	TH_{01A}		38	40	42	
	TH_{10A}		38	40	42	
	TH_{00B}		45	47	49	
	TH_{01B}		44.5	46.5	48.5	
	TH_{10B}		45	47	49	
Horizontal free-run frequency	F00	(Note HB03)	15.59	15.75	15.91	kHz
	F01		31.19	31.5	31.82	
	F10		33.41	33.75	34.09	
	F50		15.47	15.625	15.78	
Horizontal oscillation frequency variable range	$F00_{MIN}$	(Note HB04)	14.48	14.78	15.08	kHz
	$F00_{MAX}$		16.37	16.70	17.03	
	$F01_{MIN}$		28.97	29.56	30.15	
	$F01_{MAX}$		32.72	33.39	34.06	
	$F10_{MIN}$		30.91	31.54	32.17	
	$F10_{MAX}$		34.91	35.62	36.33	
	$F50_{MIN}$		14.47	14.77	15.07	
	$F50_{MAX}$		16.36	16.69	17.02	
Horizontal oscillation control sensitivity	BH00	(Note HB05), Hz / 0.1 V	240	300	360	—
	BH01		480	600	720	
	BH10		480	600	720	
H-OUT output voltage	$V15_H$	(Note HB06)	4.05	4.5	4.95	V
	$V15_L$		—	0.1	0.3	
Pin 18 control voltage threshold (Horizontal frequency SW)	$V18_L$	(Note HB07)	1.3	1.5	1.7	
	$V184_M$		4.3	4.5	4.7	
	$V187_H$		7.3	7.5	7.7	

ITEM		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
DAC output voltage	DAC1	$VDAC_{1H}$	TEST = (00), DAC1 = (0)	8.5	9.0	—	V
		$VDAC_{1L}$	TEST = (00), DAC1 = (1)	—	0.5	0.7	
	DAC2	$VDAC_{2H}$	TEST = (00), DAC2 = (0)	8.5	9.0	—	
		$VDAC_{2L}$	TEST = (00), DAC2 = (1)	—	0.5	0.7	
	DAC3	$VDAC_{3H}$	TEST = (00), DAC3 = (0)	8.5	9.0	—	
		$VDAC_{3L}$	TEST = (00), DAC3 = (1)	—	0.5	0.7	
	DAC3	$V01D_{3H}$	TEST = (01), DAC3 = (0)	8.5	8.8	9.0	
		$V01D_{3L}$	TEST = (01), DAC3 = (1)	—	0.5	0.7	
	DAC1	$V10D_{1H}$	TEST = (10), DAC1 = (0)	8.5	9.0	—	
		$V10D_{1L}$	TEST = (10), DAC1 = (1)	—	0.5	0.7	
	DAC3	$V10D_{3H}$	TEST = (10), DAC3 = (0)	8.5	8.8	9.0	
		$V10D_{3L}$	TEST = (10), DAC3 = (1)	—	0.5	0.7	
H / V frequency distinction		FV_{50}	(Note HB08)	48	50	52	Hz
		FV_{60}		57	60	63	
		FV_{MIN}		—	16	18	
		FV_{MAX}		150	162	175	
		FH_{15}		14	15.6	17	kHz
		FH_{31}		30.7	31.6	32.5	
		FH_{33}		32.9	33.7	34.6	
		FH_{45}		44	45	46	
		FH_{MIN}		—	0.42	0.85	
		FH_{MAX}		52	54	—	
		FV_{SY}		14	15.6	17	Hz
		FH_{SY}		57	60	63	kHz

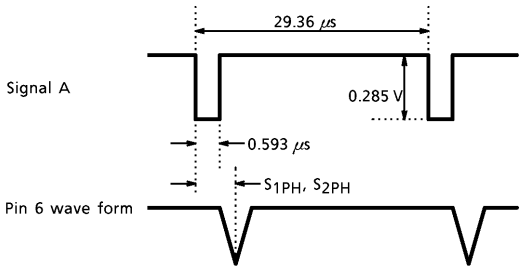
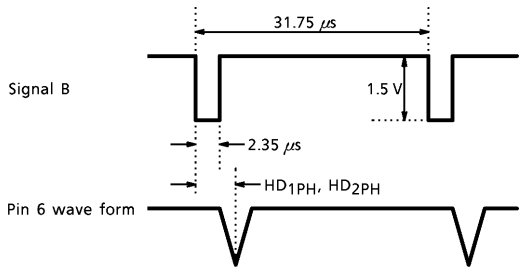
VERTICAL BLOCK

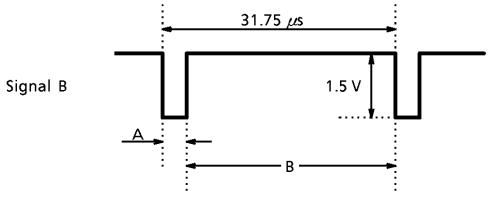
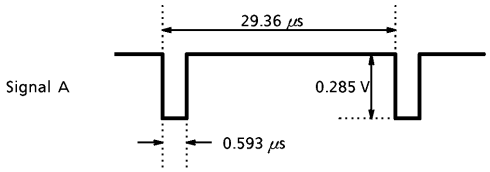
ITEM		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VP output pulse width		VP_W	(Note V01)	4	4.5	5	H
Vertical free-run (Maximum pull-in range)	000	VPt0		1278	1281	1284	
	001	VPt1		846	849	852	
	010	VPt2		634	637	640	
	011	VPt3		634	637	640	
	100	VPt4		610	613	616	
	101	VPt5		360	363	366	
	110	VPt6		304	307	310	
Vertical minimum pull-in range		T_{VPULL}	(Note V02)	48	49	50	
Vertical black peak detection pulse	000	$VBPP_{0E}$	(Note V03)	51	52	53	
		$VBPP_{0S}$		1099.5	1100.5	1101.5	
	001	$VBPP_{1E}$		51	52	53	
		$VBPP_{1S}$		729.5	730.5	731.5	
	010	$VBPP_{2E}$		49.5	50.5	51.5	
		$VBPP_{2S}$		544.5	545.5	546.5	
	011	$VBPP_{3E}$		49.5	50.5	51.5	
		$VBPP_{3S}$		544.5	545.5	546.5	
	100	$VBPP_{4E}$		51	52	53	
		$VBPP_{4S}$		499.5	500.5	501.5	
	101	$VBPP_{5E}$		51	52	53	
		$VBPP_{5S}$		289.5	290.5	291.5	
	110	$VBPP_{6E}$		51	52	53	
		$VBPP_{6S}$		239.5	240.5	241.5	
Vertical blanking stop phase	00H	V_{BLK00}	(Note V04)	16.5	17	17.5	
	10H	V_{BLK10}		32.5	33	33.5	
	1EH	V_{BLK1E}		46.5	47	47.5	
Vertical blanking start phase	010	V_{BLK512}	(Note V05)	511.5	512.5	513.5	
Vertical blanking output voltage		V_{11VBLK}	Pin 11, Vertical blanking period	2.2	2.5	2.8	V
VP output voltage	High	$V_{22VBLKH}$	Pin 22 voltage	4.6	5.0	5.4	V
	Low	$V_{22VBLKL}$		—	0.1	0.5	

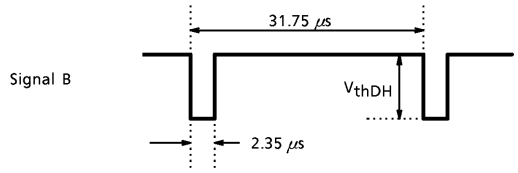
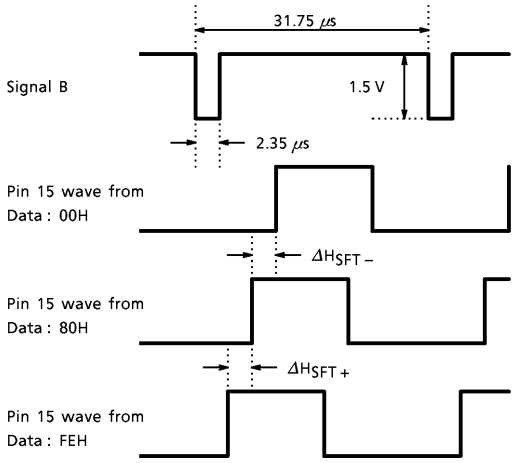
TEST CONDITION

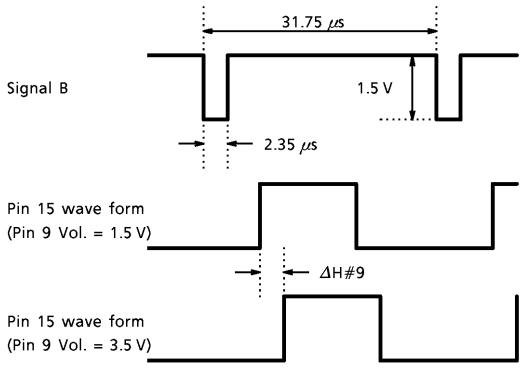
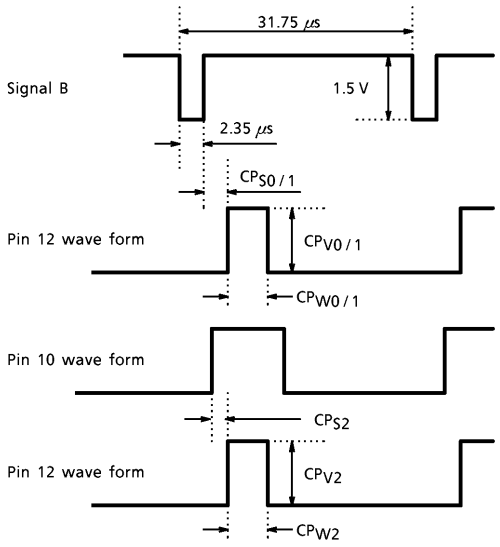
No.	SW CONDITION										
	SW06	SW09	SW10a	SW10b	SW15	SW16	SW17	SW18	SW19	SW21	SW24
1	c	a	Open	ON	ON	ON	ON	a	a or b	a or b	ON
2	c	a	Open	ON	ON	ON	ON	a	a	a	ON
3	d	a	Open	ON	ON	ON	ON	a	a	a	ON
4	a or b	a	Open	ON	ON	ON	ON	a	a	a	ON
5	c	a	Open	ON	Open	ON	ON	a	a	a	ON

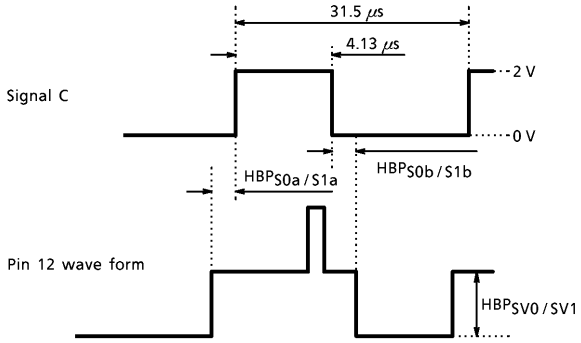
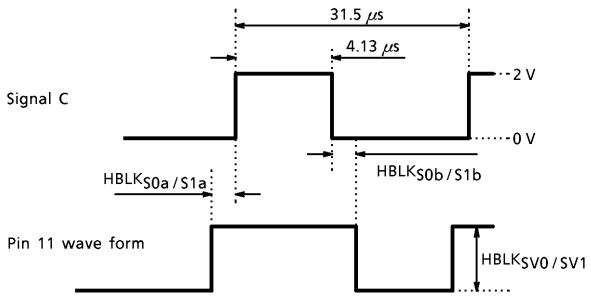
MEASUREMENT METHOD (V_{CC} = 9 V and Ta = 25°C, unless otherwise specified)

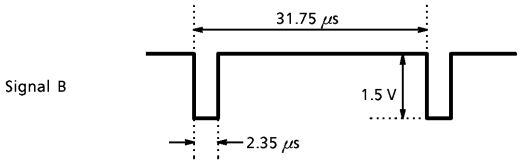
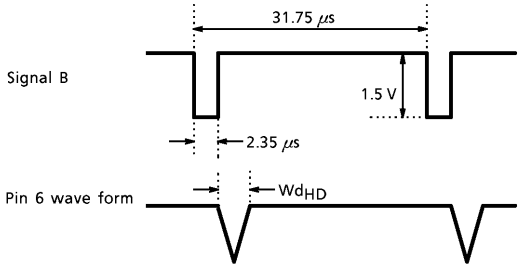
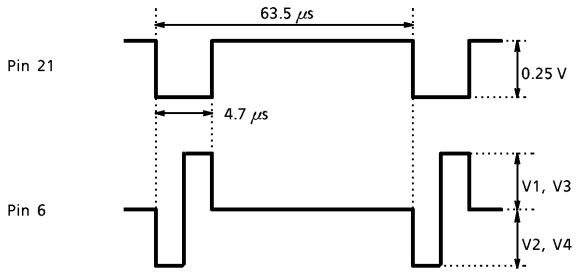
NOTE	ITEM	MEASURING METHOD
HA01	Sync1 / 2 input horizontal sync phase	① Test condition No. 1, SW19-a and SW21-b. ② Input Signal A to TPs1-in (Pin 21), and set sub-address (02) 02H. ③ Measure the difference (S_{1PH}) between signal A phase and a phase of Pin 6 (AFC filter) wave form. ④ SW19-b and SW21-a. ⑤ Input Signal A to TPs2-in (Pin 19), and set sub-address (02) 03H. ⑥ Measure the phase difference (S_{2PH}) as well. 
HA02	HD1 / 2 input horizontal sync phase	① Test condition No. 2. Set sub-address (00) 40H. ② Input Signal B to TP3 (Pin 3), and set sub-address (02) 00H. ③ Measure the phase difference (HD_{1PH}) between signal B and a wave form of Pin 6 (AFC filter). ④ Input Signal B to TP1 (Pin 1), and set sub-address (02) 01H. ⑤ Measure the phase difference (HD_{2PH}) as well. 

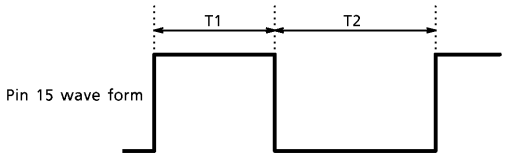
NOTE	ITEM	MEASURING METHOD
HA03	Polarity distinction active range	① Test Condition 2, and set sub-address (00) 43H. ② Input signal B to TP3 (Pin 3), and set sub-address (02) 00H. ③ Decreasing the duty of Signal B from 10% (get negative period shorter), measure the duty of Signal B (HD_{DUTY1}) when the phase between Signal B and H-OUT (Pin 15) change. ④ Increasing the duty of Signal B from 10% (get negative period longer), measure the duty of Signal B (HD_{DUTY2}) when the Pin 10 (FBP-IN) phase change against Signal B. ⑤ Increasing the duty of Signal B further (get negative period longer), measure the duty of Signal B (HD_{DUTY3}) when the phase between Signal B and H-OUT (Pin 15) change. ⑥ Decreasing the duty of Signal B from 90% (get negative period shorter), measure the duty of Signal B (HD_{DUTY4}) when the Pin 10 (FBP-IN) phase change against Signal B.  Duty = A / B × 100 [%] (0~100%)
HA04	Sync1 / 2 input threshold amplitude	① Test condition 1, SW19-a and SW21-b. Set sub-address (00) 83H. ② Input signal A to TPs1-in (Pin 21). ③ Set sub-address (02) 02H and measure the DC voltage of Sync. tip period of pin 21. (Vsync1) ④ Supply external voltage Pin 21 through 100 kΩ, and get the voltage higher than Vsync 1, and measure the DC voltage of Sync. tip period of Pin 21 when the Pin 15 (H-OUT) phase change against Signal A. (Vsync2) ⑤ V_{thS1} = Vsync2 − Vsync1 [V_{p-p}] ⑥ SW19-b and SW21-a. Input Signal A to TPs2-in (Pin 19). ⑦ Set sub-address (02) 03H, and calculate V_{thS2} as well. 

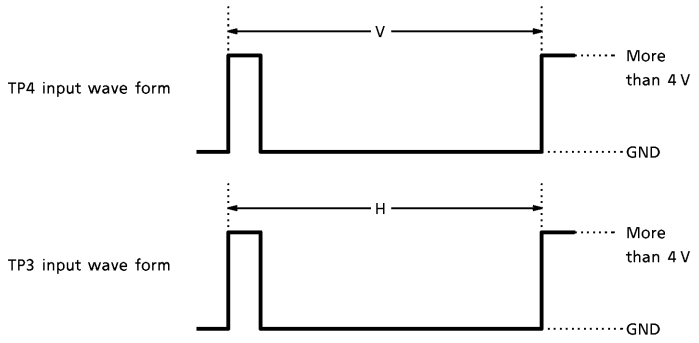
NOTE	ITEM	MEASURING METHOD
HA05	HD1 / 2 input threshold voltage	① Test condition 2. Set sub-address (00) 43H. ② Input Signal B to TP3 (Pin 3) and set sub-address (02) 00H. ③ Getting the amplitude of Signal B larger form $0V_{p\text{-}p}$, measure the amplitude of Signal B when the phase of Pin 15 (H-OUT) is same as the phase of Signal B. (V_{thHD1}) ④ Input Signal B to TP1 (Pin 1) and set sub-address (02) 01H. ⑤ Measure the amplitude as well. (V_{thHD2}) 
HA06	Horizontal phase adjustment variable range	① Test condition 2. Set sub-address (00) 40H. ② Input Signal B to TP3 (Pin 3) and set sub-address (02) 00H. ③ Change from 80H to 7FH of sub-address (01), then measure the phase change quantity of Pin 15 (H-OUT) wave form. (ΔH_{SFT-}) ④ Change from 80H to FFH of sub-address (01), then measure the phase change quantity of Pin 15 (H-OUT) wave form. (ΔH_{SFT+}) 

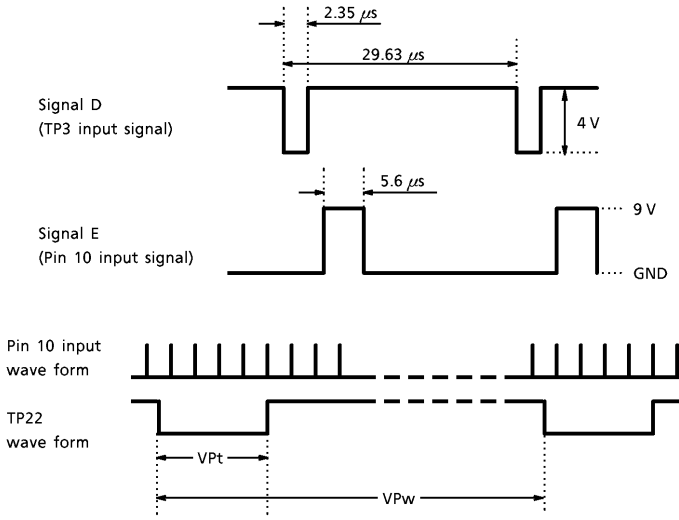
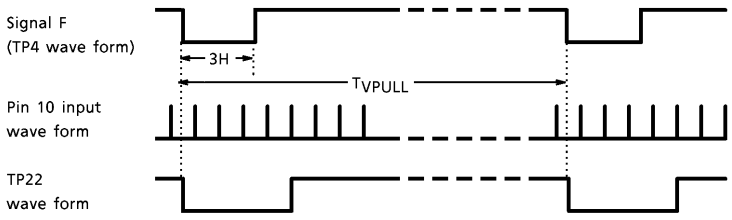
NOTE	ITEM	MEASURING METHOD
HA07	H curve correction variable range	① Test condition 2. Set sub-address (00) 40H. ② Input Signal B to TP3 (Pin 3) and set sub-address (02) 00H. ③ Connect Pin 9 (H-CURVE CORR) with external voltage. Supply 1.5 V or 3.5 V, and measure the phase change quantity of Pin 15 (H-OUT) wave form. (ΔH#9) 
HA08	Clamp pulse phase / width / level	① Test condition 2. Set sub-address (00) 40H. ② Input Signal B to TP3 (Pin 3) and set sub-address (02) 20H. ③ Measure the clamp pulse phase (CP_{S0}), width (CP_{W0}) and output level (CP_{V0}) of Pin 12 (SCP-OUT) against Signal B. ④ Set sub-address (02) 30H and measure (CP_{S1}), (CP_{W1}) and (CP_{V1}) as well. ⑤ Input no-signal to TP3. ⑥ Measure the clamp pulse phase (CP_{S2}), width (CP_{W2}) and output level (CP_{V2}) of Pin 12 (SCP-OUT) against Pin 10. 

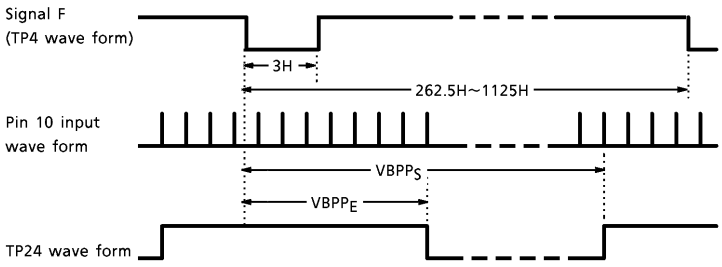
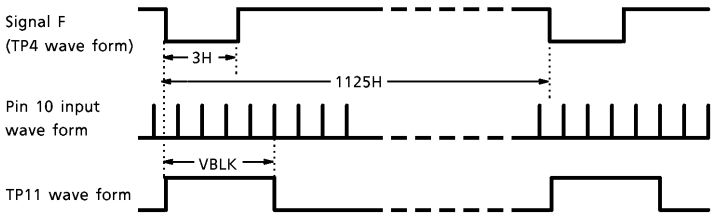
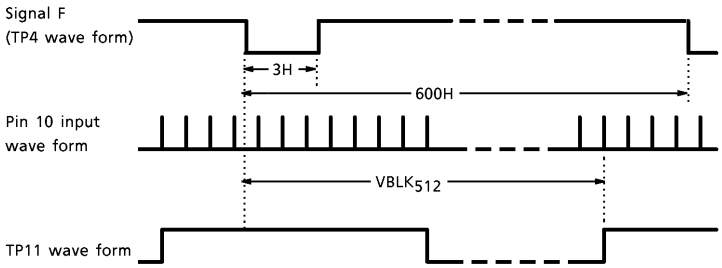
NOTE	ITEM	MEASURING METHOD
HA09	Black peak detection pulse phase / level	① Test condition 2. Set sub-address (00) 43H. ② Set sub-address (02) 00H. ③ Input Signal C to Pin 10 (FBP-IN). ④ Measure the black peak detection pulse phase of Pin 12 (SCP-OUT) against Signal C. Calculate the ratio against horizontal cycle. (HBP_{S0a}, HBP_{S0b}) ⑤ Measure its output level of Pin 12 (SCP-OUT) wave form. (HBP_{SV0}) ⑥ Set sub-address (02) 80H. ⑦ Measure the phase and output level as well. (HBP_{S1a}, HBP_{S1b}, HBP_{SV1}) 
HA10	Horizontal blanking pulse phase / width / level	① Test condition 2. Set sub-address (00) 43H. ② Set sub-address (02) 00H. ③ Input Signal C to Pin 10 (FBP-IN). ④ Measure the horizontal blanking pulse phase of Pin 11 (BLK-OUT) against Signal C. Calculate the ratio against horizontal cycle. ($HHLK_{S0a}$, $HBLK_{S0b}$) ⑤ Measure its output level of Pin 11 wave form. ($HBLK_{SV0}$) ⑥ Set sub-address (02) 80H. ⑦ Measure its phase and output level as well. ($HBLK_{S1a}$, $HVLK_{S1b}$, $HBLK_{SV1}$) 

NOTE	ITEM	MEASURING METHOD
HA11	FBP input threshold	① Test condition 2. Set sub-address (00) 40H. ② Input Signal B to TP3 (Pin 3) and set sub-address (02) 00H. ③ Increasing the amplitude of FBP of Pin 10 from 0 V_{p-p}, measure the amplitude of FBP when Signal B synchronizes with H-OUT (Pin 15). 
HA12	Delayed HD pulse width	① Test condition 2. Set sub-address (00) 40H. ② Input Signal B to TP3 (Pin 3) and set sub-address (02) 00H. ③ Measure the pulse width (Wd_{HD}) from Pin 6 (AFC filter) wave form. 
HB01	AFC phase detection current	① Test condition 3. ② Set sub-address (00) 00H. ③ Measure the voltage of TP6 (V6) when no external supply. ④ Connect an external supply with TP6, and supply the voltage (V6). ⑤ Input Signal D to TPs1-in (Pin 21) and set sub-address (02) 02H. Measure V1 and V2 from Pin 6 wave form. ⑥ Supply (V6) – 0.1 V or (V6) + 0.1 V to TP6, then measure V3 and V4. ⑦ Calculate detection currents (ID) by following equations. ID1 = V1 ÷ 1 [kΩ] × 1000 [μA] ID2 = V2 ÷ 1 [kΩ] × 1000 [μA] ID3 = V3 ÷ 1 [kΩ] × 1000 [μA] ID4 = V4 ÷ 1 [kΩ] × 1000 [μA] 

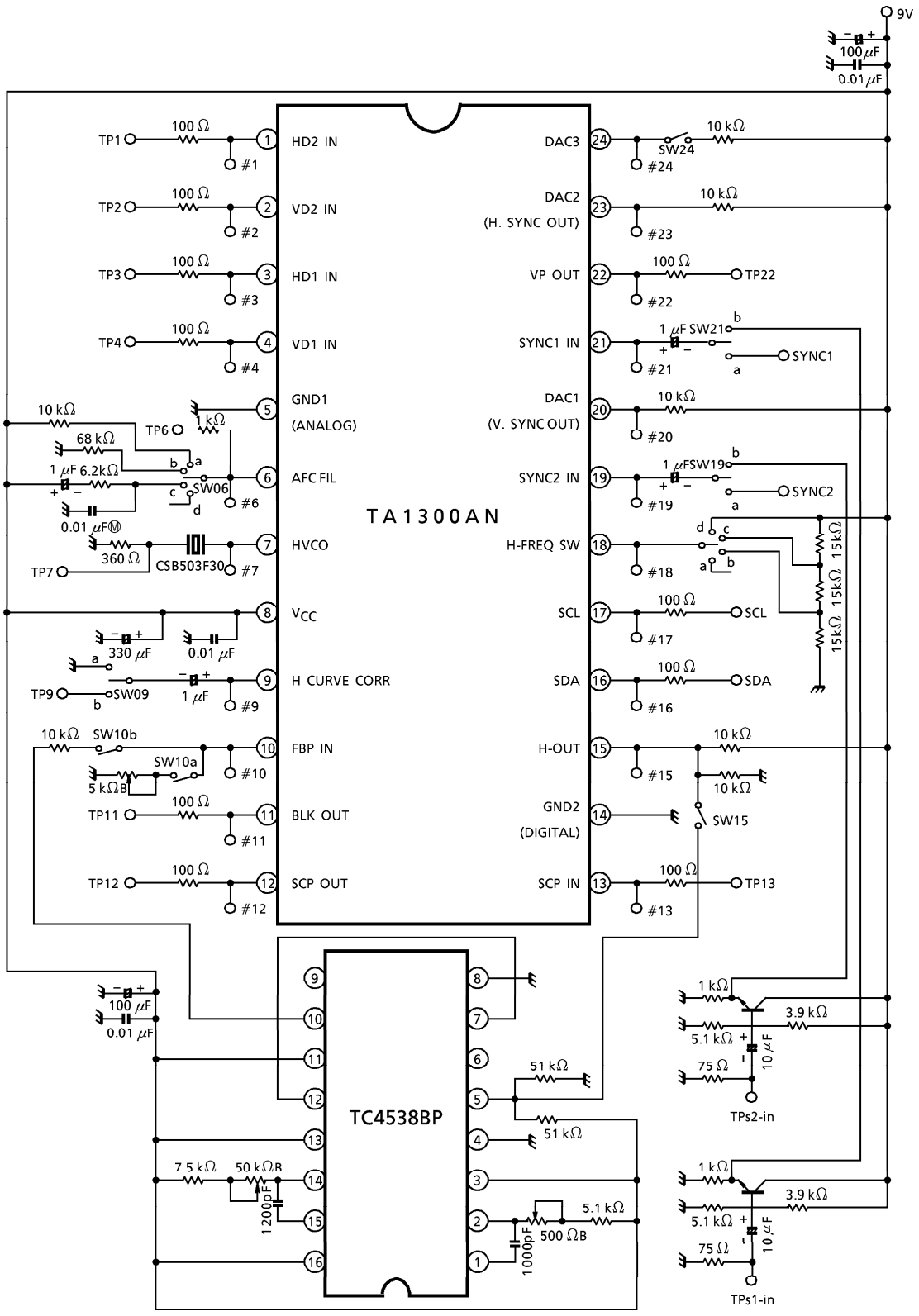
NOTE	ITEM	MEASURING METHOD
HB02	H-OUT pulse duty	① Test condition 2. Input no-signal. Set sub-address (02) 00H. ② Set sub-address (00) 80H or A0H, then measure T1 and T2 from Pin 15 (H-OUT) wave form. Calculate duties, (TH_{00A}) and (TH_{00B}) by following equation. $TH = T1 / (T1 + T2) \times 100$ [%] ③ Set sub-address (02) 01H or 02H, then measure and calculate (TH_{01A}), (TH_{01B}), (TH_{10A}) and (TH_{10B}) as well. 
HB03	Horizontal free-run frequency	① Test condition 3. ② Set sub-address (00) 00H. Measure the horizontal free-run frequency (F00) from Pin 15 (H-OUT) wave form. ③ When sub-address (00) is 01H or 02H, measure horizontal free-run frequencies, (F01) and (F10) as well. ④ Set sub-address (00) 00H and set sub-address (03) 85H. Measure horizontal free-run frequency (F50) as well.
HB04	Horizontal oscillation frequency variable range	① Test condition 4. Set sub-address (00) 00H. ② SW6-a. Measure the horizontal frequency ($F00_{MIN}$) from Pin 15 (H-OUT) wave form. ③ SW6-b. Measure the horizontal frequency ($F00_{MAX}$) from Pin 15 (H-OUT) wave form. ④ Set sub-address (00) 01H or 02H, then measure horizontal frequencies ($F01_{MIN}$), ($F01_{MAX}$), ($F10_{MIN}$) and ($F10_{MAX}$) as well. ⑤ Set sub-address (00) 00H and set sub-address (03) 85H. Measure horizontal frequencies, ($F50_{MAX}$) and ($F50_{MIN}$) as well.
HB05	Horizontal oscillation control sensitivity	① Test condition 3. ② Connect an external voltage with TP6. Set sub-address (00) 00H. Supply V6 + 0.05 [V] or V6 – 0.05 [V] to TP6 (cf. Note HB01), then measure frequencies, (FA) and (FB) from Pin 15 (H-OUT) wave form. Calculate frequency changing ratio (BH00). $BH00 = (FB - FA) / 0.1$ ③ Set sub-address (00) 01H or 02H. Measure and calculate (BH01) and (BH10) as well.
HB06	H-OUT output voltage	① Test condition 5. ② Measure voltages of the high ($V15_H$) and low level ($V15_L$) of Pin 15 (H-OUT) wave form.

NOTE	ITEM	MEASURING METHOD
HB07	Pin 18 control voltage threshold (Horizontal frequency SW)	① Test condition 2. Connect an external voltage to Pin 18. ② Increasing the voltage of Pin 18 from 0 V, measure the voltage of Pin 18 ($V18_L$) when the frequency of Pin 15 (H-OUT) output become 33.75 kHz. ③ Increasing the voltage of Pin 18 further, measure the voltage of Pin 18 ($V18_M$) when the frequency of Pin 15 (H-OUT) output become 31.5 kHz. ④ Increasing the voltage of Pin 18 further, measure the voltage of Pin 18 ($V18_H$) when the frequency of Pin 15 (H-OUT) output become 15.75 kHz.
HB08	H / V frequency distinction	① Test condition 2. Set sub-address (02) 04H. ② Input 50 Hz pulse to TP4 (Pin 4). Decimalize READ DATA, V-FREQ DET and the result is called Y. Calculate the vertical frequency (FV_{50}) by the following equation and Z = 474.1 μs FV = 1 ÷ (Y × Z) ③ Input 60 Hz, 16.5 Hz or 162 Hz pulse to TP4, then calculate (FV_{60}), (FV_{MIN}) or (FV_{MAX}) as well. ④ Input 60 Hz pulse to TP4 (Pin 4). ⑤ Input 15.75 kHz pulse to TP3 (Pin 3). Decimalize READ DATA, H-FREQ DET and the result is called Y. Calculate the horizontal frequency (FH_{15}) by the following equation and Z = 474.1 μs FH = Y ÷ (5 × Z) ⑥ Input 31.5 kHz, 33.75 kHz, 45 kHz, 420 Hz or 53 kHz pulse, then calculate (FH_{31}), (FH_{33}), (FH_{45}), (FH_{MIN}) or (FH_{MAX}) as well. ⑦ Set sub-address (02) 02H. Input Composite Sync signal (f_H = 15.75 kHz, fv = 60 Hz) to TPs1-in (Pin 21). Decimalize READ DATA, H / V-FREQ DET and calculate (FV_{SY}) and (FH_{SY}) as well. 

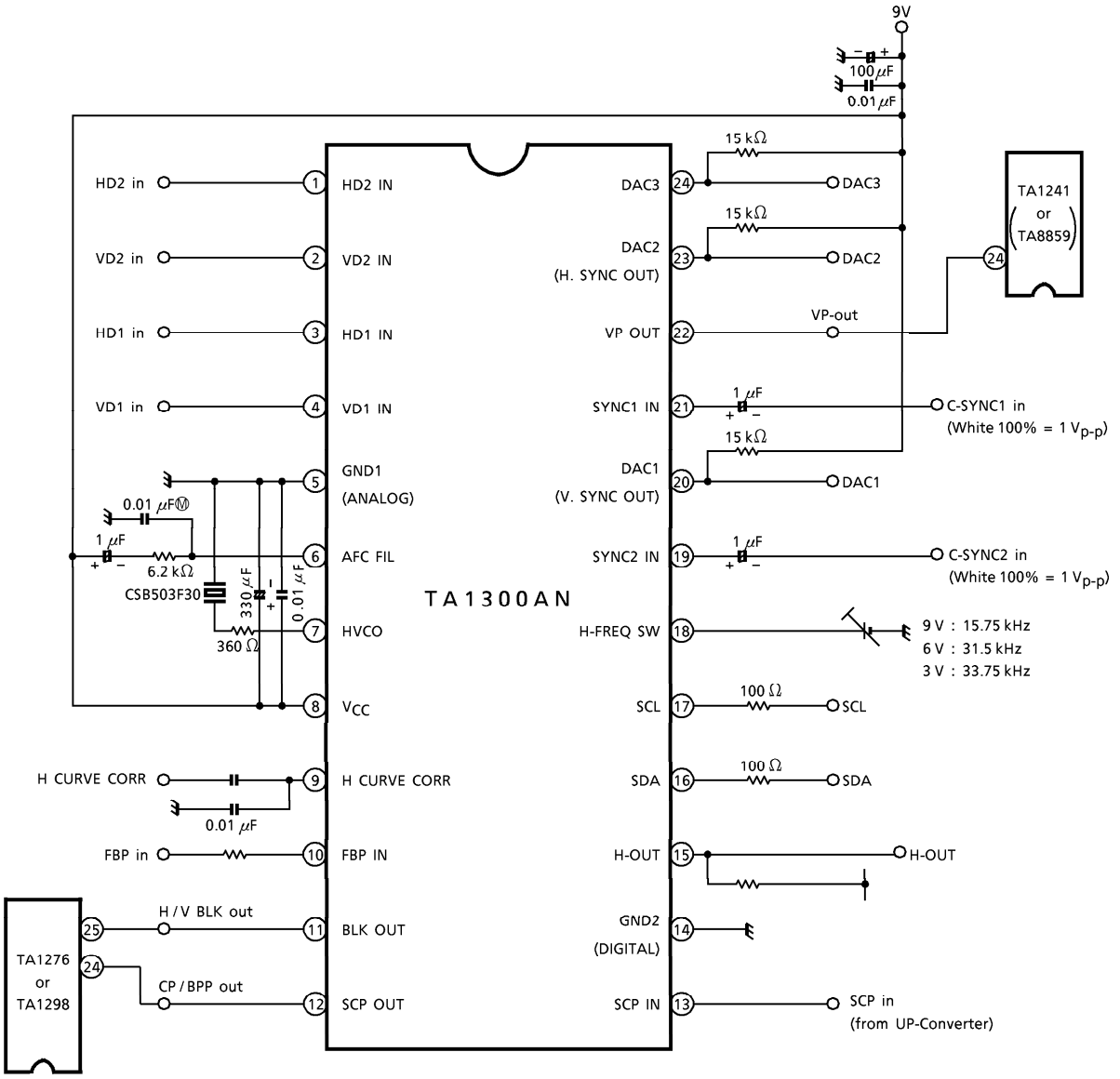
NOTE	ITEM	MEASURING METHOD
V01	VP output pulse width Vertical free-run (Maximum pull-in range)	① Test condition 2. Input Signal D to TP3 and input Signal E to pin 10 (FBP-IN). ② Set sub-address (00) 10H, (02) 00H and (03) 10H. ③ Measure the VP pulse width (VPw) from TP22 output wave form. ④ Measure its pull-in range (VPt0) from TP22 output wave form. ⑤ When sub-address (03) is 11H, 12H, 13H, 14H, 15H or 16H, measure pull-in ranges, (VPt1), (VPt2), (VPt3), (VPt4), (VPt5) or (VPt6) as well. 
V02	Vertical minimum pull-in range	① Set condition in the same way as ① and ② of Note V01. ② Input Signal F to TP4. ③ Increasing the period of Signal F from 30H, measure the period when TP22 wave synchronize with Signal F. (T_{VPULL}) 

NOTE	ITEM	MEASURING METHOD
V03	Vertical black peak detection pulse	① Set condition in the same way as ① and ② of Note V01. ② Input Signal F to TP4. ③ Measure the phase differences, ($VBPP_{0E}$) and ($VBPP_{0S}$) from TP22 and TP24 wave forms. ④ When sub-address (03) is 11H, 12H, 13H, 14H, 15H or 16H, measure phase differences, ($VBPP_{1E}$), ($VBPP_{1S}$), ($VBPP_{2E}$), ($VBPP_{2S}$), ($VBPP_{3E}$), ($VBPP_{3S}$), ($VBPP_{4E}$), ($VBPP_{4S}$), ($VBPP_{5E}$), ($VBPP_{5S}$), ($VBPP_{6E}$) or ($VBPP_{6S}$) as well. 
V04	Vertical blanking stop phase	① Set condition in the same way as ① and ② of Note V01. ② Input Signal F to TP4. ③ When sub-address (03) is 00H, 10H or F0H, measure blanking stop phases, ($VBLK_{00}$), ($VBLK_{10}$) and ($VBLK_{1E}$) from TP11 wave form. 
V05	Vertical blanking start phase	① Set condition in the same way as ① of Note V01. ② Set sub-address (00) 10H, (02) 00H and (03) 82H. ③ Measure the blanking start phase ($VBLK_{512}$) from TP11 wave form. 

TEST CIRCUIT

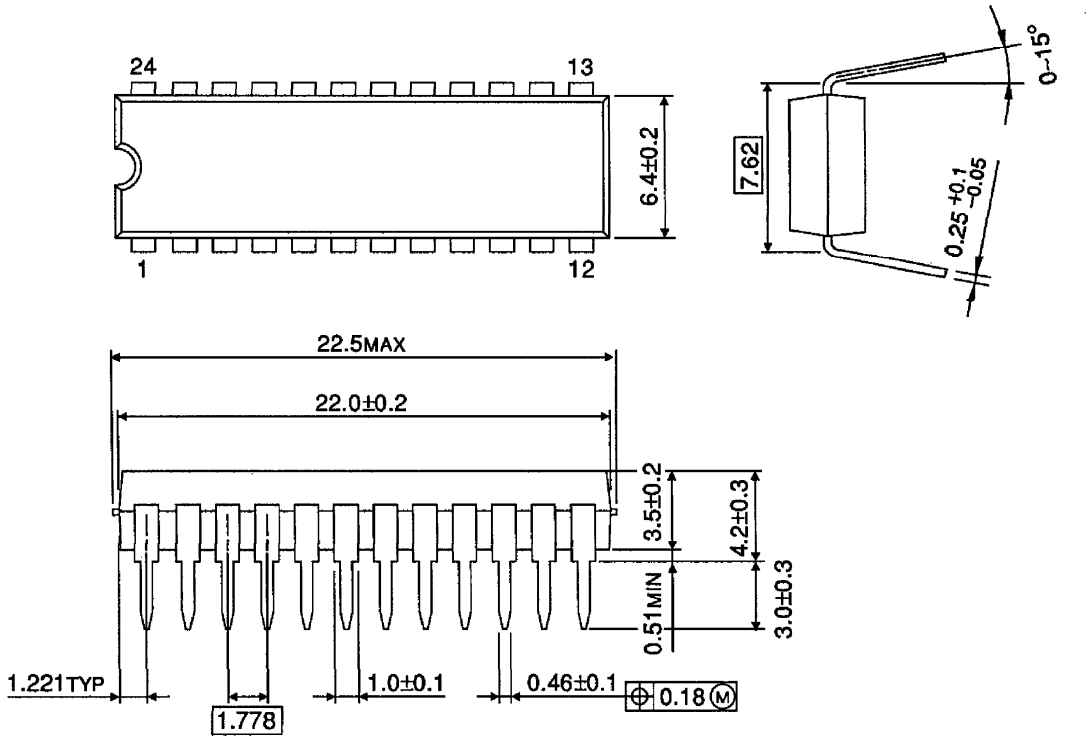


APPLICATION CIRCUIT



OUTLINE DRAWING

SDIP24-P-300-1.78 Unit : mm



Weight : 1.22 g (Typ.)