Agilent HDMP-0440
Quad Port Bypass Circuit for Fibre Channel Arbitrated Loops
Data Sheet

Description

The HDMP-0440 is a Quad Port Bypass Circuit (PBC), which provides a low-cost, low-power physical-layer solution for Fibre Channel Arbitrated Loop (FC-AL) disk array configurations. By using a PBC such as the HDMP-0440, hard disks may be pulled out or swapped while other disks in the array are available to the system.

A PBC consists of multiple 2:1 multiplexers daisy chained together. Each port has two modes of operation: “disk in loop” and “disk bypassed.” When the “disk in loop” mode is selected, the loop goes into and out of the disk drive at that port. For example, data goes from the HDMP-0440’s TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC’s (e.g. an HDMP-1636A) Rx differential input pins. Data from the Disk Drive Transceiver IC’s Tx differential outputs goes to the HDMP-0440’s FM_NODE[n]± differential input pins. Figure 2 shows connection diagrams for disk drive array applications. When the “disk bypassed” mode is selected, the disk drive is either absent or non-functional and the loop bypasses the hard disk.

The “disk bypassed” mode is enabled by pulling the BYPASS[n]- pin low. Leave BYPASS[n]- floating to enable the “disk in loop” mode. HDMP-0440s may be cascaded with other members of the HDMP-04XX/HDMP-05XX family through the appropriate FM_NODE[n]± and TO_NODE[n]± pins to accommodate any number of hard disks (see Figure 3). The unused cells in the HDMP-0440 may be bypassed by using pulldown resistors on the BYPASS[n]- pins for these cells.

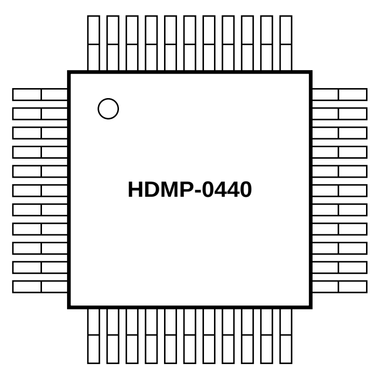
An HDMP-0440 may also be configured as five 1:1 buffers, as two 2:1 multiplexers or as two 1:2 buffers.

Features

- **Supports 1.0625 GBd Fibre Channel operation**
- **Supports 1.25 GBd Gigabit Ethernet (GE) operation**
- **Quad PBC in one package**
- **Equalizers on all inputs**
- **High-speed LVPECL I/O**
- **Buffered Line Logic (BLL) outputs (no external bias resistors required)**
- **0.5 W typical power at V_{CC} = 3.3 V**
- **44 Pin, 10 mm, low-cost plastic QFP package**

Applications

- **RAID, JBOD, BTS cabinets**
- **Two 2:1 muxes**
- **Two 1:2 buffers**
- **1 ≥ N Gigabit serial buffer**
- **N ≥ 1 Gigabit serial mux**



CAUTION: *As with all semiconductor ICs, it is advised that normal static precautionsb be taken in the handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).*

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HDMP-0440 Block Diagram

BLL OUTPUT

All TO_NODE[n]± high-speed differential outputs are driven by a Buffered Line Logic (BLL) circuit that has on-chip source termination, so no external bias resistors are required. The BLL Outputs on the HDMP-0440 are of equal strength and can drive lengthy FR-4 PCB trace.

Unused outputs should not be left unconnected. Ideally, unused outputs should have their differential pins shorted together with a short PCB trace. If longer traces or transmission lines are connected to the output pins, the lines should be differentially terminated with an appropriate resistor. The value of the termination resistor should match the PCB trace differential impedance.

EQU INPUT

All FM_NODE[n]± high-speed differential inputs have an Equalization (EQU) buffer to offset the effects of skin loss and dispersion on PCBs. An external termination resistor is required across all high-speed inputs. The value of the termination resistor should match the PCB trace differential impedance. Alternatively, instead of a single resistor, two resistors in series, with an AC ground between them, can be connected differentially across the FM_NODE[n]± inputs. The latter configuration attenuates high-frequency common mode noise.

BYPASS[n]- INPUT

The active low BYPASS[n]- inputs control the data flow through the HDMP-0440. All BYPASS pins are LVTTL and contain internal pull-up circuitry. To bypass a port, the appropriate BYPASS[n]- pin should be connected to GND through a 1 kΩ resistor. Otherwise, the BYPASS[n]- inputs should be left to float, as the internal pull-up circuitry will force them high.

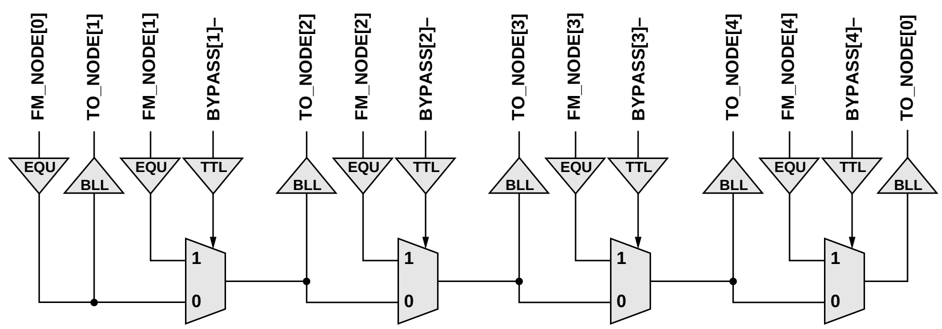


Figure 1. Block diagram of HDMP-0440.

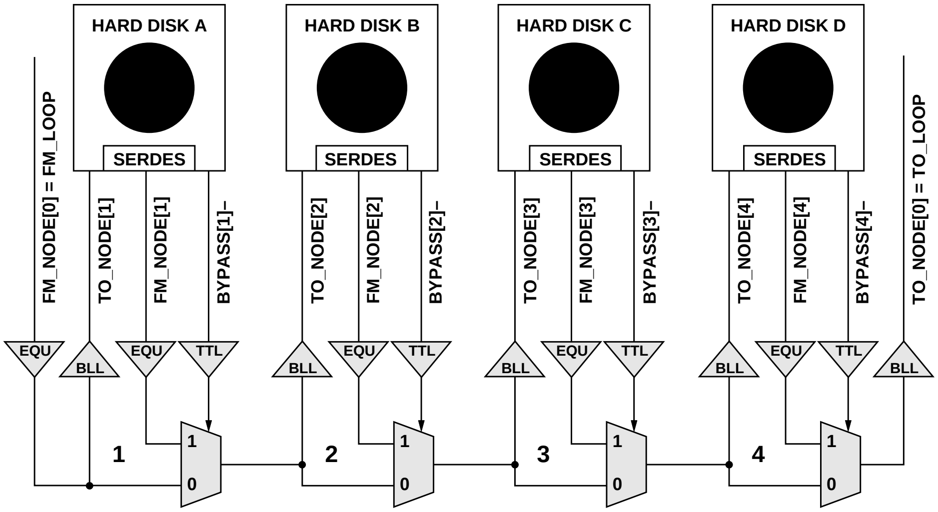


Figure 2. Connection diagram for disk array applications.

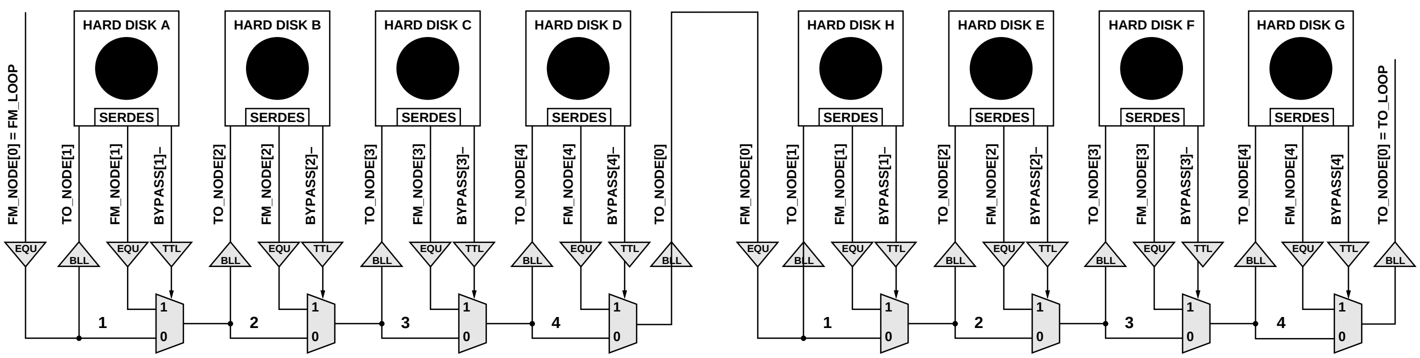


Figure 3. Connection diagram for multiple HDMP-0440s.

I/O Type Definitions

I/O Type	Definition
I-LVTTL	LVTTL Input
O-LVTTL	LVTTL Output
HS_OUT	High Speed Output, LVPECL compatible
HS_IN	High Speed Input
C	External Circuit Node
S	Power Supply or Ground

Pin Definitions

Pin Name	Pin	Pin Type	Pin Description
TO_NODE[0]+ TO_NODE[0]- TO_NODE[1]+ TO_NODE[1]- TO_NODE[2]+ TO_NODE[2]- TO_NODE[3]+ TO_NODE[3]- TO_NODE[4]+ TO_NODE[4]-	24 25 07 06 44 43 38 37 31 30	HS_OUT	**Serial Data Outputs:** High-speed outputs to a hard disk drive or to a cable.
FM_NODE[0]+ FM_NODE[0]- FM_NODE[1]+ FM_NODE[1]- FM_NODE[2]+ FM_NODE[2]- FM_NODE[3]+ FM_NODE[3]- FM_NODE[4]+ FM_NODE[4]-	10 09 04 03 41 40 35 34 28 27	HS_IN	**Serial Data Inputs:** High-speed inputs from a hard disk drive or from a cable.
BYPASS[0]- BYPASS[1]- BYPASS[2]- BYPASS[3]- BYPASS[4]-	14 15 16 17 18	I-LVTTL	**Bypass Inputs:** For "disk bypassed" mode, connect BYPASS[n]- to GND through a 1 kΩ resistor. For "disk in loop" mode, float HIGH.
GND	01 08 11 12 13 19 22 23 33 39	S	**Ground:** Normally 0 V. See Figure 9 for Recommended Power Supply Filtering.
V_{CC}HS[0] V_{CC}HS[1] V_{CC}HS[2] V_{CC}HS[3] V_{CC}HS[4]	26 05 42 36 29	S S S S S	**High Speed Supply:** Normally 3.3 V. Used only for high-speed outputs(TO_NODE[n]). See Figure 9 for Recommended Power Supply Filtering.
V_{CC}	02 14 20 21 32	S	**Logic Power Supply:** Normally 3.3 V. Used for internal logic. See Figure 9 for Recommended Power Supply Filtering.

Absolute Maximum Ratings

T_A = 25°C, except as specified. Operation in excess of any of these conditions may result in permanent damage to this device. Continuous operation at these minimum or maximum ratings is not recommended.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	–0.5	4.0
$V_{IN,LVTTL}$	LVTTL Input Voltage	V	–0.5	V_{CC} + 0.5[1]
V_{IN,HS_IN}	HS_IN Input Voltage (Differential)	mV	200	2000
$I_{O,LVTTL}$	LVTTL Output Sink/Source Current	mA		±13
T_{stg}	Storage Temperature	°C	–65	+150
T_j	Junction Temperature	°C	0	+125

Note:

1. Must remain less than or equal to absolute maximum V_{CC} voltage of 4.0 V.

DC Electrical Specifications

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V.

Symbol	Parameter	Units	Min.	Typ.	Max.
$V_{IH,LVTTL}$	LVTTL Input High Voltage Range	V	2.0		
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Range	V			0.8
$V_{OH,LVTTL}$	LVTTL Output High Voltage Range, I_{OH} = -400 µA	V	2.2		V_{CC}
$V_{OL,LVTTL}$	LVTTL Output Low Voltage Level, I_{OL} = 1 mA	V	0		0.6
$I_{IH,LVTTL}$	Input High Current (Magnitude), V_{IN} = 2.4 V, V_{CC} = 3.45 V	µA			40
$I_{IL,LVTTL}$	Input Low Current (Magnitude), V_{IN} = 0.4 V, V_{CC} = 3.45 V	µA			–600
I_{CC}	Total Supply Current, T_A = 25°C	mA		150	185

AC Electrical Specifications

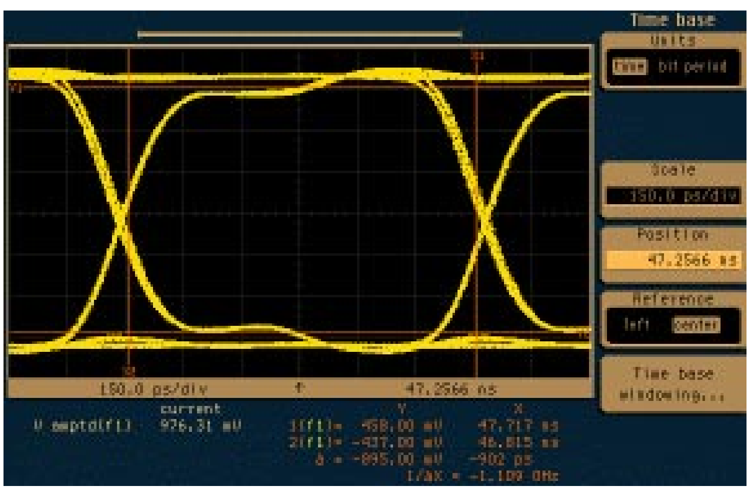
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V.

Symbol	Parameter	Units	Min.	Typ.	Max.
T_{LOOP_LAT}	Total Loop Latency from FM_NODE[0] to TO_NODE[0]	ns		2.0	
T_{CELL_LAT}	Per Cell Latency from FM_NODE[4] to TO_NODE[0]	ns		0.8	
$t_{r,LVTTLin}$	Input LVTTL Rise Time Requirement, 0.8 V to 2.0 V	ns		2.0	
$t_{f,LVTTLin}$	Input LVTTL Fall Time Requirement, 2.0 V to 0.8 V	ns		2.0	
$t_{r,LVTTLout}$	Output TTL Rise Time, 0.8 V to 2.0 V, 10 pF Load	ns		1.7	3.3
$t_{f,LVTTLout}$	Output TLL Fall Time, 2.0 V to 0.8 V, 10 pF Load	ns		1.7	2.4
t_{rs,HS_OUT}	HS_OUT Single-Ended Rise Time, 20% to 80%	ps		200	30
t_{fs,HS_OUT}	HS_OUT Single-Ended Fall Time, 20% to 80%	ps		200	300
t_{rd,HS_OUT}	HS_OUT Differential Rise Time, 20% to 80%	ps		200	300
t_{fd,HS_OUT}	HS_OUT Differential Fall Time, 20% to 80%	ps		200	30
V_{IP,HS_IN}	HS_IN Required Pk-Pk Differential Input Voltage	mV	200	1200	2000
V_{OP,HS_OUT}	HS_OUT Pk-Pk Differential Output Voltage (Z0 = 75 Ω, Figure 6)	mV	1100	1400	2000

Guaranteed Operating Rates

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V.

FC Serial Clock Rate (MBd)		GE Serial Clock Rate (MBd)	
Min.	**Max.**	**Min.**	**Max.**
1,040	1,080	1,240	1,260



Figue 4. Eye diagram of TO_NODE[1]± high speed differential output (50 Ω termination).
Note: Measurement taken with a 2^7-1 PRBS input to FM_NODE[1]±.

Simplified I/O Cells

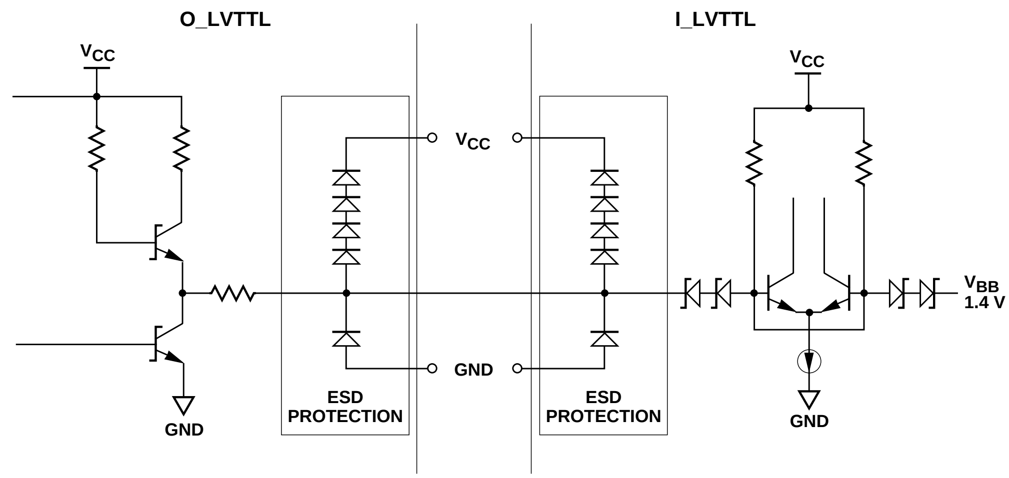


Figure 5. O-LVTTL and I-LVTTL simplified circuit schematic.

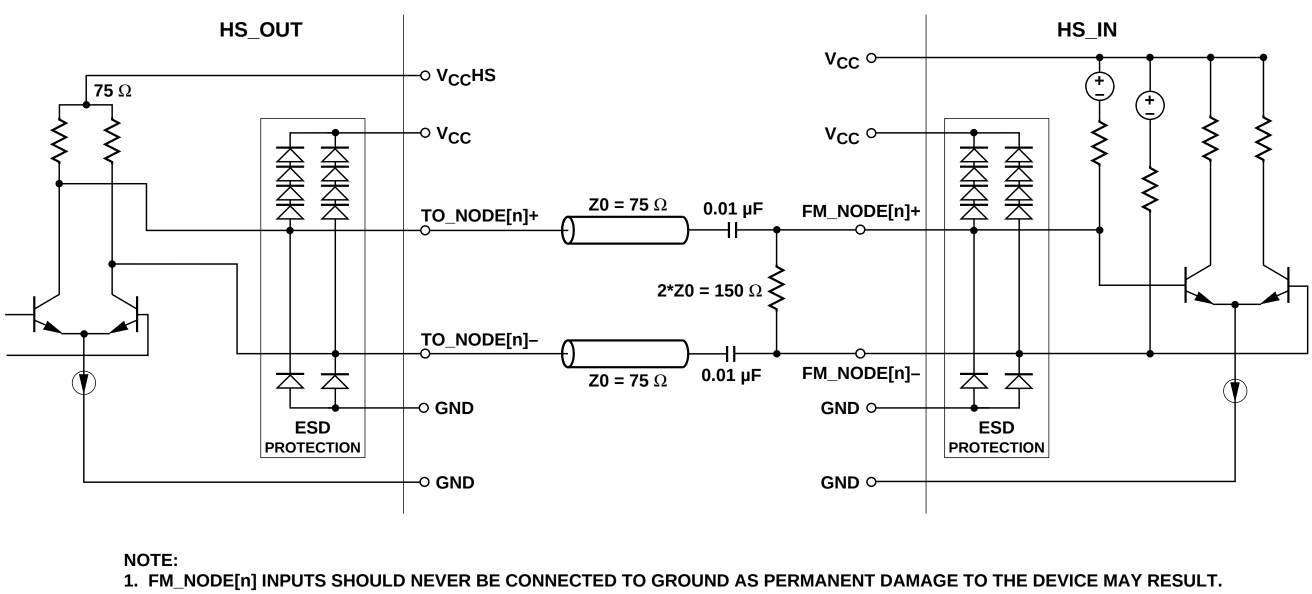


Figure 6. HS_OUT and HS_IN simplified circuit schematic.

Package Information

Power Dissipation and Thermal Resistance.

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V.

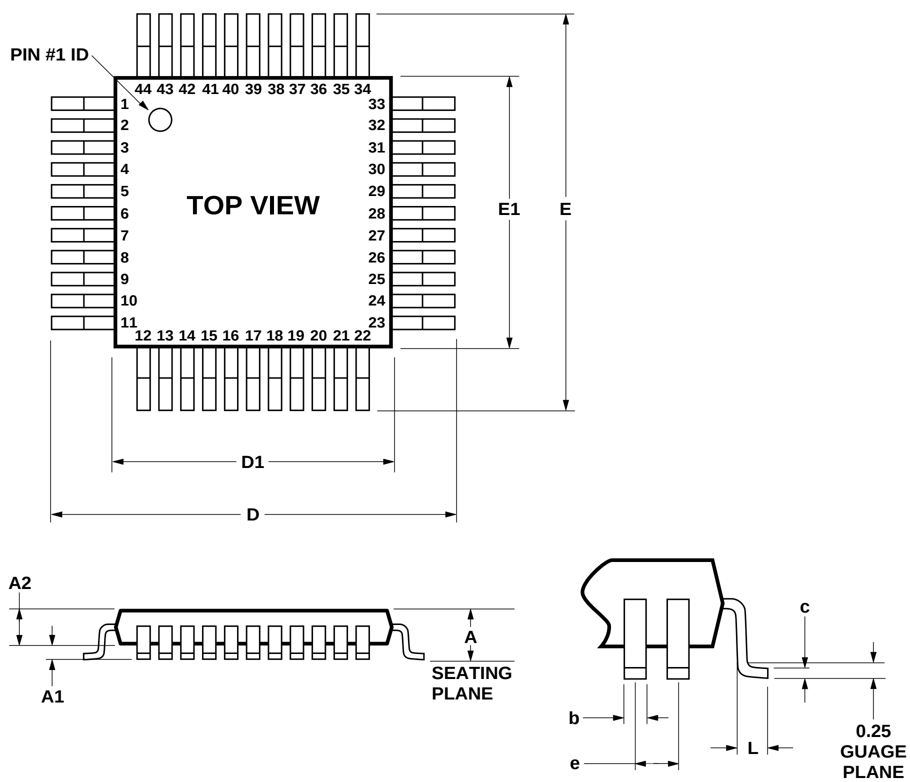
Symbol	Parameter	Units	Typ.	Max.
P_D	Power Dissipation	mW	500	640
Θ_{jc}[1]	Thermal Resistance, Junction to Case	°C/W	7	

Note:

1. Based on independent package testing by Agilent. Θ_{ja} for this device is 57ºC/W. Θ_{ja} is measured on a standard 3x3" FR4 PCB in a still air environment. To determine the actual junction temperature in a given application, use the following equation:
   $T_j = T_C + (\Theta_{ja} \times P_D)$, where T_C is the case temperature measured on the top center of the package and P_D is the power being dissipated.

Item	Details
Package Material	Plastic
Lead Finish Material	85% Tin, 15% Lead
Lead Finish Thickness	200-800 micro-inches
Lead Skew	0.33 mm max
Lead Coplanarity (Seating Plane)	0.10 mm max

Mechanical Dimensions

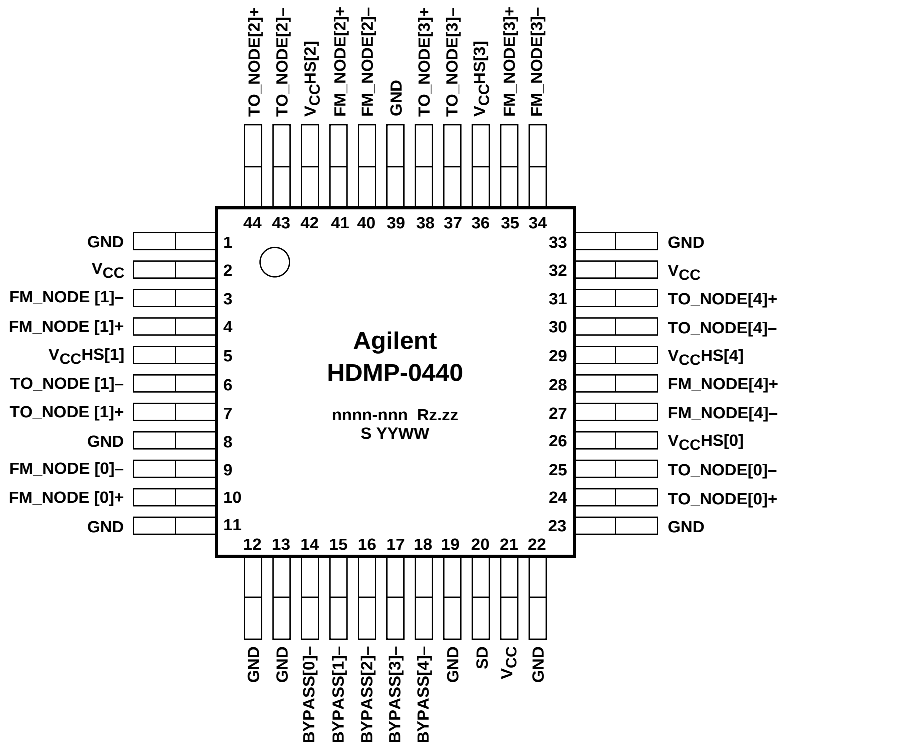


ALL DIMENSIONS ARE IN MILLIMETERS

PART NUMBER	E1/D1	E/D	b	e	L	c	A2	A1	A
HDMP-0440	10.00	13.20	0.35	0.80	0.88	0.23	2.00	0.25	2.45
TOLERANCE	± 0.10	± 0.20	± 0.05	BASIC	+ 0.15/ – 0.10	MAX.	+ 0.10/ – 0.05	± 0.25	MAX.

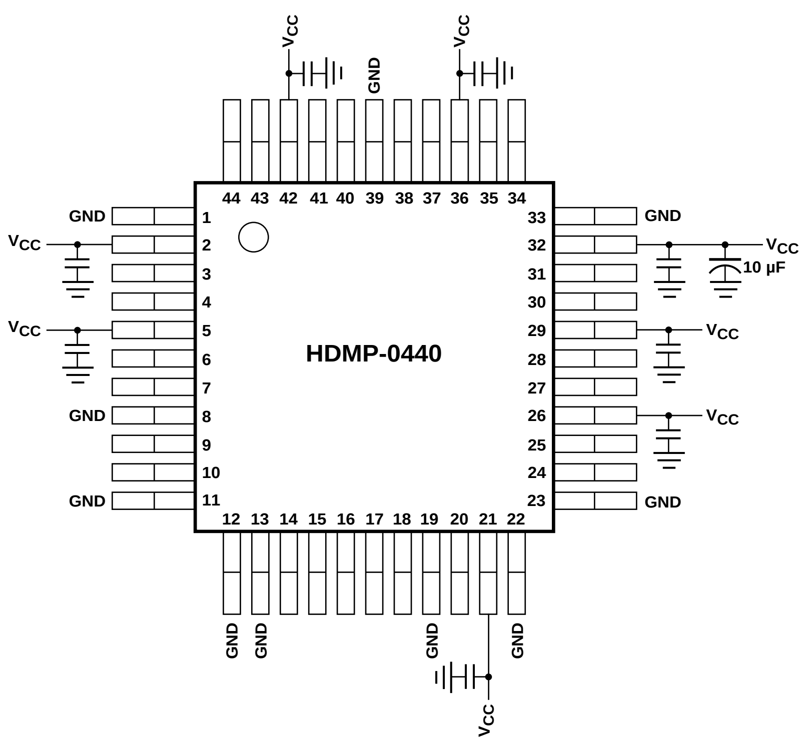
Figure 7. HDMP-0440 package drawing.

Pin Diagram and Recommended Supply Filtering



nnnn-nnn = WAFER LOT – BUILD NUMBER; *Rz.zz* = DIE REVISION; *S* = SUPPLIER CODE
YYWW = DATE CODE (*YY* = YEAR, *WW* = WORK WEEK); *COUNTRY* = COUNTRY OF MANUFACTURE (ON BACK SIDE)

Figure 8. HDMP-0440 package layout and marking, top view.



CAPACITORS = 0.1 µF (EXCEPT WHERE NOTED).

Figure 9. Recommended power supply filtering.

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Data subject to change.

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