National Semiconductor

PRELIMINARY
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DP83256/56-AP/57
PLAYER+™ Device (FDDI Physical Layer Controller)

General Description

The DP83256/56-AP/57 Enhanced Physical Layer Controller (PLAYER+ device) implements one complete Physical Layer (PHY) entity as defined by the Fiber Distributed Data Interface (FDDI) ANSI X3T9.5 standard.

The PLAYER+ device integrates state of the art digital clock recovery and improved clock generation functions to enhance performance, eliminate external components and remove critical layout requirements.

FDDI Station Management (SMT) is aided by Link Error Monitoring support, Noise Event Timer (TNE) support, Optional Auto Scrubbing support, an integrated configuration switch and built-in functionality designed to remove all stringent response time requirements such as PC__React and CF__React.

Features

- Single chip FDDI Physical Layer (PHY) solution
- Integrated Digital Clock Recovery Module provides enhanced tracking and greater lock acquisition range
- Integrated Clock Generation Module provides all necessary clock signals for an FDDI system from an external 12.5 MHz reference
- Alternate PMD Interface (DP83256-AP/57) supports UTP twisted pair FDDI PMDs with no external clock recovery or clock generation functions required
- No External Filter Components
- Connection Management (CMT) Support (LEM, TNE, PC__React, CF__React, Auto Scrubbing)
- Full on-chip configuration switch
- Low Power CMOS-BIPOLAR design using a single 5V supply
- Full duplex operation with through parity
- Separate management interface (Control Bus)
- Selectable Parity on PHY-MAC Interface and Control Bus Interface
- Two levels of on-chip loopback
- 4B/5B encoder/decoder
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Supports single attach stations, dual attach stations and concentrators with no external logic
- DP83256 for SAS/DAS single path stations
- DP83257 for SAS/DAS single/dual path stations
- DP83256-AP for SAS/DAS single path stations that require the alternate PMD interface

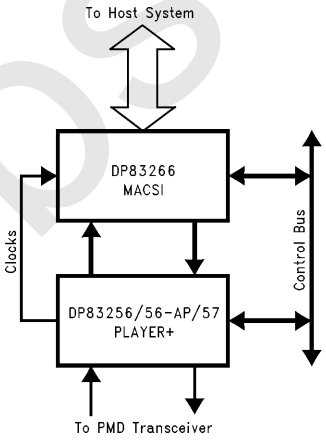

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FIGURE 1-1. FDDI Chip Set Overview

RRD-B30M115/Printed in U. S. A.

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1.0 FDDI Chip Set Overview

National Semiconductor's next generation FDDI 2-chip set consists of two components as shown in *Figure 1-1*. The PLAYER+ device integrates the features of the DP83231 CRD™ Clock Recovery Device, DP83241 CDD™ Clock Distribution Device, and DP83251/55 PLAYER™ Physical Layer Controller. In addition, the PLAYER+ device contains enhanced SMT support.

National Semiconductor's FDDI TP-PMD Solutions consist of two components—the DP83222 CYCLONE™ Twisted Pair FDDI Stream Cipher Device and the DP83223A TWISTER™ Twisted Pair FDDI Transceiver Device.

For more information on the other devices of the chip set, consult the appropriate datasheets and application notes.

1.1 FDDI 2-CHIP SET

DP83256/56-AP/57 PLAYER+ Device Physical Layer Controller

The PLAYER+ device implements the Physical Layer (PHY) protocol as defined by the ANSI FDDI PHY X3T9.5 standard.

Features

- Single chip FDDI Physical Layer (PHY) solution
- Integrated Digital Clock Recovery Module provides enhanced tracking and greater lock acquisition range
- Integrated Clock Generation Module provides all necessary clock signals for an FDDI system from an external 12.5 MHz reference
- Alternate PMD Interface (DP83256-AP/57) supports UTP twisted pair FDDI PMDs with no external clock recovery or clock generation functions required
- No External Filter Components
- Connection Management (CMT) Support (LEM, TNE, PC__React, CF__React, Auto Scrubbing)
- Full on-chip configuration switch
- Low Power CMOS-BIPOLAR design using a single 5V supply
- Full duplex operation with through parity
- Separate management interface (Control Bus)
- Selectable Parity on PHY-MAC Interface and Control Bus Interface
- Two levels of on-chip loopback
- 4B/5B encoder/decoder
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Supports single attach stations, dual attach stations and concentrators with no external logic
- DP83256/56-AP for SAS/DAS single path stations
- P83257 for SAS/DAS single/dual path stations

In addition, the DP83257 contains the additional PHY__Data.request and PHY__Data.indicate ports required for concentrators and dual attach, dual path stations.

DP83266 MACSI™ Device Media Access Controller and System Interface

The DP83266 Media Access Controller and System Interface (MACSI) implements the ANSI X3T9.5 Standard Media Access Control (MAC) protocol for operation in an FDDI token ring and provides a comprehensive System Interface.

The MACSI device transmits, receives, repeats, and strips tokens and frames. It produces and consumes optimized data structures for efficient data transfer. Full duplex architecture with through parity allows diagnostic transmission and self testing for error isolation in point-to-point connections.

The MACSI device includes the functionality of both the DP83261 BMAC device and the DP83265 BSI-2 device with additional enhancements for higher performance and reliability.

Features

- Over 9 Kbytes of on-chip FIFO
- 5 DMA Channels (2 Output and 3 Input)
- 12.5 MHz to 33 MHz operation
- Full duplex operation with through parity
- Real-time VOID frame stripping indicator for bridges
- On-chip Address bit swapping capability
- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Receive frame filtering services
- Frame-per-Page mode controllable on each DMA channel
- Demultiplexed Addresses supported on ABus
- New multicast address matching
- ANSI X3T9.5 MAC standard defined ring service options
- Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long, and External Addressing.
- Generates Beacon, Claim, and Void frames
- Extensive ring and station statistics gathering
- Extension for MAC level bridging
- Enhanced SBus compatibility
- Interfaces to DRAMs or directly to system bus
- Supports frame Header/Info splitting
- Programmable Big or Little Endian alignment

DP83222 CYCLONE Twisted Pair FDDI Stream Cipher Device

General Description

The DP83222 CYCLONE Stream Cipher Scrambler/Descrambler Device is an integrated circuit designed to interface directly with the serial bit streams of a Twisted Pair FDDI PMD. The DP83222 is designed to be fully compatible with the National Semiconductor FDDI Chip Sets, including twisted pair FDDI Transceivers, such as the DP83223A Twisted Pair Transceiver (TWISTER). The DP83222 requires a 125 MHz Transmit Clock and corresponding Receive Clock for synchronous data scrambling and descrambling. The DP83222 is compliant with the ANSI X3T9.5 TP-PMD standard and is required for the reduction of EMI emission over unshielded media. The DP83222 is specified to work in conjunction with existing twisted pair transceiver signalling schemes and enables high bandwidth transmission over Twisted Pair copper media.

Features

- Enables 100 Mbps FDDI signalling over Category 5 Unshielded Twisted Pair (UTP) cable and Type 1 Shielded Twisted Pair (STP)
- Reduces EMI emissions over Twisted Pair media
- Compatible with ANSI X3T9.5 TP-PMD standard
- Requires a single +5V supply
- Transparent mode of operation
- Flexible NRZ and NRZI format options
- Advanced BiCMOS process
- Signal Detect and Clock Detect inputs provided for enhanced functionality
- Suitable for Fiber Optic PMD replacement applications

DP83223A TWISTER High Speed Networking Transceiver Device

General Description

The DP83223A Twisted Pair Transceiver is an integrated circuit capable of driving and receiving either binary or (MLT-3) encoded datastreams. The DP83223A Transceiver is designed to interface directly with standards compliant FDDI, 100BASE-TX or STS-3c ATM chip sets, allowing low cost data links over copper based media. The DP83223A allows links of up to 100 meters over both Shielded Twisted Pair (STP) and datagrade Unshielded Twisted Pair (UTP) or equivalent. The electrical performance of the DP83223A meets or exceeds all performance parameters specified in the ANSI X3T9.5 TP-PMD standard, the IEEE 802.3 100BASE-TX Fast Ethernet Specification and the ATM Forum 155 Mbps Twisted Pair PMD Interface Specification. The DP83223A also provides important features such as baseline restoration, TRI-STATE® capable transmit outputs, and controlled transmit output edge rates (to reduce EMI radiation) for both binary and MLT-3 modes of operation.

Features

- Compliant with ANSI X3T9.5 TP-PMD standard
- Compliant with IEEE 802.3 100BASE-TX Ethernet draft standard
- Compliant with ATM Forum 155 Mbps Twisted Pair Specification
- Integrated baseline restoration circuit
- Integrated transmitter and receiver with adaptive equalization circuit
- Programmable binary or MLT-3 operation
- Isolated TX and RX power supplies for minimum noise coupling
- Controlled transmit output edge rates for reduced EMI
- TRI-STATE capable current transmit outputs
- Loopback feature for board diagnostics
- Programmable transmit voltage amplitude

2.0 Architecture Description

2.1 BLOCK OVERVIEW

The PLAYER+ device is comprised of six blocks: Clock Recovery, Receiver, Configuration Switch, Transmitter, Station Management (SMT) Support, and Clock Generation Module as shown in *Figure 2-1*.

Clock Recovery

The Clock Recovery Module accepts a 125 Mbps NRZI data stream from the external PMD receiver. It then provides the extracted and synchronized data and clock to the Receiver block.

The Clock Recovery Module performs the following operations:

- Locks to and tracks the incoming NRZI data stream
- Extracts data stream and synchronized 125 MHz clock

Receiver

During normal operation, the Receiver Block accepts serial data as inputs at the rate of 125 Mbps from the Clock Recovery Module. During the Internal Loopback mode of operation, the Receiver Block accepts data directly from the Transmitter Block.

The Receiver Block performs the following operations:

- Optionally converts the incoming data stream from NRZI to NRZ.
- Decodes the data from 5B to 4B coding.
- Converts the serial bit stream into 10-bit bytes composed of 8 bits data, 1 bit parity, and 1 bit control information.
- Compensates for the differences between the upstream station clock and the local clocks.
- Decodes Line States.
- Detects link errors.
- Presents data symbol pairs (bytes) to the Configuration Switch Block.

Configuration Switch

An FDDI station may be in one of three configurations: Isolate, Wrap or Thru. The Configuration Switch supports these configurations by switching the transmitted and received data paths between PLAYER+ devices and one or more MACSI devices.

The configuration switch is integrated into the PLAYER+ device, therefore no external logic is required for this function.

Setting the Configuration switch can be done explicitly via the Control Bus Interface or it can be set automatically with the CF_React SMT Support feature.

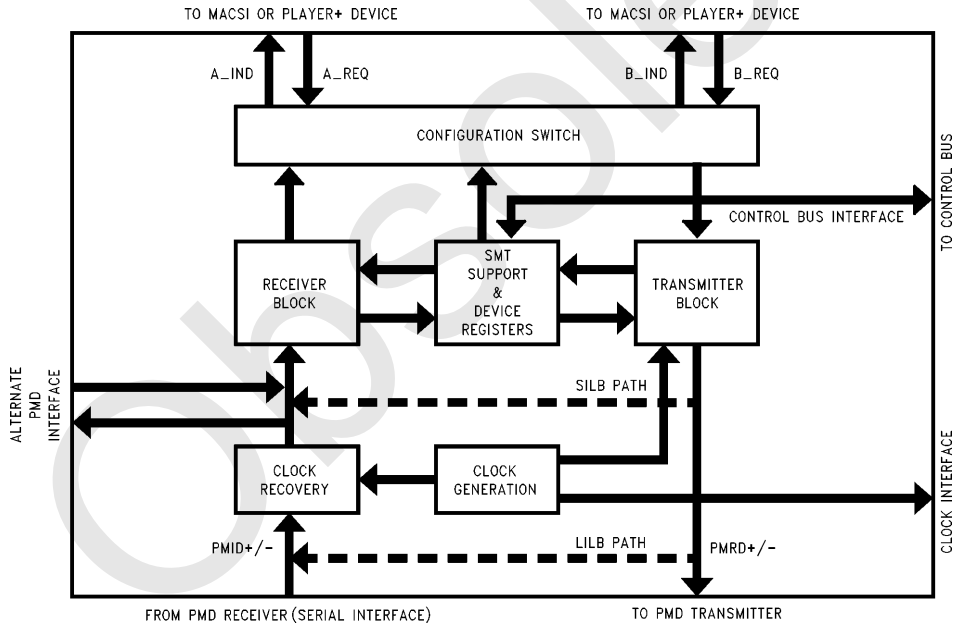

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FIGURE 2-1. PLAYER+ Device Block Diagram

2.0 Architecture Description (Continued)

Transmitter

The Transmitter Block accepts 10-bit bytes composed of 8 bits data, 1 bit parity, and 1 bit control information from the Configuration Switch.

The Transmitter Block performs the following operations:

- Encodes the data from 4B to 5B coding.
- Filters out code violations from the data stream.
- Generates Idle, Master, Halt, Quiet, or other user defined symbol pairs upon request.
- Converts the data stream from NRZ to NRZI format for transmission.
- Provides smoothing function when necessary.

During normal operation, the Transmitter Block presents serial data to the PMD transmitter. While in Internal Loopback mode, the Transmitter Block presents serial data to the Receiver Block. While in the External Loopback mode, the Transmitter Block presents serial data to the Clock Recovery Module.

Clock Generation Module

The Clock Generation Module is an integrated phase locked loop that generates all of the required clock signals for the PLAYER+ device and an FDDI system from a single 12.5 MHz reference.

The Clock Generation Module features:

- High precision clock timing generated from a single 12.5 MHz reference.
- Multiple precision phased (8 ns/16 ns) 12.5 MHz Local Byte Clocks to eliminate timing skew in large multi-board concentrator configurations.
- LBC timing which is insensitive to loading variations over a wide range (20 pF to 70 pF) of LBC loads.
- A selectable dual frequency system clock.
- Low clock edge jitter, due to high VCO stability.

Station Management (SMT) Support

The Station Management Support Block provides a number of useful features to simplify the implementation of the Connection Management (CMT) portion of SMT.

These features eliminate the time critical CMT response time constraints imposed by PC__React and CF__React times.

Integrated counters and timers eliminate the need for additional external devices.

The following are the CMT features supported:

- PC__React
- CF__React
- Auto Scrubbing (TCF Timer)
- Timer, Idle Detection (TID Timer)
- Noise Event Counter (TNE Timer)
- Link Error Monitor (LEM Counter)

2.2 INTERFACES

The PLAYER+ device connects to other devices via five functional interfaces: PMD Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and the Miscellaneous Interface.

PMD Interface

The PMD Interface connects the PLAYER+ device to a standard FDDI Physical Media Connection such as a fiber optic transceiver or a copper twisted pair transceiver. It is a 125 MHz full duplex serial connection.

The DP83256-AP and DP83257 PLAYER+ devices contain two PMD interfaces. The Primary PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMD. The second, Alternate PMD Interface can be used to support Unshielded Twisted Pair (UTP) PMDs that require external scrambling, and allows implementation with no external clock recovery or clock generation functions required.

PHY Port Interface

The PHY Port Interface connects the PLAYER+ device to one or more MAC devices and/or PLAYER+ devices. Each PHY Port Interface consists of two byte-wide interfaces, one for PHY Request data input to the PLAYER+ device and one for the PHY Indicate data output of the PLAYER+ device. Each byte-wide interface consists of a parity bit (odd parity), a control bit, and two 4-bit symbols.

The DP83257 PLAYER+ device has two PHY Port Interfaces while the DP83256 has one PHY Port Interface.

Control Bus Interface

The Control Bus Interface connects the PLAYER+ device to a wide variety of microprocessors and microcontrollers. The Control Bus is an asynchronous interface which provides access to 64 8-bit registers which monitor and control the behavior of the PLAYER+ device.

The Control Bus Interface allows a user to:

- Configure SMT features.
- Program the Configuration Switch.
- Enable/disable functions within the Transmitter and Receiver Blocks (i.e., NRZ/NRZI Encoder, Smoother, PHY Request Data Parity, Line State Generation, Symbol pair Injection, NRZ/NRZI Decoder, Cascade Mode, etc.).

The Control Bus Interface also can be used to perform the following functions:

- Monitor Line States received.
- Monitor link errors detected by the Receiver Block.
- Monitor other error conditions.

Clock Interface

The Clock Interface is used to configure the Clock Generation Module and to provide the required clock signals for an FDDI system.

The following clock signals are generated:

- 5 phase offset 12.5 MHz Local Byte Clocks
- 25 MHz Local Symbol Clock
- 15.625 or 31.25 MHz System Clock

Miscellaneous Interface

The Miscellaneous Interface consists of:

- A reset signal.
- User definable sense signals.
- User definable enable signals.
- Synchronization for cascading PLAYER+ devices (a high-performance non-FDDI mode).
- Device Power and Ground pins.

3.0 Functional Description

The PLAYER+ device is comprised of six blocks: Clock Recovery, Receiver, Transmitter, Configuration Switch, Clock Generation, and Station Management Support.

3.1 CLOCK RECOVERY MODULE

The Clock Recovery Module accepts a 125 Mbps NRZI data stream from the external PMD receiver. It then provides the extracted and synchronized data and clock to the Receiver block.

The Clock Recovery Module performs the following operations:

- Locks onto and tracks the incoming NRZI data stream
- Extracts the data stream and the synchronized 125 MHz clock

The Clock Recovery Module is implemented using an advanced digital architecture that replaces sensitive analog blocks with digital circuitry. This allows the PLAYER+ device to be manufactured to tighter tolerances since it is less sensitive to processing variations that can adversely affect analog circuits.

The Clock Recovery Module is comprised of 5 main functional blocks:

Digital Phase Detector

Digital Phase Error Processor

Digital Loop Filter

Digital Phase to Frequency Converter

Frequency Controlled Oscillator

See *Figure 3-1*, Clock Recovery Module Block Diagram.

DIGITAL PHASE DETECTOR

The Digital Phase Detector has two main functions: phase error detection and data recovery.

Phase error detection is accomplished by a digital circuit that compares the input data (PMID) to an internal phase-locked 125 MHz reference clock and generates a pair of error signals. The first signal is a pulse whose width is equal to the phase error between the input data and a reference clock and the second signal is a 4 ns reference pulse. These signals are fed into the Digital Phase Error Processor block.

The data recovery function converts the incoming encoded data stream (PMID) into synchronized data and clock signals. When the circuit is in lock the rising edge of the recovered clock is exactly centered in the recovered data bit cell.

The digital phase detector uses a common path for phase error detection and data recovery so as to minimize clock Static Alignment Error (SAE). Phase error averaging is also included so that phase errors generated by positive and negative PMID edges equally affect the clock recovery circuit. This greatly improves the immunity to Duty Cycle Distortion (DCD) in the data recovery circuit.

DIGITAL PHASE ERROR PROCESSOR

The Digital Phase Error Processor is responsible for sampling the Phase Detector's phase error outputs and producing two digital outputs that indicate to the digital loop filter how to adjust for a difference between the data phase and reference phases.

The Phase Error Processor is designed to eliminate the effects of different clock edge densities between data symbols and the various line state symbols on the PLL's loop gain.

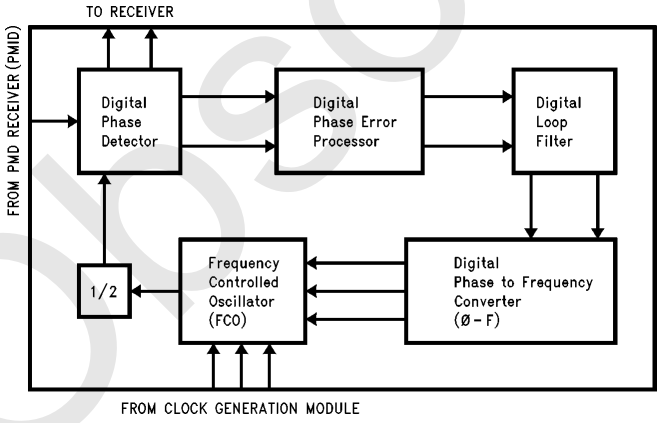

FIGURE 3-1. Clock Recovery Module Block Diagram

3.0 Functional Description (Continued)

Since the loop gain is held constant regardless of the incoming signal edge density, PLL characteristics such as jitter, acquisition rate, locking range etc., are deterministic and show minimal spread under various operating environments.

The phase error processor also automatically puts the loop in open-loop-mode when the incoming data stream contains abnormal low edge rates. When the PLL is in open-loop-mode, no update is made to the PLL's filter variables in the filter block. The PLL can then use the pretrained frequency and phase contents to perform data recovery. Since the loop is implemented digitally, these values (the frequency and phase variables) are retained. The resolution of the frequency variable is about 1.3 ppm of the incoming frequency. The resolution of the phase variable is about 40 ps.

DIGITAL LOOP FILTER

The digital loop filter emulates a 1-pole, 1-zero filter and uses an automatic acquisition speed control circuit to dynamically adjust loop parameters.

The digital loop filter takes the phase error indicator signals Data Valid and Up/Down from the Phase Error processor and accumulates errors over a few cycles before passing on the Data Valid and Up/Down signals to the Phase Error to Frequency converter.

The filter has 4 sets of bandwidth and damping parameters which are switched dynamically by an acquisition control circuit. The input Signal Detect (SD) starts the sequence and, thereafter, no user programming is required to finish the sequence.

At the completion of the locking sequence, the loop has the narrowest bandwidth such that the loop produces minimal recovered clock jitter. The PLL can track an incoming frequency offset of approximately $\pm$200 ppm. After the acquisition sequence, the equivalent natural frequency of the loop is reduced to about 7 kHz ($\pm$56 ppm) of frequency offset.

The automatic tracking mechanism allows the loop to quickly lock onto the initial data stream for data recovery (typically less than 10 μs) and yet produce very little recovered clock jitter.

PHASE ERROR TO FREQUENCY CONVERTER (∅–F)

The Phase Error to Frequency Converter takes the Data Valid and Up/Down signals modified by the Digital Loop Filter and converts them to triangle waves. The frequency of the triangle waves is then used to control the Frequency Controlled Oscillator's (FCO) 250 MHz oscillations.

Each valid Up or Down signal causes a partial 7-bit counter (using only 96 counts) to increment or decrement at the ∅–F converter's clock rate of 15.625 MHz (250 MHz/16). When the Data Valid signal is not asserted, the counter holds count.

The counter value is used to produce 3 triangle waves that are offset in phase by 120 degrees. This is done with a special Pulse Density Modulator waveform synthesizer which takes the place of a traditional Digital-Analog converter. The frequency of the triangle waves tells the Frequency Controlled Oscillator how much to adjust oscillation. The phase relationships (leading or lagging) between the 3 signals indicates the direction of change.

The minimum frequency of the triangle waves is 0 and corresponds to the case when the PLL is in perfect lock with the incoming signal.

The maximum frequency that the ∅–F converter can produce determines the locking range of the PLL. In this case the maximum frequency of each triangle wave is 162.76 kHz, which is produced when the ∅–F converter gets a continuous count in one direction that is valid every ∅–F converter clock cycle of 15.625 MHz (250 MHz/16). The triangle waves have an amplitude resolution of 48 digital steps, so a full rising and falling period takes 96 counts which produces a maximum frequency of 162.76 kHz (1/(1/15.625 kHz * 96)).

The 96 digital counts of the triangle waves also lead to a very fine PLL phase resolution of 42 ps (4 ns/96 counts). This high phase resolution is achieved using very low frequency signals, in contrast to a standard PLL which must operate at significantly higher frequencies than the data being tracked to achieve such high phase resolution.

FREQUENCY CONTROLLED OSCILLATOR (FCO)

The frequency controlled oscillator produces a 250 MHz clock that, when divided by 2, is phase locked to the incoming data's clock.

The FCO uses three 250 MHz reference clock signals from the Clock Generation Module and three 0 Hz to 162.76 kHz error clock signals from the Phase Error to Frequency Converter as inputs. Each signal in a triplet is 120 degrees phase shifted from the next.

Each corresponding pair (one 250 MHz and one error signal) of signals is mixed together using an amplitude switching modulator, with the error signal modulating the reference. All of the outputs are then summed together to produce the final 250 MHz $+f_m$ phase locked clock signal, where f_m is the error frequency.

3.0 Functional Description (Continued)

3.2 RECEIVER BLOCK

During normal operation, the Receiver Block accepts serial data input at the rate of 125 Mbps from the Clock Recovery Module. During the Internal Loopback mode of operation, the Receiver Block accepts input data from the Transmitter Block.

The Receiver Block performs the following operations:

- Optionally converts the incoming data stream from NRZI to NRZ.
- Decodes the data from 5B to 4B coding.
- Converts the serial bit stream into the National byte-wide code.
- Compensates for the differences between the upstream station clock and the local clock.
- Decodes Line States.
- Detects link errors.
- Presents data symbol pairs to the Configuration Switch Block.

The Receiver Block consists of the following functional blocks:

NRZI to NRZ Decoder
Shift Register
Framing Logic
Symbol Decoder
Line State Detector
Elasticity Buffer
Link Error Detector

See *Figure 3-2.*

NRZI TO NRZ DECODER

The NRZI to NRZ Decoder converts Non-Return-To-Zero-Invert-On-Ones data to Non-Return-To-Zero format.

NRZ format data is the natural data format that the receiver block utilizes internally, so this function is required when the standard NRZI format data is fed into the device. The receiver block can bypass this conversion function in the case where an alternate data source outputs NRZ format data.

This function can be enabled and disabled through bit 7 (RNRZ) of the Mode Register (MR). When the bit is cleared, it converts the incoming bit stream from NRZI to NRZ. This is the normal configuration required. When the bit is set, the incoming NRZ bit stream is passed unchanged.

SHIFT REGISTER

The Shift Register converts the serial bit stream into symbol-wide data for the 5B/4B Decoder.

The Shift Register also provides byte-wide data for the Framing Logic.

FRAMING LOGIC

The Framing Logic performs the Framing function by detecting the beginning of a frame or the Halt-Halt or Halt-Quiet symbol pair.

The J-K symbol pair (11000 10001) indicates the beginning of a frame during normal operation. The Halt-Halt (00100 00100) and Halt-Quiet (00100 00000) symbol pairs are detected for Connection Management (CMT).

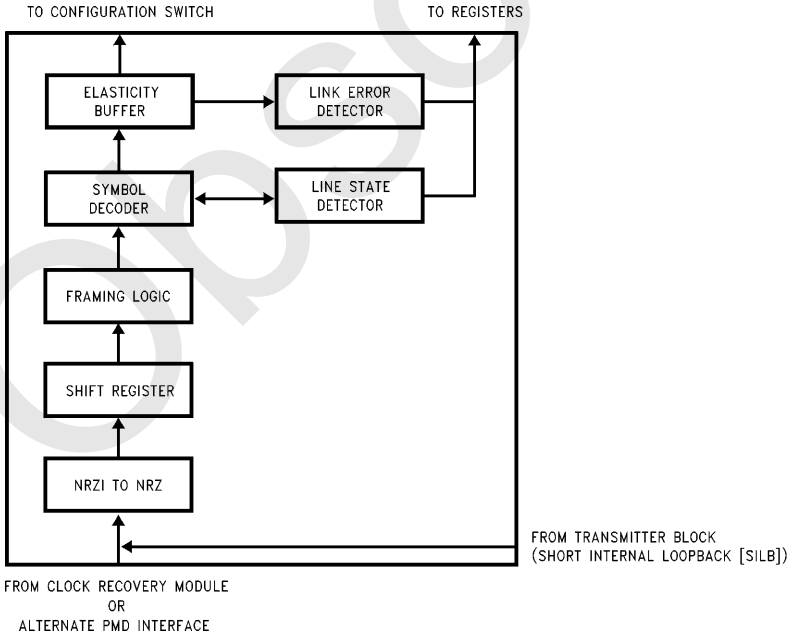

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FIGURE 3-2. Receiver Block Diagram

3.0 Functional Description (Continued)

Framing may be temporarily suspended (i.e. framing hold), in order to maintain data integrity.

Detecting JK

The JK symbol pair can be used to detect the beginning of a frame during Active Line State (ALS) and Idle Line State (ILS) conditions.

While the Line State Detector indicates Idle Line State the receiver ''reframes'' upon detecting a JK symbol pair and enters the Active Line State.

During Active Line State, acceptance of a JK symbol (reframing) is allowed for any on-boundary JK which is detected at least 1.5 byte times after the previous JK.

During Active Line State, once reframed on a JK, a subsequent off-boundary JK is ignored, even if it is detected beyond 1.5 byte times after the previous JK.

During Active Line State, an Idle or Ending Delimiter (T) symbol will allow reframing on any subsequent JK, if a JK is detected at least 1.5 byte times after the previous JK.

Detecting HALT-HALT AND HALT-QUIET

During Idle Line State, the detection of a Halt-Halt, or Halt-Quiet symbol pair will still allow the reframing of any subsequent on-boundary JK.

Once a JK is detected during Active Line State, off-boundary Halt-Halt, or Halt-Quiet symbol pairs are ignored until the Elasticity Buffer (EB) has an opportunity to recenter. They are treated as violations.

After recentering on a Halt-Halt, or Halt-Quiet symbol pair, all off boundary Halt-Halt or Halt-Quiet symbol pairs are ignored until the EB has a chance to recenter during a line state other than Active Line State (which may be as long as 2.8 byte times).

SYMBOL DECODER

The Symbol Decoder is a two level system. The first level is a 5-bit to 4-bit converter, and the second level is a 4-bit symbol pair to byte-wide code converter.

The first level latches the received 5-bit symbols and decodes them into 4-bit symbols. Symbols are decoded into two types: data and control. The 4-bit symbols are sent to the Line State Detector and the second level of the Symbol Decoder. See Table 3-1 for the 5B/4B Symbol Decoding list.

The second level translates two symbols from the 5B/4B converter and the line state information from the Line State Detector into the National byte-wide code.

LINE STATE DETECTOR

The ANSI X3T9.5 FDDI Physical Layer (PHY) standard specifies eight Line States that the Physical Layer can transmit. These Line States are used in the Connection Management process. They are also used to indicate data within a frame during normal operation.

The Line States are reported through the Current Receive State Register (CRSR), Receive Condition Register A (RCRA), and Receive Condition Register B (RCRB).

TABLE 3-1. 5B/4B Symbol Decoding

Symbol	Incoming 5B	Decoded 4B
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
I (Idle)	11111	1010
H (Halt)	00100	0001
JK (Starting Delimiter)	11000 and 10001	1101
T (Ending Delimiter)	01101	0101
R (Reset)	00111	0110
S (Set)	11001	0111
Q (Quiet)	00000	0010
V (Violation)	00001	0010
V	00010	0010
V	00011	0010
V	00101	0010
V	00110	0010
V	01000	0010
V	01100	0010
V	10000	0010

Note: V′ denotes PHY Invalid or an Elasticity Buffer stuff byte
I′ denotes Idle symbol in ILS or an Elasticity Buffer stuff byte

LINE STATES DESCRIPTION

Active Line State

The Line State Detector recognizes the incoming data to be in the Active Line State upon the reception of the Starting Delimiter (JK symbol pair).

The Line State Detector continues to indicate Active Line State while receiving data symbols, Ending Delimiter (T symbols), and Frame Status symbols (R and S) after the JK symbol pair.

Idle Line State

The Line State Detector recognizes the incoming data to be in the Idle Line State upon the reception of 2 Idle symbol pairs nominally (plus up to 9 bits of 1 in start up cases).

Idle Line State indicates the preamble of a frame or the lack of frame transmission during normal operation. Idle Line State is also used in the handshake sequence of the PHY Connection Management process.

3.0 Functional Description (Continued)

Super Idle Line State

The Line State Detector recognizes the incoming data to be in the Super Idle Line State upon the reception of 8 consecutive Idle symbol pairs nominally (plus 1 symbol pair).

The Super Idle Line State is used to insure synchronization of PCM signalling.

No Signal Detect

The Line State Detector recognizes the incoming data to be in the No Signal Detect state upon the deassertion of the Signal Detect signal or lack of internal clock detect from the Clock Recovery Module, and reception of 8 Quiet symbol pairs nominally. No Signal Detect indicates that the incoming link is inactive. This is the same as receiving Quiet Line State (QLS).

Master Line State

The Line State Detector recognizes the incoming data to be in the Master Line State upon the reception of eight consecutive Halt-Quiet symbol pairs nominally (plus up to 2 symbol pairs in start up cases).

The Master Line State is used in the handshaking sequence of the PHY Connection Management process.

Halt Line State

The Line State Detector recognizes the incoming data to be in the Halt Line State upon the reception of eight consecutive Halt symbol pairs nominally (plus up to 2 symbol pairs in start up cases).

The Halt Line State is used in the handshaking sequence of the PHY Connection Management process.

Quiet Line State

The Line State Detector recognizes the incoming data to be in the Quiet Line State upon the reception of eight consecutive Quiet symbol pairs nominally (plus up to 9 bits of 0 in start up cases).

The Quiet Line State is used in the handshaking sequence of the PHY Connection Management process.

Noise Line State

The Line State Detector recognizes the incoming data to be in the Noise Line State upon the reception of 16 noise symbol pairs without entering any known line state.

The Noise Line State indicates that data is not being received correctly.

Line State Unknown

The Line State Detector recognizes the incoming data to be in the Line State Unknown state upon the reception of 1 inconsistent symbol pair (i.e. data that is not expected). This may signify the beginning of a new line state.

Line State Unknown indicates that data is not being received correctly. If the condition persists the Noise Line State (NLS) may be entered.

ELASTICITY BUFFER

The Elasticity Buffer performs the function of a ''variable depth'' FIFO to compensate for phase and frequency clock skews between the Receive Clock (RXC±) and the Local Byte Clock (LBC).

Bit 5 (EBOU) of the Receive Condition Register B (RCRB) is set to 1 to indicate an error condition when the Elasticity Buffer cannot compensate for the clock skew.

The Elasticity Buffer will support a maximum clock skew of 50 ppm with a maximum packet length of 4500 bytes.

To make up for the accumulation of frequency disparity between the two clocks, the Elasticity Buffer will insert or delete Idle symbol pairs in the preamble. Data is written into the byte-wide registers of the Elasticity Buffer with the Receive Clock, while data is read from the registers with the Local Byte Clock.

The Elasticity Buffer will recenter (i.e. set the read and write pointers to a predetermined distance from each other) upon the detection of a JK or every four byte times during PHY Invalid (i.e. MLS, HLS, QLS, NLS, NSD) and Idle Line State. The Elasticity Buffer is designed such that a given register cannot be written and read simultaneously under normal operating conditions. To avoid metastability problems, the EB overflow event is flagged and the data is tagged before the over/under run actually occurs.

LINK ERROR DETECTOR

The Link Error Detector provides continuous monitoring of an active link (i.e. during Active and Idle Line States) to insure that it does not exceed the maximum Bit Error Rate requirement as set by the ANSI standard for a station to remain on the ring.

Upon detecting a link error, the internal 8-bit Link Error Monitor Counter is decremented. The start value for the Link Error Monitor Counter is programmed through the Link Error Threshold Register (LETR). When the Link Error Monitor Counter reaches zero, bit 4 (LEMT) of the Interrupt Condition Register (ICR) is set to 1. The current value of the Link Error Monitor Counter can be read through the Current Link Error Count Register (CLECR). For higher error rates the current value is an approximate count because the counter rolls over.

There are two ways to monitor Link Error Rate: polling and interrupt.

Polling

The Link Error Monitor Counter can be set to a large value, like FF. This will allow for the greatest time between polling the register. This start value is programmed through the Link Error Threshold Register (LETR).

Upon detecting a link error, the Line Error Monitor Counter is decremented.

The Host System reads the current value of the Link Error Monitor Counter via the Current Link Error Count Register (CLECR). The Counter is then reset to FF.

Interrupt

The Link Error Monitor Counter can be set to a small value, like 5 to 10. This start value is programmed through the Link Error Threshold Register (LETR).

Upon detecting a link error, the Line Error Monitor Counter is decremented. When the counter reaches zero, bit 4 (LEMT) of the Interrupt Condition Register (ICR) is set to 1, and the interrupt signal goes low, interrupting the Host System.

Miscellaneous Items

When bit 0 (RUN) of the Mode Register (MR) is set to zero, or when the PLAYER+ device is reset through the Reset pin (~RST), the internal signal detect line is internally forced to zero and the Line State Detector is set to Line State Unknown and No Signal Detect.

3.0 Functional Description (Continued)

3.3 TRANSMITTER BLOCK

The Transmitter Block accepts 10-bit bytes consisting of 8 bits data, 1 bit parity, and 1 bit control information, from the Configuration Switch.

The Transmitter Block performs the following operations:

- Encodes the data from 4B to 5B coding.
- Filters out code violations from the data stream.
- Is capable of generating Idle, Master, Halt, Quiet, or other user defined symbol pairs.
- Converts the data stream from NRZ to NRZI for transmission.
- Serializes data.

During normal operation, the Transmitter Block presents serial data to a PMD transmitter.

While in Internal Loopback mode, the Transmitter Block presents serial data to the Receiver Block. While in the External Loopback mode, the Transmitter Block presents serial data to the Clock Recovery Module.

The Transmitter Block consists of the following functional blocks:

Data Registers
Parity Checker
4B/5B Encoder
Repeat Filter
Smoother
Line State Generator
Injection Control Logic
Shift Register
NRZ to NRZI Encoder

See *Figure 3-3*, Transmitter Block Diagram.

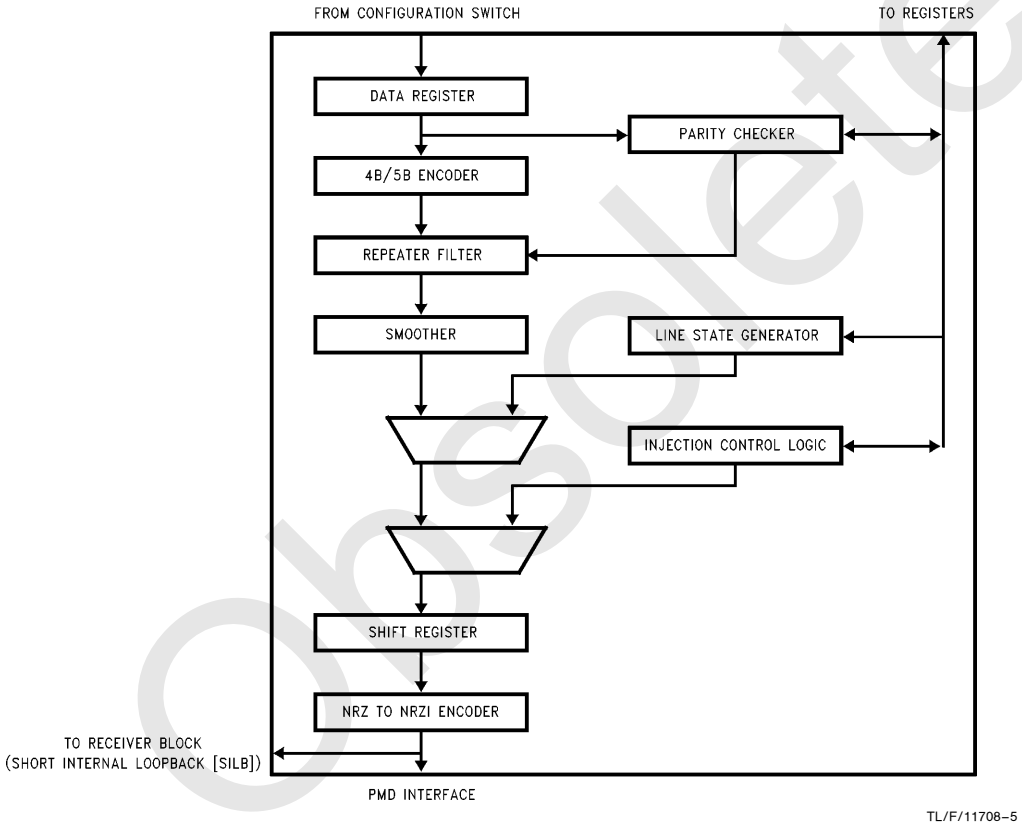


FIGURE 3-3. Transmitter Block Diagram

3.0 Functional Description (Continued)

DATA REGISTERS

Data from the Configuration Switch is stored in the Data Registers. The 10-bit byte-wide data consists of a parity bit, a control bit, and two 4-bit data symbols as shown below.

b9	b8	b7 b0
Parity Bit	Control Bit	Data Bits

FIGURE 3-4. Byte-Wide Data

The parity is odd parity. The control bit determines whether the Data bits represent Data or Control information. When the control bit is 0 the Data field is interpreted as data and when it is 1 the field is interpreted as control information according to the National Semiconductor control codes.

PARITY CHECKER

The Parity Checker verifies that the parity bit in the Data Register represents odd parity (i.e. odd number of 1s).

The parity is enabled and disabled through bit 6 (PRDPE) of the Current Transmit State Register (CTSR).

If a parity error occurs, the Parity Checker will set bit 0 (DPE) in the Interrupt Condition Register (ICR) and report the error to the Repeat Filter.

4B/5B ENCODER

The 4B/5B Encoder converts the two 4-bit data symbols from the Configuration Switch into their respective 5-bit codes.

See Table 3-2 for the Symbol Encoding list.

TABLE 3-2. 4B/5B Symbol Encoding

Symbol	4B Code	5B Code
0	0000	11110
1	0001	01001
2	0010	10100
3	0011	10101
4	0100	01010
5	0101	01011
6	0110	01110
7	0111	01111
8	1000	10010
9	1001	10011
A	1010	10110
B	1011	10111
C	1100	11010
D	1101	11011
E	1110	11100
F	1111	11101
N	0000	11110 or 11111
JK (Starting Delimiter)	1101	11000 and 10001
T (Ending Delimiter)	0100 or 0101	01101
R (Reset)	0110	00111

Note: The upper group of symbols are sent with the Control/Data pin set to Data, while the bottom grouping of symbols are sent with the Control/Data pin set to Control.

REPEAT FILTER

The Repeat Filter is used to prevent the propagation of code violations to the downstream station.

Upon receiving violations in data frames, the Repeat Filter replaces them with two Halt symbol pairs followed by Idle symbols. Thus the code violations are isolated and recovered at each link and will not be propagated throughout the entire ring.

3.0 Functional Description (Continued)

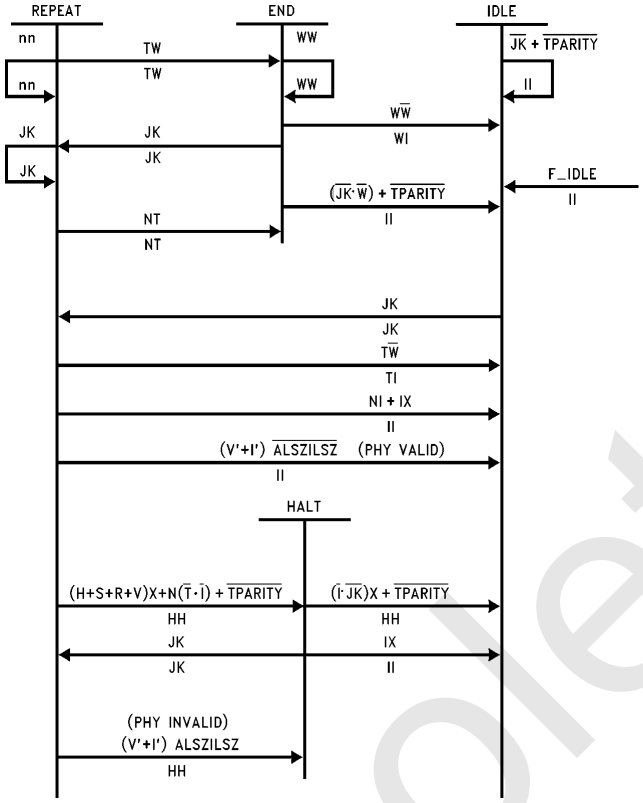


FIGURE 3-5. Repeat Filter State Diagram

Note: Inputs to the Repeat Filter state machine are shown above the transition lines, while outputs from the state machine are shown below the transition lines.

Note: Abbreviations used in the Repeat Filter State Diagram are shown in Table 3-3.

3.0 Functional Description (Continued)

TABLE 3-3. Abbreviations used in the Repeat Filter State Diagram

F__IDLE:	Force Idle__true when not in Active Transmit Mode.
W:	Represents the symbols R, or S, or T
~TPARITY:	Parity error
nn :	Data symbols (for C = 0 in the PHY-MAC interface)
N:	Data portion of a control and data symbol mixture
X:	Any symbol (i.e. don't care)
V′:	Violation symbols or symbols inserted by the Receiver Block
I′:	Idle symbols or symbols inserted by the Receiver Block
ALSZILSZ:	Active Line State or Idle Line State (i.e. PHY Invalid)
~ALSZILSZ:	Not in Active Line State nor in Idle Line State (i.e. PHY Valid)
H:	Halt Symbol
R:	Reset Symbol
S:	Set Symbol
T:	Frame ending delimiter
JK:	Frame start delimiter
I:	Idle symbol (Preamble)
V:	Code violations

The Repeat Filter complies with the FDDI standard by observing the following (see *Figure 3-5*):

1. In Repeat State, violations cause transitions to Halt State and two Halt symbol pairs are transmitted (unless JK or Ix occurs) followed by transition to Idle State.
2. When Ix is encountered, the Repeat Filter goes to the Idle State, during which Idle symbol pairs are transmitted until a JK is encountered.
3. The Repeat Filter goes to the Repeat State following a JK from any state.

The END State, which is not part of the FDDI PHY standard, allows an R or S prior to a T within a frame to be recognized as a violation. It also allows NT to end a frame as opposed to being treated as a violation.

SMOOTHER

The Smoother is used to keep the preamble length of a frame to a minimum of 6 Idle symbol pairs.

Idle symbols in the preamble of a frame may have been added or deleted by each station to compensate for the difference between the Receive Clock and its Local Clock. The preamble needs to be maintained at a minimum length to allow stations enough time to complete processing of one frame and prepare to receive another. Without the Smoother function, the minimum preamble length (6 Idle symbol pairs) cannot be maintained as several stations may consecutively delete Idle symbols.

The Smoother attempts to keep the number of Idle symbol pairs in the preamble at 7 by:

- Deleting an Idle symbol pair in preambles which have more than 7 Idle symbol pairs

and/or

- Inserting an idle symbol pair in preambles which have less than 7 idle symbol pairs (i.e. Extend State).

The Smoother Counter starts counting upon detecting an Idle symbol pair. It stops counting upon detecting a JK symbol pair.

Figure 3-6 describes the Smoother state diagram.

3.0 Functional Description (Continued)

LINE STATE GENERATOR

The Line State Generator allows the transmission of the PHY Request data and can also generate and transmit Idle, Master, Halt, or Quiet symbol pairs which can be used to implement the Connection Management procedures as specified in the FDDI Station Management (SMT) standard document.

The Line State Generator is programmed through Transmit bits 0 to 2 (TM<2:0>) of the Current Transmit State Register (CTSR).

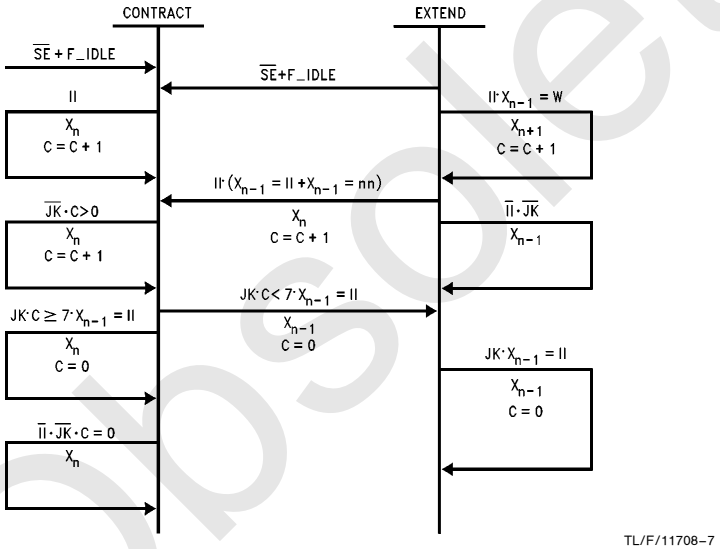
Based on the setting of these bits, the Transmitter Block operates in a Transmit Mode where the Line State Generator overwrites the Repeat Filter and Smoother outputs.

See INJECTION CONTROL LOGIC section for a listing of the injection Transmit Modes.

Table 3-4 describes the Transmit Modes.

TABLE 3-4. Transmit Modes

Transit Mode	Behavior
Active Transmit Mode	Transmit data that comes from Configuration Switch
Off Transmit Mode	Transmit Quiet symbol pairs and disable the PMD Transmitter
Idle Transmit Mode	Transmit Idle symbol pairs
Master Transmit Mode	Transmit Halt-Quiet symbol pairs
Quiet Transmit Mode	Transmit Quiet symbol pairs
Reserved Transmit Mode	Reserved for future use. If Mode selected, Quiet symbol pairs will be transmitted.
Halt Transmit Mode	Transmit Halt Symbol pairs



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Notes:

SE: Smoother Enable
C: Preamble Counter
F_IDLE: Force_Idle (Stop or ATM)
X_n: Current Byte
X_{n-1}: Previous Byte
W: RST

FIGURE 3-6. Smoother State Diagram

3.0 Functional Description (Continued)

INJECTION CONTROL LOGIC

The Injection Control Logic replaces the data stream with a programmable symbol pair. This function is used to transmit data other than the normal data frame or Line States. The injection modes can be used for station diagnostic software.

The Injection Symbols overwrite the Line State Generator (Transmit Modes) and the Repeat Filter and Smoother outputs.

These programmable symbol pairs are stored in the Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB). The Injection Threshold Register (IJTR) determines where the Injection Symbol pair will replace the data symbols.

The Injection Control Logic is programmed through the bits 0 and 1 (IC<1:0>) of the Current Transmit State Register (CTSR) to one of the following Injection Modes (see *Figure 3-7*):

1. No Injection (i.e. normal operation)
2. One Shot
3. Periodic
4. Continuous

In the No Injection mode, the data stream is transmitted unchanged.

In the One Shot mode, ISRA and ISRB are injected once on the nth byte after a JK, where n is the programmed value specified in the Injection Threshold Register.

In the Periodic mode, ISRA and ISRB are injected every nth symbol.

In the Continuous mode, all data symbols are replaced with the content of ISRA and ISRB. This is the same as periodic mode with IJTR = 0.

SHIFT REGISTER

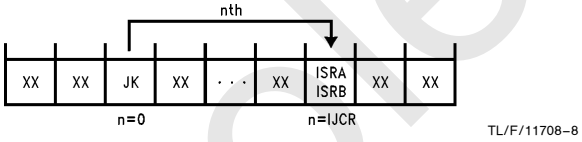
The Shift Register converts encoded parallel data to serial data. The parallel data is clocked into the Shift Register by the Local Byte Clock (LBC1), and clocked out by the Transmit Bit Clock (TXC ±) (externally available on the DP83257.)

NRZ TO NRZI ENCODER

The NRZ to NRZI Encoder converts the serial Non-Return-To-Zero data to Non-Return-To-Zero-Invert-On-One format.

This function can be enabled and disabled through bit 6 (TNRZ) of the Mode Register (MR). When programmed to "0", it converts the bit stream from NRZ to NRZI. When programmed to "1", the bit stream is transmitted NRZ.

One Shot (Notes 1,3)



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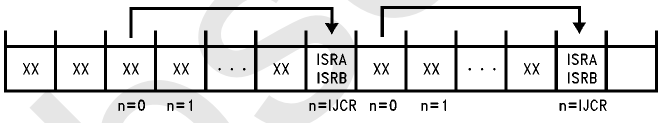
Periodic (Notes 2,3)



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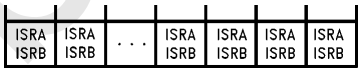
Continuous (Note 3)



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Note 1: In one shot, when n = 0, the JK is replaced

Note 2: In periodic, when n = 0, all symbols are replaced.

Note 3: Max value on n = 255.

FIGURE 3-7. Injection Modes

3.0 Functional Description (Continued)

3.4 CONFIGURATION SWITCH

The Configuration Switch consists of a set of multiplexers and latches which allow the PLAYER+ device to configure the data paths without any external logic. The Configuration Switch is controlled through the Configuration Register (CR).

The Configuration Switch has four internal buses: the A_Request bus, the B_Request bus, the Receive bus, and the PHY_Invalid bus. The two Request buses can be driven by external input data connected to the external PHY Port interface. The Receive bus is internally connected to the Receive Block of the PLAYER+ device, while the PHY_Invalid bus has a fixed 10-bit SMT PHY Invalid connection (LSU) pattern (1 0011 1010), which is useful during the connection process.

The configuration switch also has three internal multiplexers, each can select any of the four buses to connect to its respective data path. The first two are PHY Port interface output data paths, A_Indicate and B_Indicate, that can drive output data paths of the external PHY Port interface. The third output data path is connected internally to the Transmit Block.

The Configuration Switch is the same on the DP83256 device, the DP83256-AP device, and the DP83257 device. However, the DP83257 has two PHY Port interfaces connected to the Configuration Switch, whereas the DP83256 and DP83256-AP have one set of PHY port interfaces. The DP83257 uses the A_Request and A_Indicate paths as one PHY Port interface and the B_Request and B_Indicate paths as the other PHY Port interface (See *Figure 3-8*). The DP83256 and DP83256-AP, having one port interface, use the B_Request and A_Indicate paths as its external port. The A_Request and B_Indicate paths of the DP83256 and DP83256-AP are null connections and are not used by the device (See *Figure 3-9*).

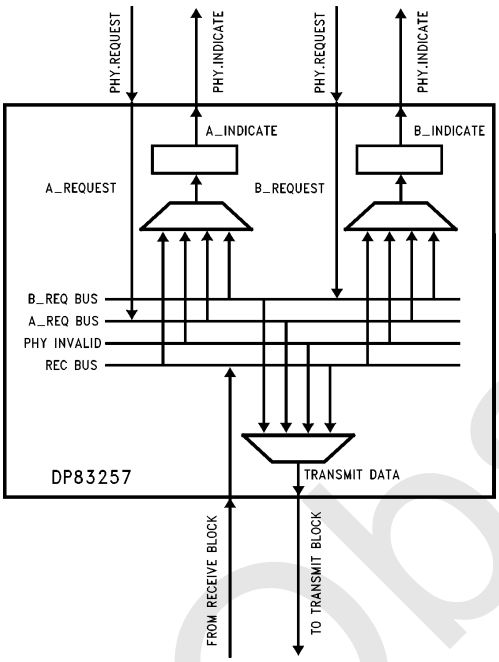

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FIGURE 3-8. Configuration Switch Block Diagram for DP83257

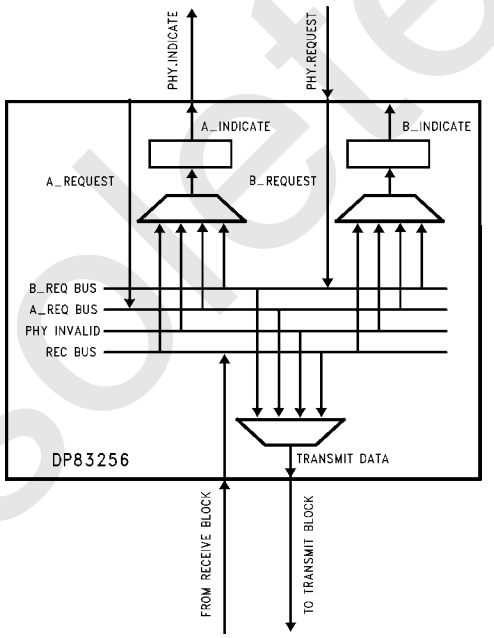

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FIGURE 3-9. Configuration Switch Block Diagram for DP83256 and DP83256-AP

3.0 Functional Description (Continued)

STATION CONFIGURATIONS

Single Attach Station (SAS)

The Single Attach Station can be connected to either the Primary or Secondary ring via a Concentrator. Only 1 MAC is needed in a SAS.

The DP83256, DP83256-AP, and DP83257 can be used in a Single Attach Station. The DP83256 and DP83256-AP can be connected to the MAC via its only PHY Port interface. The DP83257 can be connected to the MAC via either one of its 2 PHY Port Interfaces.

See *Figure 3-10* and *Figure 3-11*.

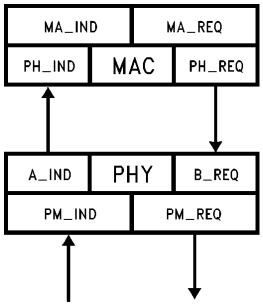

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FIGURE 3-10. Single Attach Station Using the DP83256 or DP83256-AP

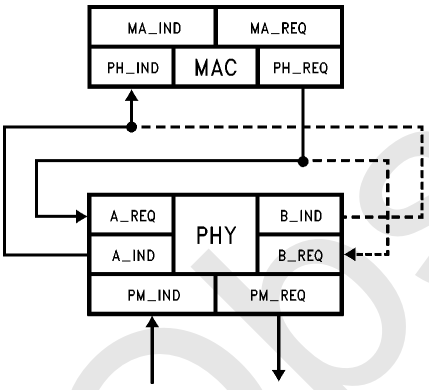

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FIGURE 3-11. Single Attachment Station (SAS) Using the DP83257

Dual Attach Station(DAS)

A Dual Attach Station can be connected directly to the dual ring, or, optionally to a concentrator. There are two types of Dual Attach Stations: DAS with a single MAC and DAS with two MAC layers. See *Figure 3-12* and *Figure 3-13*.

Two DP83256 or DP83256-AP parts can be connected together to build a Dual Attach Station, however this configuration does not support the optional Thru__B configuration. When the optional Thru__B configuration is desired, it is recommended that the DP83257 be used.

A DAS with a single MAC and two paths can be configured as follows (see *Figure 3-12*):

- B Indicate data of PHY__A is connected to A Request input of PHY__B. B__Request input of PHY__A is connected to A Indicate output of PHY__B.
- The MAC can be connected to either the A Request input and the A Indicate output of PHY__A or the B Request input and the B Indicate output of PHY__B.

A DAS with a single MAC and one path using the DP83256 or DP83256-AP can be configured as follows (see *Figure 3-13*):

- B__Request input of PHY__A is connected to A Indicate output of PHY__B.
- The MAC is connected to the B Request input of PHY__B and the A__Indicate output of PHY__A.

A DAS with dual MACs can be configured as follows (see *Figure 3-14*):

- B Indicate data of PHY__A is connected to A Request input of PHY__B. B__Request input of PHY__A is connected to A Indicate output of PHY__B.
- MAC__1 is connected to the B__Indicate output and the B__Request Input of PHY__B.
- MAC__2 is connected to the A__Indicate output and the A__Request Input of PHY__A.

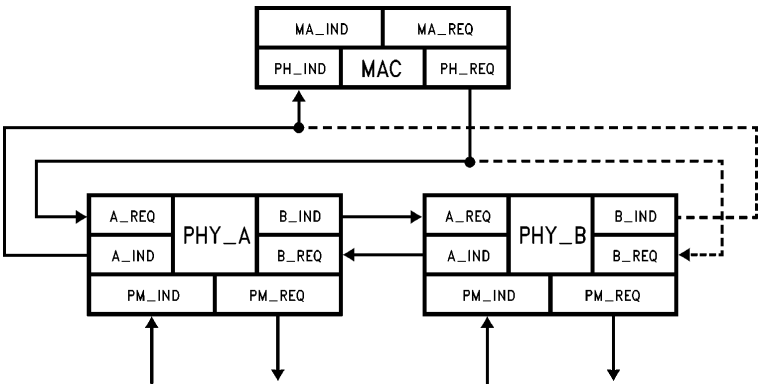

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FIGURE 3-12. Dual Attachment Station (DAS), Single MAC (DP83257)

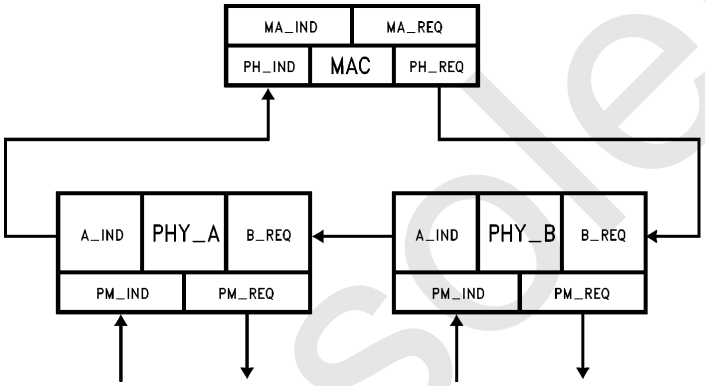

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FIGURE 3-13. Dual Attachment Station (DAS), Single MAC (DP83256/56-AP)

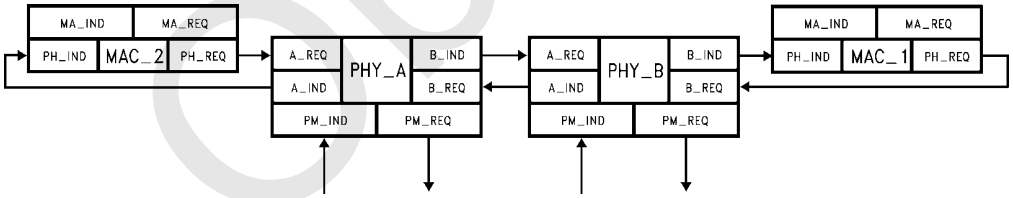

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FIGURE 3-14. Dual Attachment Station (DAS), Dual MACs

3.0 Functional Description (Continued)

CONCENTRATOR CONFIGURATIONS

There are 2 types of concentrators: Single Attach and Dual Attach. These concentrators can be designed with or without MAC(s). The configuration is determined based upon its type and the number of active MACs in the concentrator.

Using the PLAYER+ device, a concentrator can be built with many different configurations without any external logic.

The DP83256, DP83256-AP, and DP83257 can be used to build a Single Attach concentrator.

See Application Note AN-675, Designing FDDI concentrators and Application Note AN-741, Differentiating FDDI concentrators for further information.

Concepts

A concentrator is comprised of 2 parts: the Dual Ring Connect portion and the Master Ports.

The Dual Ring Connection portion connects the concentrator to the dual ring directly or to another concentrator. If the concentrator is connected directly to the dual ring, it is a part of the ''Dual Ring of Trees''. If the concentrator is connected to another concentrator, it is a ''Branch'' of the ''Dual Ring of Trees''.

The Master Ports connect the concentrator to its ''Slaves'', or S-class, Single Attach connections. A slave could be a Single Attach Station or another concentrator (thus forming another Branch of the Dual Ring Tree).

When a MAC in a concentrator is connected to the primary or secondary ring, it is required to be situated at the exit port of that ring (i.e. its PH__IND is connected to the IND Interface of the last Master Port in the concentrator (PHY__M n) that is connected to that ring).

A concentrator can have two MACs, one connected to the primary ring and one to the secondary ring. In addition, roving MACs can be included in the concentrator configuration. A roving MAC can be used to test the stations connected to the concentrator before allowing them to join the dual ring. This may require external multiplexers, if used in conjunction with two other MAC layers.

Single Attach Concentrator

A Single Attach concentrator is a concentrator that has only one PHY at the dual ring connect side. It cannot, therefore, be connected directly to the dual ring. A Single Attach concentrator is a branch to the dual ring tree. It is connected to the ring as a slave of another concentrator.

Multiple Single Attach concentrators can be connected together hierarchically to build a multiple levels of branches in a dual ring.

The Single Attach concentrator can be connected to either the primary or secondary ring depending on the connection with its concentrator (the concentrator that it is connected to as a slave).

Figure 3-15 shows a Single Attach concentrator with a single MAC.

Dual Attach Concentrator

A Dual Attach concentrator is a concentrator that has two PHYs on the dual ring connect side. It is connected directly to the dual ring and is a part of the dual ring tree.

The Dual Attach concentrator is connected to both the primary and secondary rings.

Dual Attach Concentrator with Single MAC

Figure 3-16 shows a Dual Attach concentrator with a single MAC.

Because the concentrator has one MAC, it can only transmit and receive frames on the ring to which the MAC is connected. The concentrator can only repeat frames on the other ring.

Dual Attach Concentrator with Dual MACs

Figure 3-17 shows a Dual Attach concentrator with dual MACs.

Because the concentrator has two MACs, it can transmit and receive frames on both the primary and secondary rings.

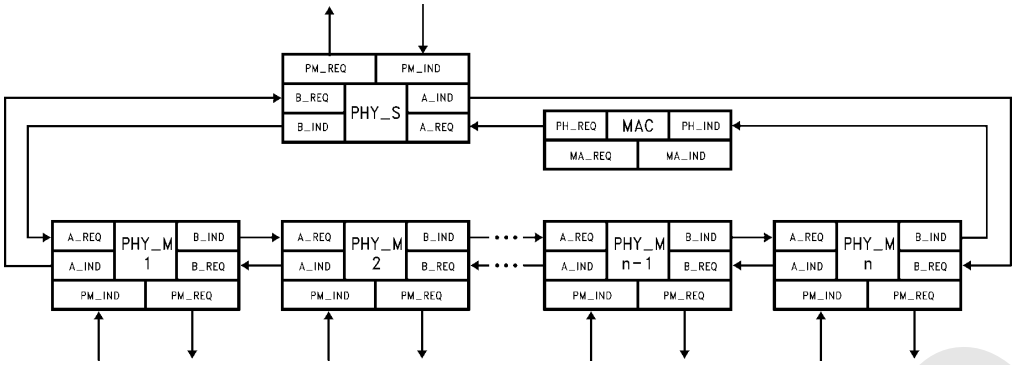

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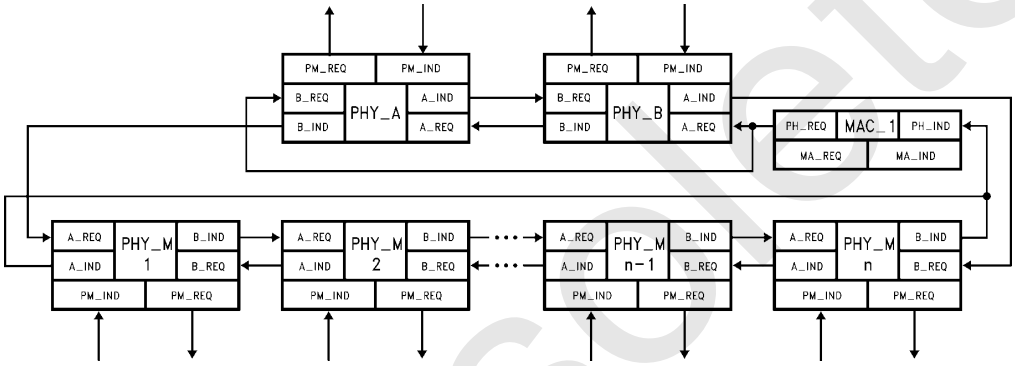
FIGURE 3-15. Single Attach Concentrator (SAC), Single MAC



TL/F/11708–19

FIGURE 3-16. Dual Attach Concentrator (DAC), Single MAC

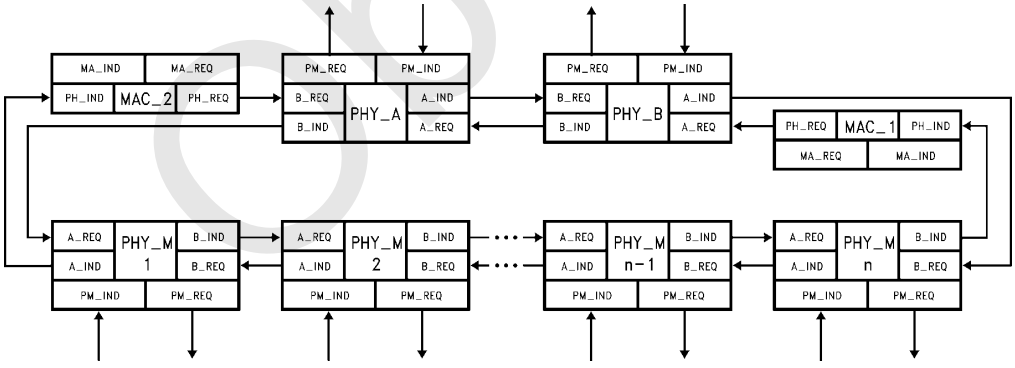


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FIGURE 3-17. Dual Attach Concentrator (DAC), Dual MACs

3.0 Functional Description (Continued)

3.5 CLOCK GENERATION MODULE

The Clock Generation Module is an integrated phase locked loop that generates all of the required clock signals for the PLAYER+ device and the rest of an FDDI system from a single 12.5 MHz reference.

The Clock Generation Module features:

- High precision clock timing generated from a single 12.5 MHz reference.
- Multiple precision phased (8 ns/16 ns) 12.5 MHz Local Byte Clocks to eliminate timing skew in large multi-board concentrator configurations.
- LBC timing which is insensitive to loading variations over a wide range (20 pF to 70 pF) of LBC loads.
- A selectable dual frequency system clock.
- Low clock edge jitter, due to high VCO stability.

The Clock Generation Module is comprised of 6 main functional blocks:

Reference Selector
Phase Comparator
Loop Filter
250 MHz Voltage Controlled Oscillator
Output Phasing and Divide by 10

See *Figure 3-18*, Clock Generation Module Block Diagram.

REFERENCE SELECTOR

The Reference Selector block allows the user to choose between 2 sources for the Clock Generation Module's 12.5 MHz reference clock.

The simplest reference clock source option is to use an external 12.5 MHz reference signal fed into the REF__IN input. This input can come from a crystal oscillator module or from a Local Byte Clock generated by another PLAYER+ device. Using the appropriate crystal oscillator ensures correct operating frequency without having to adjust any discrete components.

Using an LBC clock from another PLAYER+ device allows one PLAYER+ device to create a master clock to which other PLAYER+ devices in a system can be synchronized.

Another reference clock source option is a local 12.5 MHz crystal circuit. An example crystal circuit with component values is shown in *Figure 3-19*. This circuit is designed to operate with a crystal that has a C_L of 15 pF. The capacitor values may need to be slightly adjusted for an individual application to accomodate differences in parasitic loading.

The REF__SEL signal selects between the two references.

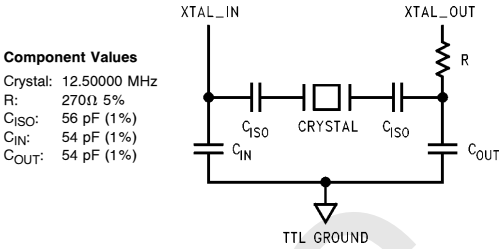

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FIGURE 3-19. Crystal Circuit

PHASE COMPARATOR

The Phase Comparator uses two signal inputs: the selected 12.5 MHz reference from the Reference Select Block and a Local Byte Clock that has been selected for the feedback input, FBK__IN. Typically, LBC1 is used as the feedback clock.

The Phase Comparator generates a pulse of current that is proportional to the phase difference between the two signals. The current pulses are used to charge and discharge a control voltage on the internal Loop Filter. This control voltage is used to minimize the phase difference between the two signals.

LOOP FILTER

The Loop Filter is a simple internal filter made up of one capacitor in parallel with a serial capacitor and resistor combination. One end of the filter is connected to Ground and the other node is driven by the Phase Comparator and controls the internal 250 MHz Voltage Controlled Oscillator. This node can be examined for diagnostic purposes on the LPFLTR pin when the FLTREN bit of the CGMREG register is enabled. The LPFLTR pin is provided for diagnostic purposes only and should not be connected in any application.

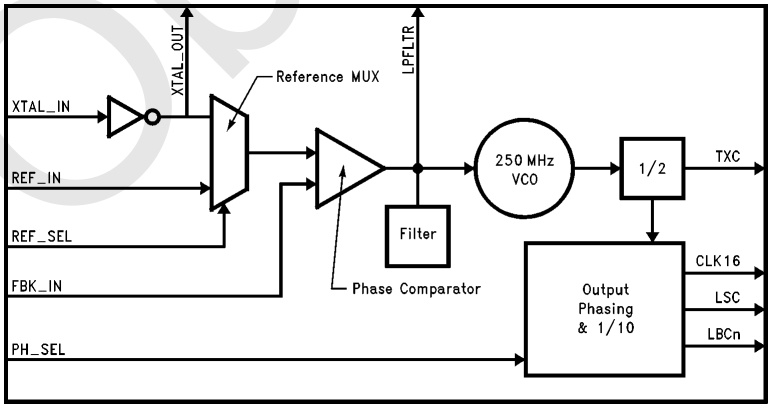

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FIGURE 3-18. Clock Generation Module Block Diagram

3.0 Functional Description (Continued)

The voltage on the Loop Filter is set by the current pulses generated by the Phase Comparator. The voltage on the Loop Filter node controls the frequency of the 250 MHz VCO.

250 MHZ VOLTAGE CONTROLLED OSCILLATOR (VCO)

The internal Voltage Controlled Oscillator is a low gain VCO whose primary frequency of oscillation centers around 250 MHz. The VCO produces little clock jitter due to its exceptional stability under all circumstances.

The VCO's output frequency is proportional to the voltage on the Loop Filter node.

OUTPUT PHASING

The Output Phasing block is a precision clock division circuit that produces clock signals of 4 distinct frequencies. Within the 12.5 MHz frequency, 5 clock signals with selectable 8 ns or 16 ns phase difference are produced.

The following clock signals are produced:

System Clock (CLK16/CLK32)
Local Symbol Clock (LSC)
Local Byte Clocks 1–5 (LBCn) (Divide by 10)

System Clock (CLK16/CLK32)

The System Clock is provided as an extra set of clock frequencies that may be used as a clock for non-FDDI chipset portions of a system or as a higher frequency System Interface clock for the MACSI device. This clock is derived by dividing the 125 MHz clock by 8 or 4 times.

The frequency is selectable through the CLKSEL bit of the MODE2 register. The output has built-in glitch suppression so that changing the CLKSEL bit will not result in glitches appearing at the output.

Local Symbol Clock (LSC)

The Local Symbol Clock is a 40% HIGH/60% LOW duty cycle clock provided for use by the MACSI device and any external logic that needs to be synchronized to the Symbol timing.

This clock is derived by dividing the 125 MHz clock by 5.

Local Byte Clocks 1–5 (LBCn)

The Local Byte Clocks are provided for use by the MACSI device, by any external logic that needs to be synchronized to the Byte timing, and for use in concentrators to synchronize the timing between multiple PLAYER+ devices.

These clocks are derived by dividing the 125 MHz clock by 10. The different phase relationships between the LBCs are achieved by tapping off of different outputs of a Johnson counter inside the Output Phasing block.

The phase relationship (separation by 8 ns or 16 ns) of the LBCs is selected using the PH__SEL pin.

One of the LBCs must be used as the source of the feedback input, FBK__IN, which requires a 12.5 MHz frequency. When the PLAYER+ device is using a crystal as a reference it does not matter which LBC is used as the feedback input. Typically the least loaded LBC is used. However, when using an external reference that is supplied by another PLAYER+ device, it is important to select the LBC that keeps your system properly synchronized. Typically, all devices will use LBC1 as the feedback input.

3.6 STATION MANAGEMENT SUPPORT

The Station Management Support Block provides a number of useful features to simplify the implementation of the Connection Management (CMT) portion of SMT.

These features eliminate the most severe CMT response time constraints imposed by the PC__React and CF__React times. The many integrated counters and timers also eliminate the need for additional external devices.

The following CMT features are supported:

- PC__React
- CF__React
- Auto Scrubbing (TCF Timer)
- Timer, Idle Detection (TID Timer)
- Noise Event Counter (TNE Timer)
- Link Error Monitor (LEM Counter)

PC__REACT

PC__React is one of the timing restrictions imposed by Connection Management (CMT). It is one of the two most critical timing restrictions imposed (the other being CF__React.)

The ANSI SMT standard states that ''PC__React is the maximum time for PCM [Physical Connection Management] to make a state transition to PC__Break when QLS, a fault condition, or PC__Start signal is present. This maximum time also places a limit on the time to react to a PC__Stop signal. This limitation does not apply to any other PCM transitions.'' PC__React puts a sharp time limit on how long it takes to transition to the PC__Break state and transmit the correct line state when a PC__Break transition is required.

The range for the timer is PC__React $\leq$ 3.0 ms and has a default value equal to 3.0 ms.

The PLAYER+ device contains a Trigger Definition Register and a set of CMT Condition Registers that can be used to satisfy the PC__React timing.

The Trigger Definition Register (TDR) controls two functions. First, it allows the selection of the line state(s) on which to trigger (SILS, MLS, HLS . . .). For PC__React, the line states used would be the ones that caused a transition to the PC__Break state from the current PCM state.

Second, it allows specification of a line state to be transmitted when the trigger condition is met. For PC__React, this is the line state that needs to be transmitted when a transition to the PC__Break state occurs, which is Quiet Line State (QLS).

The set of CMT Condition registers controls interrupt generation when a trigger condition occurs. The CMT Condition Register set includes a CMT Condition Register (CMTCR), a CMT Condition Comparison Register (CMTCCR), and a CMT Condition Mask Register (CMTCMR).

Line state triggering for PC__React is enabled by selecting line states to trigger on from the Trigger Definition Register (TDR) bits 3-7.

The Trigger Condition Occurred (TCO) bit of the CMTCR is automatically set when the trigger condition specified by the TDR register is met.

The line state specified by the Trigger Definition Register (TDR) bits 0–2 is then loaded into the Current Transmit Mode Register (CTSR), causing the line state to be transmitted.

3.0 Functional Description (Continued)

If the TCO Mask (TCOM) bit of the CMTCMR is set, then whenever the CMTCR.TCO bit becomes set the Receive Condition Register B's Connection Service Event (RCRB.CSE) bit will be set. This allows an interrupt to be generated for the trigger event.

As an example, suppose the PCM state machine is in the ACTIVE state. From this state, if a Halt Line State (HLS) or Quiet Line State (QLS) is detected, or the Noise Threshold is reached, the state machine must move to the PC__Break state and begin transmitting QLS. To implement this behavior when the PC__ACTIVE state is entered, set TDR.TTM2−0 to 110 (Quiet Transmit), set TDR.TOHLS, TDR.TOQLS, and TDR.TONT and reset all other bits (TOSILS and TOMLS). Also set CMTCMR.TCOM if an interrupt is desired.

CF__REACT

CF__React is one of the timing restrictions imposed by Connection Management (CMT). It is one of the two most critical timing restrictions imposed (the other being PC__React).

The ANSI SMT standard states that ''CF__React is the maximum time for CFM [Configuration Management] to reconfigure to remove a non-Active connection from the token path.''

The range for the timer is CF__React $\leq$ 3.0 ms and has a default value equal to 3.0 ms.

The PLAYER+ device contains a Trigger Transition Configuration Register and a set of CMT Condition Registers that can be used to satisfy the CF__React timing.

he Trigger Transition Configuration Register (TTCR) holds the new configuration switch settings to be loaded into the Configuration Register (CR) when a trigger condition occurs.

Enabling line state triggering with the Trigger Definition Register (TDR) bits 3−7 also enables the CF__React response. This means that whenever trigger conditions are actively used for PC__React, the value of the TTCR register will be used also. This implies that it either must always then be loaded with the current configuration setting, causing no change to the CR, or it must be loaded with the appropriate value to accommodate the CF__React function.

The Trigger Transition Configuration Register (TTCR) must be set the configuration desired when the trigger condition occurs. When the trigger condition occurs the value of this register is loaded into the Configuration Register (CR). During this time writes to the CR are inhibited.

To continue the example from the PC__React description, suppose that when in the ACTIVE state for the PCM state machine, the CFM state machine is also in the THRU__A state. If trigger conditions are enabled via the CMTCMR.TCOM bit and it is desired to not implement CF__React, TTCR must be set to the present value of CR. If it is desired to not implement CF__React then TTCR should be set to the value which would change the configuration to the WRAP state. The wrap conditions WRAP__A or WRAP__B depend on which PHY gets reconfigured.

AUTO SCRUBBING

Auto Scrubbing is an additional CMT feature that further enhances the automatic configuration switch setting in order to meet the CF__React timing. When enabled, Auto Scrubbing causes 2 PHY__Invalid symbols followed by Scrub Symbol pairs (Idles) to be sourced for a user selectable duration (the scrubbing time) after a trigger condition (the same one used for PC__React and CF__React) occurs and prior to a change in the configuration switch setting on all indicate ports that will be changed.

Auto Scrubbing is enabled by setting the Enable Scrubbing on Trigger Conditions (ESTC) bit of Mode Register 2 (MODE2).

The Scrub Timer Threshold Register (STTR) defines the duration of the scrubbing, which can last up to approximately 10ms. The Scrub Timer Value Register (STVR) can be used to examine a snapshot of the upper 8 bits of the STTR register.

TIMER, IDLE DETECTION

The Idle Detection Timer is required to flag the continued presence of the Idle Line State for a duration of 8 Idle Symbol pairs plus 1 symbol pair.

This feature is implemented in the Receiver Block by the Super Idle Line State (SILS).

NOISE EVENT COUNTER

The Noise Event Counter can be used to time the duration between Noise Events (which are described in detail below) and to count frame sizes. The first feature is the most often recognized, but the second is often overlooked and can lead to potential difficulty if not properly set.

The Noise Event Counter is implemented as a pair of down counters: one the actual Noise Counter and the other a Noise Counter Prescaling value. The Noise Threshold Register (NTR) and the Noise Prescale Threshold Register (NPTR) can be programmed to the counter's initial value while the Current Noise Count Register (CNCR) and the Current Noise Prescale Count Register (CNPCR) provide a snapshot of the actual counter.

The Noise Event Counter decrements whenever a Noise Line State (NLS), Line State Unknown (LSU), or Active Line State (ALS) is received and has its start value reloaded whenever it receives Halt Line State (HLS), Idle Line State (ILS), Master Line State (MLS), Quiet Line State (QLS), or No Signal Detect (NSD). The Noise Event Counter is also reset for a Start or End Delimiter. This means the Noise counter increments for bad events as well as for every data symbol in a frame. Should the Noise Counter expire, it indicates that a new line state (including ALS) has not been entered for NT__MAX time. This indicates that either a frame is too long or that noise is being received.

For this reason it is important to choose a value for the counter that is larger than the longest frame of 4500 bytes. The ANSI SMT specification recommends a value for NT__MAX of 1.3ms for the noise threshold.

A Noise Event is defined as follows:

A noise event is a noisebyte, or a byte of data which is not in line with the current line state, indicating error or corruption.

3.0 Functional Description (Continued)

TABLE 3-5. Noise Event Description

Noise Event =	[SD • ~CD] + [SD • CD • PI • ~(II + JK + AB)] + [SD • CD • ~PI • (PB = II) • AB]
Where:	
•	= Logical AND
+	= Logical OR
~	= Logical NOT
SD	= Signal Detect
CD	= Clock Detect
PB	= Previous Byte
PLS	= Previous Line State
PI	= PHY Invalid = HLS + QLS + MLS + NLS + {ULS • [PLS = (ALS + ILS)]}
ILS	= Idle Line State
ALS	= Active Line State
ULS	= Unknown Line State
HLS	= Halt Line State
QLS	= Quiet Line State
MLS	= Master Line State
NLS	= Noise Line State
ULS	= Unknown Line State
I	= Idle symbol
J	= First symbol of start delimiter
K	= Second symbol of start delimiter
R	= Reset symbol
S	= Set symbol
T	= End Delimiter
A	= n + R + S + T
B	= n + R + S + T + I
n	= any data symbol

LINK ERROR MONITOR

Link Error Monitoring is accomplished in the PLAYER+ device through the Link Error Monitor Counter. The initial value of this down counter is set using the Link Error Threshold Register (LETR). A snapshot of the counter can be taken with the Current Link Error Count Register (CLECR).

A Link Error is defined as follows:

TABLE 3-6. Link Error Event Description

Link Error Event =	[ALS • (I~I + xV + Vx + H~H)] + [ALS • ~SD] + [ILS • ~(II + JK)] + [ILS • ~SD)] + [ULS • (PLS=ALS) • Link__Error__Flag • ~SB • ~(HH + HI + II + JK)]
Set Link__Error__Flag =	[ALS • (HH + NH + RH + SH + TH)]
Clear Link__Error__Flag =	[ALS • JK] + [ILS • JK] + [ULS • (PLS=ALS • Link__Error__Flag • ~SB • ~(HH + HI + II + JK)]
Where:	
~	= Logical NOT
+	= Logical OR
•	= Logical AND
ILS	= Idle Line State
ALS	= Active Line State
ULS	= Unknown Line State
x	= Any symbol
I	= Idle symbol
H	= Halt symbol
J	= First symbol of start delimiter
K	= Second symbol of start delimiter
V	= Violation symbol
R	= Reset symbol
S	= Set symbol
T	= End delimiter symbol
N	= Data symbol converted to 0000 by the PLAYER+ device Receiver Block in symbol pairs that contain a data and a control symbol
PLS	= Previous Line State
SD	= Signal Detect
SB	= Stuff Byte: Byte inserted by EB before a JK symbol pair for recentering or due to off-axis JK

3.0 Functional Description (Continued)

3.7 PHY-MAC INTERFACE

NATIONAL BYTE-WIDE CODE

The PLAYER+ device outputs the National byte-wide code from its PHY Port Indicate Output to the MAC device. Each National byte-wide code may contain data or control codes or the line state information of the connection. Table 3-7 lists all the possible outputs.

During Active Line State all data and control symbols are being repeated to the PHY Port Indicate Output with the exception of data in data-control mixture bytes. That data symbol is replaced by zero. If only one symbol in a byte is a control symbol, the data symbol will be replaced by 0000 and the whole byte will be presented as control code. Note that the Line State Detector recognizes the incoming data to be in the Active Line State upon reception of the Starting Delimiter (JK symbol pair).

During Idle Line State any non Idle symbols will be reflected as the code I′uILS. If both symbols received during Idle Line State are Idle symbols, then the Symbol Decoder generates I′kILS as its output. Note the coded Known/Unknown Bit (b3) and the Last Known Line State (b2–0). The Receive State is 4 bits long and it represents either the PHY Invalid (0011) or the Idle Line State (1011) condition. The Known/Unknown Bit shows if the symbols received match the line state information in the last 3 bits.

During any line state other than Idle Line State or Active Line State, the Symbol Decoder generates the code V′kLS if the incoming symbols match the current line state. The symbol decoder generates V′uLS if the incoming symbols do not match the current line state.

TABLE 3-7. National Byte Wide Code

Current Line State	Symbol 1		Symbol 2		National Code	
	Control Bit	Data	Control Bit	Data	Control Bit	Data
ALS	0	n	0	n	0	n-n
ALS	0	n	1	C	1	N-C
ALS	1	C	0	n	1	C-N
ALS	1	C	1	C	1	C-C
ILS	1	I	1	I	1	I′-k-LS
ILS	1	I	x	Not I	1	I′-u-LS
ILS	x	Not I	1	I	1	I′-u-LS
ILS	x	Not I	x	Not I	1	I′-u-LS
Stuff Byte during ILS	x	x	x	x	1	I′-k-ILS
Not ALS and Not ILS	1	M	1	M	1	V′-k-LS
Not ALS and Not ILS	1	M	x	Not M	1	V′-u-LS
Not ALS and Not ILS	x	Not M	1	M	1	V′-u-LS
Not ALS and Not ILS	x	Not M	x	Not M	1	V′-u-LS
Stuff Byte during Not ALS	x	x	x	x	1	V′-k-LS, V′-u-LS or L′-u-ILS
EB Overflow/Underflow					1	0011 1011
SMT__PI Connection (LSU)					1	0011 1010
Scrub Symbol Pair					1	1011 1000

Where:

n = Any data symbol in {0, 1, 2 . . . F}
C = Any control symbol in {V, R, S, T, I, H}
N = 0000 = Code for data symbol in a data control mixture byte
I = Idle Symbol
M = Any symbol that matches the current line state
I′ = 1011 = First symbols of the byte in Idle Line State
V′ = 0011 = PHY Invalid
LS = Line State
- ALS = 000
- ILS = 001
- NSD = 010
- MLS = 100
- HLS = 101
- QLS = 110
- NLS = 111

u = 1 = Indicates symbol received does not match current line state
k = 0 = Indicate symbol received matches current line state
x = Don't care

3.0 Functional Description (Continued)

National Byte-Wide Code Example

Incoming 5B Code			**Decoded 4B Code**					**National Byte-Wide Code (w/o parity)**			
98765	**43210**		**C**	**3210**	**C**	**3210**		**C**	**7654**	**3210**	
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)*
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11000	10001	(JK)	1	1101	1	1102	(JK)	1	1101	1101	(JK Symbols)
——-	——-	(xx)	0	——	0	——	(xx)	0	—–	—–	(Data Symbols)
——-	——-	(xx)	0	——	0	——	(xx)	0	—–	—–	(Data Symbols)
——-	——-	(xx)	0	——	0	——	(xx)	0	—–	—–	(Data Symbols)
(More data __)											
——-	——-	(xx)	0	—–	0	—–	(xx)	0	—–	—–	(Data Symbols)
——-	——-	(xx)	0	—–	0	—–	(xx)	0	—–	—–	(Data Symbols)
——-	——-	(xx)	0	—–	0	—–	(xx)	0	—–	—–	(Data Symbols)
01101	00111	(TR)	1	0101	1	0110	(TR)	1	0101	0110	(T and R Symbols)
00111	00111	(RR)	1	0110	1	0110	(RR)	1	0110	0110	(Two R Symbols)
11111	11111	(II)	1	1010	1	1010	(II)	1	1010	1010	(Idle Symbols)
11111	11111	(II)	1	1010	1	1010	(II)	1	1010	1010	(Idle Symbols)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	0011	0101	(V′-k-HLS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	0011	0101	(V′-k-HLS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	0011	0101	(V′-k-HLS)
11111	11111	(II)	1	1010	1	1010	(II)	1	0011	1101	(V′-u-HLS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)

*Assume the receiver is in the Idle Line State.

3.0 Functional Description (Continued)

3.8 PMD INTERFACE

The PMD Interface connects the PLAYER+ device to a standard FDDI Physical Media Connection such as a fiber optic transceiver or a copper twisted pair transceiver. It is a 125 MHz full duplex serial connection.

The DP83256 PLAYER+ device contains one PMD interface. This PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMDs.

The DP83256-AP and DP83257 PLAYER+ devices contain two PMD interfaces. The PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMDs. The second, Alternate PMD Interface can be used to support Unshielded Twisted Pair (UTP) PMDs that require external scrambling, and allows implementation with no external clock recovery or clock generation functions required. See *Figure 3-21.*

PLAYER+ TO PMD CONNECTIONS

The following figures illustrate how the PLAYER+ device can be connected to various types of PMDs.

Figure 3-20 shows how the DP83256, DP83256-AP, or DP83257 PLAYER+ device is connected to a Fiber Optic or Shielded Twisted Pair (SDDI) PMD using the Primary PMD Interface.

Figure 3-21 shows how the DP83256-AP or DP83257 PLAYER+ device is connected to an Unshielded Twisted Pair (UTP) PMD using the Alternate PMD Interface.

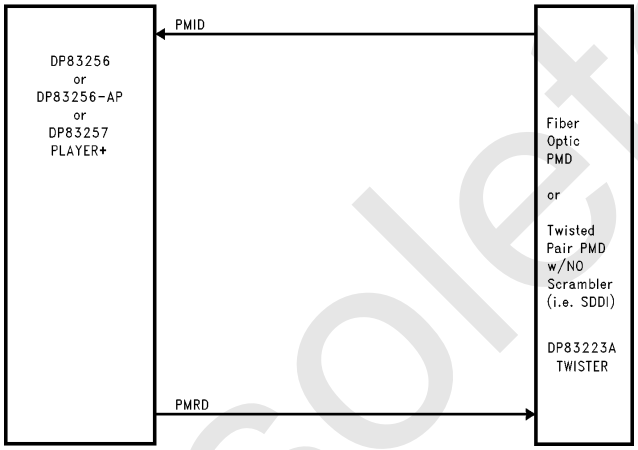

FIGURE 3-20. Fiber Optic or STP PMD Connection

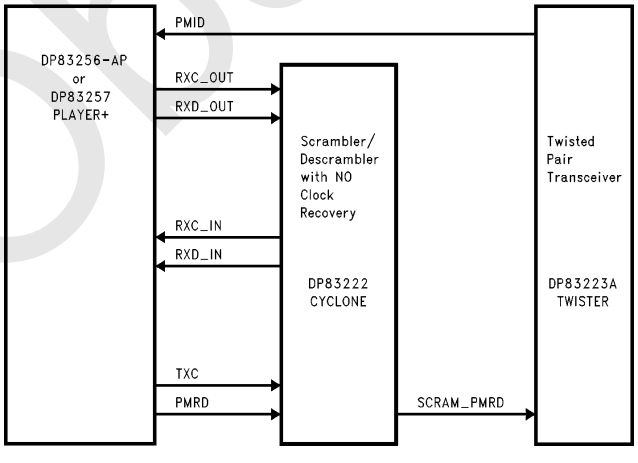

FIGURE 3-21. UTP PMD Connections

3.0 Functional Description (Continued)

INTERFACE ACTIVATION

The Primary PMD Interface is always enabled.

The Alternate PMD Interface is enabled by programming a PLAYER+ register bit. To enable the interface, write a 1 to the APMDEN bit in the APMDREG register. The interface is off by default and should be left that way unless it is being used.

It will also probably be necessary to enable the Transmit Clocks when using the Alternate PMD Interface. The Transmit Clocks (TXC) are enabled by writing a 1 to the TXCE bit in the CGMREG register. The transmit clocks are disabled by default and should be left that way unless it is being used.

Note that when the Alternate PMD Interface is active, the Primary PMD Interface can not be used without the Alternate PMD Interface connections. Also note that the Long Internal Loopback (LILB) can not be used when the Alternate PMD Interface is activated.

4.0 Modes of Operation

The PLAYER+ device can operate in 4 basic modes: RUN, STOP, LOOPBACK, and CASCADE.

4.1 RUN MODE

RUN is the normal mode of operation.

In this mode, the PLAYER+ device is configured to be connected to the media via the PMD transmitter and PMD receiver at the PMD Interface. It is also connected to any other PLAYER+ device(s) and/or MACSI device(s) via the Port A and Port B Interfaces.

While operating in the RUN mode, the PLAYER+ device receives and transmits Line States (Quiet, Halt, Master, Idle) and frames (Active LIne State).

4.2 STOP MODE

The PLAYER+ device operates in the STOP mode while it is being initialized or configured.

The PLAYER+ device is also reset to the STOP mode automatically when the ~RST pin is set to ground.

When in STOP mode, the PLAYER+ device performs the following functions:

- Resets the Repeat Filter.
- Resets the Smoother.
- Resets the Receiver Block Line State Counters.
- Resets the Clock Recovery Module
- Flushes the Elasticity Buffer.
- Forces Line State Unknown in the Receiver Block.
- Outputs PHY Invalid condition symbol pairs through the PHY Data Indicate pins (AIP, AIC, AID<7:0>, BIP, BIC, BID<7:0>), when port is enabled.
- Outputs Quiet symbol pairs through the PMD Data Request pins (PMRD±).

4.3 LOOPBACK MODE

The PLAYER+ device provides 3 types of loopback tests: Configuration Switch Loopback, Short Internal Loopback, and Long Internal Loopback. These Loopback modes can be used to test different portions of the device.

Configuration Switch Loopback

The Configuration Switch Loopback can be used to test the data paths of the MACSI device(s) that are connected to the PLAYER+ device before transmitting and receiving data through the network.

In the Configuration Switch Loopback mode, the PLAYER+ device Configuration Register (CR) can be programmed to perform the following functions:

- Select Port A PHY Request Data, Port B PHY Request Data, or PHY Invalid to connect to Port A PHY Indicate Data via the A__IND Mux.
- Select Port A PHY Request Data, Port B PHY Request Data, or PHY Invalid to connect to Port B PHY Indicate Data via the B__IND Mux.
- Connect data from the Receiver Block to the Transmitter Block via the Transmitter__Mux. (The PLAYER+ device is repeating incoming data from the media in the Configuration Switch Loopback mode.)

See *Figure 4-1* and *Figure 4-2*.

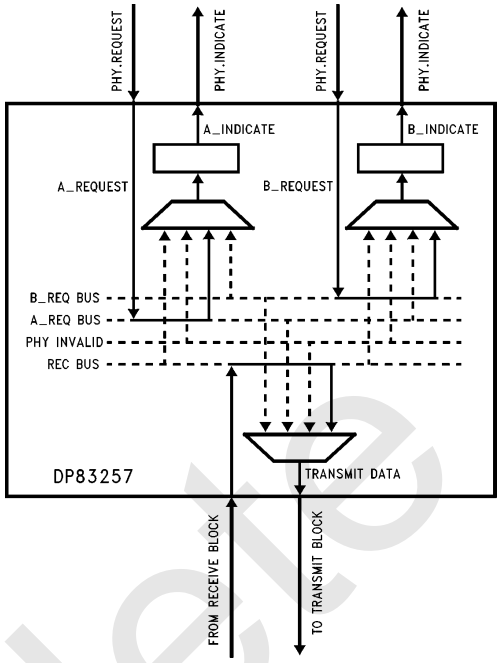

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FIGURE 4-1. Configuration Switch Loopback for DP83257

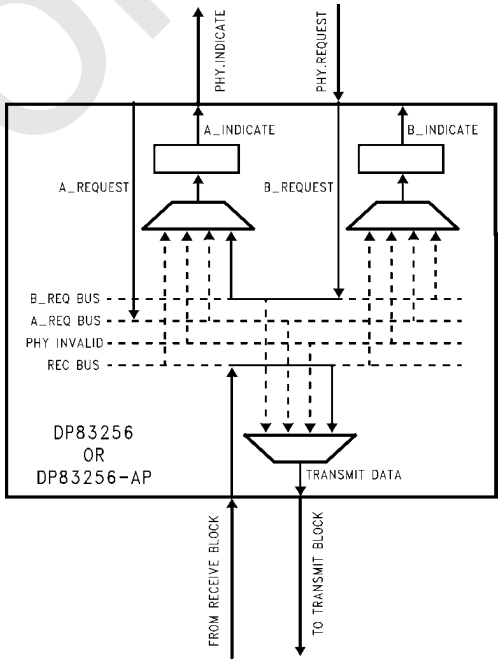

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FIGURE 4-2. Configuration Switch Loopback for DP83256 and DP 83256-AP

4.0 Modes of Operation (Continued)

Short Internal Loopback

The Short Internal Loopback mode can be used to test the functionality of the PLAYER+ device, not including the Clock Recovery function, and to test the data paths between the PLAYER+ device and MACSI devices before ring insertion.

When in the Short Internal Loopback mode, the PLAYER+ device performs the following functions:

- Directs the output data of the Transmitter Block to the input of the Receiver Block through an internal path.
- Ignores the PMD Data Indicate pins (PMID±),
- Outputs Quiet symbols through the PMD Data Request pins (PMRD±).

The level of the Quiet symbols transmitted through the PMRD± pins during loopback is automatically set to the transmitter off level.

If both Short Internal Loopback and Long Internal Loopback modes are selected, Long Internal Loopback mode will have priority over Short Internal Loopback mode. This is the longest loopback path within the PLAYER+ device.

See *Figure 4-3*, Short Internal Loopback.

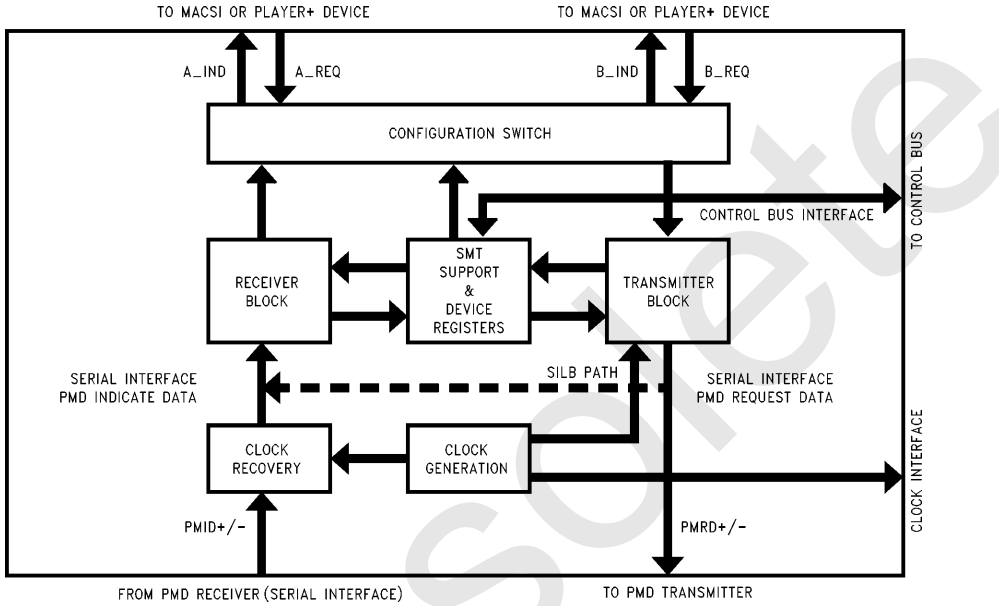

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FIGURE 4-3. Short Internal Loopback

4.0 Modes of Operation (Continued)

Long Internal Loopback

The Long Internal Loopback mode implements the longest loopback path that is completely within the PLAYER+ device.

The Long Internal Loopback mode can be used to test the functionality of the PLAYER+ device, including the Clock Recovery function, and to test the data paths between the PLAYER+ device and MACSI devices before ring insertion.

When in the Long Internal Loopback mode, the PLAYER+ device performs the following functions:

- Directs the output data of the Transmitter Block to the input of the Clock Recovery Module through an internal path.
- Ignores the PMD Data Indicate pins (PMID±),
- Outputs Quiet symbols through the PMD Data Request pins (PMRD±).

The level of the Quiet symbols transmitted through the PMRD± pins during loopback is automatically set to the transmitter off level.

If both Short Internal Loopback and Long Internal Loopback modes are selected, Long Internal Loopback mode will have priority over Short Internal Loopback mode. This is the longest loopback path within the PLAYER+ device.

Note that the LILB path is disconnected and should not be used when the Alternate PMD Interface is active.

See *Figure 4-4*, Long Internal Loopback.

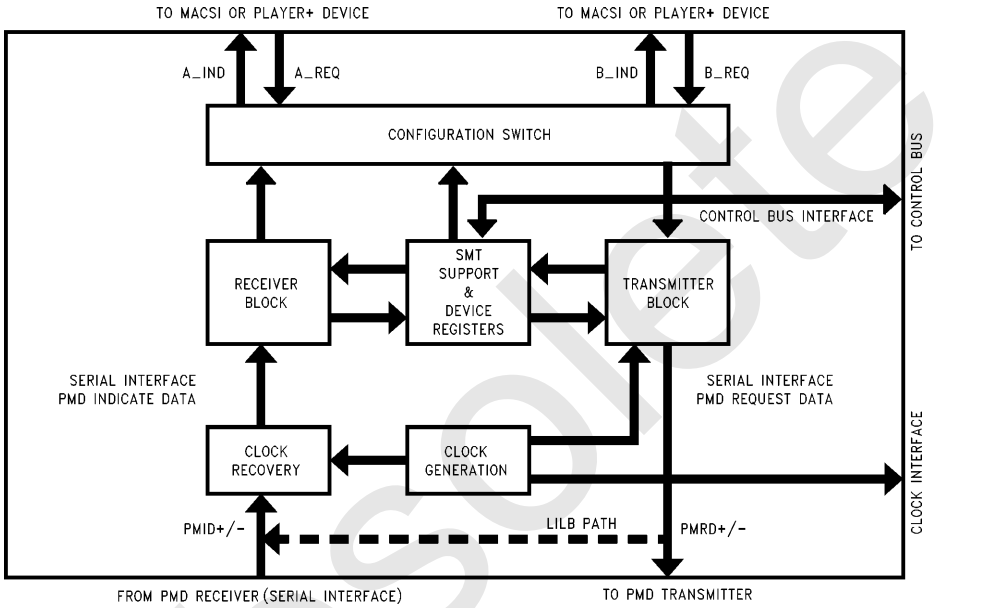

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FIGURE 4-4. Long Internal Loopback

4.0 Modes of Operation (Continued)

4.4 DEVICE RESET

The revision B PLAYER+ device has five different levels of device Reset—Power Up Reset, Hardware Reset, Player Reset, Reference Select Reset, and Stop Mode. The Resets can be used to return the whole device or a portion of the device to its default configuration.

Power Up Reset begins automatically when power is first applied to the PLAYER+ device and reaches a certain voltage level. Power Up Reset affects all of the modules in the PLAYER+ device, specifically the Clock Generation Module (CGM), Clock Recovery Module (CRM), and the Player Module, returning each module to its default configuration. This reset begins by waiting for the crystal to stabilize, then the CGM PLL proceeds to lock to the crystal and the rest of the PLAYER+ device is reset. This reset takes the longest amount of time at approximately 10 ms from the time the PLAYER+ device's power supply reaches 4.4V. Even though the Power Up Reset is usually effective, due to the variation in the start-up conditions of a systems power supply, the Power Up Reset trigger can not be guaranteed to operate correctly. Therefore, a Hardware Reset should always be performed on the PLAYER+ after waiting a minimum of 10 ms for the Power Up Reset to complete its reset attempt.

Hardware Reset occurs at the rising edge of PLAYER+ device's ~RST pin. Hardware Reset affects all of the modules in the PLAYER+ device, specifically the CGM, CRM and the Player Module, returning each module to its default configuration. During Hardware Reset it is not necessary to force the Clock Generation Module to wait for the crystal to settle again at this time because it has settled in the time since the initial reset at power up. This reset takes the second longest amount of time at approximately 1 ms from the rising edge of ~RST.

Player Reset is activated by writing a 1 to the PHYRST bit in Mode Register 2. Player Reset only affects the Player Module. This reset is the shortest and only takes about 3 μs from the completion of the register write. The device should not be accessed by the Control Bus during this reset.

Reference Select Reset occurs when the PLAYER+ device's REF__SEL pin is switched from using the REF__IN input to using a crystal with the XTAL__IN and XTAL__OUT pins. This is the same as a Power Up Reset and is done because the crystal is going from a dead stop to an active state when REF__SEL is switched. This reset, like the Power Up Reset, takes about 10 ms from the falling edge of REF__SEL.

Stop Mode is activated by writing a 0 to the RUN bit in the Mode Register. Stop Mode is a selective reset that resets the Clock Recovery Module and portions of the Player Module.

Changes from Revision A to Revision B:

The previous descriptions describe the reset logic in the revision B PLAYER+ device. Two changes were made to the original revision A PLAYER+ device reset logic.

First, the Hardware Reset was shortened by eliminating the requirement of having to wait for the crystal to settle before letting the Clock Generation Module try to lock to the crystal. This behavior is correct because the PLAYER+ device has already waited for the crystal to settle once during the Power Up Reset. The revision A PLAYER+ follows a Power Up Reset cycle when Hardware Reset is activated.

Second, a full Power Up Reset is now done when the clock reference is switched to the crystal. This is necessary to allow the crystal time to start up when it is switched to from the REF__IN input. This reset is not performed on the revision A PLAYER+.

Recommendations:

The following are some recommendations for using the reset mechanisms of the PLAYER+ most effectively:

1. Always wait a minimum of 10 ms after power-up before doing anything to the PLAYER+ device. 10 ms is a **minimum**, it may be desirable to wait **longer** if the system power supply or clock reference has not stabilized by this time.
2. Always use the Hardware Reset to reset the PLAYER+ device after Power Up. This should be done **after** the initial Power Up waiting period of **at least** 10 ms.

4.0 Modes of Operation (Continued)

4.5 CASCADE MODE

The PLAYER+ device can operate in the Cascade (parallel) mode *(Figure 4-5)* which is used in high bandwidth, point-to-point data transfer applications. This is a non-FDDI mode of operation. This is only available on the DP83257 device.

Concepts

In the Cascade mode, multiple PLAYER+ devices are connected together to provide data transfer at multiples of the FDDI data rate. Two cascaded PLAYER+ devices provide a data rate twice the FDDI data rate; three cascaded PLAYER+ devices provide a data rate three times the FDDI data rate, etc.

Multiple data streams are transmitted in parallel over each pair of cascaded PLAYER+ devices. All data streams start simultaneously and begin with the JK symbol pair on each PLAYER+ device.

Data is synchronized at the receiver of each PLAYER+ device by the JK symbol pair. Upon receiving a JK symbol pair, a PLAYER+ device asserts the Cascade Ready signal to indicate the beginning of data reception.

The Cascade Ready signals of all PLAYER+ devices are open drain ANDed together to create the Cascade Start signal. The Cascade Start signal is used as the input to indicate that all PLAYER+ devices have received the JK symbol pair. Data is now being received at every PLAYER+ device and can be transferred from the cascaded PLAYER+ devices to the host system.

See *Figure 4-6* for more information.

Operating Rules

When the PLAYER+ device is operating in Cascade mode, the following rules apply:

1. Data integrity can be guaranteed if the worst case PMD transmission skew between parallel media is less than 40 ns. For example, this amounts to about 785 meters of fiber optic cable, assuming a 1% worst case variance.
2. Even though this is a non-FDDI application, the general rules for FDDI frames must be obeyed.
   - Data frames must be a minimum of three bytes long (including the JK symbol pair). Smaller frames will cause Elasticity Buffer errors.
   - Data frames must have a maximum size of 4500 bytes, with a JK starting delimiter and a T or R or S ending delimiter.
3. Due to the different clock rates, the JK symbol pair may arrive at different times at each PLAYER+ device. The total skew between the fastest and slowest cascaded PLAYER+ devices receiving the JK starting delimiter must not exceed 80 ns.
4. The first PLAYER+ device to receive a JK symbol pair will present it to the host system and release the Cascade Ready signal. The PLAYER+ device will present one more JK as it waits for the other PLAYER+ devices to recognize their JK. The maximum number of consecutive JKs that can be presented to the host is 2.
5. The Cascade Start signal is set to 1 when all the cascaded PLAYER+ devices release their Cascade Ready signals.
6. Bit 4 (CSE) of the Receive Condition Register B (RCRB) is set to 1 if the Cascade Start signal (CS) is **not** set before the second falling edge of clock signal LBC from when Cascade Ready (CR) was released. CS has to be set approximately within 80 ns of CR release. This condition signifies that not all cascaded PLAYER+ devices have received their respective JK symbol pair with the allowed skew range.
7. PLAYER+ devices may not report a Cascaded Synchronization Error if the JK symbols are corrupted in the point-to-point links.
8. To guarantee integrity of the interframe information, the user must put at least 8 Idle symbol pairs between frames. The PLAYER+ device will function properly with only 4 Idle symbol pairs, however the interframe symbols may be corrupted with random non-JK symbols.

The MACSI device could be used to provide the required framing and optional FCS support.

4.0 Modes of Operation (Continued)

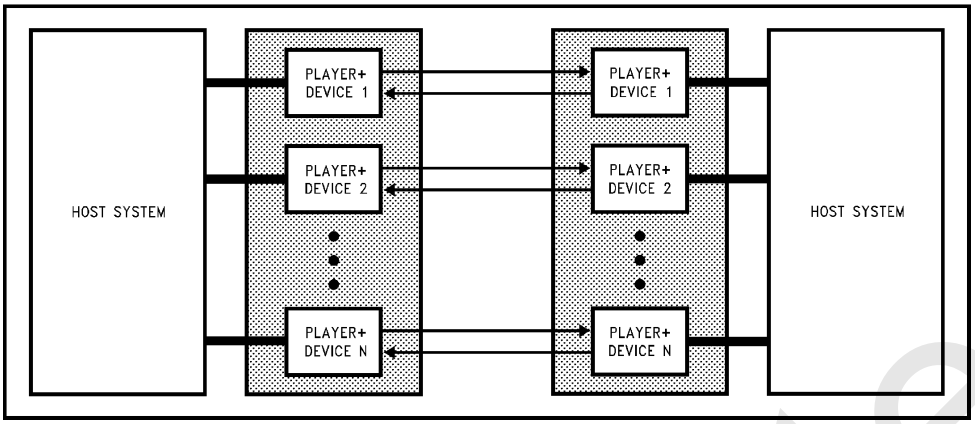

FIGURE 4-5. Parallel Transmission

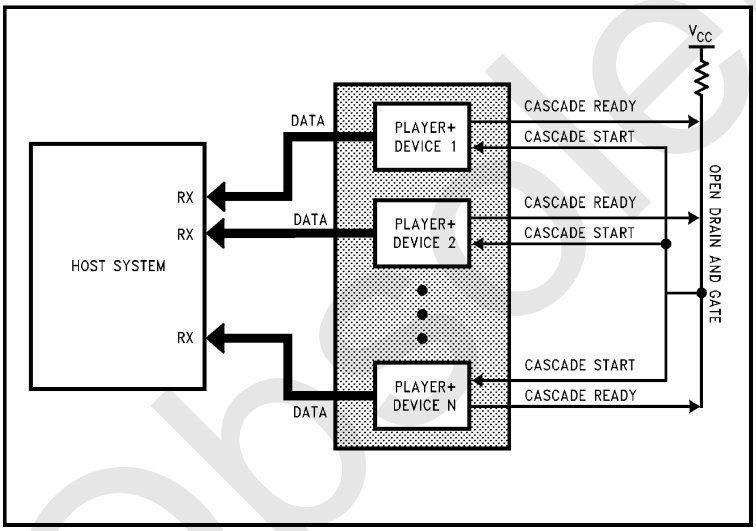

FIGURE 4-6. Cascade Mode of Operation

5.0 Registers

The PLAYER+ device can be initialized, configured, and monitored using 64 8-bit registers. These registers are accessible through the Control Bus Interface.

The following tables summarize each register's attributes.

Note: RESERVED Registers may be read at any time, although the values read are not specified. The results of RESERVED Register writes are not specified, and may have adverse implications. The user should not write to RESERVED Register locations.

TABLE 5-1. Register Summary

Register Address	Register Symbol	Register Name	Access Rules	
			Read	Write
00h	MR	Mode Register	Always	Always
01h	CR	Configuration Register	Always	Conditional
02h	ICR	Interrupt Condition Register	Always	Conditional
03h	ICMR	Interrupt Condition Mask Register	Always	Always
04h	CTSR	Current Transmit State Register	Always	Conditional
05h	IJTR	Injection Threshold Register	Always	Always
06h	ISRA	Injection Symbol Register A	Always	Always
07h	ISRB	Injection Symbol Register B	Always	Always
08h	CRSR	Current Receive State Register	Always	Write Reject
09h	RCRA	Receive Condition Register A	Always	Conditional
0Ah	RCRB	Receive Condition Register B	Always	Conditional
0Bh	RCMRA	Receive Condition Mask Register A	Always	Always
0Ch	RCMRB	Receive Condition Mask Register B	Always	Always
0Dh	NTR	Noise Threshold Register	Always	Always
0Eh	NPTR	Noise Prescale Threshold Register	Always	Always
0Fh	CNCR	Current Noise Count Register	Always	Write Reject
10h	CNPCR	Current Noise Prescale Count Register	Always	Write Reject
11h	STR	State Threshold Register	Always	Always
12h	SPTR	State Prescale Threshold Register	Always	Always
13h	CSCR	Current State Count Register	Always	Write Reject
14h	CSPCR	Current State Prescale Count Register	Always	Write Reject
15h	LETR	Link Error Threshold Register	Always	Always
16h	CLECR	Current Link Error Count Register	Always	Write Reject
17h	UDR	User Definable Register	Always	Always
18h	IDR	Device ID Register	Always	Write Reject
19h	CIJCR	Current Injection Count Register	Always	Write Reject
1Ah	ICCR	Interrupt Condition Comparison Register	Always	Always
1Bh	CTSCR	Current Transmit State Comparison Register	Always	Always
1Ch	RCCRA	Receive Condition Comparison Register A	Always	Always

5.0 Registers (Continued)

TABLE 5-1. Register Summary (Continued)

Register Address	Register Symbol	Register Name	Access Rules	
			Read	Write
1Dh	RCCRB	Receive Condition Comparison Register B	Always	Always
1Eh	MODE2	Mode Register 2	Always	Conditional
1Fh	CMTCCR	CMT Condition Comparison Register	Always	Always
20h	CMTCR	CMT Condition Register	Always	Conditional
21h	CMTMR	CMT Condition Mask Register	Always	Always
22h	RR22	Reserved Register 22	Always	DO NOT WRITE
23h	RR23	Reserved Register 23	Always	DO NOT WRITE
24h	STTR	Scrub Timer Threshold Register	Always	Always
25h	STVR	Scrub Timer Value Register	Always	Write Reject
26h	TDR	Trigger Definition Register	Always	Always
27h	TTCR	Trigger Transition Configuration Register	Always	Always
28h	RR28	Reserved Register 28	Always	DO NOT WRITE
29h	RR29	Reserved Register 29	Always	DO NOT WRITE
2Ah	RR2A	Reserved Register 2A	Always	DO NOT WRITE
2Bh	RR2B	Reserved Register 2B	Always	DO NOT WRITE
2Ch	RR2C	Reserved Register 2C	Always	DO NOT WRITE
2Dh	RR2D	Reserved Register 2D	Always	DO NOT WRITE
2Eh	RR2E	Reserved Register 2E	Always	DO NOT WRITE
2Fh	RR2F	Reserved Register 2F	Always	DO NOT WRITE
30h	RR30	Reserved Register 30	Always	DO NOT WRITE
31h	RR31	Reserved Register 31	Always	DO NOT WRITE
32h	RR32	Reserved Register 32	Always	DO NOT WRITE
33h	RR33	Reserved Register 33	Always	DO NOT WRITE
34h	RR34	Reserved Register 34	Always	DO NOT WRITE
35h	RR35	Reserved Register 35	Always	DO NOT WRITE
36h	RR36	Reserved Register 36	Always	DO NOT WRITE
37h	RR37	Reserved Register 37	Always	DO NOT WRITE
38h	RR38	Reserved Register 38	Always	DO NOT WRITE
39h	RR39	Reserved Register 39	Always	DO NOT WRITE
3Ah	RR3A	Reserved Register 3A	Always	DO NOT WRITE
3Bh	CGMREG	Clock Generation Module Register	Always	Always
3Ch	APMDREG	Alternate PMD Register	Always	Always
3Dh	GAINREG	Gain Register	Always	Always
3Eh	RR3E	Reserved Register 3E	Always	DO NOT WRITE
3Fh	RR3F	Reserved Register 3F	Always	DO NOT WRITE

5.0 Registers (Continued)

TABLE 5-2. Register Bit Summary

Register Address	Register Symbol	Bit Symbols							
		D7	D6	D5	D4	D3	D2	D1	D0
00h	MR	RNRZ	TNRZ	TE	TQL	CM	EXLB	ILB	RUN
01h	CR	BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0
02h	ICR	UDI	RCB	RCA	LEMT	CWI	CCR	CPE	DPE
03h	ICMR	UDIM	RCBM	RCAM	LEMTM	CWIM	CCRM	CPEM	DPEM
04h	CTSR	RES	PRDPE	SE	IC1	IC0	TM2	TM1	TM0
05h	IJTR	IJT7	IJT6	IIJ5	IJT4	IJT3	IJT2	IJT1	IJT0
06h	ISRA	RES	RES	RES	IJS4	IJS3	IJS2	IJS1	IJS0
07h	ISRB	RES	RES	RES	IJS9	IJS8	IJS7	IJS6	IJS5
08h	CRSR	RES	RES	RES	RES	LSU	LS2	LS1	LS0
09h	RCRA	LSUPI	LSC	NT	NLS	MLS	HLS	QLS	NSD
0Ah	RCRB	RES	SILS	EBOU	CSE	LSUPV	ALS	ST	ILS
0Bh	RCMRA	LSUPIM	LSCM	NTM	NLSM	MLSM	HLSM	QLSM	NSDM
0Ch	RCMRB	RES	SILSM	EBOUM	CSEM	LSUPVM	ALSM	STM	ILSM
0Dh	NTR	RES	NT6	NT5	NT4	NT3	NT2	NT1	NT0
0Eh	NPTR	NPT7	NPT6	NPT5	NPT4	NPT3	NPT2	NPT1	NPT0
0Fh	CNCR	NCLSCD	CNC6	CNC5	CNC4	CNC3	CNC2	CNC1	CNC0
10h	CNPCR	CNPC7	CNPC6	CNPC5	CNPC4	CNPC3	CNPC2	CNPC1	CNPC0
11h	STR	RES	ST6	ST5	ST4	ST3	ST2	ST1	ST0
12h	SPTR	SPT7	SPT6	SPT5	SPT4	SPT3	SPT2	SPT1	SPT0
13h	CSCR	SCLSCD	CSC6	CSC5	CSC4	CSC3	CSC2	CSC1	CSC0
14h	CSPCR	CSPC7	CSPC6	CSPC5	CSPC4	CSPC3	CSPC2	CSPC1	CSPC0
15h	LETR	LET7	LET6	LET5	LET4	LET3	LET2	LET1	LET0
16h	CLECR	LEC7	LEC6	LEC5	LEC4	LEC3	LEC2	LEC1	LEC0
17h	UDR	RES	RES	RES	RES	EB1	EB0	SB1	SB0
18h	IDR	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
19h	CIJCR	IJC7	IJC6	IJC5	IJC4	IJC3	IJC2	IJC1	IJC0
1Ah	ICCR	UDIC	RCBC	RCAC	LEMTC	CWIC	CCRC	CPEC	DPEC
1Bh	CTSCR	RESC	PRDPEC	SEC	IC1C	IC0C	TM2C	TM1C	TM0C
1Ch	RCCRA	LSUPIC	LSCC	NTC	NLSC	MLSC	HLSC	QLSC	NSDC
1Dh	RCCRB	RESC	SILSC	EBOUC	CSEC	LSUPVC	ALSC	STC	ILSC
1Eh	MODE2	ESTC	RES	CLKSEL	RES	RES	RES	CBPE	PHYRST
1Fh	CMTCCR	TCOC	STEC	RES	RES	RES	RES	RES	RES
20h	CMTCR	TCO	STE	RES	RES	RES	RES	RES	RES
21h	CMTMR	TCOM	STEM	RES	RES	RES	RES	RES	RES
22h	RR22	RES	RES	RES	RES	RES	RES	RES	RES

5.0 Registers (Continued)

TABLE 5-2. Register Bit Summary (Continued)

Register Address	Register Symbol	Bit Symbols							
		D7	D6	D5	D4	D3	D2	D1	D0
23h	RR23	RES	RES	RES	RES	RES	RES	RES	RES
24h	STTR	STT7	STT6	STT5	STT4	STT3	STT2	STT1	STT0
25h	STVR	STV7	STV6	STV5	STV4	STV3	STV2	STV1	STV0
26h	TDR	TONT	TOQLS	TOHLS	TOMLS	TOSILS	TTM2	TTM1	TTM0
27h	TTCR	BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0
28h	RR28	RES	RES	RES	RES	RES	RES	RES	RES
29h	RR29	RES	RES	RES	RES	RES	RES	RES	RES
2Ah	RR2A	RES	RES	RES	RES	RES	RES	RES	RES
2Bh	RR2B	RES	RES	RES	RES	RES	RES	RES	RES
2Ch	RR2C	RES	RES	RES	RES	RES	RES	RES	RES
2Dh	RR2D	RES	RES	RES	RES	RES	RES	RES	RES
2Eh	RR2E	RES	RES	RES	RES	RES	RES	RES	RES
2Fh	RR2F	RES	RES	RES	RES	RES	RES	RES	RES
30h	RR30	RES	RES	RES	RES	RES	RES	RES	RES
31h	RR31	RES	RES	RES	RES	RES	RES	RES	RES
32h	RR32	RES	RES	RES	RES	RES	RES	RES	RES
33h	RR33	RES	RES	RES	RES	RES	RES	RES	RES
34h	RR34	RES	RES	RES	RES	RES	RES	RES	RES
35h	RR35	RES	RES	RES	RES	RES	RES	RES	RES
36h	RR36	RES	RES	RES	RES	RES	RES	RES	RES
37h	RR37	RES	RES	RES	RES	RES	RES	RES	RES
38h	RR38	RES	RES	RES	RES	RES	RES	RES	RES
39h	RR39	RES	RES	RES	RES	RES	RES	RES	RES
3Ah	RR3A	RES	RES	RES	RES	RES	RES	RES	RES
3Bh	CGMREG	RES	RES	FLTREN	RES	TXCE	RES	RES	RES
3Ch	APMDREG	RES	RES	RES	RES	APMDEN	RES	RES	RES
3Dh	GAINREG	FILT2	FILT1	FILT0	RES	RES	RES	RES	RES
3Eh	RR3E	RES	RES	RES	RES	RES	RES	RES	RES
3Fh	RR3F	RES	RES	RES	RES	RES	RES	RES	RES

5.0 Registers (Continued)

TABLE 5-3. Register Reset Value Summary

Register Address	Register Symbol	Reset Contents	
		MSB-LSB	Comments
00h	MR	00 h	
01h	CR	00 h	
02h	ICR	X001 0000 B	depends on sense pins
03h	ICMR	00 h	
04h	CTSR	A2 h	
05h	IJTR	00 h	
06h	ISRA	00 h	
07h	ISRB	00 h	
08h	CRSR	0A h	
09h	RCRA	20 h	
0Ah	RCRB	00X0 0010 B	depends on EB state
0Bh	RCMRA	00 h	
0Ch	RCMRB	00 h	
0Dh	NTR	00 h	
0Eh	NPTR	00 h	
0Fh	CNCR	00 h	
10h	CNPCR	00 h	
11h	STR	00 h	
12h	SPTR	00 h	
13h	CSCR	00 h	
14h	CSPCR	00 h	
15h	LETR	00 h	
16h	CLECR	00 h	
17h	UDR	000X 00XX B	depends on sense pins
18h	IDR	XX h	depends on chip version
19h	CIJCR	00 h	
1Ah	ICCR	00 h	same as reg 02 h if reg 02 h is read first
1Bh	CTSCR	00 h	same as reg 04 h if reg 04 h is read first
1Ch	RCCRA	00 h	same as reg 09 h if reg 09 h is read first
1Dh	RCCRB	00 h	same as reg 0A h if reg 0A h is read first

5.0 Registers (Continued)

TABLE 5-3. Register Reset Value Summary (Continued)

Register Address	Register Symbol	Reset Contents	
		MSB-LSB	Comments
1Eh	MODE2	00 h	
1Fh	CMTCCR	00 h	
20h	CMTCR	00 h	
21h	CMTMR	00 h	
22h	RR22	XX h	
23h	RR23	XX h	
24h	STTR	00 h	
25h	STVR	00 h	
26h	TDR	00 h	
27h	TTCR	00 h	
28h	RR28	XX h	
29h	RR29	XX h	
2Ah	RR2A	XX h	
2Bh	RR2B	XX h	
2Ch	RR2C	XX h	
2Dh	RR2D	XX h	
2Eh	RR2E	XX h	
2Fh	RR2F	XX h	
30h	RR30	XX h	
31h	RR31	XX h	
32h	RR32	XX h	
33h	RR33	XX h	
34h	RR34	XX h	
35h	RR35	XX h	
36h	RR36	XX h	
37h	RR37	XX h	
38h	RR38	XX h	
39h	RR39	XX h	
3Ah	RR3A	XX h	
3Bh	CGMREG	05 h	
3Ch	APMDREG	00 h	
3Dh	GAINREG	00 h	
3Eh	RR3E	XX h	
3Fh	RR3F	XX h	

5.0 Registers (Continued)

5.1 MODE REGISTER (MR)

The Mode Register is used to initialize and configure the PLAYER+ device.

ACCESS RULES

ADDRESS	READ	WRITE
00h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RNRZ	TNRZ	TE	TQL	CM	LILB	SILB	RUN

Bit	Symbol	Description
D0	RUN	**RUN/~STOP:** 0: Enables the STOP mode. Refer to section 4.2, STOP MODE, for more information. 1: Normal operation (i.e. RUN mode). **Note:** The RUN bit is automatically set to 0 when the ~RST pin is asserted (i.e. set to ground).
D1	SILB	**SHORT INTERNAL LOOPBACK:** 0: Disables Internal Loopback mode (i.e. normal operation). 1: Enables Internal Loopback mode. Refer to section 4.3, LOOPBACK MODE, for more information.
D2	LILB	**LONG INTERNAL LOOPBACK:** 0: Disables Long Internal Loopback mode (i.e. normal operation). 1: Enables Long Internal Loopback mode. **Note:** Long Internal Loopback should not be used when the Alternate PMD Interface is enabled. Refer to section 4.3, LOOPBACK MODE, for more information.
D3	CM	**CASCADE MODE:** 0: Disables synchronization of cascaded PLAYER+ devices. 1: Enables the synchronization of cascaded PLAYER+ devices. Refer to section 4.4, CASCADE MODE, for more information. **Note:** Cascade Mode is only available on the DP83257 device. The other devices do not have the required CS and CR pins. Do not set this bit for any device but the DP83257.
D4	TQL	**TRANSMIT QUIET LEVEL:** This bit is used to program the transmission level of the Quiet symbols during Off Transmit mode (OTM) only. 0: Low (PMD OFF) level Quiet symbols are transmitted through the PMD Data Request pins (i.e. PMRD + = low, PMRD − = high). 1: High (PMD ON) level Quiet symbols are transmitted through the PMD Data Request pins (i.e. PMRD + = high, PMRD − = low).
D5	TE	**TRANSMIT ENABLE:** The TE bit controls the action of the PMD transmitter Enable (TXE) pin. When TE is 0, the TXE output disables the PMD transmitter; when TE is 1, the PMD transmitter is disabled during the Off Transmit Mode (OTM) and enabled otherwise. The On and Off level of the TXE is depended on the PMD transmitter Enable Level (TEL) pin to the PLAYER+ device. The following rules summaries the output of TXE. 1. If TE = 0, then TXE = Off 2. If TE = 1 and OTM, then TXE = Off 3. If TE = 1 and not OTM, then TXE = On.
D6	TNRZ	**TRANSMIT NRZ DATA:** 0: Transmits data in Non-Return-To-Zero-Invert-On-Ones (NRZI) format (normal format). 1: Transmits data in Non-Return-To-Zero format (NRZ).
D7	RNRZ	**RECEIVE NRZ DATA:** 0: Receives data in Non-Return-To-Zero-Invert-On-Ones format (NRZI) (normal format). 1: Receives data in Non-Return-To-Zero format (NRZ).

5.0 Registers (Continued)

5.2 CONFIGURATION REGISTER (CR)

The Configuration Register controls the Configuration Switch Block and enables/disables both the A and B ports. The CR can be used to create a number of Configuration Loopback paths.

The CR is conditionally writable because the TTCR can be writing a new value into the register if this feature is enabled.

Note that the A__Request and B__Indicate port are offered only on the DP83257, and not in the DP83256. For further information, refer to section 3.4, CONFIGURATION SWITCH.

ACCESS RULES

ADDRESS	READ	WRITE
01h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0

Bit	Symbol	Description
D0, D1	AIS0, AIS1	**A__INDICATE SELECTOR <0, 1>:** The A__Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the A__Indicate output port (AIP, AIC, AID<7:0>). **AIS1 AIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A__Request Bus 1 1 B__Request Bus
D2, D3	BIS0, BIS1	**B__INDICATE SELECTOR <0, 1>:** The B__Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the B__Indicate output port (BIP, BIC, BID<7:0>) **BIS1 BIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A__Request Bus 1 1 B__Request Bus **Note:** Even though this bit can be set and/or cleared in the DP83256, it will not affect any I/Os since the DP83256 does not offer a B__Indicate port.
D4, D5	TRS0, TRS1	**TRANSMIT REQUEST SELECTOR <0, 1>:** The Transmit Request Selector <0, 1> bits select one of the four Configuration Switch data buses for the input to the Transmitter Block. **TRS1 TRS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A__Request Bus 1 1 B__Request Bus **Note:** If the PLAYER+ device is in Active Transmit Mode (i.e. the Transmit Mode bits (TM<2:0>) of the Current Transmit State Register (CTSR) are set to 00) and the PHY Invalid Bus is selected, then the PLAYER+ device will transmit a maximum of four Halt symbol pairs and then continuous Idle symbols due to the Repeat Filter when in the Repeat state.
D6	AIE	**A__INDICATE ENABLE:** 0: Disables the A__Indicate output port. The A__Indicate port pins will be tri-stated when the port is disabled. 1: Enables the A__Indicate output port (AIP, AIC, AID<7:0>).
D7	BIE	**B__INDICATE ENABLE:** 0: Disables the B__Indicate output port. The B__Indicate port pins will be tri-stated when the port is disabled. 1: Enables the B__Indicate output port (BIP, BIC, BID<7:0>). **Note:** Even though this bit can be set and/or cleared in the DP83256, it will not affect any I/Os since the DP83256 does not offer a B__Indicate port.

5.0 Registers (Continued)

5.3 INTERRUPT CONDITION REGISTER (ICR)

The Interrupt Condition Register records the occurrence of an internal error event, the detection of Line State, an unsuccessful write by the Control Bus Interface, the expiration of an internal counter, or the assertion of one or more of the User Definable Sense pins.

The Interrupt Condition Register will assert the Interrupt pin (~INT) when one or more bits within the register are set to 1 and the corresponding mask bits in the Interrupt Condition Mask Register (ICMR) are also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
02h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
UDI	RCB	RCA	LEMT	CWI	CCR	CPE	DPE

Bit	Symbol	Description
D0	DPE	**PHY__REQUEST__DATA PARITY ERROR:** This bit will be set to 1 when: 1. The PHY Request Data Parity Enable bit (PRDPE) of the Current Transmit State Register (CTSR) is set to 1 and 2. The Transmitter Block detects a parity error in the incoming PHY Request Data. The source of the data can be from the PHY Invalid Bus, the Receive Bus, the A__Bus, or the B__Bus of the Configuration Switch. **Note:** Parity is only checked on data that goes into the transmitter block. This means that any data that is just routed through the configuration switch without going into the transmit block is not checked.
D1	CPE	**Control Bus DATA PARITY ERROR:** This bit will be set to 1 when the Control Bus Interface detects a parity error in the incoming Control Bus Data (CBD<7:0>), CBP during a write cycle.
D2	CCR	**Control Bus WRITE COMMAND REJECT:** This bit will be set to 1 when an attempt to write into one of the following read-only registers is made: Current Receive State Register (Register 08, CRSR) Current Noise Count Register (Register 0F, CNCR) Current Noise Prescale Count Register (Register 10, CNPCR) Current State Count Register (Register 13, CSCR) Current State Prescale Count Register (Register 14, CSPCR) Current Link Error Count Register (Register 16, CLECR) Device ID Register (Register 18, IDR) Current Injection Count Register (Register 19, CIJCR) Scrub Timer Value Register (Register 25, STVR)

5.0 Registers (Continued)

Bit	Symbol	Description
D3	CWI	**CONDITIONAL WRITE INHIBIT:** Set to 1 when bits within mentioned registers do not match bits in the corresponding compare register. This bit ensures that new (i.e. unread) data is not inadvertently cleared while old data is being cleared through the Control Bus Interface. This bit is set to 1 to indicate that a bit in a condition write register was not written because it had changed since the previous read. The following registers are affected: Interrupt Condition Register (Register 02, ICR) Current Transmit State Register (Register 04, CTSR) Receive Condition Register A (Register 09, RCRA) Receive Condition Register B (Register 0A, RCRB) CMT Condition Register (Register 20, CMTCR) The previous registers are affected when they differ from the value of the corresponding bit in the following registers respectively: Interrupt Condition Compare Register (Register 1A, ICCR) Current Transmit State Compare Register (Register 1B, CTSCR) Receive Condition Compare Register A (Register 1C, RCCRA) Receive Condition Compare Register B (Register 1D, RCCRB) CMT Condition Compare Register (Register 1F, CMTCCR) This bit must be cleared by software. Note that this differs from the MACSI, BMAC and BSI device bits of the same name. The Configuration Register (Register 01, CR) can not be written to during scrubbing.
D4	LEMT	**LINK ERROR MONITOR THRESHOLD:** This bit is set to 1 when the internal 8-bit Link Error Monitor Counter reaches zero. It will remain set and is cleared by software. During the reset process (i.e. ~RST = GND), the Link Error Monitor Threshold bit is set to 1 because the Link Error Monitor Counter is initialized to zero.
D5	RCA	**RECEIVE CONDITION A:** This bit is set to 1 when: 1. One or more bits in the Receive Condition Register A (RCRA) is set to 1 and 2. The corresponding mask bits in the Receive Condition Mask Register A (RCMRA) are also set to 1. In order to clear (i.e. set to 0) the Receive Condition A bit, the bits within the Receive Condition Register A that are set to 1 must first be either cleared or masked.
D6	RCB	**RECEIVE CONDITION B:** This bit is set to 1 when: 1. One or more bits in the Receive Condition Register B (RCRB) is set to 1 and 2. The corresponding mask bits in the Receive Condition Mask Register A (RCMRB) are also set to 1. In order to clear (i.e. set to 0) the Receive Condition B bit, the bits within the Receive Condition Register B that are set to 1 must first be either cleared or masked.
D7	UDI	**USER DEFINABLE INTERRUPT:** This bit is set to 1 when one or any combination of the Sense Bits (SB0, SB1, or SB2) in the User Definable Register (UDR) are set to 1. In order to clear (i.e. set to 0) the User Definable Interrupt Bit, all Sense Bits must be set to 0.

5.0 Registers (Continued)

5.4 INTERRUPT CONDITION MASK REGISTER (ICMR)

The Interrupt Condition Mask Register allows the user to dynamically select which events will generate an interrupt.

The Interrupt pin will be asserted (i.e. ~INT = GND) when one or more bits within the Interrupt Condition Register (ICR) are set to 1 and the corresponding mask bits in this register are also set to 1.

This register is cleared (i.e. set to 0) and all interrupts are initially masked during the reset process.

ACCESS RULES

ADDRESS	READ	WRITE
03h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
UDIM	RCBM	RCAM	LEMTM	CWIM	CCRM	CPEM	DPEM

Bit	Symbol	Description
D0	DPEM	**PHY__REQUEST__DATA PARITY ERROR MASK:** The mask bit for the PHY__Request Data Parity Error bit (DPE) of the Interrupt Condition Register (ICR).
D1	CPEM	**Control Bus DATA PARITY ERROR MASK:** The mask bit for the Control Bus Data Parity Error bit (CPE) of the Interrupt Condition Register (ICR).
D2	CCRM	**Control Bus WRITE COMMAND REJECT MASK:** The mask bit for the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR).
D3	CWIM	**CONDITIONAL WRITE INHIBIT MASK:** The mask bit for the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR).
D4	LEMTM	**LINK ERROR MONITOR THRESHOLD MASK:** The mask bit for the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR).
D5	RCAM	**RECEIVE CONDITION A MASK:** The mask bit for the Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR).
D6	RCBM	**RECEIVE CONDITION B MASK:** The mask bit for the Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR).
D7	UDIM	**USER DEFINABLE INTERRUPT MASK:** The mask bit for the User Definable Interrupt bit (UDI) of the Interrupt Condition Register (ICR).

5.0 Registers (Continued)

5.5 CURRENT TRANSMIT STATE REGISTER (CTSR)

The Current Transmit State Register can program the Transmitter Block to internally generate and transmit Idle, Master, Halt, Quiet, or user programmable symbol pairs, in addition to the normal transmission of incoming PHY Request data. The Smoother and PHY Request Data Parity are also enabled and disabled through this register.

When the Trigger Definition register (TDR) is used, the CTSR can automatically be set to a preprogrammed line state when a trigger condition occurs. This capability can be used to implement both PC__React and CF__React.

The Transmit Modes have priority over the Repeat Filter and Smoother outputs. The Injection Symbols have priority over the Transmit Modes.

During the reset process (i.e. ~RST = GND) the Transmit Mode is set to Off (TM<2:0> = 010), the Smoother is enabled (i.e. SE is set to 1), and the Reserved bit (b7) is set to 1. All other bits of this register are cleared (i.e. set to 0) during the reset process.

When the TDR register is used to respond to trigger conditions the CTSR will be blocked when the TDR register transmit mode is copied into the CTSR. The Write Reject bit of the ICR will be set if any writes are attempted at this time.

Note: This register has no effect while the device is in Stop Mode.

ACCESS RULES

ADDRESS	READ	WRITE
04h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
RES	PRDPE	SE	IC1	IC0	TM2	TM1	TM0

Bit	Symbol	Description
D0, D1, D2	TM0, TM1, TM2	**Transmit Mode <0, 1, 2>:** These bits select one of the 6 transmission modes for the PMD Request Data output port (TXD±).

TM2	TM1	TM0	
0	0	0	**Active Transmit Mode (ATM):** Normal transmission of incoming PHY Request data.
0	0	1	**Idle Transmit Mode (ITM):** Transmission of Idle symbol pairs (11111 11111).
0	1	0	**Off Transmit Mode (OTM):** Transmission of Quiet symbol pairs (00000 00000) and deassertion of the PMD transmitter Enable pin (TXE). **Note:** This is the default transmit mode after reset.
0	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).
1	0	0	**Master Transmit Mode (MTM):** Transmission of Halt and Quiet symbol pairs (00100 00000).
1	0	1	**Halt Transmit Mode (HTM):** Transmission of Halt symbol pairs (00100 00100).
1	1	0	**Quiet Transmit Mode (QTM):** Transmission of Quiet symbol pairs (00000 00000).
1	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).

5.0 Registers (Continued)

Bit	Symbol	Description
D3, D4	IC0, IC1	**Injection Control <0, 1>:** These bits select one of the 4 injection modes. The injection modes have priority over data from the Smoother, Repeat Filter, Encoder, and Transmit Modes. IC0 is the only bit of the register that is automatically cleared by the PLAYER+ device after the One Shot Injection is executed. The automatic clear of IC0 during the One Shot mode can be interpreted as a acknowledgment that the One Shot has been completed. **IC1 IC0** 0 0 **No Injection:** The normal transmission of incoming PHY Request data (i.e. symbols are not injected). 0 1 **One Shot:** In one shot mode, the contents of Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are injected n symbol pairs after a JK, where n is the programmed value of the Injection Count Register (IJCR). If IJCR is set to 0, the JK symbol pair is replaced by ISRA and ISRB. Once the One Shot is executed, the PLAYER+ device automatically sets IC0 to 0, thereby returning to normal transmission of data. 1 0 **Periodic:** In Periodic mode, the contents of Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are injected every n-th symbol pair, where n is the programmed value of the Injection Count Register (IJCR). If IJCR is set to 0, all data symbols are replaced with ISRA and ISRB. **Note:** The inserted symbol is not automatically aligned to a JK boundary. 1 1 **Continuous:** In Continuous mode, all data symbols are replaced with the contents of Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB).
D5	SE	**SMOOTHER ENABLE:** 0: Disables the Smoother. 1: Enables the Smoother. When enabled, the Smoother can redistribute Idle symbol pairs which were added or deleted by the local or upstream receivers. **Note:** Once the counter has started, it will continue to count irrespective of the incoming symbols with the exception of a JK symbol pair.
D6	PRDPE	**PHY__REQUEST DATA PARITY ENABLE:** 0: Disables PHY__Request Data parity. 1: Enables PHY__Request Data parity.
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.6 INJECTION THRESHOLD REGISTER (IJTR)

The Injection Threshold Register, in conjunction with the Injection Control bits (IC<1:0>) in the Current Transmit State Register (CTSR), set the frequency at which the contents of the Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are inserted into the data stream. It contains the start value for the Injection Counter.

The Injection Threshold Register value is loaded into the Injection Counter when the counter reaches zero or during every Control Bus Interface write-cycle of this register.

The Injection Counter is an 8-bit down-counter which decrements every 80 ns. It's current value is read for CIJCR.

The counter is active only during One Shot or Periodic Injection Modes (i.e. Injection Control<1:0> bits (IC<1:0>) of the Current Transmit State Register (CTSR) are set to either 01 or 10). The Transmitter Block will replace a data symbol pair with ISRA and ISRB when the counter reaches 0 and the Injection Mode is either One Shot or Periodic.

If the Injection Threshold Register is set to 0 during the One Shot mode, the JK will be replaced with ISRA and ISRB. If the Injection Threshold Register is set to 0 during the Periodic mode, all data symbols are replaced with ISRA and ISRB.

The counter is initialized to 0 during the reset process (i.e. ~RST=GND).

For further information, see the INJECTION CONTROL LOGIC section.

ACCESS RULES

ADDRESS	READ	WRITE
05h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
IJT7	IJT6	IJT5	IJT4	IJT3	IJT2	IJT1	IJT0

Bit	Symbol	Description
D0-D7	IJT0–IJT7	**INJECTION THRESHOLD BIT<0-7>:** Start value for the Injection Counter. IJT0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.7 INJECTION SYMBOL REGISTER A (ISRA)

The Injection Symbol Register A, along with Injection Symbol Register B, contains the programmable value (already in 5B code) that can be inserted to replace the data symbol pairs.

In One Shot mode, ISRA and ISRB are injected n bytes after a JK, where n is the programmed value of the Injection Threshold Register. In the Periodic mode, ISRA and ISRB are injected every n-th symbol pair. In the Continuous mode, all data symbols are replaced with ISRA and ISRB.

ACCESS RULES

ADDRESS	READ	WRITE
06h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	IJS4	IJS3	IJS2	IJS1	IJS0

Bit	Symbol	Description
D0–D4	IJS0–IJS4	**INJECTION SYMBOL BIT<0-4>:** Symbol to be injected. IJS0 is the Least Significant Bit (LSB) and goes out onto the media last.
D5–D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are set to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.8 INJECTION SYMBOL REGISTER B (ISRB)

The Injection Symbol Register B, along with Injection Symbol Register A, contains the programmable value (already in 5B code) that will replace the data symbol pairs.

In One Shot mode, ISRA and ISRB are injected n bytes after a JK, where n is the programmed value of the Injection Threshold Register. In the Periodic mode, ISRA and ISRB are injected every n-th symbol pair. In the Continuous mode, all data symbols are replaced with ISRA and ISRB.

ACCESS RULES

ADDRESS	READ	WRITE
07h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	IJS9	IJS8	IJS7	IJS6	IJS5

Bit	Symbol	Description
D0–D4	IJS0–IJS4	**INJECTION SYMBOL BIT<0-4>:** Symbol to be injected. IJS0 is the Least Significant Bit (LSB) and goes out onto the media last.
D5–D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are set to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.9 CURRENT RECEIVE STATE REGISTER (CRSR)

The Current Receive State Register represents the current line state being detected by the Receiver Block. When the Receiver Block recognizes a new Line State, the bits corresponding to the previous line state are cleared, and the bits corresponding to the new line state are set.

During the reset process (~RST = GND), the Receiver Block is forced to Line State Unknown (i.e. the Line State Unknown bit (LSU) is set to 1).

Note: Users are discouraged from writing to this register. An attempt to write into this register will cause the PLAYER+ device to ignore the Control Bus write cycle and set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1.

ACCESS RULES

ADDRESS	READ	WRITE
08h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	LSU	LS2	LS1	LS0

Bit	Symbol	Description
D0, D1, D2	LS0, LS1, LS2	**LINE STATE<0, 1, 2>:** These bits represent the current Line State being detected by the Receiver Block. Once the Receiver Block recognizes a new line state, the bits corresponding to the previous line state are cleared, and the bits corresponding to the new line state are set. **LS2 LS1 LS0** 0 0 0 **Active Line State (ALS):** Received a JK symbol pair (11000 10001), possibly followed by data symbols. 0 0 1 **Idle Line State (ILS):** Received a minimum of two consecutive Idle symbol pairs (11111 11111). 0 1 0 **No Signal Detect (NSD):** The Signal Detect (SD) has been deasserted, indicating that the PLAYER+ device is not receiving data from the PMD receiver or that clock detect is not being received from the Clock Recovery Module. SD is ignored during internal loopback. **Note:** NSD is the default value when the device is in Stop mode. However, while in Stop mode certain data patterns entering the Receiver Block may cause the PLAYER+ to set LS0. Therefore, the user may see either the NSD (010) or Reserved Value (011) during Stop mode. 0 1 1 **Reserved:** Reserved for future use. 1 0 0 **Master Line State (MLS):** Received a minimum of 8 consecutive Halt-Quiet symbol pairs (00100 00000). 1 0 1 **Halt Line State (HLS):** Received a minimum of 8 consecutive Halt symbol pairs (00100 00100). 1 1 0 **Quiet Line State (QLS):** Received a minimum of 8 consecutive Quiet symbol pairs (00000 00000). 1 1 1 **Noise Line State (NLS):** Detected a minimum of 16 noise events. Refer to the Receiver Block description for further information on noise events.
D3	LSU	**LINE STATE UNKNOWN:** The Receiver Block has not detected the minimum conditions to enter a known line state. When the Line State Unknown bit is set, LS<2:0> represent the most recently known line state.
D4-D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are reset to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.10 RECEIVE CONDITION REGISTER A (RCRA)

The Receive Condition Register A maintains a historical record of the Line States recognized by the Receiver Block.

When a new Line State is entered, the bit corresponding to that line state is set to 1. The bits corresponding to the previous Line States are not cleared by the PLAYER+ device, thereby maintaining a record of the Line States detected.

The Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register A is set to 1 and the corresponding mask bit(s) in Receive Condition Mask Register A (RCMRA) is also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
09h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
LSUPI	LSC	NT	NLS	MLS	HLS	QLS	NSD

Bit	Symbol	Description
D0	NSD	**NO SIGNAL DETECT:** Indicates that the Signal Detect pin (TTLSD) has been deasserted and that the Clock Recovery Module is not receiving data from the PMD receiver.
D1	QLS	**QUIET LINE STATE:** Received a minimum of eight consecutive Quiet symbol pairs (00000 00000).
D2	HLS	**HALT LINE STATE:** Received a minimum of eight consecutive Halt symbol pairs (00100 00100).
D3	MLS	**MASTER LINE STATE:** Received a minimum of eight consecutive Halt-Quiet symbol pairs (00100 00000).
D4	NLS	**NOISE LINE STATE:** Detected a minimum of sixteen noise events.
D5	NT	**NOISE THRESHOLD:** This bit is set to 1 when the internal Noise Counter reaches 0. It will remain set until a value equal to or greater than one is loaded into the Noise Threshold Register or Noise Prescale Threshold Register. During the reset process (i.e. ~RST=GND), since the Noise Counter is initialized to 0, the Noise Threshold bit will be set to 1.
D6	LSC	**LINE STATE CHANGE:** A line state change has been detected.
D7	LSUPI	**LINE STATE UNKNOWN AND PHY INVALID:** The Receiver Block has not detected the minimum conditions to enter a known line state. In addition, the most recently known line state was one of the following line states: No Signal Detect, Quiet Line State, Halt Line State, Master Line State, or Noise Line State.

5.0 Registers (Continued)

5.11 RECEIVE CONDITION REGISTER B (RCRB)

The Receive Condition Register B maintains a historical record of the Lines States recognized by the Receiver Block.

When a new Line State is entered, the bit corresponding to that line state is set to 1. The bits corresponding to the previous Line States are not cleared, thereby maintaining a record of the Line States detected.

The Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register B is set to 1 and the corresponding mask bit(s) in Receive Condition Mask Register B (RCMRB) is also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
0Ah	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
RES	SILS	EBOU	CSE	LSUPV	ALS	ST	ILS

Bit	Symbol	Description
D0	ILS	**IDLE LINE STATE:** Received a minimum of two consecutive Idle symbol pairs (11111 11111).
D1	ST	**STATE THRESHOLD:** This bit will be set to 1 when the internal State Counter reaches zero. It will remain set until a value equal to or greater than one is loaded into the State Threshold Register or State Prescale Threshold Register, and this register is cleared. During the reset process (i.e. ~RST = GND), since the State Counter is initialized to 0, the State Threshold bit is set to 1.
D2	ALS	**ACTIVE LINE STATE:** Received a JK symbol pair (11000 10001), and possibly data symbols following.
D3	LSUPV	**LINE STATE UNKNOWN AND PHY VALID:** The Receiver Block has not detected the minimum conditions to enter a known line state. In addition, the most recently known line state was either Active Line State or Idle Line State.
D4	CSE	**CONNECTION SERVICE EVENT/CASCADE SYNCHRONIZATION ERROR:** When one or more bits in the CMT Condition Register (CMTCR) are set and the corresponding bit(s) in the CMT Condition Mask Register (CMTCMR) are set, the Connection service event bit will be set to a 1. When a synchronization error occurs, the Cascade Synchronization Error bit is set to 1. A synchronization error occurs if the Cascade Start signal (CS) is not asserted within approximately 80 ns of Cascade Ready (CR) release. **Note:** Cascade mode and the CMT features can not be used at the same time. **Note:** Cascade mode is only supported on the DP83257 device.
D5	EBOU	**ELASTICITY BUFFER UNDERFLOW / OVERFLOW:** The Elasticity Buffer has either overflowed or underflowed. The Elasticity Buffer will automatically recover if the condition which caused the error is only transient, but the event bit will remain set until cleared by software.
D6	SILS	**SUPER IDLE LINE STATE:** Received a minimum of eight Idle symbol pairs (11111 11111).
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are reset to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device

5.0 Registers (Continued)

5.12 RECEIVE CONDITION MASK REGISTER A (RCMRA)

The Receive Condition Mask Register A allows the user to dynamically select which events will generate an interrupt.

The Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register A (RCRA) is set to 1 and the corresponding mask bit(s) in this register is also set to 1.

Since this register is cleared (i.e. set to 0) during the reset process, all interrupts are initially masked.

ACCESS RULES

ADDRESS	READ	WRITE
0Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LSUPIM	LSCM	NTM	NLSM	MLSM	HLSM	QLSM	NSDM

Bit	Symbol	Description
D0	NSDM	**NO SIGNAL DETECT MASK:** The mask bit for the No Signal Detect bit (NSD) of the Receive Condition Register A (RCRA).
D1	QLSM	**QUIET LINE STATE MASK:** The mask bit for the Quiet Line State bit (QLS) of the Receive Condition Register A (RCRA).
D2	HLSM	**HALT LINE STATE MASK:** The mask bit for the Halt Line State bit (HLS) of the Receive Condition Register A (RCRA).
D3	MLSM	**MASTER LINE STATE MASK:** The mask bit for the Master Line State bit (MLS) of the Receive Condition Register A (RCRA).
D4	NLSM	**NOISE LINE STATE MASK:** The mask bit for the Noise Line State bit (NLS) of the Receive Condition Register A (RCRA).
D5	NTM	**NOISE THRESHOLD MASK:** The mask bit for the Noise Threshold bit (NT) of the Receive Condition Register A (RCRA).
D6	LSCM	**LINE STATE CHANGE MASK:** The mask bit for the Line State Change bit (LSC) of the Receive Condition Register A (RCRA).
D7	LSUPIM	**LINE STATE UNKNOWN AND PHY INVALID MASK:** The mask bit for the Line State Unknown and PHY Invalid bit (LSUPI) of the Receive Condition Register A (RCRA).

5.0 Registers (Continued)

5.13 RECEIVE CONDITION MASK REGISTER B (RCMRB)

The Receive Condition Mask Register B allows the user to dynamically select which events will generate an interrupt.

The Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register B (RCRA) is set to 1 and the corresponding mask bits in this register is also set to 1.

Since this register is cleared (i.e. set to 0) during the reset process, all interrupts are initially masked.

ACCESS RULES

ADDRESS	READ	WRITE
0Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESM	SILSM	EBOUM	CSEM	LSUPVM	ALSM	STM	ILSM

Bit	Symbol	Description
D0	ILSM	**IDLE LINE STATE MASK:** The mask bit for the Idle Line State bit (ILS) of the Receive Condition Register B (RCRB).
D1	STM	**STATE THRESHOLD MASK:** The mask bit for the State Threshold bit (ST) of the Receive Condition Register B (RCRB).
D2	ALSM	**ACTIVE LINE STATE MASK:** The mask bit for the Active Line State bit (ALS) of the Receive Condition Register B (RCRB).
D3	LSUPVM	**LINE STATE UNKNOWN AND PHY VALID MASK:** The mask bit for the Line State Unknown and PHY Valid bit (LSUPV) of the Receive Condition Register B (RCRB).
D4	CSEM	**CASCADE SYNCHRONIZATION ERROR MASK/CONNECTION SERVICE EVENT MASK:** The mask bit for the Cascade Synchronization Error/Connection service event bit (CSE) of the Receive Condition Register B (RCRB).
D5	EBOUM	**ELASTICITY BUFFER OVERFLOW/UNDERFLOW MASK:** The mask bit for the Elasticity Buffer Overflow/ Underflow bit (EBOU) of the Receive Condition Register B (RCRB).
D6	SILSM	**SUPER IDLE LINE STATE MASK:** The mask bit for the Super Idle Line State bit (SILS) of the Receive Condition Register B (RCRB).
D7	RESM	**RESERVED MASK:** The mask bit for the Reserved bit (RES) of the Receive Condition Register B (RCRB).

5.0 Registers (Continued)

5.14 NOISE THRESHOLD REGISTER (NTR)

The Noise Threshold Register contains the start value for the Noise Timer. This threshold register is used in conjunction with the Noise Prescale Threshold register for setting the maximum allowable time between entry to ILS, HLS, MLS, ALS, or NSD line states. The Noise timer is used to implement the TNE timing requirement of PCM. The Noise timer decrements by one for every 80 x (NPTR + 1) ns in case of Noise events. As a result, the internal noise counter takes the following amount of time to reach zero:

$$((NPTR + 1) \times NTR + NPTR) \times 80 \text{ ns}$$

The threshold values for the Noise Counter and Noise Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

1. Both the Noise Counter and Noise Prescale Counter reach zero and the current Line State is either Noise Line State, Active Line State, or Line State Unknown.

or

2. The current Line State is either Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

3. The Noise Threshold Register or Noise Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the Noise Prescale Threshold register is loaded into the Noise Prescale Counter if the Noise Prescale Counter reaches zero.

The Noise Counter and Noise Prescale Counter will continue to count, without resetting or reloading the threshold values, if a Line State change occurs and the new line state is either Noise Line State, Active Line State, or Line State Unknown.

When both the Noise Threshold Counter and Noise Counter both reach zero, the Noise Threshold bit of the Receive Condition Register A will be set.

The recommended default value for the NTR register is 40h and for the NPTR register is F9h which corresponds to 1.3 ms as specified in the ANSI standard.

ACCESS RULES

ADDRESS	READ	WRITE
0Dh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	NT6	NT5	NT4	NT3	NT2	NT1	NT0

Bit	Symbol	Description
D0-D6	NT0-NT6	**NOISE THRESHOLD BIT<0-6>:** Start value for the Noise Counter. NT0 is the Least Significant Bit (LSB).
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. Write data is ignored since the reserved bit is permanently set to 0.

5.0 Registers (Continued)

5.15 NOISE PRESCALE THRESHOLD REGISTER (NPTR)

The Noise Prescale Threshold Register contains the start value for the Noise Prescale Timer. This threshold register is used in conjunction with the Noise Threshold register for setting the maximum allowable time between entry to ILS, HLS, MLS, ALS, or NSD. The Noise timer is used to implement the TNE timing requirement of PCM. The Noise Prescale threshold controls how often the Noise timer is decremented. When the Noise Prescale Timer reaches zero, it reloads the count with the contents of the Noise Prescale Threshold Register and also causes the Noise Timer to decrement.

The threshold values for the Noise Counter and Noise Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

1. Both the Noise Counter and Noise Prescale Counter reach zero and the current Line State is either Noise Line State, Active Line State, or Line State Unknown.

or

2. The Current Line State is either Halt Line State. Idle Line State, Master Line State, Quiet Line State, or No Signal Detect

or

3. The Noise Threshold Register or Noise Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the Noise Prescale Threshold Register is loaded into the Noise Prescale Counter if the Noise Prescale Counter reaches zero.

The Noise Counter and Noise Prescale Counter will continue to count, without resetting or reloading the threshold values, if a Line State change occurs and the new line state is either Noise Line State, Active Line State, or Line State Unknown.

When both the Noise Threshold Counter and Noise Counter both reach zero, the Noise Threshold bit of the Receive Condition Register A will be set.

See the NTR register description for default value recommendations.

ACCESS RULES

ADDRESS	READ	WRITE
0Eh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
NPT7	NPT6	NPT5	NPT4	NPT3	NPT2	NPT1	NPT0

Bit	Symbol	Description
D0-D7	NPT0-NPT7	**NOISE PRESCALE THRESHOLD BIT <0-7>:** Start value for the Noise Prescale Timer. NPT0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.16 CURRENT NOISE COUNT REGISTER (CNCR)

The Current Noise Count Register takes a snap-shot of the Noise Timer during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
0Fh	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
NCLSCD	CNC6	CNC5	CNC4	CNC3	CNC2	CNC1	CNC0

Bit	Symbol	Description
D0–D6	CNC0–CNC6	**CURRENT NOISE COUNT BIT <0–6>:** Snapshot of the Noise Counter.
D7	NCLSCD	**NOISE COUNTER LINE STATE CHANGE DETECTION**

5.0 Registers (Continued)

5.17 CURRENT NOISE PRESCALE COUNT REGISTER (CNPCR)

The Current Noise Prescale Count Register takes a snap-shot of the Noise Prescale Timer during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
10h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
CNPC7	CNPC6	CNPC5	CNPC4	CNPC3	CNPC2	CNPC1	CNPC0

Bit	Symbol	Description
D0–D7	CNPC0–7	**CURRENT NOISE PRESCALE COUNT BIT <0–7>:** Snapshot of the Noise Prescale Timer.

5.0 Registers (Continued)

5.18 STATE THRESHOLD REGISTER (STR)

The State Threshold Register contains the start value for the State Timer. This timer is used in conjunction with the State Prescale Timer to count the Line State duration. The State Timer will decrement every 80 ns if the State Prescale Timer is zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect. The State Timer takes

$$((SPTR + 1) \times STR + SPTR) \times 80 \text{ ns}$$

to reach zero during a continuous line state condition.

The threshold values for the State Timer and State Prescale Timer are simultaneously loaded into both counters if one of the following conditions is true:

1. Both the State Timer and State Prescale Timer reach zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

2. A line state change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

3. The State Threshold Register or State Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the State Prescale Threshold Register is loaded into the State Prescale Counter if the State Prescale Timer reaches zero.

The State Timer and State Prescale Timer will reset by reloading the threshold values, if a Line State change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect. On detection of ALS, NLS, or LSU the timer will not decrement.

ACCESS RULES

ADDRESS	READ	WRITE
11h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	ST6	ST5	ST4	ST3	ST2	ST1	ST0

Bit	Symbol	Description
D0-D6	ST0-ST6	**STATE THRESHOLD BIT<0-6>:** Start value for the State Timer. ST0 is the Least Significant Bit (LSB).
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. Write data is ignored since the reserved bit is permanently set to 0.

5.0 Registers (Continued)

5.19 STATE PRESCALE THRESHOLD REGISTER (SPTR)

The State Prescale Threshold Register contains the start value for the State Prescale Timer. The State Prescale Timer is a down counter. It is used in conjunction with the State Timer to count the Line State duration.

The threshold values for the State Timer and State Prescale Timer are simultaneously loaded into both timers if one of the following conditions is true:

1. Both the State Timer and State Prescale Timer reach zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

2. A Line State change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

3. The State Threshold Register or State Prescale Threshold Register goes through a Control Bus Interface write cycle.

The State Prescale Timer will decrement every 80 ns if the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

ACCESS RULES

ADDRESS	READ	WRITE
12h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
SPT7	SPT6	SPT5	SPT4	SPT3	SPT2	SPT1	SPT0

Bit	Symbol	Description
D0–D7	SPT0–SPT7	**STATE PRESCALE THRESHOLD BIT <0–7>:** Start value for the State Prescale Timer. SPT0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.20 CURRENT STATE COUNT REGISTER (CSCR)

The Current State Count Register takes a snap-shot of the State Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
13h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
SCLSCD	CSC6	CSC5	CSC4	CSC3	CSC2	CSC1	CSC0

Bit	Symbol	Description
D0–D6	CSC0–CSC6	**CURRENT STATE COUNT BIT <0–6>:** Snapshot of the State Counter.
D7	SCLSCD	**STATE COUNTER LINE STATE CHANGE DETECTION**

5.0 Registers (Continued)

5.21 CURRENT STATE PRESCALE COUNT REGISTER (CSPCR)

The Current State Prescale Count Register takes a snap-shot of the State Prescale Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
14h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
CSPC7	CSPC6	CSPC5	CSPC4	CSPC3	CSPC2	CSPC1	CSPC0

Bit	Symbol	Description
D0–D7	CSPC0–7	**CURRENT STATE PRESCALE COUNT <0–7>:** Snapshot of the State Prescale Counter.

5.0 Registers (Continued)

5.22 LINK ERROR THRESHOLD REGISTER (LETR)

The Link Error Threshold Register contains the start value for the Link Error Monitor Counter. It is an 8-bit down-counter which decrements if link errors are detected.

When the Counter reaches 0, the Link Error Monitor Threshold Register value is loaded into the Link Error Monitor Counter and the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR) is set to one.

The Link Error Monitor Threshold Register value is also loaded into the Link Error Monitor Counter during every Control Bus Interface write cycle of LETR.

The counter is initialized to 0 during the reset process (i.e. ~RST = GND).

ACCESS RULES

ADDRESS	READ	WRITE
15h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LET7	LET6	LET5	LET4	LET3	LET2	LET1	LET0

Bit	Symbol	Description
D0–D7	LET0–LET7	**LINK ERROR THRESHOLD BIT <0–7>:** Start value for the Link Error Monitor Counter. LET0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.23 CURRENT LINK ERROR COUNT REGISTER (CLECR)

The Current Link Error Count Register takes a snap-shot of the Link Error Monitor Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
16h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
LEC7	LEC6	LEC5	LEC4	LEC3	LEC2	LEC1	LEC0

Bit	Symbol	Description
D0–D7	LEC0–LEC7	**LINK ERROR COUNT BIT <0–7>:** Snapshot of the Link Error Monitor Counter.

5.0 Registers (Continued)

5.24 USER DEFINABLE REGISTER (UDR)

The User Definable Register is used to monitor and control events which are external to the PLAYER+ device.

The value of the Sense Bits reflect the asserted/deasserted state of their corresponding Sense pins. On the other hand, the Enable bits assert/deassert the Enable pins.

Note: SB2 and EB2 are only effective for the DP83257.

ACCESS RULES

ADDRESS	READ	WRITE
17h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	EB2	RES	SB2	EB1	EB0	SB1	SB0

Bit	Symbol	Description
D0	SB0	**SENSE BIT 0:** This bit is set to 1 if the Sense Pin 0 (SP0) is asserted (i.e. SP0 = V_{CC}) for a minimum amount of time. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner.
D1	SB1	**SENSE BIT 1:** This bit is set to 1 if the Sense Pin 1 (SP1) is asserted (i.e. SP1 = V_{CC}) for a minimum amount of time. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner.
D2	EB0	**ENABLE BIT 0:** The Enable Bit 0 allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 0 (EP0) is asserted/deasserted by this bit. 0: EP0 is deasserted (i.e. EP0 = GND). 1: EP0 is asserted (i.e. EP0 = V_{CC}).
D3	EB1	**ENABLE BIT 1:** This bit allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 0 (EP0) is asserted/deasserted by this bit. 0: EP1 is deasserted (i.e. EP1 = GND). 1: EP1 is asserted (i.e. EP1 = V_{CC}).
D4	SB2	**SENSE BIT 2:** This bit is set to 1 if the Sense Pin 2 (SP2) is asserted (i.e. SP2 = V_{CC}) for a minimum amount of time. Once the asserted signal is latched, Sense Bit 2 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner. **Note:** SB2 and EB2 are only effective for the DP83257.
D5	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0 during the initialization process (i.e. ~RST = GND). **Note:** Users are discouraged from using this bit. It may be set or cleared without any effects to the functionality of the PLAYER+ device.
D6	EB2	**ENABLE BIT2:** The Enable Bit 2 allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 2 (EP2) is asserted/deasserted by this bit. **Note:** SB2 and EB2 are only effective for the DP83257. 0: EP2 is deasserted (i.e. EP2 = GND). 1: EP2 is asserted (i.e. EP2 = V_{CC}).
D7	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0 during the initialization process (i.e. ~RST = GND). **Note:** Users are discouraged from using this bit. It may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.25 DEVICE ID REGISTER (IDR)

The Device ID Register contains the binary equivalent of the revision number for this device. It can be used to ensure proper software and hardware versions are matched.

During a Control Bus Interface write cycle, the Control Bus Write Command Register bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1, and will ignore write cycle.

REVISION TABLE

IDR (hex)	DEVICE DESCRIPTION
10	PLAYER+ Revision A
11	PLAYER+ Revision B

ACCESS RULES

ADDRESS	READ	WRITE
18h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

Bit	Symbol	Description
D0–D3	DID0–DID3	**DEVICE ID BIT <0-3>:** Circuit enhancement revision number. Bit 3 is the MSB. The initial revision of the PLAYER+ is equal to 0 and enhancements will increment this number.
D4–D7	DID4–DID7	**DEVICE ID BIT <4-7>:** Architecture level of the PHY device. Bit 7 is the MSB. The original PLAYER device was equal to 0 and the PLAYER+ is equal to 1. This number will only be incremented after a significant architectural change.

5.0 Registers (Continued)

5.26 CURRENT INJECTION COUNT REGISTER (CIJCR)

The Current Injection Count Register takes a snap-shot of the Injection Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

The Injection Counter is an 8-bit down-counter which decrements every 80 ns.

The counter is active only during One Shot or Periodic Injection Modes (i.e. Injection Control<1:0> bits (IC<1:0>) of the Current Transmit State Register (CTSR) are set to either 01 or 10).

The Injection Threshold Register (IJTR) value is loaded into the Injection Counter when the counter reaches zero and during every Control Bus Interface write cycle of IJTR.

The counter is initialized to 0 during the reset process (i.e. ~RST=GND).

ACCESS RULES

ADDRESS	READ	WRITE
19h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
IJC7	IJC6	IJC5	IJC4	IJC3	IJC2	IJC1	IJC0

Bit	Symbol	Description
D0–D7	IJC0–IJC7	**INJECTION COUNT BIT<0-7>:** Current value of the Injection Counter. IJC0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.27 INTERRUPT CONDITION COMPARISON REGISTER (ICCR)

The Interrupt Condition Comparison Register ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of the Interrupt Condition Register (ICR) is automatically written into the Interrupt Condition Comparison Register (i.e. ICCR = ICR) during a Control Bus Interface read-cycle of ICR.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and disallow the setting or clearing of a bit within ICR when the value of a bit in ICR differs from the value of the corresponding bit in the interrupt Condition Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Ah	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
UDIC	RCBC	RCAC	LEMTC	CWIC	CCRC	CPEC	DPEC

Bit	Symbol	Description
D0	DPEC	**PHY__REQUEST DATA PARITY ERROR COMPARISON:** The comparison bit for the PHY__Request Data Parity Error bit (DPE) of the Interrupt Condition Register (ICR).
D1	CPEC	**CONTROL BUS DATA PARITY ERROR COMPARISON:** The comparison bit for the Control Bus Data Parity Error bit (CPE) of the Interrupt Condition Register (ICR).
D2	CCRC	**CONTROL BUS WRITE COMMAND REJECT COMPARISON:** The comparison bit for the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR).
D3	CWIC	**CONDITIONAL WRITE INHIBIT COMPARISON:** The comparison bit for the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR).
D4	LEMTC	**LINK ERROR MONITOR THRESHOLD COMPARISON:** The comparison bit for the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR).
D5	RCAC	**RECEIVE CONDITION A COMPARISON:** The comparison bit for the Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR).
D6	RCBC	**RECEIVE CONDITION B COMPARISON:** The comparison bit for the Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR).
D7	UDIC	**USER DEFINABLE INTERRUPT COMPARISON:** The comparison bit for the User Definable Interrupt bit (UDIC) of the Interrupt Condition Register (ICR).

5.0 Registers (Continued)

5.28 CURRENT TRANSMIT STATE COMPARISON REGISTER (CTSCR)

The Current Transmit State Comparison Register ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of the Current Transmit State Register (CTSR) is automatically written into the Current Transmit State Comparison Register A (i.e. CTSCR = CTSR) during a Control Bus Interface read cycle of CTSR.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and disallow the setting or clearing of a bit within the CTSR when the value of a bit in the CTSR differs from the value of the corresponding bit in the Current Transmit State Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESC	PRDPEC	SEC	IC1C	IC0C	TM2C	TM1C	TM0C

Bit	Symbol	Description
D0	TM0C	**TRANSMIT MODE <0> COMPARISON:** The comparison bit for the Transmit Mode <0> bit (TM0) of the Current Transmit State Register (CTSR).
D1	TM1C	**TRANSMIT MODE <1> COMPARISON:** The comparison bit for the Transmit Mode <1> bit (TM1) of the Current Transmit State Register (CTSR).
D2	TM2C	**TRANSMIT MODE <2> COMPARISON:** The comparison bit for the Transmit Mode <2> bit (TM2) of the Current Transmit State Register (CTSR).
D3	IC0C	**INJECTION CONTROL <0> COMPARISON:** The comparison bit for the Injection Control <0> bit (IC0) of the Current Transmit State Register (CTSR).
D4	IC1C	**INJECTION CONTROL <1> COMPARISON:** The comparison bit for the Injection Control <1> bit (IC1) of the Current Transmit State Register (CTSR).
D5	SEC	**SMOOTHER ENABLE COMPARISON:** The comparison bit for the Smoother Enable bit (SE) of the Current Transmit State Register (CTSR).
D6	PRDPEC	**PHY__REQUEST DATA PARITY ENABLE COMPARISON:** The comparison bit for the PHY__Request Data Parity Enable bit (PRDPE) of the Current Transmit State Register (CTSR).
D7	RESC	**RESERVED COMPARISON:** The comparison bit for the Reserved bit (RES) of the Current Transmit State Register (CTSR).

5.0 Registers (Continued)

5.29 RECEIVE CONDITION COMPARISON REGISTER A (RCCRA)

The Receive Condition Comparison Register A ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of RCRA is automatically written into the Receive Condition Comparison Register A (i.e. RCCRA = RCRA) during a Control Bus Interface read cycle of RCRA.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and prevent the setting or clearing of a bit within RCRA when the value of a bit in RCRA differs from the value of the corresponding bit in the Receive Condition Comparison Register A.

ACCESS RULES

ADDRESS	READ	WRITE
1Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LSUPIC	LSCC	NTC	NLSC	MLSC	HLSC	QLSC	NSDC

Bit	Symbol	Description
D0	NSDC	**NO SIGNAL DETECT COMPARISON:** The comparison bit for the No Signal Detect bit (NSD) of the Receive Condition Register A (RCRA).
D1	QLSC	**QUIET LINE STATE COMPARISON:** The comparison bit for the Quiet Line State bit (QLS) of the Receive Condition Register A (RCRA).
D2	HLSC	**HALT LINE STATE COMPARISON:** The comparison bit for the Halt Line State bit (HLS) of the Receive Condition Register A (RCRA).
D3	MLSC	**MASTER LINE STATE COMPARISON:** The comparison bit for the Master Line State bit (MLS) of the Receive Condition Register A (RCRA).
D4	NLSC	**NOISE LINE STATE COMPARISON:** The comparison bit for the Noise Line State bit (NLS) of the Receive Condition Register A (RCRA).
D5	NTC	**NOISE THRESHOLD COMPARISON:** The comparison bit for the Noise Threshold bit (NT) of the Receive Condition Register A (RCRA).
D6	LSCC	**LINE STATE CHANGE COMPARISON:** The comparison bit for the Line State Change bit (LSC) of the Receive Condition Register A (RCRA).
D7	LSUPIC	**LINE STATE UNKNOWN AND PHY INVALID COMPARISON:** The comparison bit for the Line State Unknown and PHY Invalid bit (LSUPI) of the Receive Condition Register A (RCRA).

5.0 Registers (Continued)

5.30 RECEIVE CONDITION COMPARISION REGISTER B (RCCRB)

The Receive Condition Comparison Register B ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of RCRB is automatically written into the Receive Condition Comparison Register B (i.e. RCCRB = RCRB) during a Control Bus Interface read cycle RCRB.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and prevent the setting or clearing of a bit within RCRB when the value of a bit in RCRB differs from the value of the corresponding bit in the Receive Condition Comparison Register B.

ACCESS RULES

ADDRESS	READ	WRITE
1Dh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESC	SILSC	EBOUC	CSEC	LSUPVC	ALSC	STC	ILSC

Bit	Symbol	Description
D0	ILSC	**IDLE LINE STATE COMPARISON:** The comparison bit for the Idle Line State bit (ILS) of the Receive Condition Register B (RCRB).
D1	STC	**STATE THRESHOLD COMPARISON:** The comparison bit for the State Threshold bit (ST) of the Receive Condition Register B (RCRB).
D2	ALSC	**ACTIVE LINE STATE COMPARISON:** The comparison bit for the Active Line State bit (ALS) of the Receive Condition Register B (RCRB).
D3	LSUPVC	**LINE STATE UNKNOWN AND PHY VALID COMPARISON:** The comparison bit for the Line State Unknown and PHY Valid bit (LSUPV) of the Receive Condition Register B (RCRB).
D4	CSEC	**CONNECTION SERVICE EVENT COMPARISON / CASCADE SYNCHRONIZATION ERROR:** The comparison bit for the Cascade Synchronization Error/Connection Service Event bit (CSE) of the Receive Condition Register B (RCRB).
D5	EBOUC	**ELASTICITY BUFFER OVERFLOW / UNDERFLOW COMPARISON:** The comparison bit for the Elasticity Buffer Overflow/Underflow bit (EBOU) of the Receive Condition Register B (RCRB).
D6	SILSC	**SUPER IDLE LINE STATE COMPARISON:** The comparison bit for the Super Idle Line State bit (SILS) of the Receive Condition Register B (RCRB).
D7	RESC	**RESERVED COMPARISON:** The comparison bit for the Reserved bit (RES) of the Receive Condition Register B (RCRB).

5.0 Registers (Continued)

5.31 MODE REGISTER 2 (MODE2)

The Mode Register 2 (MODE2) is used to configure the PLAYER+ device.

The register is used to software reset the chip, setup data parity, and enable scrubbing functions.

Note: This register can not be written to during reset.

ACCESS RULES

ADDRESS	READ	WRITE
1Eh	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
ESTC	RES	CLKSEL	RES	RES	RES	CBPE	PHYRST

Bit	Symbol	Description
D0	PHYRST	**PLAYER RESET:** This bit can be used as a master software reset of the PLAYER function within the PLAYER+ device. The clock distribution and recovery sections of the chip are not affected by this reset. The PLAYER+ automatically clears this bit 32 byte time after its assertion to indicate that the reset action has been completed. This bit can be set through a C-Bus write, but can only be cleared by the PLAYER+.
D1	CBPE	**C-Bus Parity Enable:** This bit disables or enables parity checking on C-Bus data. When this bit is set to 0, no parity checking is done. When the bit is set to 1, parity checking is enabled during a C-Bus write cycle. Should a mismatch occur, the C-Bus Data Parity Error (ICR.CPE) bit will be set and the corresponding C-Bus access is discarded. C-Bus data parity is always generated during a C-Bus read cycle.
D2–D4	RES	**RESERVED:** Reserved for future use.
D5	CLKSEL	**CLOCK SELECT:** This bit controls the frequency of the CLK16 output. It resets to 0 which sets the CLK16 output to a 15.625 MHz frequency. When set to 1 a 31.25 MHz frequency is generated. **Note:** When the value of this bit is changed, no glitches appear on the CLK16 output due to the frequency change.
D6	RES	**RESERVED:** Reserved for future use.
D7	ESTC	**ENABLE SCRUBBING on TRIGGER CONDITIONS:** When ESTC is set to 1 and a Trigger Condition occurs (as set in the TDR register), the Trigger Transition Configuration Register (TTCR) is loaded into the Configuration Register (CR) and scrubbing is started on all indicate ports that have changed. Scrubbing is accomplished by sending out 2 Phy__Invalid symbols followed by ''scrub''symbol pairs for a time defined by the Scrub Timer Threshold register.

5.0 Registers (Continued)

5.32 CMT CONDITION COMPARISON REGISTER (CMTCCR)

The CMT Condition Comparison Register (CMTCR) ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of the CMT Condition Register (CMTCR) is automatically written into the CMT Condition Comparison Register (CMTCR) (i.e. CMTCCR = CMTCR) during a Control Bus Interface read-cycle of CMTCR.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Control Register (ICR) to 1 and disallow the setting or clearing of a bit within the CMTCR when the value of a bit in the CMTCR differs from the value of the corresponding bit in the CMT Condition Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Fh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
TCOC	STEC	RES	RES	RES	RES	RES	RES

Bit	Symbol	Description
D0-D5	RES	**RESERVED:** Reserved for future use.
D6	STEC	**SCRUB TIMER EXPIRED COMPARISON:** The comparison bit for the Scrub Timer Expire bit (STE) of the CMT Condition Register (CMTCR).
D7	TCOC	**TRIGGER CONDITION OCCURRED COMPARISON:** The comparison bit for the Trigger Condition Occurred (TCO) bit of the CMT Condition Register (CMTCR).

5.0 Registers (Continued)

5.33 CMT CONDITION REGISTER (CMTCR)

The CMT Condition Register maintains a history of all CMT events and actions performed. The corresponding CMT Condition Mask Register (CMTCMR) can be used to generate an interrupt. When the bits in both the CMTCMR and CMTCR are set, the Receive Condition Register B's Connection Service Event (RCRB.CSE) bit will be set.

ACCESS RULES

ADDRESS	READ	WRITE
20h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
TCO	STE	RES	RES	RES	RES	RES	RES

Bit	Symbol	Description
D0-D5	RES	**RESERVED:** Reserved for future use.
D6	STE	**SCRUB TIMER EXPIRED:** This bit is set to 1 when the Scrub Timer expires. **Note:** When STE is set, the Configuration Register (CR) is protected.
D7	TCO	**TRIGGER CONDITION OCCURRED:** This bit is set to 1 when a trigger condition is met. When a trigger occurs, the values in the Trigger Transmit Mode (TDR.TTM2-0) are loaded into the Current Transmit Mode Register (CTSR.TM2-0). **Note:** When TCO is set, the Current Transmit State Register (CTSR) is protected.

5.0 Registers (Continued)

5.34 CMT CONDITION MASK REGISTER (CMTCMR)

This is the mask register for the CMT Condition Register (CMTCR). When the bits in both the CMTCMR and CMTCR are set, the Receive Condition Register B's Connection Service Event (RCRB.CSE) bit will be set.

ACCESS RULES

ADDRESS	READ	WRITE
21h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
TCOM	STEM	RES	RES	RES	RES	RES	RES

Bit	Symbol	Description
D0-D5	RES	**RESERVED:** Reserved for future use.
D6	STEM	**SCRUB TIMER EXPIRED MASK:** The mask bit for the Scrub Timer Expired (STE) bit of the CMT Condition Register (CMTCR).
D7	TCOM	**TRIGGER CONDITION OCCURRED MASK:** The mask bit for the Trigger Condition Occurred (TCO) bit of the CMT Condition Register (CMTCR).

5.0 Registers (Continued)

5.35 RESERVED REGISTERS 22H–23H (RR22H–RR23H)

This register is reserved for future use.

DO NOT ACCESS THIS REGISTER

ACCESS RULES

ADDRESS	READ	WRITE
22h–23h	Always	DO NOT WRITE

5.0 Registers (Continued)

5.36 SCRUB TIMER THRESHOLD REGISTER (STTR)

This is the threshold value of the internal scrub timer. It has a resolution of 40.96 μs and a maximum value of ~10 ms. When the scrub timer reaches zero, the Scrub Timer Expired (CMTCR.STE) bit is set.

Scrubbing is initiated when MODE2.ESTC = 1 and a trigger condition occurs.

Writing to STTR during scrubbing will not affect the scrubbing action.

ACCESS RULES

ADDRESS	READ	WRITE
24h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
STT7	STT6	STT5	STT4	STT3	STT2	STT1	STT0

Bit	Symbol	Description
D0–D7	STT0–STT7	**SCRUB TIMER THRESHOLD BIT <0-7>:** Scrub Timer threshold. STT0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.37 SCRUB TIMER VALUE REGISTER (STVR)

This is a snap-shot of the current value of the upper 8 bits of the scrub timer.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
25h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
STV7	STV6	STV5	STV4	STV3	STV2	STV1	STV0

Bit	Symbol	Description
D0–D7	STV0–STV7	**SCRUB TIMER VALUE BIT<0-7>:** Snap-shot of the scrub timer. STV0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.38 TRIGGER DEFINITION REGISTER (TDR)

This register determines which events cause a trigger transition and which transmit mode is entered when a trigger transition is detected. The trigger transmit modes are the same as those found in the Current Transmit State Register (CTSR), and are loaded from the TDR into the CTSR when any of the selected trigger conditions occur. When a trigger condition occurs CMTCR.TCO is set.

The Trigger Definition Register is useful to implement the strict PC__React time requirement.

ACCESS RULES

ADDRESS	READ	WRITE
26h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
TONT	TOQLS	TOHLS	TOMLS	TOSILS	TTM2	TTM1	TTM0

Bit	Symbol	Description
D0, D1, D2	TTM0, TTM1, TTM2	**TRIGGER TRANSMIT MODE <0, 1, 2>:** These bits select one of 6 transmission modes to be loaded into the Current Transmit State Register (CTSR) when a trigger condition is detected. The trigger condition is selected by the upper 5 bits of this register.
D3	TOSILS	**TRIGGER ON SILS:** Trigger when SILS is received.
D4	TOMLS	**TRIGGER ON MLS:** Trigger when MLS is received.
D5	TOHLS	**TRIGGER ON HLS:** Trigger when HLS is received.
D6	TOQLS	**TRIGGER ON QLS (or NSD):** Trigger when QLS is received.
D7	TONT	**TRIGGER ON Noise Threshold:** Trigger when Noise Threshold is reached (Current Noise Register = 0).

TTM2	TTM1	TTM0	
0	0	0	**Active Transmit Mode (ATM):** Normal transmission of incoming PHY Request data.
0	0	1	**Idle Transmit Mode (ITM):** Transmission of Idle symbol pairs (11111 11111).
0	1	0	**Off Transmit Mode (OTM):** Transmission of Quiet symbol pairs (00000 00000) and deassertion of the PMD transmitter Enable pin (TXE).
0	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).
1	0	0	**Master Transmit Mode (MTM):** Transmission of Halt and Quiet symbol pairs (00100 00000).
1	0	1	**Halt Transmit Mode (HTM):** Transmission of Halt symbol pairs (00100 00100).
1	1	0	**Quiet Transmit Mode (QTM):** Transmission of Quiet symbol pairs (00000 00000).
1	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).

5.0 Registers (Continued)

5.39 TRIGGER TRANSITION CONFIGURATION REGISTER (TTCR)

The Trigger Transition Configuration Register holds the configuration switch setting to be loaded into the Configuration Register (CR) when a trigger transition takes place. When scrubbing is enabled, scrubbing is performed for a period of time indicated by the Scrub Timer Threshold Register (STTR).The register bit descriptions for the Configuration Register and, therefore, the Trigger Transition Configuration Register are reprinted below.

ACCESS RULES

ADDRESS	READ	WRITE
27h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0

Bit	Symbol	Description
D0, D1	AIS0, AIS1	**A__INDICATE SELECTOR <0, 1>:** The A__Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the A__Indicate output port (AIP, AIC, AID<7:0>). **AIS1 AIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A__Request Bus 1 1 B__Request Bus
D2, D3	BIS0, BIS1	**B__INDICATE SELECTOR <0, 1>:** The B__Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the B__Indicate output port (BIP, BIC, BID<7:0>). **BIS1 BIS0** 0 0 PHY Invalid Bus 0 1 Receiver 1 0 A__Request Bus 1 1 B__Request Bus **Note:** Even though this bit can be set and/or cleared in the DP83256 (for single path stations), it will not affect any I/Os since the DP83256 does not offer a B__Indicate port.
D4, D5	TRS0, TRS1	**TRANSMIT REQUEST SELECTOR <0, 1>:** The Transmit Request Selector <0, 1> bits selects one of the four Configuration Switch data buses for the input to the Transmitter Block. **TRS1 TRS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A__Request Bus 1 1 B__Request Bus **Note:** If the PLAYER+ device is in Active Transmit Mode (i.e. the Transmit Mode bits (TM<2:0>) of the Current Transmit State Register (CTSR) are set to 00) and the PHY Invalid Bus is selected, then the PLAYER+ device will transmit continuous Idle symbols due to the Repeat Filter.
D6	AIE	**A__INDICATE ENABLE:** 0: Disables the A__Indicate output port. The A__Indicate port pins will be tri-stated when the port is disabled. 1: Enables the A__Indicate output port (AIP, AIC, AID<7:0>).
D7	BIE	**B__INDICATE ENABLE:** 0: Disables the B__Indicate output port. The B__Indicate port pins will be tri-stated when the port is disabled. 1: Enables the B__Indicate output port (BIP, BIC, BID<7:0>). **Note:** Even though this bit can be set and/or cleared in the DP83256 (for single path stations), it will not affect any I/Os since the DP83256 does not offer a B__Indicate port.

5.0 Registers (Continued)

5.40 RESERVED REGISTERS 28H-3AH (RR28H-RR3AH)

These registers are reserved for future use.

DO NOT ACCESS THESE REGISTERS

ACCESS RULES

ADDRESS	READ	WRITE
28h–3Ah	Always	DO NOT WRITE

5.0 Registers (Continued)

5.41 CLOCK GENERATION MODULE REGISTER (CGMREG)

This register is used to enable or disable the 125 MHz ECL Transmit clock outputs. These outputs are not required for use in a standard FDDI board implementation and are disabled by default to reduce high frequency noise.

These TXC outputs are included for support of alternate FDDI PMDs, such as unshielded twisted pair copper cable.

DO NOT WRITE TO RESERVED REGISTER BITS. Writes to reserved register bits could prevent proper device operation. Therefore, read the register first, and then write it back with the non-reserved bits set to the desired value.

ACCESS RULES

ADDRESS	READ	WRITE
3Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	FLTREN	RES	TXCE	RES	RES	RES

Bit	Symbol	Description
D0-D2	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.
D3	TXCE	**TRANSMIT CLOCK ENABLE:** When bit is set to 1, 125 MHz ECL TXC outputs are enabled. When this bit is reset to 0, TXC outputs are disabled. TXC outputs are disabled on reset. **Note:** TXC clocks are only available on the 160-pin DP83257 PLAYER+ device.
D4	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.
D5	FLTREN	**FILTER ENABLE:** When bit is set to 1, the internal loop filter node is connected to the LPFLTR pin for diagnostic viewing. This bit is reset to 0 by default, which disconnects the filter node from the LPFLTR pin. **Note:** In normal operation this bit should be disabled (=0).
D6-D7	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.

5.0 Registers (Continued)

5.42 ALTERNATE PMD REGISTER (APMDREG)

This register is used to enable or disable the Alternate PMD inputs and ouputs. These signals are not required for use in FDDI board implementations that do not require a scrambler that is external to the PLAYER+ device. The actual interface consists of the signal pairs RXC__OUT, RXD__OUT, RXC__IN, and RXD__IN.

The interface is disabled by default and should only be enabled if it is being used. Note that Long Internal Loopback should not be used when the Alternate PMD Interface is enabled.

DO NOT WRITE TO RESERVED REGISTER BITS. Writes to reserved register bits could prevent proper device operation. Therefore, read the register first, and then write it back with the non-reserved bits set to the desired value.

Note: The Alternate PMD Interface pins are only available on the 100-pin DP83256-AP and 160-pin DP83257 PLAYER+ devices. The Alternate PMD Interface is disabled on reset.

ACCESS RULES

ADDRESS	READ	WRITE
3Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	APMDEN	RES	RES	RES

Bit	Symbol	Description
D0–D2	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.
D3	APMDEN	**ALTERNATE PMD ENABLE:** When bit is set to 1, the Alternate PMD Interface is enabled. When this bit is reset to 0, the Alternate PMD Interface is disabled. The Alternate PMD Interface consists of the following extra ECL signal pairs RXC__OUT, RXD__OUT, RXC__IN, and RXD__IN. In some alternate PMD implementations it may also be necessary to use the 125 MHz Transmit Clock signals (TXC). The TXC outputs must be separately enabled by the TXCE bit in the CGMREG register. **Note:** The Alternate PMD Interface pins are only available on the 100-pin DP83256-AP and 160-pin DP83257 PLAYER+ devices. The Alternate PMD Interface is disabled on reset.
D4–D7	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.

5.0 Registers (Continued)

5.43 GAIN REGISTER (GAINREG)

The Gain Register contains the settings for the CGM's on-chip programmable loop filter. For optimal jitter performance on the revision A and B PLAYER+ device's Filter Position 4 should be used. The user should check that the IDR register is equal to revision A or B (10h or 11h) before changing the filter setting as later revisions will default to the correct setting which may be a different filter position number.

Pseudo Code Programming Example:

Care must be taken when changing the settings of the on-chip programmable loop filter. The filter should only be set to the recommended value and the additional bits in the Gain Register must not be altered. Alteration of the reserved bits in the Gain Register may result in improper PLAYER+ device operation.

The following pseudo code outlines the proper procedure for setting the Gain Register loop filter settings to the correct value.

```
// Register names and constants are all in UPPERCASE
//
//
#define REV_B 0x11
#define REV_A 0x10
#define LOOP_MASK 0x1F
#define NEW_LOOP 0x40

if (IDR <= REV_B) {
          temp = GAIN_REG
          temp = temp & LOOP_MASK
          temp = temp | NEW_LOOP
          GAIN_REG = temp
}
else {Do Nothing}
```

ACCESS RULES

ADDRESS	READ	WRITE
3Dh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
FILT2	FILT1	FILT0	RES	RES	RES	RES	RES

Bit	Symbol	Description
D0–D4	RES	**RESERVED:** Do not alter these bits. The device may cease to operate properly if these bits are changed.
D5–D7	FILT0, FILT1, FILT2	**FILTER SELECTION <0, 1, 2>:** The Filter Selection <0, 1, 2> bits select one of five on-chip CGM loop filters. **Note:** Filter combinations that are not specified or recommended should not be used and may result in non-optimal device performance. FILT2 FILT1 FILT0 1 1 0 FP0: Filter Position 0. 1 1 1 FP1: Filter Position 1. 0 0 0 FP2: Filter Position 2. This is the filter selected after reset on the revision A and B PLAYER+ devices. 0 0 1 FP3: Filter Position 3. 0 1 0 FP4: Filter Position 4. This is the recommended filter position for the revision A and B PLAYER+ devices.

5.0 Registers (Continued)

5.44 RESERVED REGISTERS 3EH-3FH (RR3EH-RR3FH)

These registers are reserved for future use.

DO NOT ACCESS THESE REGISTERS

ACCESS RULES

ADDRESS	READ	WRITE
3Eh–3Fh	Always	DO NOT WRITE

6.0 Signal Descriptions

6.1 DP83256VF PIN DESCRIPTIONS

The pin descriptions for the DP83256VF are divided into 5 functional interfaces: PMD Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and Miscellaneous Interface.

For a Pinout Summary list, refer to Table 8-1 and *Figure 8-1*, DP83256VF 100-Pin JEDEC Metric PQFP Pinout.

PMD INTERFACE

The PMD Interface consists of I/O signals used to connect the PLAYER+ device to the Physical Medium Dependant (PMD) sublayer.

Symbol	Pin #	I/O	Description
PMID+ PMID−	39 38	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD receiver.
PMRD+ PMRD−	33 32	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
SD+ SD−	37 36	I	**Signal Detect:** Differential 100k ECL input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.
TEL	47	I	**PMD Transmitter Enable Level:** A TTL input signal to select the PMD transmitter Enable (TXE) signal level.
TXE	46	O	**PMD Transmitter Enable:** A TTL output signal to enable/disable the PMD transmitter. The output level of the TXE pin is determined by three parameters: the Transmit Enable (TE) bit in the Mode Register, the TM2-TM0 bits in the Current Transmit State Register, and the input to the TEL pin. The following rules summarize the output of the TXE pin: 1. If TE = 0 and TEL = GND, then TXE = V_{CC} 2. If TE = 0 and TEL = V_{CC}, then TXE = GND 3. If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} 4. If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND 5. If TE = 1 and not OTM and TEL = GND, then TXE = GND 6. If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

6.0 Signal Descriptions (Continued)

PHY PORT INTERFACE

The PHY Port Interface consists of I/O signals used to connect the PLAYER+ device to the Media Access Control (MAC) sublayer or other PLAYER+ device. The DP83256 Device has two PHY Port Interfaces. The A__Indicate path from one PHY Port Interface and the B__Request path from the second PHY Port Interface. Each path consists of an odd parity bit, a control bit, and two 4-bit symbols.

Refer to section 3.3, the Configuration Switch, for more information.

Symbol	Pin #	I/O	Description
AIP	6	O	**PHY Port A Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (AIP, AIC, and AID<7:0>).
AIC	7	O	**PHY Port A Indicate Control:** TTL output signal indicating that the two 4-bit symbols (AID<7:4> and AID<3:0>) are either control symbols (AIC=1) or data symbols (AIC=0).
AID7 AID6 AID5 AID4	8 9 10 13	O	**PHY Port A Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. AID7 is the most significant bit and AID4 is the least significant bit of the first symbol.
AID3 AID2 AID1 AID0	14 15 16 17	O	**PHY Port A Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. AID3 is the most significant bit and AID0 is the least significant bit of the second symbol.
BRP	70	I	**PHY Port B Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (BRP, BRC, and BRD<7:0>).
BRC	69	I	**PHY Port B Request Control:** A TTL input signal indicating that the two 4-bit symbols (BRD<7:4> and BRD<3:0>) are either control symbols (BRC=1) or data symbols (BRC=0).
BRD7 BRD6 BRD5 BRD4	68 67 66 63	I	**PHY Port B Request Data:** TTL input signals representing the first 4-bit data/control symbol. BRD7 is the most significant bit and BRD4 is the least significant bit of the first symbol.
BRD3 BRD2 BRD1 BRD0	62 61 60 59	I	**PHY Port B Request Data:** TTL input signals representing the second 4-bit data/control symbol. BRD3 is the most significant bit and BRD0 is the least significant bit of the second symbol.

6.0 Signal Descriptions (Continued)

CONTROL BUS INTERFACE

The Control Bus Interface consists of I/O signals used to connect the PLAYER+ device to Station Management (SMT).

The Control Bus is an asynchronous interface between the PLAYER+ device and a general purpose microprocessor or other controller. It provides access to 64 8-bit internal registers.

In the PLAYER+ device the Control Bus address range has been expanded by 1-bit to 6 bits of address space.

Symbol	Pin #	I/O	Description
~CE	73	I	**Control Enable:** An active-low, TTL, input signal which enables the Control Bus port for a read or write cycle. R/~W, CBA<5:0>, CBP, and CBD<7:0> must be valid at the time ~CE is low.
R/~W	72	I	**Read/~Write:** A TTL input signal which indicates a read Control Bus cycle(R/~W=1), or a write Control Bus cycle (R/~W=0).
~ACK	75	O	~**Acknowledge:** An active low, TTL, open drain output signal which indicates the completion of a read or write cycle. During a read cycle, CBD<7:0> are valid as long as ~ACK is low (~ACK=0). During a write cycle, a microprocessor must hold CBD<7:0> valid until ~ACK becomes low. Once ~ACK is low, it will remain low as long as ~CE remains low (~CE=0).
~INT	74	O	~**Interrupt:** An active low, open drain, TTL, output signal indicating that an interrupt condition has occurred. The Interrupt Condition Register (ICR) should be read in order to find out the source of the interrupt. Interrupts can be masked through the use of the Interrupt Condition Mask Register (ICMR).
CBA5 CBA4 CBA3 CBA2 CBA1 CBA0	83 82 81 80 77 76	I	**Control Bus Address:** TTL input signals used to select the address of the register to be read or written. CBA5 is the most significant bit (MSB) and CBA0 is the least significant bit (LSB) of the address signals.
CBP	96	I/O	**Control Bus Parity:** A bidirectional, TTL signal representing odd parity for the Control Bus data (CBD<7:0>). During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low. If incorrect parity is used during a write cycle, the PLAYER+ device will inhibit the write cycle and set the Control Bus Data Parity Error (CPE) bit in the Interrupt Condition Register (ICR).
CBD7 CBD6 CBD5 CBD4 CBD3 CBD2 CBD1 CBD0	95 94 93 92 91 90 89 86	I/O	**Control Bus Data:** Bidirectional, TTL signals containing the data to be read from or written to a register. During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low.

6.0 Signal Descriptions (Continued)

CLOCK INTERFACE

The Clock Interface consists of 12.5 MHz and 25 MHz clocks supplied by the PLAYER+ device as well as reference and feedback inputs.

Symbol	Pin #	I/O	Description
LBC1 LBC2 LBC3 LBC4 LBC5	4 3 2 1 100	O	**Local Byte Clock:** TTL compatible, 12.5 MHz, 50% duty cycle clock outputs which are phase locked to a crystal oscillator or reference signal. The PH__SEL input determines whether the five phase outputs are phase offset by 8 ns or 16 ns.
PH__SEL	22	I	**Phase Select:** TTL compatible input used to select either a 8 ns or 16 ns phase offset between the 5 local byte clocks (LBC's). The LBC's are phase offset 8ns apart when PH__SEL is at a logic LOW level and 16 ns apart when at a logic HI level.
FBK__IN	25	I	**Feedback Input:** TTL compatible input for use as the PLL's phase comparator feedback input to close the Phase Locked Loop. This input is intended to be driven from one of the Local Byte Clocks (LBC's) from the same PLAYER+ device.
LSC	99	O	**Local Symbol Clock:** TTL compatible 25 MHz output for driving the MACSI or BMAC devices. This output's negative phase transition is aligned with the LBC1 output transitions and has a 40% HI and 60% LOW duty cycle.
CLK16	5	O	**Clock 16/32:** TTL compatible clock with a selectable frequency of approximately 15.625 MHz or 31.25 MHz. The frequency can be selected using the Clock Select (CLKSEL) bit of the Mode 2 Register (MODE2). **Note:** No glitches appear at the output when switching frequencies.
XTAL__IN	27	I	**External Crystal Oscillator Input:** This input in conjunction with the XTAL__OUT output, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*. This input is selected when the REF__SEL input is at a logic LOW level. When not being used, this input should be tied to ground.
XTAL__OUT	26	O	**External Crystal Oscillator Output:** This output in conjunction with the XTAL__IN input, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*.
REF__IN	24	I	**Reference Input:** TTL compatible input for use as the PLL's phase comparator reference frequency. This input is for use in dual attach station or concentrator configurations where there are multiple PLAYER+ devices at a given site requiring synchronization. This input is selected when the REF__SEL input is at a logic HI level.
REF__SEL	23	I	**Reference Select:** TTL compatible input which selects either the crystal oscillator inputs XTAL__IN and XTAL__OUT or the REF__IN inputs as the reference frequency inputs for the PLL. The crystal oscillator inputs are selected when REF__SEL is at a logic LOW level and the REF__IN input is selected as the reference when REF__SEL is at a logic HI level.
LPFLTR	30	O	**Loop Filter:** This is a diagnostic output that allows monitoring of the clock generation module's filter node. This output is disabled by default and does not need to be connected to any external device. It can be enabled using the FLTREN bit of the Clock generation module register (CGMREG). **Note:** In normal operation this pin should be disabled.

6.0 Signal Descriptions (Continued)

MISCELLANEOUS INTERFACE

The Miscellaneous Interface consist of a reset signal, user definable sense signals, and user definable enable signals.

Symbol	Pin #	I/O	Description
~RST	71	I	**Reset:** An active low, TTL, input signal which clears all registers. The signal must be kept asserted for a minimum amount of time. Once the ~RST signal is asserted, the PLAYER+ device should be allowed the specified amount of time to reset internal logic. Note that bit zero of the Mode Register will be set to zero (i.e. Stop Mode). See section 4.2, Stop Mode of Operation for more information
SP0	40	I	**User Definable Sense Pin 0:** A TTL input signal from a user defined source. Sense Bit 0 (SB0) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP1	42	I	**User Definable Sense Pin 1:** A TTL input signal from a user defined source. Sense Bit 1 (SB1) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
EP0	41	O	**User Definable Enable Pin 0:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP0 is asserted/deasserted through Enable Bit 0 (EB0) of the User Definable Register (UDR). When Enable Bit 0 is set to zero, EP0 is deasserted. When Enable Bit 0 is set to one, EP0 is asserted.
EP1	43	O	**User Definable Enable Pin 1:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP1 is asserted/deasserted through Enable Bit 1 (EB1) of the User Definable Register (UDR). When Enable Bit 1 is set to zero, EP1 is deasserted. When Enable Bit 1 is set to one, EP1 is asserted.

6.0 Signal Descriptions (Continued)

POWER AND GROUND

All power pins should be connected to a single +5V power supply using the recommended filtering. All ground pins should be connected to a common 0V ground supply. Bypassing and filtering requirements are given in a separate User Information Document.

Symbol	Pin #	I/O	Description
V_{CC}__ANALOG	20		**Power:** Positive 5V power supply for the PLAYER+ device's CGM VCO.
GND__ANALOG	21		**Ground:** Power supply return for the PLAYER+ device's CGM VCO.
V_{CC}__CORE	88		**Power:** Positive 5V power supply for the core PLAYER section logic gates.
GND__CORE	87		**Ground:** Power supply return for the core PLAYER section logic gates.
V_{CC}__ECL	31, 34, 44, 56		**Power:** Positive 5V power supply for the PLAYER+ device's ECL logic gates.
GND__ECL	35, 45, 55		**Ground:** Power supply return for the PLAYER+ device's ECL logic gates.
V_{CC}__ESD	28		**Power:** Positive 5V power supply for the PLAYER+ device's ESD protection circuitry.
GND__ESD	29		**Ground:** Power supply return for the PLAYER+ device's ESD protection circuitry.
V_{CC}__IO	11, 65, 79, 98		**Power:** Positive 5V power supply for the input/output buffers.
GND__IO	12, 64, 78, 97		**Ground:** Power supply return for the input/output buffers.

SPECIAL CONNECT PINS

These are pins that have special connection requirements.

No Connect (N/C) pins should not be connected to anything. This means not to power, not to ground, and not to each other.

Reserved__0 (RES__0) pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Reserved__1 (RES__1) pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Symbol	Pin #	I/O	Description
N/C	49, 54		**No Connect:** Pins should not be connected to anything. This means not to power, not to ground, and not to each other.
RES__0	18, 19, 48, 50, 51, 52, 53, 57, 58, 84		**Reserved 0:** Pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.
RES__1	85		**Reserved 1:** Pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

6.0 Signal Descriptions (Continued)

6.2 DP83256VF-AP SIGNAL DESCRIPTIONS

The pin descriptions for the DP83256VF-AP are divided into five functional interfaces; PMD Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and Miscellaneous Interface.

For a Pinout Summary List, refer to Table 8-2 and *Figure 8-2*, DP83256VF-AP 100-Pin JEDEC Metric PQFP Pinout.

PMD INTERFACE

The PMD Interface consists of I/O signals used to connect the PLAYER+ device to the Physical Medium Dependant (PMD) sublayer.

The DP83256VF-AP PLAYER+ device actually has two PMD interfaces. The Primary PMD Interface and the Alternate PMD Interface.

The Primary PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMD. The second, Alternate PMD Interface can be used to support Unshielded Twisted Pair (UTP) PMDs that require external scrambling, with no external clock recovery or clock generation functions required.

Section 3.8 describes how the PLAYER+ can be connected to the PMD and how the Alternate PMD can be enabled.

Note that when the Alternate PMD Interface is not being used, the pins that make up the interface must be connected in the specific way described in the following Alternate PMD Interface table.

Primary PMD Interface

Symbol	Pin #	I/O	Description
PMID+ PMID−	42 41	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD Receiver into the Clock Recovery Module (CRM) of the PLAYER+.
PMRD+ PMRD−	34 33	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
SD+ SD−	40 39	I	**Signal Detect:** Differential 100k ECL input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.

6.0 Signal Descriptions (Continued)

Alternate PMD Interface

Symbol	Pin #	I/O	Description
PMID+ PMID−	42 41	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD Receiver into the Clock Recovery Module (CRM) of the PLAYER+.
RXC__OUT+ RXC__OUT−	36 35	O	**Recovered Clock Out:** 125 MHz clock recovered by the Clock Recovery Module (CRM) from the PMID data input. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used they should be left Not Connected (N/C).
RXD__OUT+ RXD__OUT−	52 51	O	**Recovered Data Out:** 125 Mbps data recovered by the Clock Recovery Module (CRM) from the PMID data input. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used they should be left Not Connected (N/C).
RXC__IN+ RXC__IN−	48 47	I	**Receive Clock In:** Clock inputs to the Player section of the PLAYER+. These inputs must be synchronized with the RXD__IN inputs. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used, pin 76 should be left Not Connected (N/C) and pin 75 should be connected directly to ground (Reserved__0).
RXD__IN+ RXD__IN−	50 49	I	**Receive Data In:** Data inputs to the Player section of the PLAYER+. These inputs must be synchronized with the RXC__IN inputs. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used, pin 78 should be left Not Connected (N/C) and pin 77 should be connected directly to ground (Reserved__0).
PMRD+ PMRD−	34 33	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
TXC+ TXC−	31 30	O	**Transmit Clock:** 125 MHz, 100k ECL compatible differential outputs synchronized to the outgoing PMRD data. These signals can be enabled using the Transmit Clock Enable (TXCE) bit in the Clock Generation Module Register (CGMREG). When these two pins are not used they should be left Not Connected (N/C).
SD+ SD−	40 39	I	**Signal Detect:** Differential, 100k ECL, input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.

6.0 Signal Descriptions (Continued)

PHY PORT INTERFACE

The PHY Port Interface consists of I/O signals used to connect the PLAYER+ device to the Media Access Control (MAC) sublayer or other PLAYER+ device. The DP83256 Device has two PHY Port Interfaces. The A__Indicate path from one PHY Port Interface and the B__Request path from the second PHY Port Interface. Each path consists of an odd parity bit, a control bit, and two 4-bit symbols.

Refer to section 3.3, the Configuration Switch, for more information.

Symbol	Pin #	I/O	Description
AIP	6	O	**PHY Port A Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (AIP, AIC, and AID<7:0>).
AIC	7	O	**PHY Port A Indicate Control:** TTL output signal indicating that the two 4-bit symbols (AID<7:4> and AID<3:0>) are either control symbols (AIC=1) or data symbols (AIC=0).
AID7 AID6 AID5 AID4	8 9 10 13	O	**PHY Port A Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. AID7 is the most significant bit and AID4 is the least significant bit of the first symbol.
AID3 AID2 AID1 AID0	14 15 16 17	O	**PHY Port A Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. AID3 is the most significant bit and AID0 is the least significant bit of the second symbol.
BRP	70	I	**PHY Port B Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (BRP, BRC, and BRD<7:0>).
BRC	69	I	**PHY Port B Request Control:** A TTL input signal indicating that the two 4-bit symbols (BRD<7:4> and BRD<3:0>) are either control symbols (BRC=1) or data symbols (BRC=0).
BRD7 BRD6 BRD5 BRD4	68 67 66 63	I	**PHY Port B Request Data:** TTL input signals representing the first 4-bit data/control symbol. BRD7 is the most significant bit and BRD4 is the least significant bit of the first symbol.
BRD3 BRD2 BRD1 BRD0	62 61 60 59	I	**PHY Port B Request Data:** TTL input signals representing the second 4-bit data/control symbol. BRD3 is the most significant bit and BRD0 is the least significant bit of the second symbol.

6.0 Signal Descriptions (Continued)

CONTROL BUS INTERFACE

The Control Bus Interface consists of I/O signals used to connect the PLAYER+ device to Station Management (SMT).

The Control Bus is an asynchronous interface between the PLAYER+ device and a general purpose microprocessor or other controller. It provides access to 64 8-bit internal registers.

In the PLAYER+ device the Control Bus address range has been expanded by 1-bit to 6 bits of address space.

Symbol	Pin #	I/O	Description
~CE	73	I	**Control Enable:** An active-low, TTL, input signal which enables the Control Bus port for a read or write cycle. R/~W, CBA<5:0>, CBP, and CBD<7:0> must be valid at the time ~CE is low.
R/~W	72	I	**Read/~Write:** A TTL input signal which indicates a read Control Bus cycle (R/~W=1), or a write Control Bus cycle (R/~W=0).
~ACK	75	O	~**Acknowledge:** An active low, TTL, open drain output signal which indicates the completion of a read or write cycle. During a read cycle, CBD<7:0> are valid as long as ~ACK is low (~ACK=0). During a write cycle, a microprocessor must hold CBD<7:0> valid until ~ACK becomes low. Once ~ACK is low, it will remain low as long as ~CE remains low (~CE=0).
~INT	74	O	~**Interrupt:** An active low, open drain, TTL, output signal indicating that an interrupt condition has occurred. The Interrupt Condition Register (ICR) should be read in order to find out the source of the interrupt. Interrupts can be masked through the use of the Interrupt Condition Mask Register (ICMR).
CBA5 CBA4 CBA3 CBA2 CBA1 CBA0	83 82 81 80 77 76	I	**Control Bus Address:** TTL input signals used to select the address of the register to be read or written. CBA5 is the most significant bit (MSB) and CBA0 is the least significant bit (LSB) of the address signals.
CBP	96	I/O	**Control Bus Parity:** A bidirectional, TTL signal representing odd parity for the Control Bus data (CBD<7:0>). During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low. If incorrect parity is used during a write cycle, the PLAYER+ device will inhibit the write cycle and set the Control Bus Data Parity Error (CPE) bit in the Interrupt Condition Register (ICR).
CBD7 CBD6 CBD5 CBD4 CBD3 CBD2 CBD1 CBD0	95 94 93 92 91 90 89 86	I/O	**Control Bus Data:** Bidirectional, TTL signals containing the data to be read from or written to a register. During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low.

6.0 Signal Descriptions (Continued)

CLOCK INTERFACE

The Clock Interface consists of 12.5 MHz and 25 MHz clocks supplied by the PLAYER+ device as well as reference and feedback inputs.

Symbol	Pin #	I/O	Description
LBC1 LBC2 LBC3 LBC4 LBC5	4 3 2 1 100	O	**Local Byte Clock:** TTL compatible, 12.5 MHz, 50% duty cycle clock outputs which are phase locked to a crystal oscillator or reference signal. The PH__SEL input determines whether the five phase outputs are phase offset by 8 ns or 16 ns.
PH__SEL	22	I	**Phase Select:** TTL compatible input used to select either a 8 ns or 16 ns phase offset between the 5 local byte clocks (LBC's). The LBC's are phase offset 8 ns apart when PH__SEL is at a logic LOW level and 16 ns apart when at a logic HI level.
FBK__IN	25	I	**Feedback Input:** TTL compatible input for use as the PLL's phase comparator feedback input to close the Phase Locked Loop. This input is intended to be driven from one of the Local Byte Clocks (LBC's) from the same PLAYER+ device.
LSC	99	O	**Local Symbol Clock:** TTL compatible 25 MHz output for driving the MACSI or BMAC devices. This output's negative phase transition is aligned with the LBC1 output transitions and has a 40% HI and 60% LOW duty cycle.
CLK16	5	O	**Clock 16/32:** TTL compatible clock with a selectable frequency of approximately 15.625 MHz or 31.25 MHz. The frequency can be selected using the Clock Select (CLKSEL) bit of the Mode 2 Register (MODE2). **Note:** No glitches appear at the output when switching frequencies.
XTAL__IN	27	I	**External Crystal Oscillator Input:** This input in conjunction with the XTAL__OUT output, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*. This input is selected when the REF__SEL input is at a logic LOW level. When not being used, this input should be tied to ground.
XTAL__OUT	26	O	**External Crystal Oscillator Output:** This output in conjunction with the XTAL__IN input, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*.
REF__IN	24	I	**Reference Input:** TTL compatible input for use as the PLL's phase comparator reference frequency. This input is for use in dual attach station or concentrator configurations where there are multiple PLAYER+ devices at a given site requiring synchronization. This input is selected when the REF__SEL input is at a logic HI level.
REF__SEL	23	I	**Reference Select:** TTL compatible input which selects either the crystal oscillator inputs XTAL__IN and XTAL__OUT or the REF__IN inputs as the reference frequency inputs for the PLL. The crystal oscillator inputs are selected when REF__SEL is at a logic LOW level and the REF__IN input is selected as the reference when REF__SEL is at a logic HI level.

6.0 Signal Descriptions (Continued)

MISCELLANEOUS INTERFACE

The Miscellaneous Interface consist of a reset signal and user definable enable signals.

Symbol	Pin #	I/O	Description
~RST	71	I	**Reset:** An active low, TTL, input signal which clears all registers. The signal must be kept asserted for a minimum amount of time. Once the ~RST signal is asserted, the PLAYER+ device should be allowed the specified amount of time to reset internal logic. Note that bit zero of the Mode Register will be set to zero (i.e. Stop Mode). See section 4.2, Stop Mode of Operation for more information
EP0	41	O	**User Definable Enable Pin 0:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP0 is asserted/deasserted through Enable Bit 0 (EB0) of the User Definable Register (UDR). When Enable Bit 0 is set to zero, EP0 is deasserted. When Enable Bit 0 is set to one, EP0 is asserted.
EP1	43	O	**User Definable Enable Pin 1:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP1 is asserted/deasserted through Enable Bit 1 (EB1) of the User Definable Register (UDR). When Enable Bit 1 is set to zero, EP1 is deasserted. When Enable Bit 1 is set to one, EP1 is asserted.

6.0 Signal Descriptions (Continued)

POWER AND GROUND

All power pins should be connected to a single +5V power supply using the recommended filtering. All ground pins should be connected to a common 0V ground supply. Bypassing and filtering requirements are given in a separate User Information Document.

Symbol	Pin #	I/O	Description
V_{CC}__ANALOG	20		**Power:** Positive 5V power supply for the Clock Generation Module VCO.
GND__ANALOG	21		**Ground:** Power supply return for the Clock Generation Module VCO.
V_{CC}__CORE	88		**Power:** Positive 5V power supply for the core PLAYER section logic gates.
GND__CORE	87		**Ground:** Power supply return for the core PLAYER section logic gates.
V_{CC}__ECL	32, 37, 45, 56		**Power:** Positive 5V power supply for the PLAYER+ device's ECL logic gates.
GND__ECL	38, 46, 55		**Ground:** Power supply return for the PLAYER+ device's ECL logic gates.
V_{CC}__ESD	28		**Power:** Positive 5V power supply for the PLAYER+ device's ESD protection circuitry.
GND__ESD	29		**Ground:** Power supply return for the PLAYER+ device's ESD protection circuitry.
V_{CC}__IO	11, 65, 79, 98		**Power:** Positive 5V power supply for the input/output buffers.
GND__IO	12, 64, 78, 97		**Ground:** Power supply return for the input/output buffers.

SPECIAL CONNECT PINS

These are pins that have special connection requirements.

No Connect (N/C) pins should not be connected to anything. This means not to power, not to ground, and not to each other.

Reserved__0 (RES__0) pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Reserved__1 (RES__1) pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Symbol	Pin #	I/O	Description
N/C	49, 53, 54		**No Connect:** Pins should not be connected to anything. This means not to power, not to ground, and not to each other.
RES__0	18, 19, 48, 50, 51, 52, 57, 58, 84		**Reserved 0:** Pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.
RES__1	85		**Reserved 1:** Pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

6.0 Signal Descriptions (Continued)

6.3 DP83257VF SIGNAL DESCRIPTIONS

The pin descriptions for the DP83257VF are divided into five functional interfaces; PMD Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and Miscellaneous Interface.

For a Pinout Summary List, refer to Table 8-3 and *Figure 8-3*, DP83257VF 160-Pin JEDEC Metric PQFP Pinout.

PMD INTERFACE

The PMD Interface consists of I/O signals used to connect the PLAYER+ device to the Physical Medium Dependant (PMD) sublayer.

The DP83257 PLAYER+ device actually has two PMD interfaces. The Primary PMD Interface and the Alternate PMD Interface.

The Primary PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMD. The second, Alternate PMD Interface can be used to support Unshielded Twisted Pair (UTP) PMDs that require external scrambling, with no external clock recovery or clock generation functions required.

Section 3.8 describes how the PLAYER+ can be connected to the PMD and how the Alternate PMD can be enabled.

Note that when the Alternate PMD Interface is not being used, the pins that make up the interface must be connected in the specific way described in the following Alternate PMD Interface table.

Primary PMD Interface

Symbol	Pin #	I/O	Description
PMID+ PMID−	62 61	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD Receiver into the Clock Recovery Module (CRM) of the PLAYER+.
PMRD+ PMRD−	54 53	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
SD+ SD−	60 59	I	**Signal Detect:** Differential 100k ECL input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.
TEL	74	I	**PMD Transmitter Enable Level:** A TTL input signal to select the PMD transmitter Enable (TXE) signal level.
TXE	73	O	**PMD Transmitter Enable:** A TTL output signal to enable/disable the PMD transmitter. The output level of the TXE pin is determined by three parameters: the Transmit Enable (TE) bit in the Mode Register, the TM2–TM0 bits in the Current Transmit State Register, and the input to the TEL pin. The following rules summarize the output of the TXE pin: 1. If TE = 0 and TEL = GND, then TXE = V_{CC} 2. If TE = 0 and TEL = V_{CC}, then TXE = GND 3. If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} 4. If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND 5. If TE = 1 and not OTM and TEL = GND, then TXE = GND 6. If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

6.0 Signal Descriptions (Continued)

Alternate PMD Interface

Symbol	Pin #	I/O	Description
PMID+ PMID−	62 61	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD Receiver into the Clock Recovery Module (CRM) of the PLAYER+.
RXC__OUT+ RXC__OUT−	56 55	O	**Recovered Clock Out:** 125 MHz clock recovered by the Clock Recovery Module (CRM) from the PMID data input. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used they should be left Not Connected (N/C).
RXD__OUT+ RXD__OUT−	83 82	O	**Recovered Data Out:** 125 Mbps data recovered by the Clock Recovery Module (CRM) from the PMID data input. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used they should be left Not Connected (N/C).
RXC__IN+ RXC__IN−	76 75	I	**Receive Clock In:** Clock inputs to the Player section of the PLAYER+. These inputs must be synchronized with the RXD__IN inputs. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used, pin 76 should be left Not Connected (N/C) and pin 75 should be connected directly to ground (Reserved__0).
RXD__IN+ RXD__IN−	78 77	I	**Receive Data In:** Data inputs to the Player section of the PLAYER+. These inputs must be synchronized with the RXC__IN inputs. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used, pin 78 should be left Not Connected (N/C) and pin 77 should be connected directly to ground (Reserved__0).
PMRD+ PMRD−	54 53	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
TXC+ TXC−	51 50	O	**Transmit Clock:** 125 MHz, 100k ECL compatible differential outputs synchronized to the outgoing PMRD data. These signals can be enabled using the Transmit Clock Enable (TXCE) bit in the Clock Generation Module Register (CGMREG). When these two pins are not used they should be left Not Connected (N/C).
SD+ SD−	60 59	I	**Signal Detect:** Differential, 100k ECL, input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.
TEL	74	I	**PMD Transmitter Enable Level:** A TTL input signal to select the PMD transmitter Enable (TXE) signal level.
TXE	73	O	**PMD Transmitter Enable:** A TTL output signal to enable/disable the PMD transmitter. The output level of the TXE pin is determined by three parameters: the Transmit Enable (TE) bit in the Mode Register, the TM2–TM0 bits in the Current Transmit State Register, and the input to the TEL pin. The following rules summarize the output of the TXE pin: 1. If TE = 0 and TEL = GND, then TXE = V_{CC} 2. If TE = 0 and TEL = V_{CC}, then TXE = GND 3. If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} 4. If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND 5. If TE = 1 and not OTM and TEL = GND, then TXE = GND 6. If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

6.0 Signal Descriptions (Continued)

PHY PORT INTERFACE

The PHY Port Interface consists of I/O signals used to connect the PLAYER+ device to the Media Access Control (MAC) sublayer or other PLAYER+ device. The DP83257 Device has two PHY Port Interfaces. The A__Request and A__Indicate paths from one PHY Port Interface and the B__Request and B__Indicate paths from the second PHY Port Interface. Each path consists of an odd parity bit, a control bit, and two 4-bit symbols.

Refer to section 3.3, the Configuration Switch, for more information.

Symbol	Pin #	I/O	Description
AIP	6	O	**PHY Port A Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (AIP, AIC, and AID<7:0>).
AIC	8	O	**PHY Port A Indicate Control:** A TTL output signal indicating that the two 4-bit symbols (AID<7:4> and AID<3:0>) are either control symbols (AIC=1) or data symbols (AIC=0).
AID7 AID6 AID5 AID4	10 12 14 18	O	**PHY Port A Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. AID7 is the most significant bit and AID4 is the least significant bit of the first symbol.
AID3 AID2 AID1 AID0	20 22 24 26	O	**PHY Port A Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. AID3 is the most significant bit and AID0 is the least significant bit of the second symbol.
ARP	7	I	**PHY Port A Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (ARP, ARC, and ARD<7:0>).
ARC	9	I	**PHY Port A Request Control:** A TTL input signal indicating that the two 4-bit symbols (ARD<7:4> and ARD<3:0>) are either control symbols (ARC=1) or data symbols (ARC=0).
ARD7 ARD6 ARD5 ARD4	11 13 15 19	I	**PHY Port A Request Data:** TTL input signals representing the first 4-bit data/control symbol. ARD7 is the most significant bit and ARD4 is the least significant bit of the first symbol.
ARD3 ARD2 ARD1 ARD0	21 23 25 27	I	**PHY Port A Request Data:** TTL input signals representing the second 4-bit data/control symbol. ARD3 is the most significant bit and ARD0 is the least significant bit of the second symbol.
BIP	114	O	**PHY Port B Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (BIP, BIC, and BID<7:0>).
BIC	112	O	**PHY Port B Indicate Control:** A TTL output signal indicating that the two 4-bit symbols (BID<7:4> and BID<3:0>) are either control symbols (BIC=1) or data symbols (BIC=0).
BID7 BID6 BID5 BID4	110 108 106 102	O	**PHY Port B Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. BID7 is the most significant bit and BID4 is the least significant bit of the first symbol.
BID3 BID2 BID1 BID0	100 98 96 94	O	**PHY Port B Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. BID3 is the most significant bit and BID0 is the least significant bit of the second symbol.
BRP	115	I	**PHY Port B Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (BRP, BRC, and BRD<7:0>).
BRC	113	I	**PHY Port B Request Control:** A TTL input signal indicating that the two 4-bit symbols (BRD<7:4> and BRD<3:0>) are either control symbols (BRC=1) or data symbols (BRC=0).

6.0 Signal Descriptions (Continued)

Symbol	Pin #	I/O	Description
BRD7 BRD6 BRD5 BRD4	111 109 107 103	I	**PHY Port B Request Data:** TTL input signals representing the first 4-bit data/control symbol. BRD7 is the most significant bit and BRD4 is the least significant bit of the first symbol.
BRD3 BRD2 BRD1 BRD0	101 99 97 95	I	**PHY Port B Request Data:** TTL input signals representing the second 4-bit data/control symbol. BRD3 is the most significant bit and BRD0 is the least significant bit of the second symbol.

6.0 Signal Descriptions (Continued)

CONTROL BUS INTERFACE

The Control Bus Interface consists of I/O signals used to connect the PLAYER+ device to Station Management (SMT).

The Control Bus is an asynchronous interface between the PLAYER+ device and a general purpose microprocessor or other controller. It provides access to 64 8-bit internal registers.

In the PLAYER+ device the Control Bus address range has been expanded by 1-bit to 6 bits of address space.

Symbol	Pin #	I/O	Description
~CE	118	I	**Control Enable:** An active-low, TTL, input signal which enables the Control Bus port for a read or write cycle. R/~W, CBA<5:0>, CBP, and CBD<7:0> must be valid at the time ~CE is low.
R/~W	117	I	**Read/~Write:** A TTL input signal which indicates a read Control Bus cycle (R/~W=1), or a write Control Bus cycle (R/~W=0).
~ACK	120	O	~**Acknowledge:** An active low, TTL, open drain output signal which indicates the completion of a read or write cycle. During a read cycle, CBD<7:0> are valid as long as ~ACK is low (~ACK=0). During a write cycle, a microprocessor must hold CBD<7:0> valid until ~ACK becomes low. Once ~ACK is low, it will remain low as long as ~CE remains low (~CE=0).
~INT	119	O	~**Interrupt:** An active low, open drain, TTL, output signal indicating that an interrupt condition has occurred. The Interrupt Condition Register (ICR) should be read in order to find out the source of the interrupt. Interrupts can be masked through the use of the Interrupt Condition Mask Register (ICMR).
CBA5 CBA4 CBA3 CBA2 CBA1 CBA0	135 134 133 132 129 128	I	**Control Bus Address:** TTL input signals used to select the address of the register to be read or written. CBA5 is the most significant bit (MSB) and CBA0 is the least significant bit (LSB) of the address signals.
CBP	148	I/O	**Control Bus Parity:** A bidirectional, TTL signal representing odd parity for the Control Bus data (CBD>7:0>). During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low. If incorrect parity is used during a write cycle, the PLAYER+ device will inhibit the write cycle and set the Control Bus Data Parity Error (CPE) bit in the Interrupt Condition Register (ICR).
CBD7 CBD6 CBD5 CBD4 CBD3 CBD2 CBD1 CBD0	147 146 145 144 143 142 141 138	I/O	**Control Bus Data:** Bidirectional, TTL signals containing the data to be read from or written to a register. During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low.

6.0 Signal Descriptions (Continued)

CLOCK INTERFACE

The Clock Interface consists of 12.5 MHz and 25 MHz clocks supplied by the PLAYER+ device as well as reference and feedback inputs.

Symbol	Pin #	I/O	Description
LBC1 LBC2 LBC3 LBC4 LBC5	4 3 2 1 160	O	**Local Byte Clock:** TTL compatible, 12.5 MHz, 50% duty cycle clock outputs which are phase locked to a crystal oscillator or reference signal. The PH__SEL input determines whether the five phase outputs are phase offset by 8 ns or 16 ns.
PH__SEL	34	I	**Phase Select:** TTL compatible input used to select either a 8 ns or 16 ns phase offset between the 5 local byte clocks (LBC's). The LBC's are phase offset 8 ns apart when PH__SEL is at a logic LOW level and 16 ns apart when at a logic HI level.
FBK__IN	37	I	**Feedback Input:** TTL compatible input for use as the PLL's phase comparator feedback input to close the Phase Locked Loop. This input is intended to be driven from one of the Local Byte Clocks (LBC's) from the same PLAYER+ device.
LSC	159	O	**Local Symbol Clock:** TTL compatible 25 MHz output for driving the MACSI or BMAC devices. This output's negative phase transition is aligned with the LBC1 output transitions and has a 40% HI and 60% LOW duty cycle.
CLK16	5	O	**Clock 16/32:** TTL compatible clock with a selectable frequency of approximately 15.625 MHz or 31.25 MHz. The frequency can be selected using the Clock Select (CLKSEL) bit of the Mode 2 Register (MODE2). **Note:** No glitches appear at the output when switching frequencies.
XTAL__IN	46	I	**External Crystal Oscillator Input:** This input in conjunction with the XTAL__OUT output, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*. This input is selected when the REF__SEL input is at a logic LOW level. When not being used, this input should be tied to ground.
XTAL__OUT	45	O	**External Crystal Oscillator Output:** This output in conjunction with the XTAL__IN input, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*.
REF__IN	36	I	**Reference Input:** TTL compatible input for use as the PLL's phase comparator reference frequency. This input is for use in dual attach station or concentrator configurations where there are multiple PLAYER+ devices at a given site requiring synchronization. This input is selected when the REF__SEL input is at a logic HI level.
REF__SEL	35	I	**Reference Select:** TTL compatible input which selects either the crystal oscillator inputs XTAL__IN and XTAL__OUT or the REF__IN inputs as the reference frequency inputs for the PLL. The crystal oscillator inputs are selected when REF__SEL is at a logic LOW level and the REF__IN input is selected as the reference when REF__SEL is at a logic HI level.
LPFLTR	49	O	**Loop Filter:** This is a diagnostic output that allows monitoring of the clock generation module's filter node. This output is disabled by default and does not need to be connected to any external device. It can be enabled using the FLTREN bit of the Clock generation module register (CGMREG). **Note:** In normal operation this pin should be disabled.

6.0 Signal Descriptions (Continued)

MISCELLANEOUS INTERFACE

The Miscellaneous Interface consist of a reset signal, user definable sense signals, and user definable enable signals.

Symbol	Pin #	I/O	Description
~RST	116	I	**Reset:** An active low, TTL, input signal which clears all registers. The signal must be kept asserted for a minimum amount of time. Once the ~RST signal is asserted, the PLAYER+ device should be allowed the specified amount of time to reset internal logic. Note that bit zero of the Mode Register will be set to zero (i.e. Stop Mode). See section 4.2, Stop Mode of Operation for more information
SP0	63	I	**User Definable Sense Pin 0:** A TTL input signal from a user defined source. Sense Bit 0 (SB0) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP1	65	I	**User Definable Sense Pin 1:** A TTL input signal from a user defined source. Sense Bit 1 (SB1) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP2	67	I	**User Definable Sense Pin 2:** A TTL input signal from a user defined source. Sense Bit 2 (SB2) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 2 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
EP0	64	O	**User Definable Enable Pin 0:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP0 is asserted/deasserted through Enable Bit 0 (EB0) of the User Definable Register (UDR). When Enable Bit 0 is set to zero, EP0 is deasserted. When Enable Bit 0 is set to one, EP0 is asserted.
EP1	66	O	**User Definable Enable Pin 1:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP1 is asserted/deasserted through Enable Bit 1 (EB1) of the User Definable Register (UDR). When Enable Bit 1 is set to zero, EP1 is deasserted. When Enable Bit 1 is set to one, EP1 is asserted.
EP2	68	O	**User Definable Enable Pin 2:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP2 is asserted/deasserted through Enable Bit 2 (EB2) of the User Definable Register (UDR). When Enable Bit 2 is set to zero, EP2 is deasserted. When Enable Bit 2 is set to one, EP2 is asserted.
CS	69	I	**Cascade Start:** A TTL input signal used to synchronize cascaded PLAYER+ devices in point-to-point applications. The signal is asserted when all of the cascaded PLAYER+ devices have the Cascade Mode (CM) bit of the Mode Register (MR) set to one, and all of the Cascade Ready (CR) pins of the cascaded PLAYER+ devices have been released. When Cascade Mode is not being used, this input should be tied to Ground. For further information, refer to section 4.4, Cascade Mode of Operation.
CR	70	O	**Cascade Ready:** An Open Drain output signal used to synchronize cascaded PLAYER+ devices in point-to-point applications. The signal is released (i.e. an Open Drain line is released) when all the cascaded PLAYER+ devices have the Cascade Mode (CM) bit of the Mode Register (MR) is set to one and a JK symbol pair has been received. When Cascade Mode is not being used, this input should be left Not Connected (N/C). For further information, refer to section 4.4, Cascade Mode of Operation.

6.0 Signal Descriptions (Continued)

POWER AND GROUND

All power pins should be connected to a single +5V power supply using the recommended filtering. All ground pins should be connected to a common 0V ground supply. Bypassing and filtering requirements are given in a separate User Information Document.

Symbol	Pin #	I/O	Description
V_{CC}__ANALOG	32		**Power:** Positive 5V power supply for the PLAYER+ device's CGM VCO.
GND__ANALOG	33		**Ground:** Power supply return for the PLAYER+ device's CGM VCO.
V_{CC}__CORE	140		**Power:** Positive 5V power supply for the core PLAYER logic gates.
GND__CORE	139		**Ground:** Power supply return for the core PLAYER logic gates.
V_{CC}__ECL	52, 57, 71, 89		**Power:** Positive 5V power supply for the PLAYER+ device's ECL logic gates.
GND__ECL	58, 72, 88		**Ground:** Power supply return for the PLAYER+ device's ECL logic gates.
V_{CC}__ESD	47		**Power:** Positive 5V power supply for the PLAYER+ device's ESD protection circuitry.
GND__ESD	48		**Ground:** Power supply return for the PLAYER+ device's ESD protection circuitry.
V_{CC}__IO	16, 105, 131, 158		**Power:** Positive 5V power supply for the input/output buffers.
GND__IO	17, 104, 130, 157		**Ground:** Power supply return for the input/output buffers.

SPECIAL CONNECT PINS

These are pins that have special connection requirements.

No Connect (N/C) pins should not be connected to anything. This means not to power, not to ground, and not to each other.

Reserved__0 (RES__0) pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Reserved__1 (RES__1) pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Symbol	Pin #	I/O	Description
N/C	38, 39, 40, 41, 42, 43, 44, 79, 80, 81, 87, 121, 122, 123, 124, 125, 126, 127, 149, 150, 151, 152, 153,154, 155, 156		**No Connect:** Pins should not be connected to anything. This means not to power, not to ground, and not to each other.
RES__0	28, 29, 30, 31, 84, 85, 86, 90, 91, 92, 93, 136		**Reserved 0:** Pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.
RES__1	137		**Reserved 1:** Pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

7.0 Electrical Characteristics

7.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		−0.5		7.0	V
DC_{IN}	Input Voltage		−0.5		V_{CC} + 0.5	V
DC_{OUT}	Output Voltage		−0.5		V_{CC} + 0.5	V
	V_{CC}—ESD to other V_{CC} Maximum Voltage Differential				0.3	V
	Storage Temperature		−65		150	°C
ECL	Signal Output Current				−50	mA
	ESD Protection		2000			V

7.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75		5.25	V
T_A	Operating Temperature		0		70	°C
FREF	Reference Input Frequency		12.5−50 ppm	12.5	12.5 + 50 ppm	MHz

7.3 RECOMMENDED EXTERNAL COMPONENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
XTAL	Crystal Specifications					
	Center Frequency			12.5		MHz
	Frequency Calibration		−10		10	ppm
	Frequency Stability	Over Temperature	−10		10	ppm
	Aging	Less Than	−5		5	ppm
	Recommended Power Supply Bypassing Capacitor Value **Note:** Capacitors should be placed between each supply pair as close to the device as possible.			0.1		µF

7.4 DC ELECTRICAL CHARACTERISTICS

The DC characteristics are specified over the Recommended Operating Conditions, unless otherwise specified.

DC Electrical Characteristics for All TTL-Compatible Inputs

The following signals are covered: PHY Port Request Signals (ARD, ARC, ARP, BRD, BRC, BRP), Phase Select (PH__SEL), Reference Select (REF__SEL), Sense Pins (SP), Cascade Start (CS), PMD Transmitter Enable Level (TEL), Device Reset (~RST), and Control Bus Interface Inputs (R/~W, ~CE, CBA).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA			−1.5	V
I_{IL}	Input Low Current	V_{IN} = GND			−10	µA
I_{IH}	Input High Current	V_{IN} = V_{CC}			+10	µA

7.0 Electrical Characteristics (Continued)

DC Electrical Characteristics for All TTL-Compatible Non-TRI-STATE Outputs

The following signals are covered: Clock 16/32 (CLK16), Enable Pins (EP), and PMD Transmitter Enable (TXE).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -2$ mA	$V_{CC} - 0.5$			V
V_{OL}	Output Low Voltage	$I_{OL} = 4$ mA			0.5	V

DC Electrical Characteristics for All TTL-Compatible TRI-STATE Outputs

The following signals are covered: PHY Port Indicate Signals (AID, AIC, AIP, BID, BIC, BIP).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -2$ mA	$V_{CC} - 0.5$			V
V_{OL}	Output Low Voltage	$I_{OL} = 4$ mA			0.5	V
I_{OZ3}	TRI-STATE Leakage	$V_{OUT} = V_{CC}$ (Note 1)			60	μA
I_{OZ4}	TRI-STATE Leakage	$V_{OUT} = V_{GND}$ (Note 1)			-500	μA

Note 1: Output buffer has a p-channel pullup device.

DC Electrical Characteristics for All TTL-Compatible Input/Outputs

The following signals are covered: Control Bus Interface I/O (CBD, CBP).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
V_{IC}	Input Clamp Voltage	$I_{IN} = -18$ mA			-1.5	V
I_{IL}	Input Low Current	$V_{IN} = GND$			-10	μA
I_{IH}	Input High Current	$V_{IN} = V_{CC}$			$+10$	μA
V_{OH}	Output High Voltage	$I_{OH} = -2$ mA	$V_{CC} - 0.5$			V
V_{OL}	Output Low Voltage	$I_{OL} = 4$ mA			0.5	V
I_{OZ1}	TRI-STATE Leakage	$V_{OUT} = V_{CC}$			10	μA
I_{OZ2}	TRI-STATE Leakage	$V_{OUT} = V_{GND}$			-10	μA

7.0 Electrical Characteristics (Continued)

DC Electrical Characteristics for All FDDI Clock Outputs

The following signals are covered: Local Byte Clocks (LBC1–LBC5), and Local Symbol Clock (LSC).

These outputs are designed to drive capacitive loads from 20 pF to 60 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$	$V_{CC} - 2$			V
V_{OL}	Output Low Voltage	$I_{OL} = 8$ mA			0.5	V

DC Electrical Characteristics for All Clock Reference Inputs

The following signals are covered: Reference In (REF__IN) and Feedback In (FBK__IN).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
V_{IC}	Input Clamp Voltage	$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current	$V_{IN} =$ GND			−10	μA
I_{IH}	Input High Current	$V_{IN} = V_{CC}$			+10	μA

DC Electrical Characteristics for Crystal Inputs and Outputs

The following signals are covered: Crystal In (XTAL__IN) and Crystal Out (XTAL__OUT).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OL}	Output Low Current	$V_{OUT} = 1$V (Note A)		4		mA
I_{OH}	Output High Current	$V_{OUT} = V_{CC} - 1$V (Note A)		−4		mA
	Small Signal Gain	XTAL__IN = 100 mV Centered about V_{TH} (Note A)		45		
V_{TH}	Input Threshold Voltage	(Note A)		2.2		V
	XTAL__IN to XTAL__OUT Delay	(Note A)		7.0		ns
	Output Impedance	(Note A)		270		Ω
	Internal Resistor Variation	(Note A)		10		kΩ

Note A: This parameter is presented as a typical value to provide enough information to design an appropriate crystal network.

DC Electrical Characteristics for All Open Drain Outputs

The following signals are covered: Interrupt (~INT), Acknowledge (~ACK), and Cascade Ready (CR).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	$I_{OL} = 8$ mA			0.5	V
I_{OZ}	TRI-STATE Leakage	$V_{OUT} = V_{CC}$			10	μA

7.0 Electrical Characteristics (Continued)

DC Electrical Characteristics for All 100K ECL Compatible Inputs

The following signals are covered: PMD Indicate Data (PMID), Receive Clock In (RXC__IN), Receive Data In (RXD__IN), and Signal Detect (SD).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DIFF}	Input Voltage Differential	(Note 1)	150			mV
V_{CM}	Common Mode Voltage	V_{DIFF} = 300 mV (Notes 1, 2)	V_{CC} − 2.0		V_{CC} − 0.5	V
I_{IN}	Input Current	V_{IN} = V_{CC} or GND	−200		200	μA

Note 1: Both inputs of each differential pair are tested together. These specifications guarantee that the inputs are compatible with standard 100K ECL voltage level outputs.

Note 2: V_{CM} is measured from the crossover point of the 300 mV differential test input.

DC Electrical Characteristics for 100K ECL Compatible Outputs

The following signals are covered: PMD Request Data (PMRD) and Transmit Clock (TXC).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{IL} = V_{CC} − 1.810 V_{IH} = V_{CC} − 0.880	V_{CC} − 1.025		V_{CC} − 0.880	V
V_{OL}	Output Low Voltage		V_{CC} − 1.810		V_{CC} − 1.620	V

DC Electrical Characteristics for Alternate PMD ECL Outputs

The following signals are covered: Receive Clock Out (RXC__OUT) and Receive Data Out (RXD__OUT).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{IL} = V_{CC} − 1.810 V_{IH} = V_{CC} − 0.880 (Note 3)	V_{CC} − 1.155		V_{CC} − 0.880	V
V_{OL}	Output Low Voltage		V_{CC} − 1.810		V_{CC} − 1.550	V

Note 3: It is recommended that RXC__OUT+ and RXC__OUT− always be used together as a differential pair. It is recommended that RXD__OUT+ and RXD__OUT− always be used together as a differential pair.

Supply Current Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Total Supply	LBC1 = 12.5 MHz			350*	mA
ECL__I_{CC}	ECL Supply Current	LBC1 = 12.5 MHz		200*		mA
ANALOG__I_{CC}	ANALOG Supply Current	LBC1 = 12.5 MHz		20*		mA

***Note:** The PLAYER+ device has multiple pairs of differential ECL outputs that need to be terminated. The additional current needed for this termination is not included in the PLAYER+'s total supply current, but can be calculated as follows:

V_{OH}__max = V_{CC} − 0.88V
V_{OL}__max = V_{CC} − 1.62V

Since the outputs are differential, the average output level is V_{CC} − 1.25V. The test load per output is 50Ω at V_{CC} − 2V, therefore the external load current through the 50Ω resistor is:

I_{LOAD} = [(V_{CC} − 1.25) − (V_{CC} − 2)]/50
= 0.015A
= 15 mA

As a result, the termination for each pair of active ECL outputs typically consumes 30 mA, time averaged.

7.0 Electrical Characteristics (Continued)

7.5 AC ELECTRICAL CHARACTERISTICS

The AC Electrical characteristics are specified over the Recommended Operating Conditions, unless otherwise specified.

AC Characteristics for the Control Bus Interface

The following signals are covered: Control Bus Interface (R/~W, ~CE, ~INT, ~ACK, CBA, CBD, and CBP).

Symbol	Descriptions	Min	Max	Units
T1	$\overline{CE}$ Setup to LBC	15		ns
T2	LBC Period	80		ns
T3	LBC1 to $\overline{ACK}$ Low		45	ns
T4	$\overline{CE}$ Low to $\overline{ACK}$ Low	290	540	ns
T5	LBC1 Low to CBD(7–0) and CBP Valid		60	ns
T6	LBC1 to CBD(7–0) and CBP Active	5		ns
T7	$\overline{CE}$ Low to CBD(7–0) and CBP Active	225	475	ns
T8	$\overline{CE}$ Low to CBD(7–0) and CBP Valid	265	515	ns
T9	LBC Pulse Width High	35	45	ns
T10	LBC Pulse Width Low	35	45	ns
T11	$\overline{CE}$ High to $\overline{ACK}$ High		45	ns
T12	R/$\overline{W}$, CBA(5–0), CBD(7–0) and CBP Setup to $\overline{CE}$ Low	5		ns
T13	$\overline{CE}$ High to R/W, CBA(5–0), CBD(7–0) and CBP Hold Time	0		ns
T14	R/$\overline{W}$, CBA(5–0), CBD(7–0) and CBP to LBC1 Setup Time	20		ns
T15	$\overline{ACK}$ Low to $\overline{CE}$ High Lead Time	0		ns
T16	$\overline{CE}$ Minimum Pulse Width High	20		ns
T17	$\overline{CE}$ High to CBD(7–0) and CBP TRI-STATE		55	ns
T18	$\overline{ACK}$ High to $\overline{CE}$ Low	0		ns
T19	CBD(7–0) Valid to $\overline{ACK}$ Low Setup	20		ns
T20a	LBC1 to R/$\overline{W}$ Hold Time	10		ns
T20b	LBC1 to CBA Hold Time	10		ns
T20c	LBC1 to CBD and CBP Hold Time	20		ns
T21	LBC1 to $\overline{INT}$ Low		55	ns
T22	LBC1 to EP Change	5	25	ns

Asynchronous Definitions

T4 (min)	T1 + (3 * T2) + T3
T4 (max)	T1 + (6 * T2) + T3
T7 (min)	T1 + (2 * T2) + T6
T7 (max)	T1 + (5 * T2) + T6
T8 (min)	T1 + (2 * T2) + T9 + T5
T8 (max)	T1 + (5 * T2) + T9 + T5

Note: Min/Max numbers are based on T2 = 80 ns and T9 = T10 = 40 ns.

7.0 Electrical Characteristics (Continued)

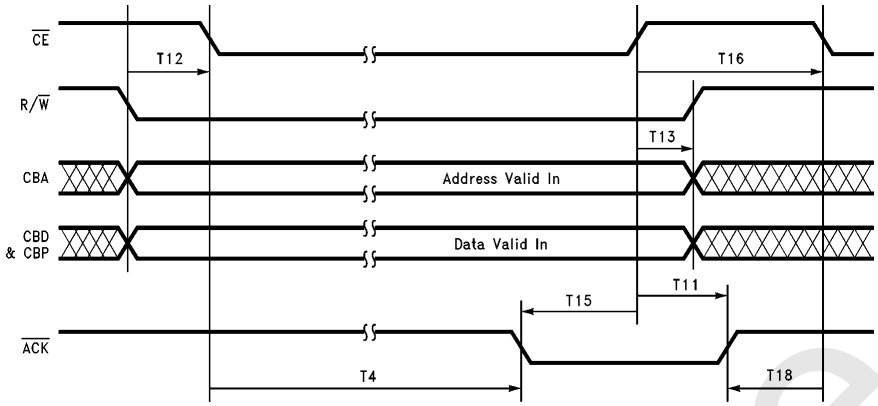

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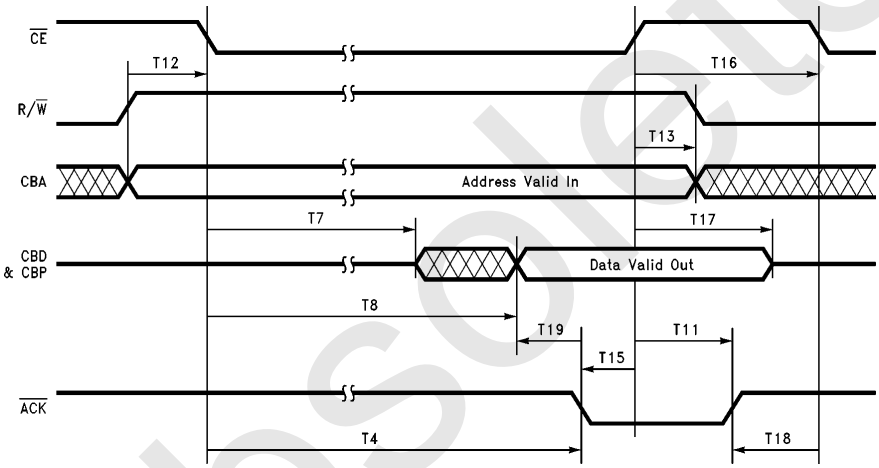
FIGURE 7-1. Asynchronous Control Bus Write Cycle Timing



TL/F/11708–30

FIGURE 7-2. Asynchronous Control Bus Read Cycle Timing

7.0 Electrical Characteristics (Continued)

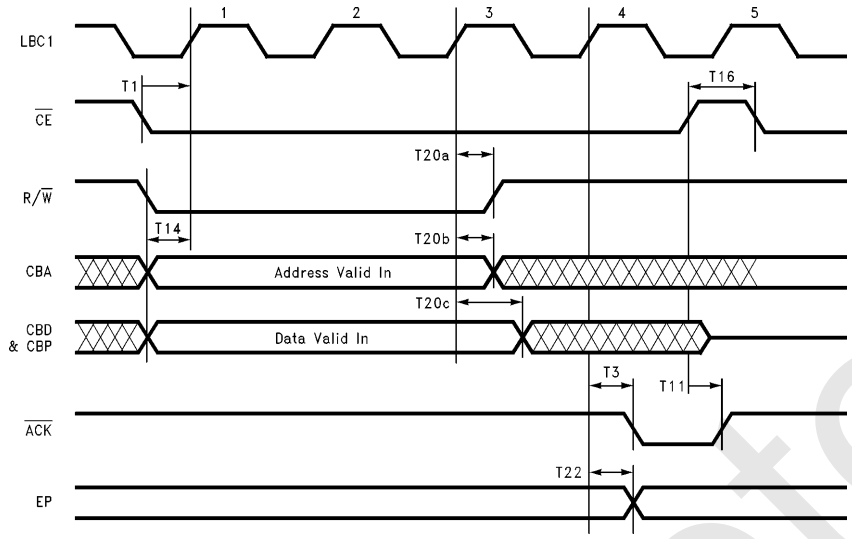


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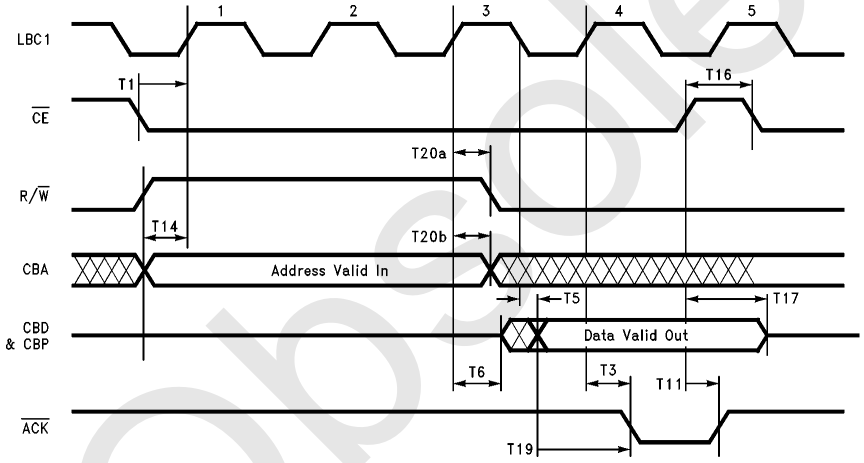
FIGURE 7-3. Control Bus Synchronous Writes



TL/F/11708–32

FIGURE 7-4. Control Bus Synchronous Reads

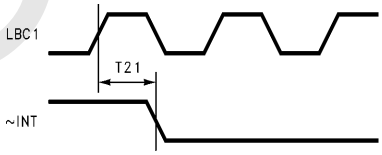


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FIGURE 7-5. Control Bus Interrupt Timing

7.0 Electrical Characteristics (Continued)

AC Characteristics for the Clock Interface Signals (Timing and Relationships)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{Phase1}	LBC1–LBC2 Timing	PH__SEL = LOW	5.0	8	11.0	ns
T_{Phase2}	LBC1–LBC3 Timing	PH__SEL = LOW	13.0	16	19.0	ns
T_{Phase3}	LBC1–LBC4 Timing	PH__SEL = LOW	21.0	24	27.0	ns
T_{Phase4}	LBC1–LBC5 Timing	PH__SEL = LOW	29.0	32	35.0	ns
T_{Phase1}	LBC1–LBC2 Timing	PH__SEL = HIGH	45.0	48	51.0	ns
T_{Phase2}	LBC1–LBC3 Timing	PH__SEL = HIGH	13.0	16	19.0	ns
T_{Phase3}	LBC1–LBC4 Timing	PH__SEL = HIGH	61.0	64	67.0	ns
T_{Phase4}	LBC1–LBC5 Timing	PH__SEL = HIGH	29.0	32	35.0	ns
T_{Phase5}	LBC5 Rising- LBC1 Falling Timing	PH__SEL = LOW or PH__SEL = HIGH	5.0	8	12.0	ns
T23	LSC Falling to LBC1	(Note 1)	−3		+6	ns
T24	REF__IN to FBK__IN	In Lock	−2		+2	ns

Note 1: LSC loading must always be less than or equal to LBC1 loading.

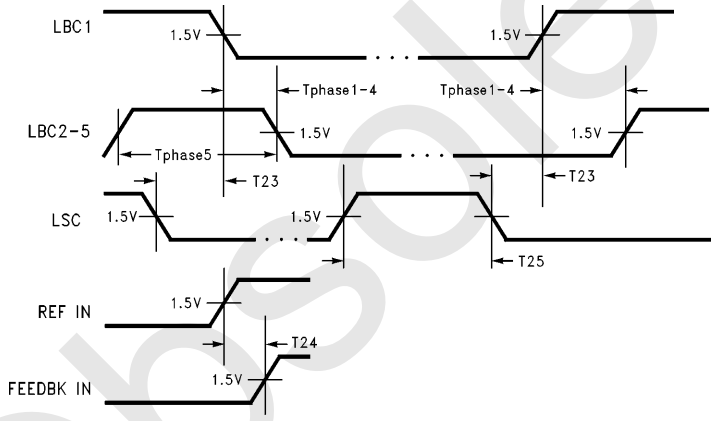

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FIGURE 7-6. Clock Signal Relationships

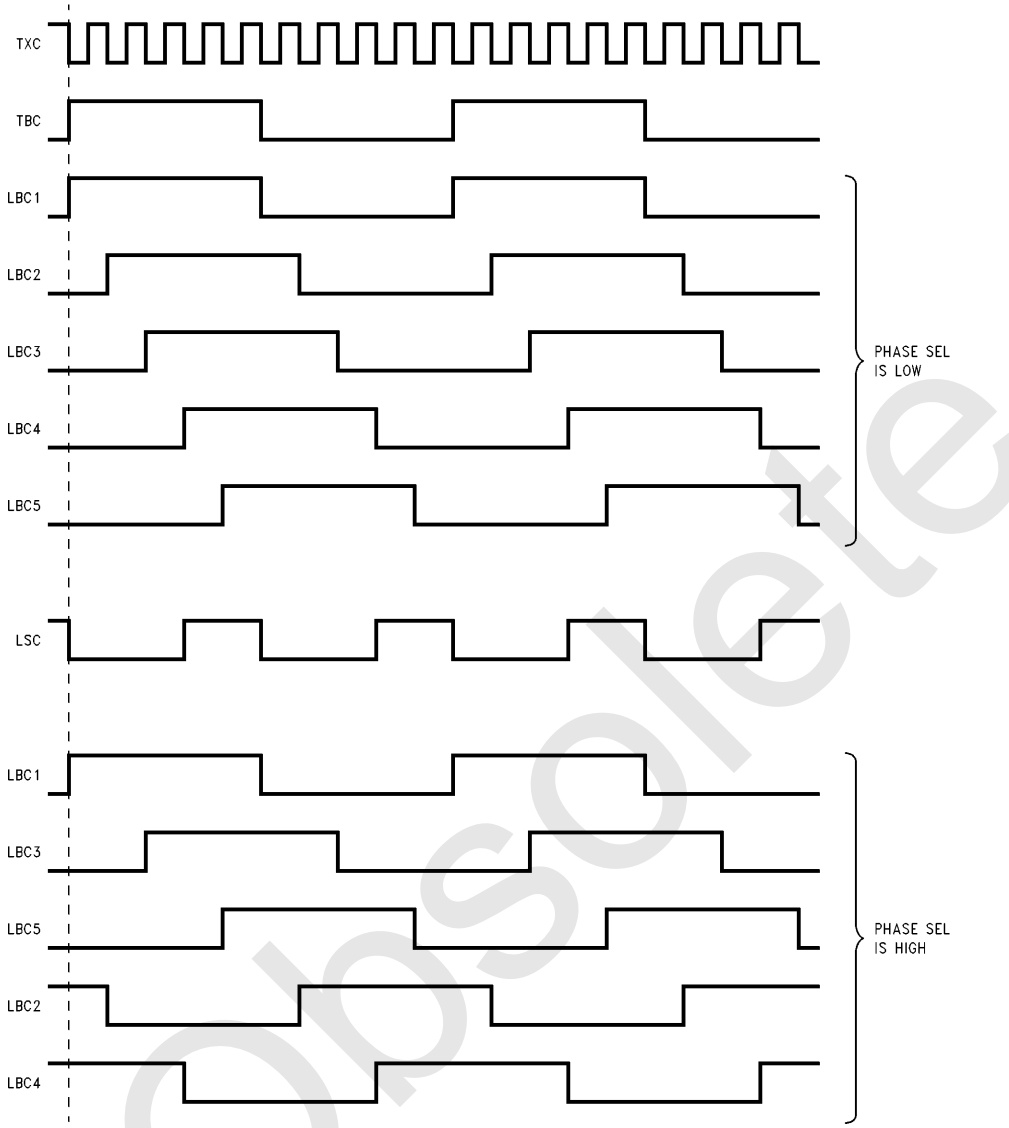

FIGURE 7-7. Typical Clock Signal Relationships Based on Phase Select (PH__SEL) Setting

7.0 Electrical Characteristics (Continued)

AC Characteristics for the Clock Interface Signals (Periods and Pulse Widths)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T2	LBC Period			80		ns
T9	LBC Pulse Width High		35		45	ns
T10	LBC Pulse Width Low		35		45	ns
T25	LSC Pulse Width High		12		19	ns
T26	LSC Pulse Width Low		21		28	ns
T27	CLK16 Period	MODE2.CLKSEL = 0		64		ns
T28	CLK16 Pulse Width	MODE2.CLKSEL = 0 (Note 1)	27	32	37	ns
T27	CLK16 Period	MODE2.CLKSEL = 1		32		ns
T28	CLK16 Pulse Width	MODE2.CLKSEL = 1 (Note 1)	11	16	21	ns
T29	REF__IN Pulse Width High		35		45	ns

Note 1: This parameter is not tested, but is assured by correlation with characterization data.

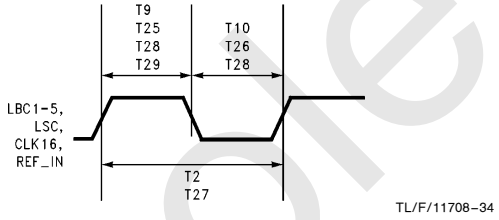

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FIGURE 7-8. Clock Pulse Widths

AC Characteristics for Port A Interface and Port B Interface

The following signals are covered: PHY Port A (AID, AIP, AIC, ARD, ARP, ARC) and PHY Port B (BID, BIP, BIC, BRD, BRP, BRC).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T30	LBC1 to Indicate Data Changes from TRI-STATE to Valid Data				70	ns
T31	LBC1 to Indicate Data Changes from Active to TRI-STATE				70	ns
T32	LBC1 to Indicate Data Sustain		9			ns
T33	LBC1 to Valid Indicate Data				45	ns
T34	Request Data to LBC1 Setup Time		15			ns
T35	Request Data to LBC1 Hold Time		3			ns

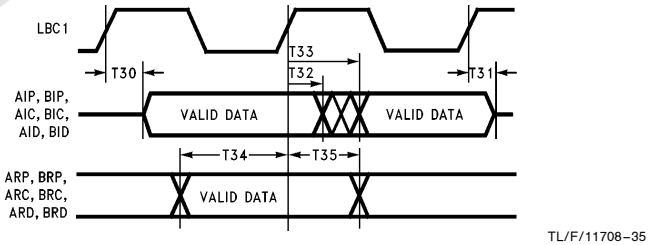

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FIGURE 7-9. PHY Port Interface Timing

7.0 Electrical Characteristics (Continued)

AC Characteristics for the PMD Interface

The following signals are covered: PMD Indicate Data (PMID), Signal Detect (SD), and PMD Request Data (PMRD).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T36	PMID± to PMRD± Latency	Looped Back through Configuration Switch. LBC1 = 12.5 MHz In Lock (Note 1)		5		LBC Cycles
T37	SD Minimum Pulse Width		120			ns
T38	PMRD Rise Time	(Note 2)			1.5	ns
T39	PMRD Fall Time	(Note 2)			1.5	ns

Note 1: This only applies when the Alternate PMD Interface is disabled, APMDREG.APMDEN = 0.

Note 2: This parameter is not tested, but is assured by correlation with characterization data.

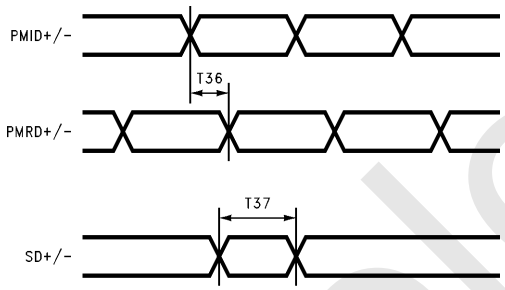

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FIGURE 7-10. Primary PMD Timing Diagrams

7.0 Electrical Characteristics (Continued)

AC Characteristics for the Alternate PMD Interface

The following input signals are covered: PMD Indicate Data (PMID), Signal Detect (SD), Receive Data In (RXD__IN), Receive Clock In (RXC__IN).

The following output signals are covered: PMD Request Data (PMRD), Transmit Clock (TXC), Recovered Data Out (RXD__OUT), Recovered Clock Out (RXC__OUT).

Note: The Alternate PMD Interface is only available on the 160 pin DP83257 PLAYER+ Device and the 100 pin DP83256-AP Device. The Transmit Clock is enabled by the CGMREG.TXCE bit. The rest of the Alternate PMD Interface is enabled by the APMDREG.APMDEN bit.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T40	RXC__OUT+ to RXD__OUT± Change Time		1.0		5.0	ns
T41	PMID± to RXD__OUT Latency	In Lock		16		ns
T42	RXD__IN± to RXC__IN+ Setup Time		4.0			ns
T43	RXD__IN± to RXC__IN+ Hold Time		0.5			ns
T44	TXC+ to PMRD± Change Time		4.0		7.0	ns
T42	SD Minimum Pulse Width		120			ns
T45	RXC__OUT± Pulse Width High	(Note 1)	3.5		4.5	ns
T46	RXC__OUT± Rise Time	(Note 1)			1.5	ns
T47	RXC__OUT± Fall Time	(Note 1)			1.5	ns
T48	RXD__OUT± Rise Time	(Note 1)			1.5	ns
T49	RXD__OUT± Fall Time	(Note 1)			1.5	ns
T50	TXC± Pulse Width High	(Note 1)	3.5		4.5	ns
T51	TXC± Rise Time	(Note 1)			1.5	ns
T52	TXC± Fall Time	(Note 1)			1.5	ns
T38	PMRD Rise Time	(Note 1)			1.5	ns
T39	PMRD Fall Time	(Note 1)			1.5	ns

Note 1: This parameter is not tested, but is assured by correlation with characterization data.

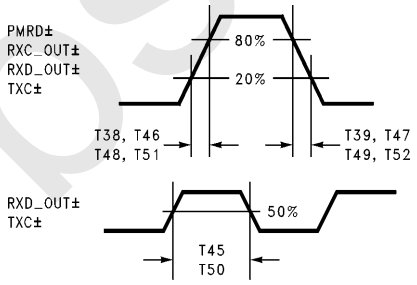

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FIGURE 7-11. ECL Rise and Fall Times

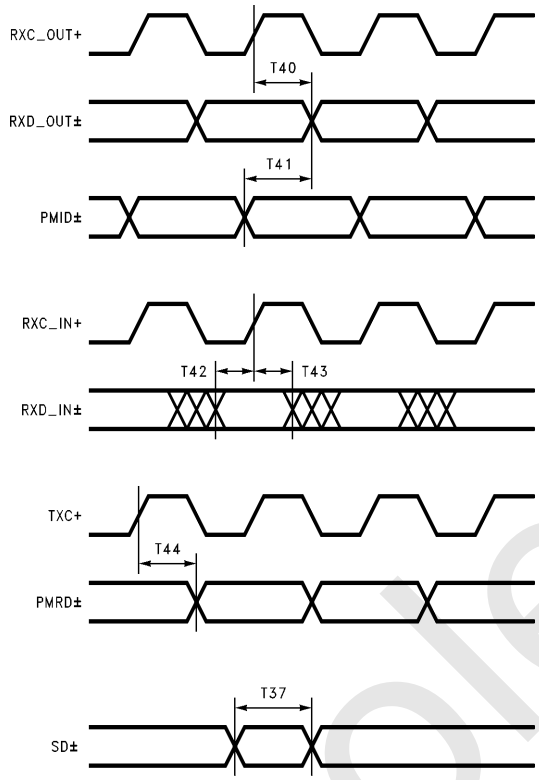

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FIGURE 7-12. Alternate PMD Timing Diagrams

7.0 Electrical Characteristics (Continued)

AC Characteristics for the PMD Interface Inputs (ANSI Specifications)

The following input signals are covered: PMD Indicate Data (PMID), Receive Data In (RXD__IN), Receive Clock In (RXC__IN).

Note: The Alternate PMD Interface is only available on the 160 pin DP83257 PLAYER+ Device and the 100 pin DP83256-AP Device. The Transmit Clock is enabled by the CGMREG.TXCE bit. The rest of the Alternate PMD Interface is enabled by the APMDREG.APMDEN bit.

All comments in square brackets are section references to the ANSI documents where these specifications can be found.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T53	CRM Window Recognition Region (PMID Inputs)	[PMD E.2]	−3		3	ns
T54	PMID Receive Clock Tolerance (Lock Acquisition Range)	[PHY 5.2.4]	−100		100	ppm
T55	Receive Clock Acquisition Time	From 1st Data and SD Active [PHY 5.2.6]			100	μs
T56	Receive Clock Acquisition Time	From Line State Change [PHY 5.2.6]			15	μs

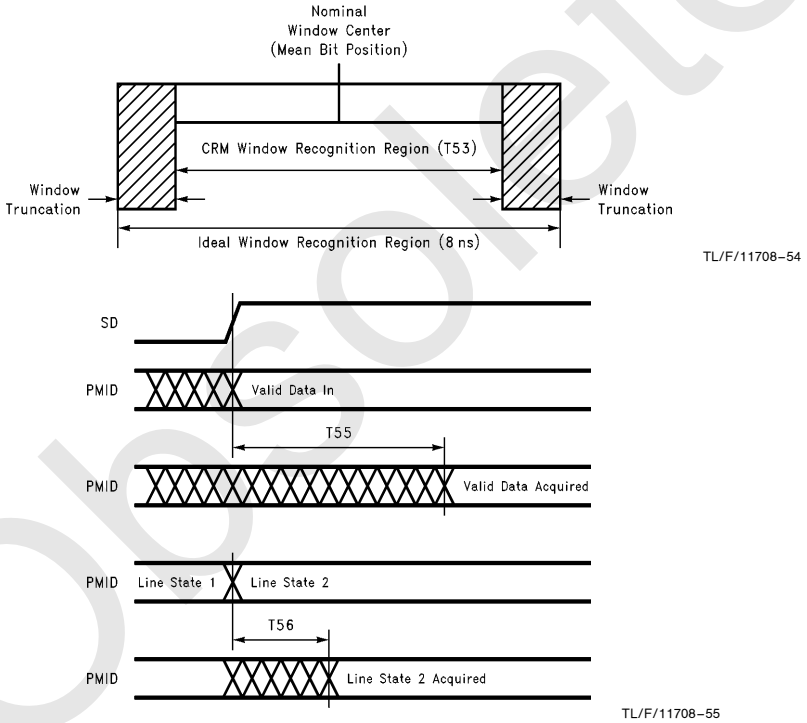

FIGURE 7-13. Alternate PMD Input Timing Diagrams—ANSI Specifications

7.0 Electrical Characteristics (Continued)

AC Characteristics for the PMD Interface Outputs (ANSI Specifications)

The following output signals are covered: PMD Request Data (PMRD), Transmit Clock (TXC), Recovered Data Out (RXD__OUT), Recovered Clock Out (RXC__OUT).

Note: The Alternate PMD Interface is only available on the 160 pin DP83257 PLAYER+ Device and the 100 pin DP83256-AP Device. The Transmit Clock is enabled by the CGMREG.TXCE bit. The rest of the Alternate PMD Interface is enabled by the APMDREG.APMDEN bit.

Comments in square brackets are section references to the ANSI documents where these specifications can be found.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T57	PMRD Total Transmit Jitter [Duty Cycle Distortion (DCD)+ Data Dependent Jitter (DDJ)+ Random Jitter (RJ)]	(Note 1) [PMD 8.1]			0.72	ns p-p
T58	Total Recovered Clock (RXC__OUT) Jitter [Static Alignment Error Accuracy (SAE)+ Clock Data Dependent Jitter (C__DDJ)+ Random Jitter (C__RJ)]	(Note 1) [PMD E.2]			2.5	ns p-p

Note 1: This parameter is not tested, but is assured through characterization data and periodic testing of sample units.

7.0 Electrical Characteristics (Continued)

AC Characteristics for User Definable Pins

The following signals are covered: Sense Pins (SP).

For Enable Pins (EP) timing see AC Characteristics for the Control Bus Interface.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T59	SP Minimum Pulse Width		120			ns

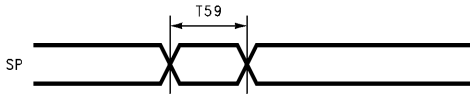

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FIGURE 7-14. SP Minimum Pulse Width

AC Characteristics for Miscellaneous Interface

The following signal is covered: Reset (~RST).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T60	Minimum Reset (~RST) Pulse Width		300			ns
T61	Maximum Power Up Reset Cycle Duration	(Notes 1, 2)			10	ms
T62	Maximum Hardware Reset (~RST) Cycle Duration				0.5	ms

Note 1: This parameter is not tested, but is assured by correlation with characterization data.

Note 2: User must wait this long before trying to access the device after power up. It is recommended that a Hardware Reset be used sometime after the Power Up Reset cycle is complete to insure proper device reset.

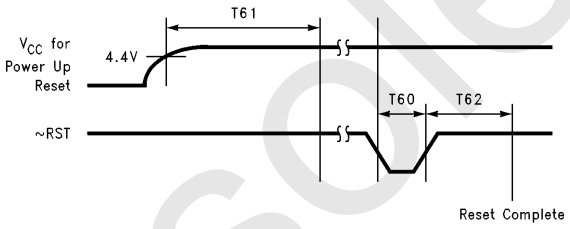

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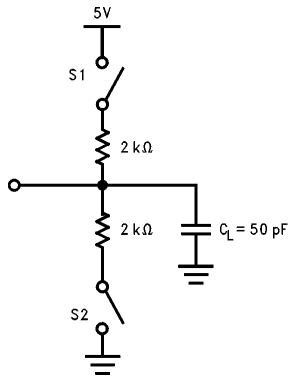
FIGURE 7-15. Reset Timing

7.0 Electrical Characteristics (Continued)

AC TEST CIRCUITS



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Note: S_1 is closed for T_{PZL} and T_{PLZ}
S_2 is closed for T_{PZH} and T_{PHZ}
S_1 and S_2 are open otherwise

FIGURE 7-16. Switching Test Circuit for All TRI-STATE Output Signals

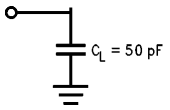

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FIGURE 7-17. Switching Test Circuit for All TTL Output Signals

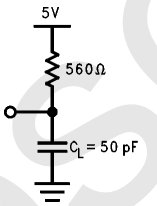

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FIGURE 7-18. Switching Test Circuit for All Open Drain Output Signals ($\overline{INT}$, $\overline{ACK}$, and CR)

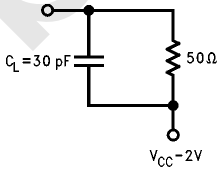

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FIGURE 7-19. Switching Test Circuit for All ECL Input and Output Signals

7.0 Electrical Characteristics (Continued)

TEST WAVEFORMS

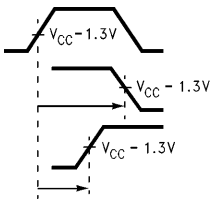

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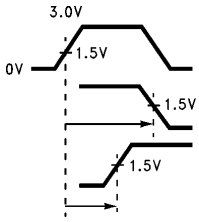
FIGURE 7-20. ECL Output Test Waveform



TL/F/11708–42

Note: All CMOS Inputs and outputs are TTL compatible.

FIGURE 7-21. TTL Output Test Waveform

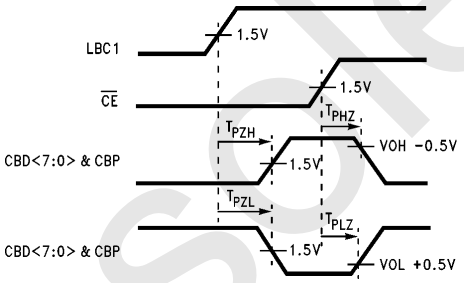


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FIGURE 7-22. TRI-STATE Output Test Waveform

8.0 Connection Diagrams

8.1 DP83256VF CONNECTION DIAGRAM

For a Pinout Summary List, refer to Table 8-1.

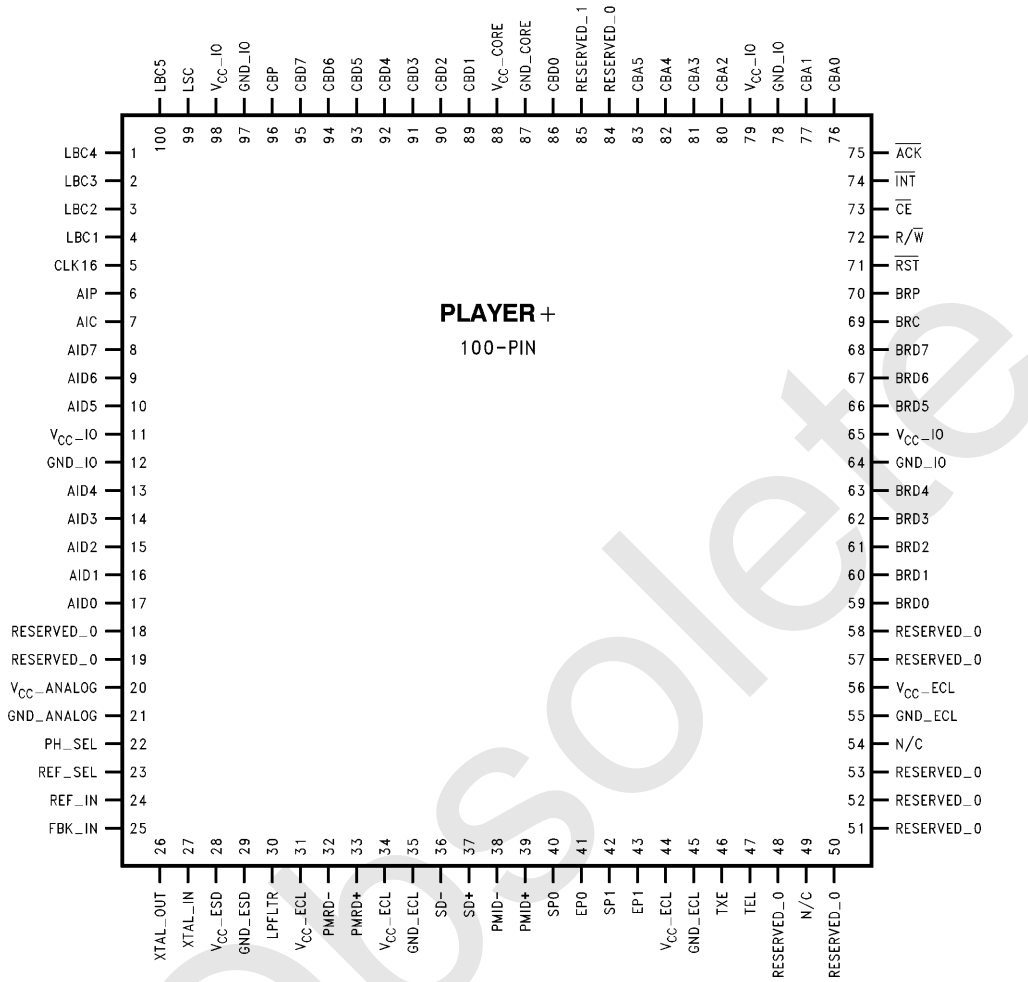

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FIGURE 8-1. DP83256VF 100-Pin JEDEC Metric PQFP Pinout

8.0 Connection Diagrams (Continued)

TABLE 8-1. DP83256 100-Pin PQFP Pinout Summary

Pin No.	Signal Name	Symbol	I/O	Pin Type
1	Local Byte Clock 4	LBC4	O	TTL
2	Local Byte Clock 3	LBC3	O	TTL
3	Local Byte Clock 2	LBC2	O	TTL
4	Local Byte Clock 1	LBC1	O	TTL
5	Clock 16/32	CLK16	O	TTL
6	PHY Port A Indicate Parity	AIP	O	TTL
7	PHY Port A Indicate Control	AIC	O	TTL
8	PHY Port A Indicate Data<7>	AID7	O	TTL
9	PHY Port A Indicate Data<6>	AID6	O	TTL
10	PHY Port A Indicate Data<5>	AID5	O	TTL
11	I/O Power	V_{CC}_IO		+5V
12	I/O Ground	GND_IO		+0V
13	PHY Port A Indicate Data<4>	AID4	O	TTL
14	PHY Port A Indicate Data<3>	AID3	O	TTL
15	PHY Port A Indicate Data<2>	AID2	O	TTL
16	PHY Port A Indicate Data<1>	AID1	O	TTL
17	PHY Port A Indicate Data<0>	AID0	O	TTL
18	Reserved_0	RES_0		+0V
19	Reserved_0	RES_0		+0V
20	ANALOG Power	V_{CC}_ANALOG		+5V
21	ANALOG Ground	GND_ANALOG		+0 V
22	Phase Select	PH_SEL	I	TTL
23	Reference Select	REF_SEL	I	TTL
24	Reference Input	REF_IN	I	TTL
25	Feedback Input	FBK_IN	I	TTL
26	Crystal Output	XTAL_OUT	O	
27	Crystal Input	XTAL_IN	I	
28	ESD Power	V_{CC}_ESD		+5V
29	ESD Ground	GND_ESD		+0V
30	Loop Filter	LPFLTR	O	
31	ECL Power	V_{CC}_ECL		+5V
32	PMD Request Data −	PMRD−	O	ECL
33	PMD Request Data +	PMRD+	O	ECL
34	ECL Power	V_{CC}_ECL		+5V
35	ECL Ground	GND_ECL		+0V
36	Signal Detect −	SD−	I	ECL
37	Signal Detect +	SD+	I	ECL
38	PMD Indicate Data −	PMID−	I	ECL

8.0 Connection Diagrams (Continued)

TABLE 8-1. DP83256 100-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
39	PMD Indicate Data +	PMID+	I	ECL
40	Sense Pin 0	SP0	I	TTL
41	Enable Pin 0	EP0	O	TTL
42	Sense Pin 1	SP1	I	TTL
43	Enable Pin 1	EP1	O	TTL
44	ECL Power	V_{CC}_ECL		+5V
45	ECL Ground	GND_ECL		+0V
46	PMD Transmitter Enable	TXE	O	TTL
47	PMD Transmitter Enable Level	TEL	I	TTL
48	Reserved_0	RES_0		+0V
49	No Connect	N/C		
50	Reserved_0	RES_0		+0V
51	Reserved_0	RES_0		+0V
52	Reserved_0	RES_0		+0V
53	Reserved_0	RES_0		+0V
54	No Connect	N/C		
55	ECL Ground	GND_ECL		+0V
56	ECL Power	V_{CC}_ECL		+5V
57	Reserved_0	RES_0		+0V
58	Reserved_0	RES_0		+0V
59	PHY Port B Request Data<0>	BRD0	I	TTL
60	PHY Port B Request Data<1>	BRD1	I	TTL
61	PHY Port B Request Data<2>	BRD2	I	TTL
62	PHY Port B Request Data<3>	BRD3	I	TTL
63	PHY Port B Request Data<4>	BRD4	I	TTL
64	I/O Ground	GND_IO		+0V
65	I/O Power	V_{CC}_IO		+5V
66	PHY Port B Request Data<5>	BRD5	I	TTL
67	PHY Port B Request Data<6>	BRD6	I	TTL
68	PHY Port B Request Data<7>	BRD7	I	TTL
69	PHY Port B Request Control	BRC	I	TTL
70	PHY Port B Request Parity	BRP	O	TTL
71	~Device Reset	~RST	I	TTL
72	Read/~Write	R/~W	I	TTL
73	Chip Enable	~CE	I	TTL
74	~Interrupt	~INT	O	Open Drain
75	~Acknowledge	~ACK	O	Open Drain
76	Control Bus Address<0>	CBA0	I	TTL

8.0 Connection Diagrams (Continued)

TABLE 8-1. DP83256 100-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
77	Control Bus Address<1>	CBA1	I	TTL
78	I/O Logic Ground	GND_IO		+0V
79	I/O Logic Power	V_{CC}_IO		+5V
80	Control Bus Address<2>	CBA2	I	TTL
81	Control Bus Address<3>	CBA3	I	TTL
82	Control Bus Address<4>	CBA4	I	TTL
83	Control Bus Address<5>	CBA5	I	TTL
84	Reserved_0	RES_0		+0V
85	Reserved_1	RES_1		+5V
86	Control Bus Data<0>	CBD0	I/O	TTL
87	Core Ground	GND_CORE		+0V
88	Core Power	V_{CC}_CORE		+5V
89	Control Bus Data<1>	CBD1	I/O	TTL
90	Control Bus Data<2>	CBD2	I/O	TTL
91	Control Bus Data<3>	CBD3	I/O	TTL
92	Control Bus Data<4>	CBD4	I/O	TTL
93	Control Bus Data<5>	CBD5	I/O	TTL
94	Control Bus Data<6>	CBD6	I/O	TTL
95	Control Bus Data<7>	CBD7	I/O	TTL
96	Control Bus Data Parity	CBP	I/O	TTL
97	I/O Ground	GND_IO		+0V
98	I/O Power	V_{CC}_IO		+5V
99	Local Symbol Clock	LSC	O	TTL
100	Local Byte Clock5	LBC5	O	TTL

8.0 Connection Diagrams (Continued)

8.2 DP83256VF-AP CONNECTION DIAGRAM

For a Pinout Summary List, refer to Table 8-2.

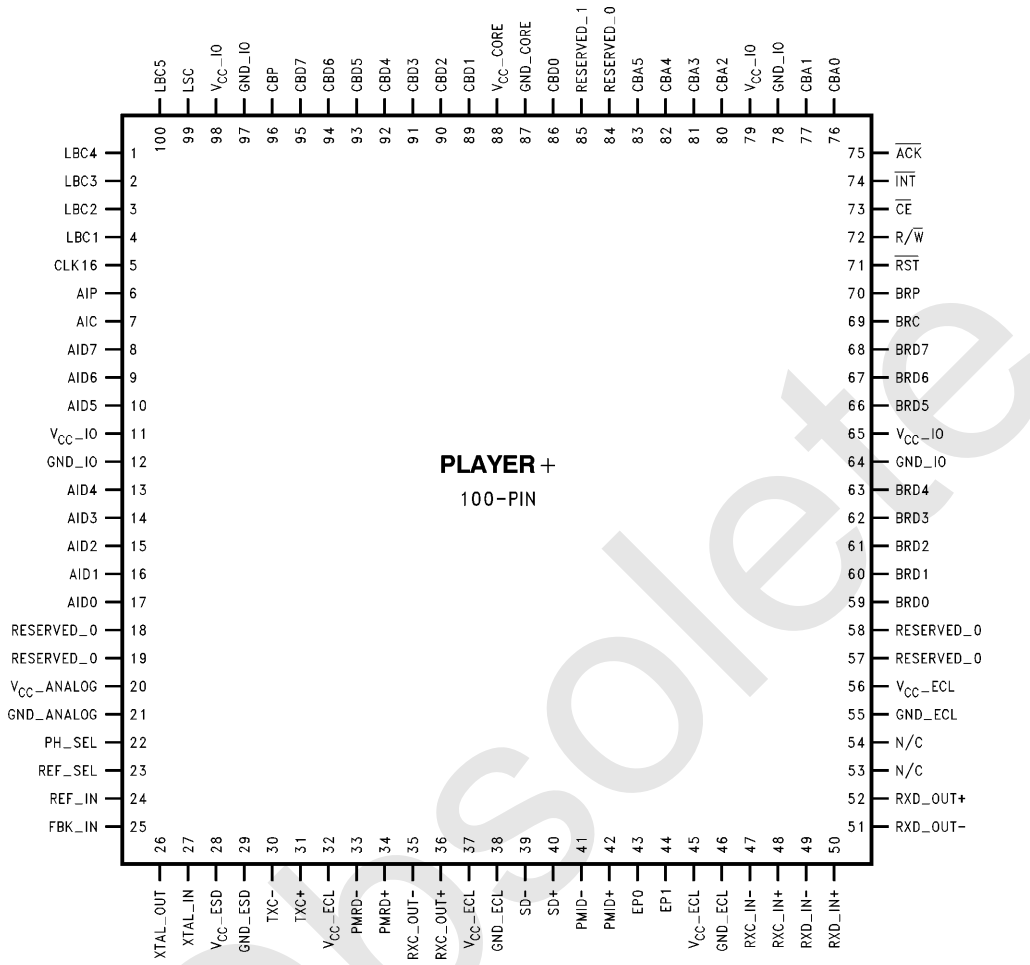

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FIGURE 8-2. DP83256VF-AP 100-Pin JEDEC Metric PQFP Pinout

8.0 Connection Diagrams (Continued)

TABLE 8-2. DP83256VF-AP 100-Pin PQFP Pinout Summary

Pin No.	Signal Name	Symbol	I/O	Pin Type
1	Local Byte Clock 4	LBC4	O	TTL
2	Local Byte Clock 3	LBC3	O	TTL
3	Local Byte Clock 2	LBC2	O	TTL
4	Local Byte Clock 1	LBC1	O	TTL
5	Clock 16/32	CLK16	O	TTL
6	PHY Port A Indicate Parity	AIP	O	TTL
7	PHY Port A Indicate Control	AIC	O	TTL
8	PHY Port A Indicate Data<7>	AID7	O	TTL
9	PHY Port A Indicate Data<6>	AID6	O	TTL
10	PHY Port A Indicate Data<5>	AID5	O	TTL
11	I/O Power	V_{CC}_IO		+5V
12	I/O Ground	GND_IO		+0V
13	PHY Port A Indicate Data<4>	AID4	O	TTL
14	PHY Port A Indicate Data<3>	AID3	O	TTL
15	PHY Port A Indicate Data<2>	AID2	O	TTL
16	PHY Port A Indicate Data<1>	AID1	O	TTL
17	PHY Port A Indicate Data<0>	AID0	O	TTL
18	Reserved_0	RES_0		+0V
19	Reserved_0	RES_0		+0V
20	ANALOG Power	V_{CC}_ANALOG		+5V
21	ANALOG Ground	GND_ANALOG		+0 V
22	Phase Select	PH_SEL	I	TTL
23	Reference Select	REF_SEL	I	TTL
24	Reference Input	REF_IN	I	TTL
25	Feedback Input	FBK_IN	I	TTL
26	Crystal Output	XTAL_OUT	O	
27	Crystal Input	XTAL_IN	I	
28	ESD Power	V_{CC}_ESD		+5V
29	ESD Ground	GND_ESD		+0V
30	Transmit Clock−	TXC−	O	ECL
31	Transmit Clock+	TXC+	O	ECL
32	ECL Power	V_{CC}_ECL		+5V
33	PMD Request Data −	PMRD−	O	ECL
34	PMD Request Data +	PMRD+	O	ECL
35	Receive Clock Out−	RXC_OUT−	O	ECL
36	Receive Clock Out+	RXC_OUT+	O	ECL
37	ECL Power	V_{CC}_ECL		+5V
38	ECL Ground	GND_ECL		+0V

8.0 Connection Diagrams (Continued)

TABLE 8-2. DP83256VF-AP 100-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
39	Signal Detect −	SD −	I	ECL
40	Signal Detect +	SD +	I	ECL
41	PMD Indicate Data −	PMID −	I	ECL
42	PMD Indicate Date +	PMID +	I	ECL
43	Enable Pin 0	EP0	O	TTL
44	Enable Pin 1	EP1	O	TTL
45	ECL Power	V_{CC}__ECL		+ 5V
46	ECL Ground	GND__ECL		+ 0V
47	Receive Clock In −	RXC__IN −	I	ECL
48	Receive Clock In +	RXC__IN +	I	ECL
49	Receive Data In −	RXD__IN −	I	ECL
50	Receive Data In +	RXD__IN +	I	ECL
51	Receive Data Out −	RXD__OUT −	O	ECL
52	Receive Data Out +	RXD__OUT +	O	ECL
53	No Connect	N/C		
54	No Connect	N/C		
55	ECL Ground	GND__ECL		+ 0V
56	ECL Power	V_{CC}__ECL		+ 5V
57	Reserved__0	RES__0		+ 0V
58	Reserved__0	RES__0		+ 0V
59	PHY Port B Request Data < 0 >	BRD0	I	TTL
60	PHY Port B Request Data < 1 >	BRD1	I	TTL
61	PHY Port B Request Data < 2 >	BRD2	I	TTL
62	PHY Port B Request Data < 3 >	BRD3	I	TTL
63	PHY Port B Request Data < 4 >	BRD4	I	TTL
64	I/O Ground	GND__IO		+ 0V
65	I/O Power	V_{CC}__IO		+ 5V
66	PHY Port B Request Data < 5 >	BRD5	I	TTL
67	PHY Port B Request Data < 6 >	BRD6	I	TTL
68	PHY Port B Request Data < 7 >	BRD7	I	TTL
69	PHY Port B Request Control	BRC	I	TTL
70	PHY Port B Request Parity	BRP	O	TTL
71	~ Device Reset	~ RST	I	TTL
72	Read/ ~ Write	R/ ~ W	I	TTL
73	Chip Enable	~ CE	I	TTL
74	~ Interrupt	~ INT	O	Open Drain
75	~ Acknowledge	~ ACK	O	Open Drain
76	Control Bus Address < 0 >	CBA0	I	TTL

8.0 Connection Diagrams (Continued)

TABLE 8-2. DP83256VF-AP 100-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
77	Control Bus Address<1>	CBA1	I	TTL
78	I/O Logic Ground	GND_IO		+0V
79	I/O Logic Power	V_{CC}_IO		+5V
80	Control Bus Address<2>	CBA2	I	TTL
81	Control Bus Address<3>	CBA3	I	TTL
82	Control Bus Address<4>	CBA4	I	TTL
83	Control Bus Address<5>	CBA5	I	TTL
84	Reserved_0	RES_0		+0V
85	Reserved_1	RES_1		+5V
86	Control Bus Data<0>	CBD0	I/O	TTL
87	Core Ground	GND_CORE		+0V
88	Core Power	V_{CC}_CORE		+5V
89	Control Bus Data<1>	CBD1	I/O	TTL
90	Control Bus Data<2>	CBD2	I/O	TTL
91	Control Bus Data<3>	CBD3	I/O	TTL
92	Control Bus Data<4>	CBD4	I/O	TTL
93	Control Bus Data<5>	CBD5	I/O	TTL
94	Control Bus Data<6>	CBD6	I/O	TTL
95	Control Bus Data<7>	CBD7	I/O	TTL
96	Control Bus Data Parity	CBP	I/O	TTL
97	I/O Ground	GND_IO		+0V
98	I/O Power	V_{CC}_IO		+5V
99	Local Symbol Clock	LSC	O	TTL
100	Local Byte Clock5	LBC5	O	TTL

8.0 Connection Diagrams (Continued)

8.3 DP83257VF CONNECTION DIAGRAM

For a Pinout Summary List, refer to Table 8-3.

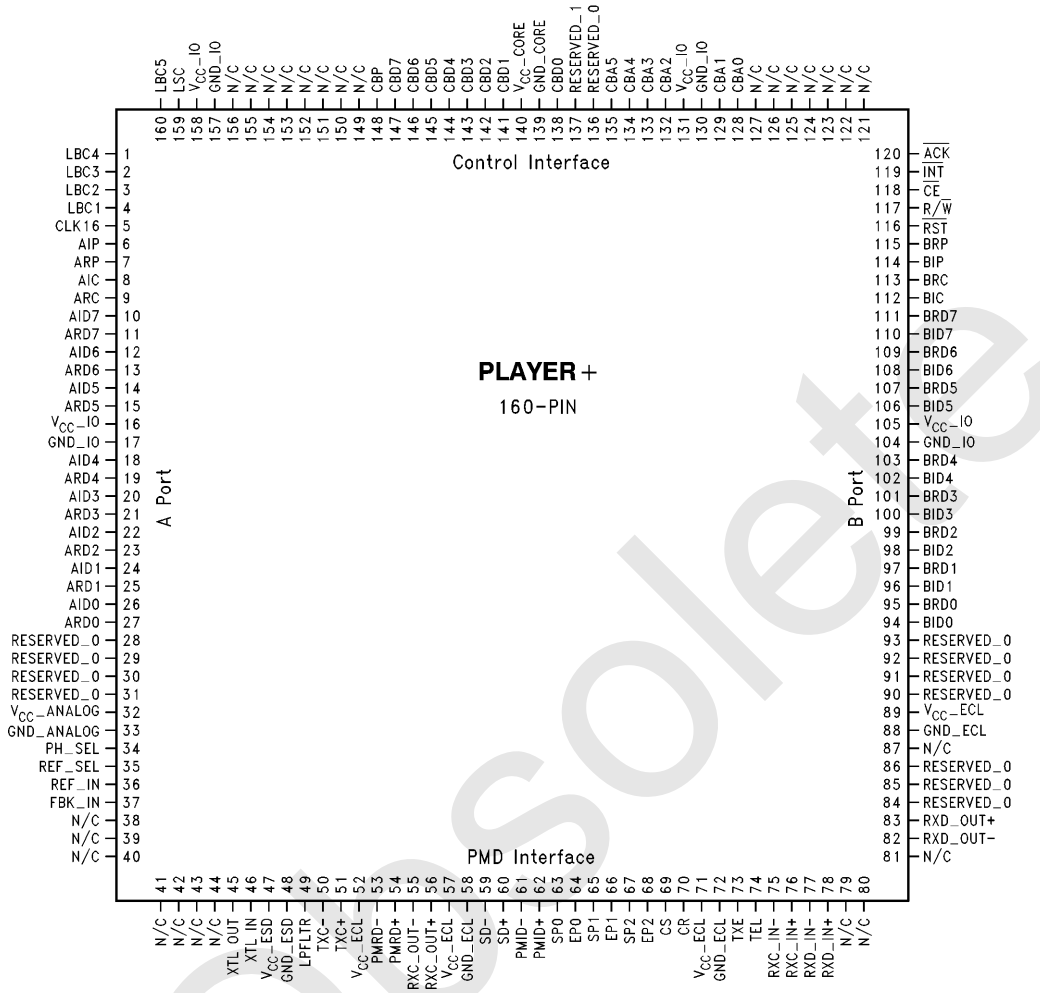

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FIGURE 8-3. DP83257VF 160-Pin JEDEC Metric PQFP Pinout

8.0 Connection Diagrams (Continued)

TABLE 8-3. DP83257 160-Pin PQFP Pinout Summary

Pin No.	Signal Name	Symbol	I/O	Pin Type
1	Local Byte Clock 4	LBC4	O	TTL
2	Local Byte Clock 3	LBC3	O	TTL
3	Local Byte Clock 2	LBC2	O	TTL
4	Local Byte Clock 1	LBC1	O	TTL
5	Clock 16/32	CLK16	O	TTL
6	PHY Port A Indicate Parity	AIP	O	TTL
7	PHY Port A Request Parity	ARP	I	TTL
8	PHY Port A Indicate Control	AIC	O	TTL
9	PHY Port A Request Control	ARC	I	TTL
10	PHY Port A Indicate Data<7>	AID7	O	TTL
11	PHY Port A Request Data<7>	ARD7	I	TTL
12	PHY Port A Indicate Data<6>	AID6	O	TTL
13	PHY Port A Request Data<6>	ARD6	I	TTL
14	PHY Port A Indicate Data<5>	AID5	O	TTL
15	PHY Port A Request Data<5>	ARD5	I	TTL
16	I/O Power	V_{CC}_IO		+5V
17	I/O Ground	GND_IO		+0V
18	PHY Port A Indicate Data<4>	AID4	O	TTL
19	PHY Port A Request Data<4>	ARD4	I	TTL
20	PHY Port A Indicate Data<3>	AID3	O	TTL
21	PHY Port A Request Data<3>	ARD3	I	TTL
22	PHY Port A Indicate Data<2>	AID2	O	TTL
23	PHY Port A Request Data<2>	ARD2	I	TTL
24	PHY Port A Indicate Data<1>	AID1	O	TTL
25	PHY Port A Request Data<1>	ARD1	I	TTL
26	PHY Port A Indicate Data<0>	AID0	O	TTL
27	PHY Port A Request Data<0>	ARD0	I	TTL
28	Reserved_0	RES_0		+0V
29	Reserved_0	RES_0		+0V
30	Reserved_0	RES_0		+0V
31	Reserved_0	RES_0		+0V
32	ANALOG Power	V_{CC}_ANALOG		+5V
33	ANALOG Ground	GND_ANALOG		+0V
34	Phase Select	PH_SEL	I	TTL
35	Reference Select	REF_SEL	I	TTL
36	Reference Input	REF_IN	I	TTL
37	Feedback Input	FBK_IN	I	TTL
38	No Connect	N/C		

8.0 Connection Diagrams (Continued)

TABLE 8-3. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
39	No Connect	N/C		
40	No Connect	N/C		
41	No Connect	N/C		
42	No Connect	N/C		
43	No Connect	N/C		
44	No Connect	N/C		
45	Crystal Output	XTAL_OUT	O	
46	Crystal Input	XTAL_IN	I	
47	ESD Power	V_{CC}_ESD		+5V
48	ESD Ground	GND_ESD		+0V
49	Loop Filter	LPFLTR	O	
50	Transmit Clock−	TXC−	O	ECL
51	Transmit Clock+	TXC+	O	ECL
52	ECL Power	V_{CC}_ECL		+5V
53	PMD Request Data−	PMRD−	O	ECL
54	PMD Request Data +	PMRD+	O	ECL
55	Receive Clock Out−	RXC_OUT−	O	ECL
56	Receive Clock Out+	RXC_OUT+	O	ECL
57	ECL Power	V_{CC}_ECL		+5V
58	ECL Ground	GND_ECL		+0V
59	Signal Detect−	SD−	I	ECL
60	Signal Detect+	SD+	I	ECL
61	PMD Indicate Data−	PMID−	I	ECL
62	PMD Indicate Data+	PMID+	I	ECL
63	Sense Pin 0	SP0	I	TTL
64	Enable Pin 0	EP0	O	TTL
65	Sense Pin 1	SP1	I	TTL
66	Enable Pin 1	EP1	O	TTL
67	Sense Pin 2	SP2	I	TTL
68	Enable Pin 2	EP2	O	TTL
69	Cascade Start	CS	I	TTL
70	Cascade Ready	CR	O	Open Drain
71	ECL Power	V_{CC}_ECL		+5V
72	ECL Ground	GND_ECL		+0V
73	PMD Transmitter Enable	TXE	O	TTL
74	PMD Transmitter Enable Level	TEL	I	TTL
75	Receive Clock In−	RXC_IN−	I	ECL
76	Receive Clock In+	RXC_IN+	I	ECL

8.0 Connection Diagrams (Continued)

TABLE 8-3. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
77	Receive Data In−	RXD__IN−	I	ECL
78	Receive Data In+	RXD__IN+	I	ECL
79	No Connect	N/C		
80	No Connect	N/C		
81	No Connect	N/C		
82	Receive Data Out−	RXD__OUT−	O	ECL
83	Receive Data Out+	RXD__OUT+	O	ECL
84	Reserved__0	RES__0		+0V
85	Reserved__0	RES__0		+0V
86	Reserved__0	RES__0		+0V
87	No Connect	N/C		
88	ECL Ground	GND__ECL		+0V
89	ECL Power	V_{CC}__ECL		+5V
90	Reserved__0	RES__0		+0V
91	Reserved__0	RES__0		+0V
92	Reserved__0	RES__0		+0V
93	Reserved__0	RES__0		+0V
94	PHY Port B Indicate Data<0>	BID0	O	TTL
95	PHY Port B Request Data<0>	BRD0	I	TTL
96	PHY Port B Indicate Data<1>	BID1	O	TTL
97	PHY Port B Request Data<1>	BRD1	I	TTL
98	PHY Port B Indicate Data<2>	BID2	O	TTL
99	PHY Port B Request Data<2>	BRD2	I	TTL
100	PHY Port B Indicate Data<3>	BID3	O	TTL
101	PHY Port B Request Data<3>	BRD3	I	TTL
102	PHY Port B Indicate Data<4>	BID4	O	TTL
103	PHY Port B Request Data<4>	BRD4	I	TTL
104	I/O Ground	GND__IO		+0V
105	I/O Power	V_{CC}__IO		+5V
106	PHY Port B Indicate Data<5>	BID5	O	TTL
107	PHY Port B Request Data<5>	BRD5	I	TTL
108	PHY Port B Indicate Data<6>	BID6	O	TTL
109	PHY Port B Request Data<6>	BRD6	I	TTL
110	PHY Port B Indicate Data<7>	BID7	O	TTL
111	PHY Port B Request Data<7>	BRD7	I	TTL
112	PHY Port B Indicate Control	BIC	O	TTL
113	PHY Port B Request Control	BRC	I	TTL
114	PHY Port B Indicate Parity	BIP	O	TTL

8.0 Connection Diagrams (Continued)

TABLE 8-3. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
115	PHY Port B Request Parity	BRP	I	TTL
116	~ Device Reset	~ RST	I	TTL
117	Read/ ~ Write	R/ ~ W	I	TTL
118	Chip Enable	~ CE	I	TTL
119	~ Interrupt	~ INT	O	Open Drain
120	~ Acknowledge	~ ACK	O	Open Drain
121	No Connect	N/C		
122	No Connect	N/C		
123	No Connect	N/C		
124	No Connect	N/C		
125	No Connect	N/C		
126	No Connect	N/C		
127	No Connect	N/C		
128	Control Bus Address<0>	CBA0	I	TTL
129	Control Bus Address<1>	CBA1	I	TTL
130	I/O Logic Ground	GND_IO		+0V
131	I/O Logic Power	V_{CC}_IO		+5V
132	Control Bus Address<2>	CBA2	I	TTL
133	Control Bus Address<3>	CBA3	I	TTL
134	Control Bus Address<4>	CBA4	I	TTL
135	Control Bus Address<5>	CBA5	I	TTL
136	Reserved_0	RES_0		+0V
137	Reserved_1	RES_1		+5V
138	Control Bus Data<0>	CBD0	I/O	TTL
139	Core Ground	GND_CORE		+0V
140	Core Power	V_{CC}_CORE		+5V
141	Control Bus Data<1>	CBD1	I/O	TTL
142	Control Bus Data<2>	CBD2	I/O	TTL
143	Control Bus Data<3>	CBD3	I/O	TTL
144	Control Bus Data<4>	CBD4	I/O	TTL
145	Control Bus Data<5>	CBD5	I/O	TTL
146	Control Bus Data<6>	CBD6	I/O	TTL
147	Control Bus Data<7>	CBD7	I/O	TTL
148	Control Bus Data Parity	CBP	I/O	TTL
149	No Connect	N/C		
150	No Connect	N/C		
151	No Connect	N/C		

8.0 Connection Diagrams (Continued)

TABLE 8-3. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
152	No Connect	N/C		
153	No Connect	N/C		
154	No Connect	N/C		
155	No Connect	N/C		
156	No Connect	N/C		
157	I/O Ground	GND_IO		+0V
158	I/O Power	V_{CC}_IO		+5V
159	Local Symbol Clock	LSC	O	TTL
160	Local Byte Clock5	LBC5	O	TTL

9.0 Package Information

The information contained in this section describes the two packages used for the PLAYER+ device.
Land pattern information is provided to assist in surface mount layout using each of the available PLAYER+ device packages.
Mechanical drawings of each of the packages are also provided.

9.1 LAND PATTERNS

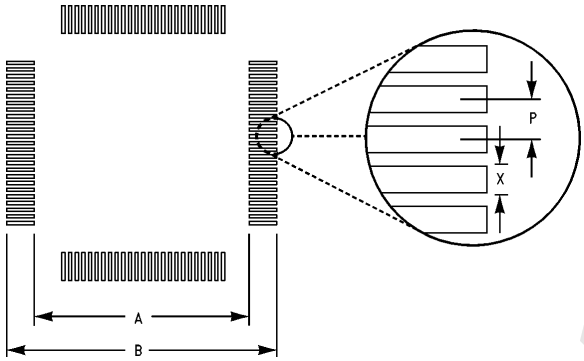

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FIGURE 9-1. Layout Land Patterns

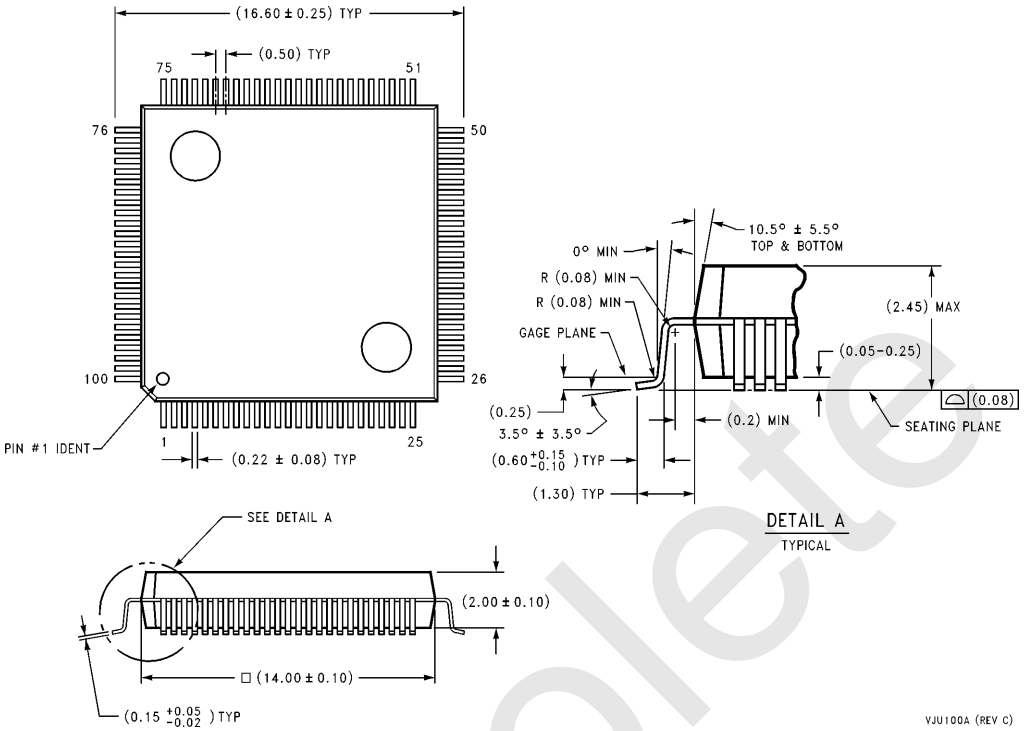
TABLE 9-1. Layout Land Pattern Dimensions

Device	A (mm)	B (mm)	P (mm)	X (mm)
DP83256VF and DP83256VF-AP 14mm x 14mm x 2.0mm 100-lead JEDEC FPQFP	14.60	18.45	0.50	0.35
DP83257VF 28mm x 28mm x 3.42mm 160-lead JEDEC MQFP	28.90	33.40	0.65	0.45

9.2 MECHANICAL DRAWINGS

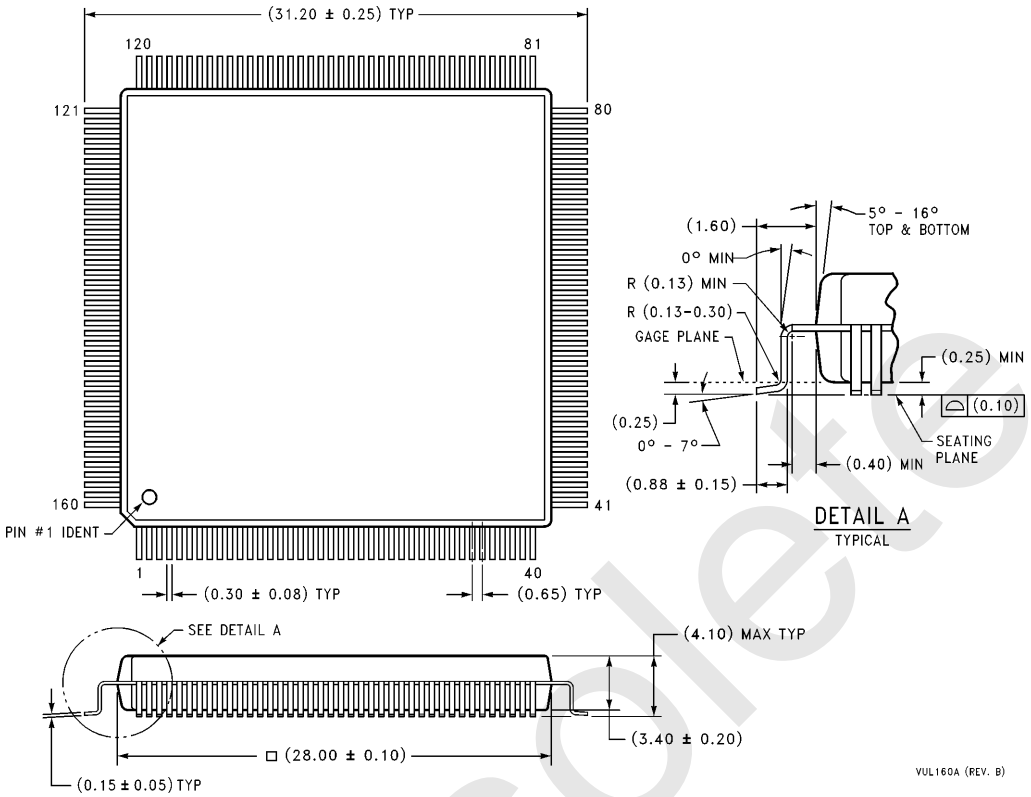
The following two pages contain the mechanical drawings for each of the available PLAYER+ device packages.

Physical Dimensions millimeters



Plastic Quad Flatpak (VJU)
Order Number DP83256VF and DP83256VF-AP
NS Package Number VJU100A

Physical Dimensions millimeters (Continued)



Plastic Quad Flatpak (V)
Order Number DP83257VF
NS Package Number VUL160A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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