# 64-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

## *IDT49C466*
## *IDT49C466A*

## FEATURES:

- 64-bit wide Flow-thruEDC™
- Separate System and Memory Data Input/Output Buses
  - Error Detect Time: 10ns
  - Error Correct Time: 15ns
- Corrects all single bit errors; Detects all double bit errors and some multiple bit errors
- Configurable 16-deep bus read/write FIFOs with flags
- Simultaneous check bit generation and correction of memory data
- Supports partial word writes on byte boundaries
- Low noise output
- Sophisticated error diagnostics and error logging
- Parity generation on system data bus
- 208-pin Plastic Quad Flatpack

## DESCRIPTION:

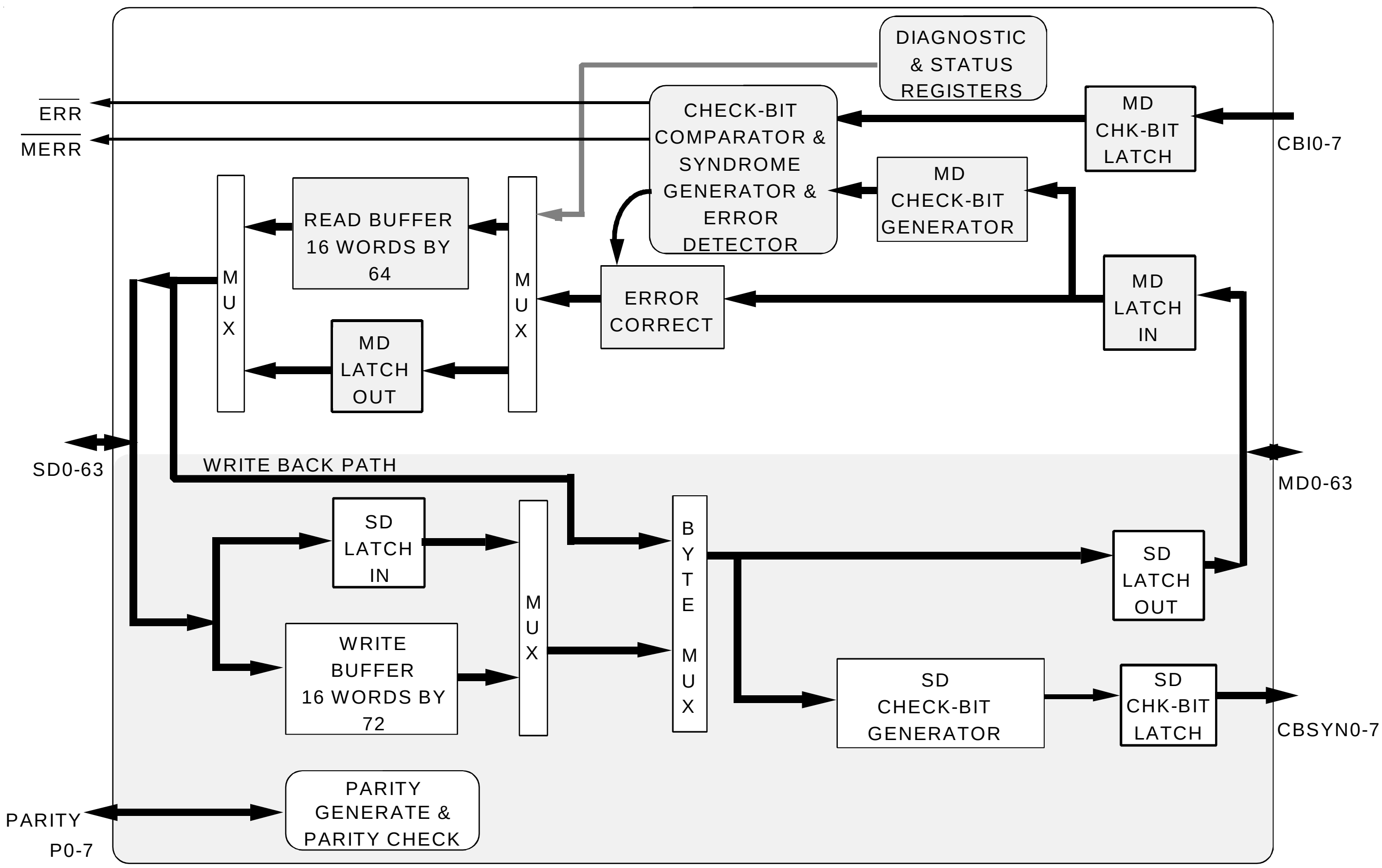
The IDT49C466/A 64-bit Flow-thruEDC is a high-speed error detection and correction unit that ensures data integrity in memory systems. The flow-thru architecture, with separate system and memory data buses, is ideally suited for pipelined memory systems.

Implementing a modified Hamming code, the IDT49C466/A corrects all single bit hard and soft errors, and detects all double bit errors. The read/write FIFOs can store up to sixteen words. FIFO full and empty flags indicate whether additional data can be written to or read from the EDC.

Check bit generation for partial word writes on byte boundaries is supported on the IDT49C466/A.

Diagnostic features include a check bit register, syndrome registers, a four bit error counter which logs up to fifteen errors, and an error data register which stores the complete error data word. Parity can be generated and checked on the system bus by the IDT49C466/A.

## FUNCTIONAL BLOCK DIAGRAM

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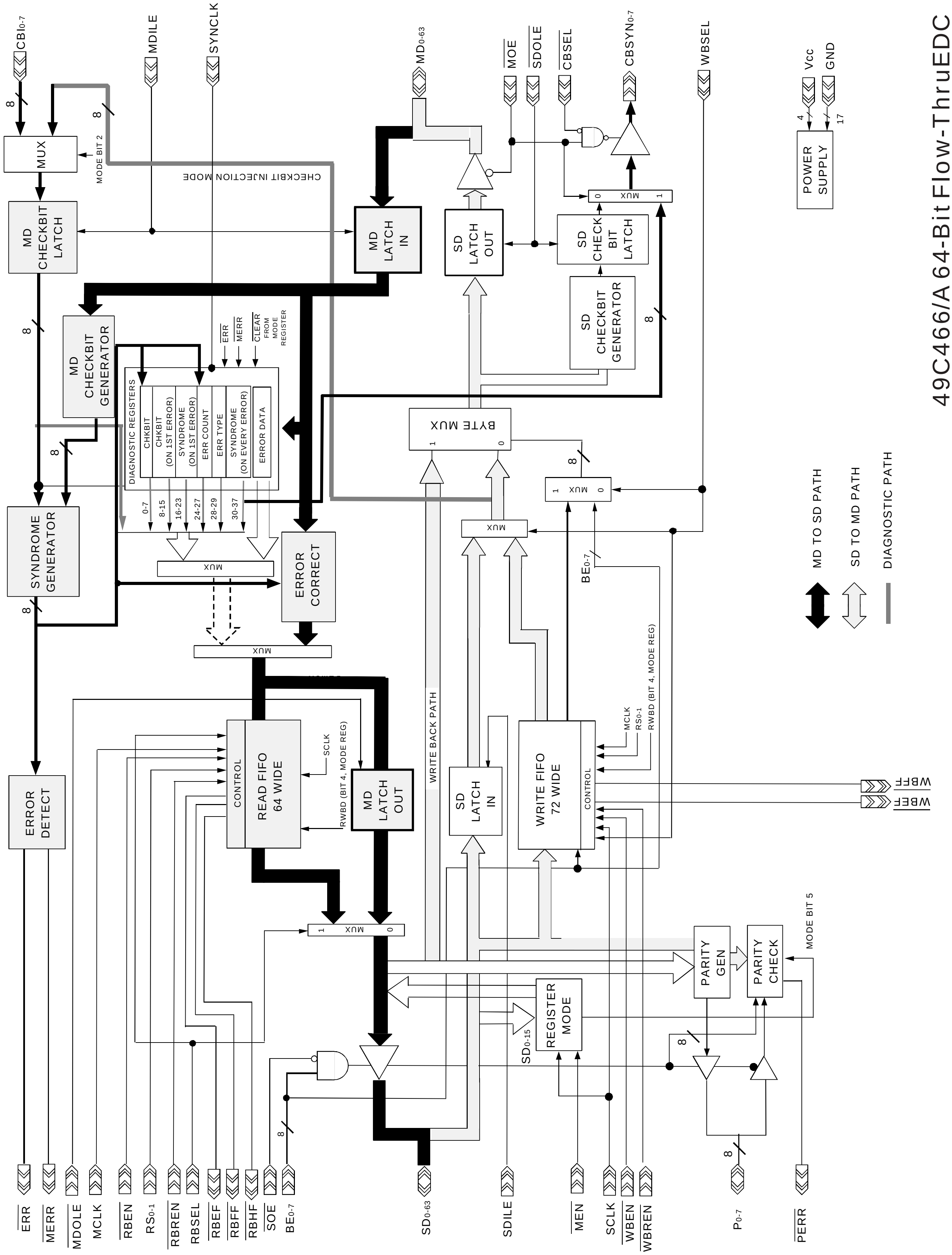
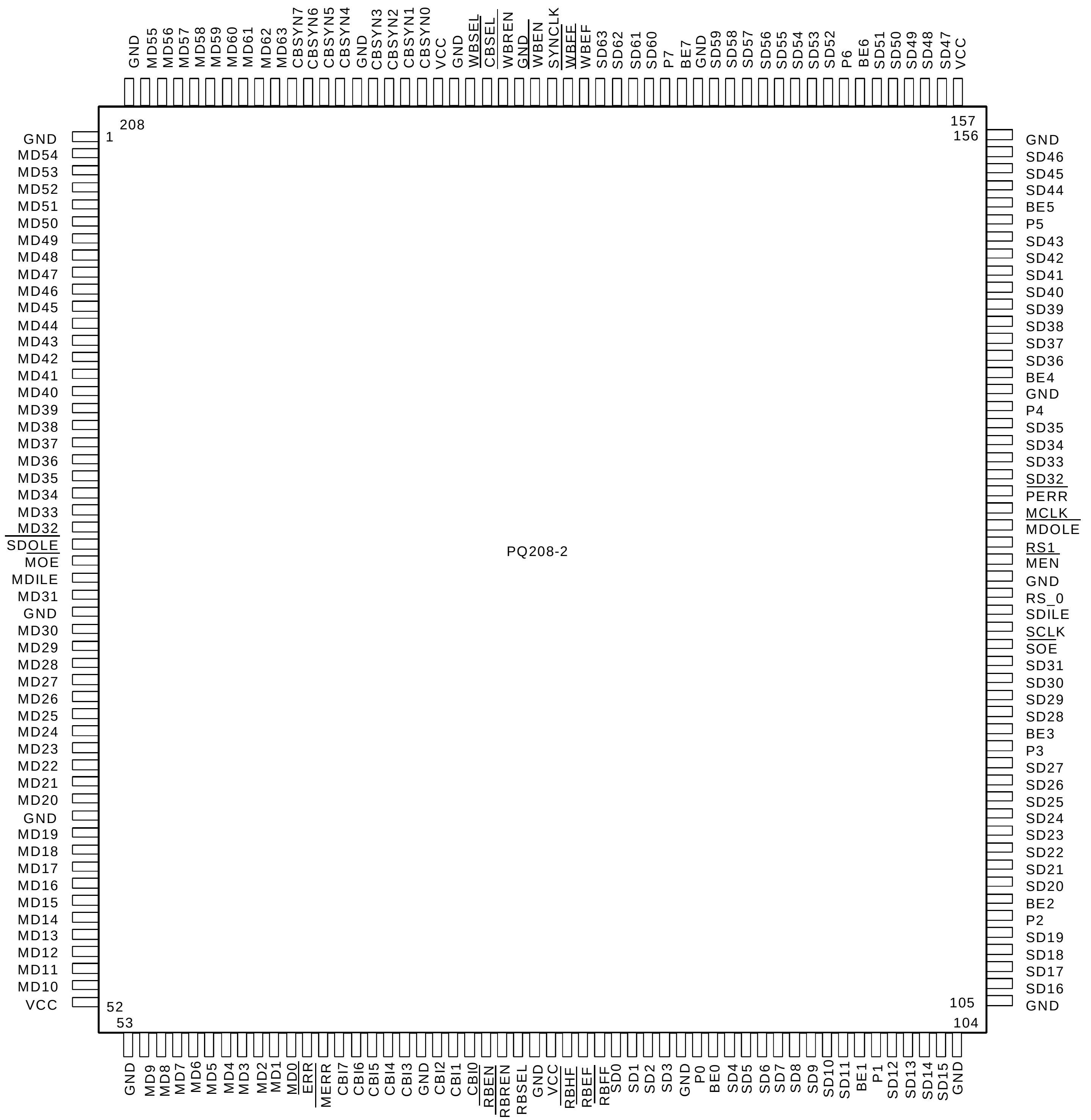

49C466/A 64-Bit Flow-ThruEDC
MD TO SD PATH
SD TO MD PATH
DIAGNOSTIC PATH
MUX
MD CHECKBIT LATCH
MD CHECKBIT GENERATOR
SYNDROME GENERATOR
ERROR DETECT
ERROR CORRECT
MD LATCH IN
MD LATCH OUT
READ FIFO 64 WIDE
CONTROL
SD LATCH OUT
SD LATCH IN
SD CHECK BIT LATCH
SD CHECKBIT GENERATOR
BYTE MUX
WRITE FIFO 72 WIDE
REGISTER MODE
PARITY GEN
PARITY CHECK
POWER SUPPLY
DIAGNOSTIC REGISTERS
CHKBIT
CHKBIT (ON 1ST ERROR)
SYNDROME (ON 1ST ERROR)
ERR COUNT
ERR TYPE
SYNDROME (ON EVERY ERROR)
ERROR DATA
CHECKBIT INJECTION MODE
MODE BIT 2
MODE BIT 5
WRITE BACK PATH
RWBD (BIT 4, MODE REG)
CBI0-7
MDILE
SYNCLK
MD0-63
MOE
SDOLE
CBSEL
CBSYN0-7
WBSEL
Vcc
GND
WBFF
WBEF
BE0-7
ERR
MERR
MDOLE
MCLK
RBEN
RS0-1
RBREN
RBSEL
RBEF
RBFF
RBHF
SOE
SD0-63
SDILE
MEN
SCLK
WBEN
WBREN
P0-7
PERR
SD0-15

## PIN CONFIGURATION




**PQFP**
**TOP VIEW**

## PIN DESCRIPTION

| Pin Name | I/O | Description |
|---|---|---|
| | | |
| $SD_{0-63}$ | I/O | **System Data Bus:** is a bidirectional 64-bit bus interfacing to the system or CPU. When System Output Enable, $\overline{SOE}$, is HIGH or Byte Enable, $BE_{0-7}$, is LOW, data can be input. When System Output Enable, $\overline{SOE}$, is LOW and Byte Enable, $BE_{0-7}$, is HIGH, the SD bus output drivers are enabled. |
| $MD_{0-63}$ | I/O | **Memory Data Bus:** is a bidirectional 64-bit bus interfacing to the memory. During a read cycle, ($\overline{MOE}$ HIGH) memory data is input for error detection and correction. Data is output on the Memory Data Bus, when $\overline{MOE}$ is LOW. |
| $CBI_{0-7}$ | I | **Check Bit Inputs:** interface to the check bit memory. |
| $CBSYN_{0-7}$ | O | **Check Bit/Syndrome Output:** when $\overline{MOE}$ is LOW, the generated check bits are output. When CBSEL is HIGH and $\overline{MOE}$ is HIGH, the syndrome bits are output. The bus is tristated when $\overline{MOE}$ = 1 and CBSEL = 0. |
| $P_{0-7}$ | I/O | **Parity for bytes 0 to 7:** these pins are parity inputs when the corresponding Byte Enable (BE) is LOW or $\overline{SOE}$ is HIGH, and are used to generate the parity error signal ($\overline{PERR}$). These pins are outputs when the corresponding Byte Enable (BE) is HIGH and $\overline{SOE}$ is LOW. |
| **Control Inputs** | | |
| $\overline{SOE}$ | I | **System Output Enable:** enables system data bus output drivers if the corresponding Byte Enable ($BE_{0-7}$) is HIGH. |
| $BE_{0-7}$ | I | **Byte Enable:** is used along with $\overline{SOE}$ to enable the System Data outputs for a particular byte. For example, if $BE_1$ is HIGH, the System data outputs for byte 1 ($SD_{8-15}$) are enabled. The $BE_{0-7}$ pins also control the byte mux. If a particular BE is HIGH during a memory read cycle, that byte is fed back to the memory data bus. This is used during partial word write operations and writing corrected data back to memory. |
| $\overline{MOE}$ | I | **Memory Output Enable:** when LOW, enables the output buffers of the memory data bus (MD) and CBSYN bus. It also controls the CBSYN mux. When LOW, checkbits are selected, when HIGH, syndrome is selected. |
| MDILE | I | **Memory Data Input Latch Enable:** on the HIGH-to-LOW transition, latches MD and CBI in MD input latch and MD check bit latch respectively. The latches are transparent when MDILE is HIGH. |
| $\overline{MDOLE}$ | I | **Memory Data Output Latch Enable:** latches data in the MD output latch on the LOW-to-HIGH transition of $\overline{MDOLE}$. When $\overline{MDOLE}$ is LOW, the MD output latch is transparent. |
| $\overline{SDOLE}$ | I | **System Data Output Latch Enable:** latches data in the SD output latch and the SD checkbit latch on the LOW-to-HIGH transition of $\overline{SDOLE}$. The latch is transparent when $\overline{SDOLE}$ is LOW. |
| SDILE | I | **System Data Input Latch Enable:** latches SD in the SD input latch on the HIGH-to-LOW transition. When SDILE is HIGH, the SD input latch is transparent. |
| WBSEL | I | **Write FIFO Select:** when HIGH, the write FIFO is selected. When WBSEL is LOW, the SD input latch is selected. |
| $\overline{WBEN}$ | I | **Write FIFO Enable:** when LOW, allows SD data to be written to the write FIFO on the SCLK rising edge. |
| $\overline{WBREN}$ | I | **Write FIFO Read Enable:** when LOW, allows data to be read from the the write FIFO on MCLK rising edge. |
| $RS_{0-1}$ | I | **Reset and Select pins** (read and write FIFO FIFOs)<br>$RS_1$ $RS_0$ Function<br>0 0 Reset 16-deep FIFO or first 8-deep FIFO<br>0 1 Reset second 8-deep FIFO<br>1 0 Select 16-deep FIFO or first 8-deep FIFO<br>1 1 Select second 8-deep FIFO |

## PIN DESCRIPTION (cont.)

| Pin Name | I/O | Description |
|---|---|---|
| RBSEL | I | **Read FIFO Select:** when HIGH, read FIFO is selected (data goes through read FIFO, not MD output latch). When LOW, the MD output latch is selected. |
| $\overline{\mathrm{RBEN}}$ | I | **Read FIFO Enable:** when LOW, allows data to be written into the read FIFO on the LOW-to-HIGH transition of the memory clock. |
| $\overline{\mathrm{RBREN}}$ | I | **Read FIFO Enable:** when LOW, allows data to be read from the read FIFO on the LOW-to-HIGH transition of SCLK. |
| $\overline{\mathrm{CBSEL}}$ | I | **Checkbit Syndrome Output Enable:** controls the CBSYN output buffer.When HIGH, the buffer is enabled. When CBSEL is LOW, $\overline{\mathrm{MOE}}$ controls the buffer. |
| $\overline{\mathrm{MEN}}$ | I | **Mode Enable Input:** when LOW, $SD_{0-15}$ is loaded into the EDC mode register on the LOW-to-HIGH transition of the SCLK. This pin must be held LOW for the entire SCLK HIGH period, as shown in Figure 4. |
| **Clock Inputs** | | |
| MCLK | I | **Memory Clock:** on the LOW-to-HIGH transition of MCLK, memory data is written to the read FIFO when $\overline{\mathrm{RBEN}}$ is LOW. Data is read from the write FIFO when $\overline{\mathrm{WBREN}}$ is LOW, on the LOW-to-HIGH transition of MCLK. |
| SCLK | I | **System Clock:** on the LOW-to-HIGH transition of the SCLK, data is read from the read FIFO when $\overline{\mathrm{RBREN}}$ is LOW. Data on the system data bus is written into the write FIFO when $\overline{\mathrm{WBEN}}$ is LOW on the LOW-to-HIGH transition of SCLK. Clocks data into mode register when $\overline{\mathrm{MEN}}$ is LOW. |
| SYNCLK | I | **Syndrome Clock:** used to load diagnostic registers. When an error occurs, Error Counter is incremented on the rising SYNCLK edge (up to 15 errors). On the first error after a diagnostic reset, SYNCLK rising edge clocks data into Check Bit, Syndrome, Error Type and Error Data registers. One of the syndrome registers has new data clocked in on every SYNCLK rising edge. |
| **Status Outputs** | | |
| $\overline{\mathrm{WBEF}}$ | O | **Write FIFO Empty Flag:** when LOW, indicates that the write FIFO is empty. After a reset, the $\overline{\mathrm{WBEF}}$ goes LOW. |
| $\overline{\mathrm{WBFF}}$ | O | **Write FIFO Full Flag:** when LOW, indicates that the write FIFO is full. After a reset, $\overline{\mathrm{WBFF}}$ goes HIGH. |
| $\overline{\mathrm{RBEF}}$ | O | **Read FIFO Empty Flag:** when LOW, indicates that the read FIFO is empty. After a reset, the $\overline{\mathrm{RBEF}}$ goes LOW. |
| $\overline{\mathrm{RBHF}}$ | O | **Read FIFO Half-full Flag:** when LOW, indicates that there are eight or more data words (in the 16-deep configuration) or four or more data words (in the dual 8-deep configuration) in the read FIFO. The flag will return HIGH when less than eight (or four) data words are in the FIFO. |
| $\overline{\mathrm{RBFF}}$ | O | **Read FIFO Full Flag:** when LOW, indicates that the read FIFO is full. After a reset, $\overline{\mathrm{RBFF}}$ goes HIGH. |
| $\overline{\mathrm{ERR}}$ | O | **Error Flag:** when $\overline{\mathrm{ERR}}$ is LOW, a data error is indicated. The $\overline{\mathrm{ERR}}$ is not latched internally. |
| $\overline{\mathrm{MERR}}$ | O | **Multiple Error Flag:** when $\overline{\mathrm{MERR}}$ is LOW, a multiple data error is indicated. The $\overline{\mathrm{MERR}}$ is not latched internally. |
| $\overline{\mathrm{PERR}}$ | O | **Parity Error Flag:** when LOW, indicates a parity error on the system data bus input. |
| **Power Supply** | | |
| $V_{CC}$ | P | Power Supply Voltage. |
| GND | P | Ground. |

# DETAILED DESCRIPTION —

### 64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART(1, 2)

| Generated | | Participating Data Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Checkbits | Parity | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| CB0 | Even (XOR) | | X | X | X | | X | | | X | X | | X | | | X | |
| CB1 | Even (XOR) | X | X | X | | X | | X | | X | | X | | X | | | |
| CB2 | Odd (XNOR) | X | | | X | X | | | X | | X | X | | | X | | X |
| CB3 | Odd (XNOR) | X | X | | | | X | X | X | | | | X | X | X | | |
| CB4 | Even (XOR) | | | X | X | X | X | X | X | | | | | | | X | X |
| CB5 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |
| CB6 | Even (XOR) | X | X | X | X | X | X | X | X | | | | | | | | |
| CB7 | Even (XOR) | X | X | X | X | X | X | X | X | | | | | | | | |

| Generated | | Participating Data Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Checkbits | Parity | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| CB0 | Even (XOR) | | X | X | X | | X | | | X | X | | X | | | X | |
| CB1 | Even (XOR) | X | X | X | | X | | X | | X | | X | | X | | | |
| CB2 | Odd (XNOR) | X | | | X | X | | | X | | X | X | | | X | | X |
| CB3 | Odd (XNOR) | X | X | | | | X | X | X | | | | X | X | X | | |
| CB4 | Even (XOR) | | | X | X | X | X | X | X | | | | | | | X | X |
| CB5 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |
| CB6 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |
| CB7 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |

| Generated | | Participating Data Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Checkbits | Parity | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| CB0 | Even (XOR) | X | | | | X | | X | X | | | X | | X | X | | X |
| CB1 | Even (XOR) | X | X | X | | X | | X | | X | | X | | X | | | |
| CB2 | Odd (XNOR) | X | | | X | X | | | X | | X | X | | | X | | X |
| CB3 | Odd (XNOR) | X | X | | | | X | X | X | | | | X | X | X | | |
| CB4 | Even (XOR) | | | X | X | X | X | X | X | | | | | | | X | X |
| CB5 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |
| CB6 | Even (XOR) | X | X | X | X | X | X | X | X | | | | | | | | |
| CB7 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |

| Generated | | Participating Data Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Checkbits | Parity | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |
| CB0 | Even (XOR) | X | | | | X | | X | X | | | X | | X | X | | X |
| CB1 | Even (XOR) | X | X | X | | X | | X | | X | | X | | X | | | |
| CB2 | Odd (XNOR) | X | | | X | X | | | X | | X | X | | | X | | X |
| CB3 | Odd (XNOR) | X | X | | | | X | X | X | | | | X | X | X | | |
| CB4 | Even (XOR) | | | X | X | X | X | X | X | | | | | | | X | X |
| CB5 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |
| CB6 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |
| CB7 | Even (XOR) | X | X | X | X | X | X | X | X | | | | | | | | |

**NOTES:**

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit CB0 is the Exclusive-OR function of the 64 data input bits marked with an "X".
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an “X” in the table.

# DETAILED DESCRIPTION —

### 64-BIT SYNDROME DECODE TO BIT-IN-ERROR[1]

| | | | | | **HEX** | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | **S7** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | | **S6** | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | | **Syndrome** | | | **S5** | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | | **Bits** | | | **S4** | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| **HEX** | **S3** | **S2** | **S1** | **S0** | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | | * | C4 | C5 | T | C6 | T | T | 62 | C7 | T | T | 46 | T | M | M | T |
| 1 | 0 | 0 | 0 | 1 | | C0 | T | T | 14 | T | M | M | T | T | M | M | T | M | T | T | 30 |
| 2 | 0 | 0 | 1 | 0 | | C1 | T | T | M | T | 34 | 56 | T | T | 50 | 40 | T | M | T | T | M |
| 3 | 0 | 0 | 1 | 1 | | T | 18 | 8 | T | M | T | T | M | M | T | T | M | T | 2 | 24 | T |
| 4 | 0 | 1 | 0 | 0 | | C2 | T | T | 15 | T | 35 | 57 | T | T | 51 | 41 | T | M | T | T | 31 |
| 5 | 0 | 1 | 0 | 1 | | T | 19 | 9 | T | M | T | T | 63 | M | T | T | 47 | T | 3 | 25 | T |
| 6 | 0 | 1 | 1 | 0 | | T | 20 | 10 | T | M | T | T | M | M | T | T | M | T | 4 | 26 | T |
| 7 | 0 | 1 | 1 | 1 | | M | T | T | M | T | 36 | 58 | T | T | 52 | 42 | T | M | T | T | M |
| 8 | 1 | 0 | 0 | 0 | | C3 | T | T | M | T | 37 | 59 | T | T | 53 | 43 | T | M | T | T | M |
| 9 | 1 | 0 | 0 | 1 | | T | 21 | 11 | T | M | T | T | M | M | T | T | M | T | 5 | 27 | T |
| A | 1 | 0 | 1 | 0 | | T | 22 | 12 | T | 33 | T | T | M | 49 | T | T | M | T | 6 | 28 | T |
| B | 1 | 0 | 1 | 1 | | 17 | T | T | M | T | 38 | 60 | T | T | 54 | 44 | T | 1 | T | T | M |
| C | 1 | 1 | 0 | 0 | | T | 23 | 13 | T | M | T | T | M | M | T | T | M | T | 7 | 29 | T |
| D | 1 | 1 | 0 | 1 | | M | T | T | M | T | 39 | 61 | T | T | 55 | 45 | T | M | T | T | M |
| E | 1 | 1 | 1 | 0 | | 16 | T | T | M | T | M | M | T | T | M | M | T | 0 | T | T | M |
| F | 1 | 1 | 1 | 1 | | T | M | M | T | 32 | T | T | M | 48 | T | T | M | T | M | M | T |

**NOTES:**

1. The table indicates the decoding of the eight syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single data bit-in-error
   T = Two errors detected
   M = Three or more detected
   C# = The number of the single checkbits in error

# IDT49C466 OPERATION

The EDC is involved in two types of operation — memory reads and memory writes. With the IDT49C466, both these can be accomplished by utilizing either of two possible data paths — one incorporating the FIFO and the other without the FIFO. These operations are treated separately below.

### Memory Write

The involvement of the EDC in this type of operation is relatively minimal since it does not call for any error checking. It only generates the check bits associated with each 64-bit wide data word. The EDC can be in generate-detect or normal mode for this operation.

When a write operation is performed, it must be ensured that the SD output buffer (enabled by $\overline{SOE}$ and $BE_{0-7}$) is disabled so that no attempt is made to simultaneously transfer read data onto the System Data (SD) Bus.

When the write FIFO (WFIFO) is bypassed (WBSEL LOW), data passes through the SD Latch In. To latch data, the SDILE signal should be pulled LOW. The special case of a partial word write or byte merge is discussed later. Here it is assumed that all 64 bits are being written. Consequently, $BE_{0-7}$ must all be LOW.

The data is fed to the SD Checkbit generator where appropriate checkbits are generated. Both system data and the generated checkbits can be latched by pulling the $\overline{SDOLE}$ signal HIGH. Asserting $\overline{MOE}$ enables the MD output buffer and data is output to the Memory Data (MD) bus. $\overline{CBSEL}$ (=1) or $\overline{MOE}$(=0) need to be asserted to enable the CBSYN output buffer and output checkbits on $CBSYN_{0-7}$.

When the write FIFO is selected (WBSEL = 1), instead of asserting SDILE, $\overline{WBEN}$ is asserted and data is clocked into the write FIFO on the rising edge of SCLK. $\overline{WBFF}$ is asserted when the WFIFO is full and this inhibits further write attempts (see section on "Clock Skew" and "R/W FIFO Operation at Boundaries") to the WFIFO. When $\overline{WBREN}$ is asserted, data can be clocked out of the write FIFO on the rising edge of MCLK. $\overline{WBEF}$ is asserted when the WFIFO is empty and this inhibits further read attempts (see section on "Clock Skew") from the WFIFO.

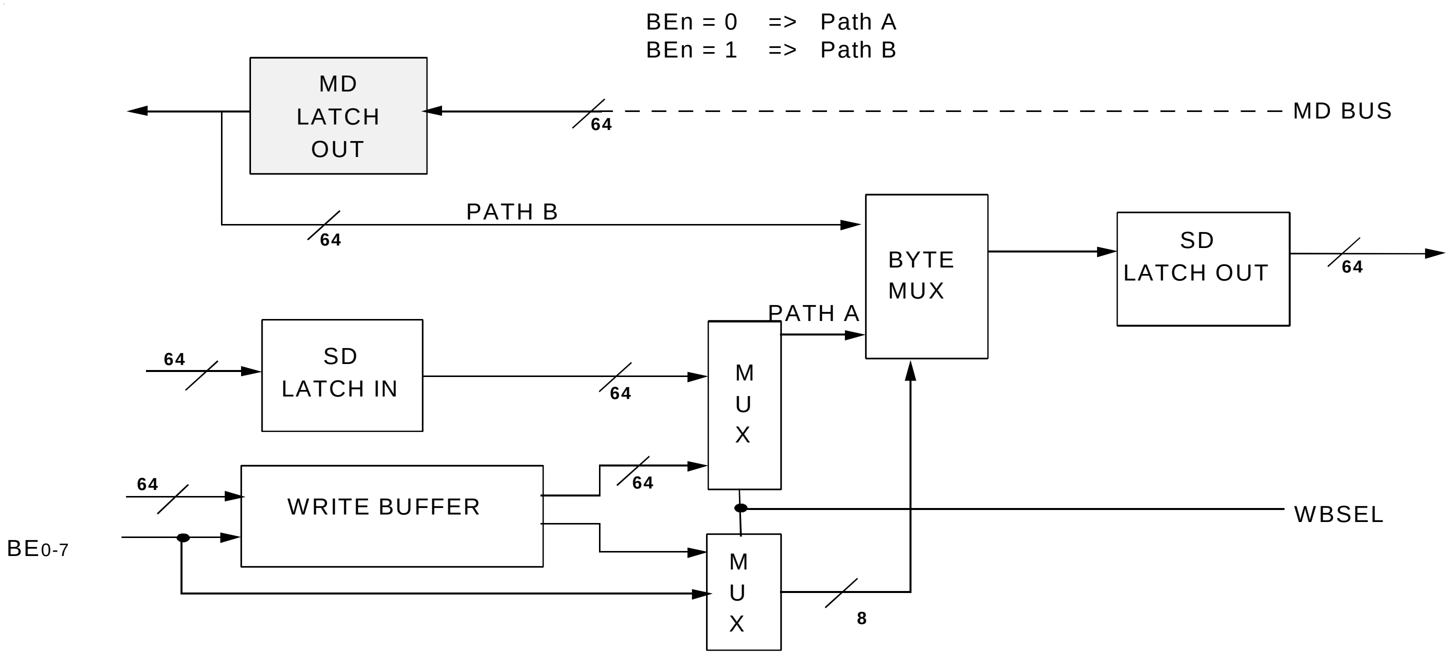



**Figure 1. Byte Merge**

## Memory Read

During a memory read, data and the corresponding input checkbits are read from the MD bus and CBI0-7, respectively. The memory and checkbit data may both be latched as they come in (MD Latch In and MD Checkbit latch) by the MDILE signal. Memory data is sent to the MD checkbit generator (where checkbits corresponding to the input data are generated) and to the error correct circuitry. The generated checkbits are X-ORed with the input checkbits to produce the syndrome word. This is sent to the error correction circuitry which generates the corrected data (normal mode). The corrected data is output to the SD bus via either of two data paths. When RBSEL is LOW, data flows through MD Latch Out. Pulling $\overline{\text{MDOLE}}$ HIGH latches this data. The output buffer is enabled by asserting $\overline{\text{SOE}}$ (=0) and BE0-7 (=1). Corrected data can be written back to memory by enabling the MD output buffer. In order to ensure selection of the write back path (Path B in figure 1) at the byte mux, BEO-7 should be all 1's while WBSEL = 0. If WBSEL = 1, buffered BEO-7 from the output of the write FIFO controls the byte mux.

If the read FIFO (RFIFO) is selected (RBSEL HIGH), data is clocked into the FIFO (Read_FIFO Write) when $\overline{\text{RBEN}}$ is LOW, on the rising edge of MCLK. $\overline{\text{RBFF}}$ is asserted when the RFIFO is full and this inhibits further write attempts to the RFIFO (see section on "Clock Skew" and "R/W FIFO operation at Boundaries"). Data is clocked out of the FIFO (Read_FIFO Read) when $\overline{\text{RBREN}}$ is LOW on the rising edge of SCLK. $\overline{\text{RBEF}}$ is asserted when the RFIFO is empty and this inhibits further read attempts (see section on "Clock Skew") from the RFIFO.

**Note**: In case of multiple error, SD should be ignored in correct mode.

## Clock Skew

A skew between the read and write clocks, as specified by tskew, is recommended. This specification is not a stringent one, in the manner of setup and hold times, but is important in preempting latencies at FIFO boundaries. For example – When a word is written to an empty FIFO, there is a finite delay before the FIFO is recognized as no longer being empty and hence allowing a read from the same FIFO. Similarly when a word is read from a full FIFO, there is a delay before a write can successfully be attempted. The tskew specification accounts for these cases. During cycles other than on full/empty FIFO boundaries, the clock skew is not required and the device functions correctly even when the reads and writes occur simultaneously. If the tskew specification is ignored and SCLK and MCLK were permanently tied together, there is an extra cycle latency in the cases mentioned above. Clock skew violation is illustrated in Figure 13.

## FIFO Write Latency

The first data written to either of the (read or write) FIFOs, after the FIFO is reset, suffers a single clock latency. Data that is set-up with respect to the first clock is ignored and the data that is set-up with respect to the second clock edge after the reset, is stored as the first data in the FIFO (Refer to Figures 9 and 10). The empty-flag is deasserted after this second clock edge and 15 more data words (in a 16 deep configuration) can be written to the FIFO after this.

The latency can be reduced or eliminated by providing a "dummy" or "set-up" clock edge before the actual write to the FIFO. The dummy write clock can be provided any time after reset and before the next buffer write operation takes place. The latency described here (shown in Figures 10 and 13) occurs only after a FIFO reset. In other cases where the FIFO becomes empty there is no latency.

## R/W FIFO Operation At Boundaries

In the 49C466 the write pointer is incremented on every FIFO write. Similarly the read pointer is incremented on every FIFO read. In most cases on a FIFO read, the last data read remains at the output of the FIFO, until the read pointer is further incremented. On the last (the write that fills the FIFO) FIFO write after the FIFO read, however, this last read data is overwritten by the 16th write following the empty condition and consequently the data at the FIFO output is liable to change. The situation is depicted in the diagram below.

The diagram in figure 2 progresses from the FIFO initialization(reset) through a sequence of write operations. After the first write, a read is executed which establishes the data at the FIFO output(AA). On the last write to the FIFO(the write that fills the FIFO), the location of the last read data is overwritten and the FIFO output changes from AA to the data just written, namely QQ.

This operation needs to be taken into account in the design of the system. In case of a burst operation where FIFO data is output at a much slower rate than the rate at which data is input and the full flag is expected to inhibit further writes, the user cannot expect the FIFO output to remain static through the 16th write of the burst. If this is a requisite to the design, the FIFO output should be latched. In the case of the write FIFO this can be accomplished on-chip by latching the FIFO output in the SD output latch. For the read FIFO, the FIFO output must be latched externally to accomplish the same thing, since there is no latch on-chip following the FIFO. If this cannot be done and the situation described above is expected to occur in normal operation, the write must be inhibited one cycle before the FIFO becomes full.

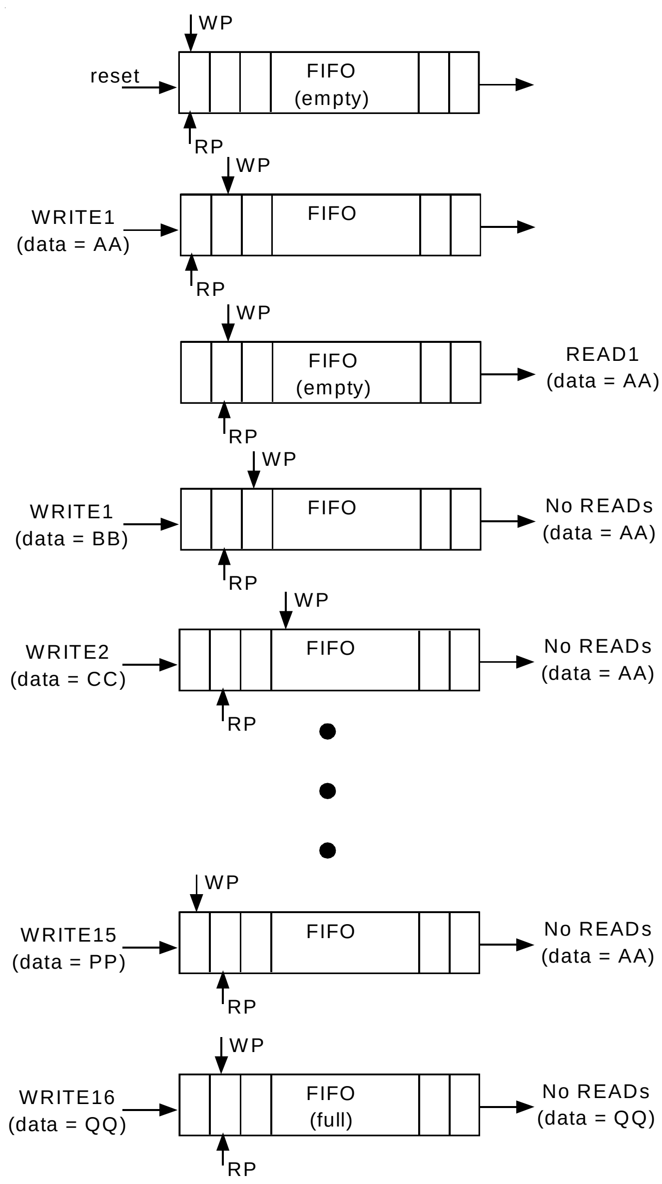



**Figure 2. R/W FIFO Operation**

### Partial Word Write/Byte Merge

Writing a word shorter than 64 bits to memory is treated as a special case. The checkbits generated for a data word shorter than 64 bits and written to a particular memory location differ from the checkbits that would be generated by the entire 64-bit data word at the same location. Hence, the byte merge operation requires reading of the contents of the memory location to be written to, merging the byte/bytes being written (from SD side) with the other component bytes previously at that memory location (from MD side), generating a checkbit word for this composite word and writing both the composite data word and the generated checkbits to memory. The BEn bits supplied by the user determine the bytes that come from SD and those that come from MD, as illustrated in Figure 1.

### EDC Modes

The IDT49C466 has five modes of operation. Refer to the Operating Mode Description table for a description of the modes.

The **Error Data Output** mode is useful for memory initialization as described below. In **Checkbit Injection mode**, the MD Checkbit Latch is loaded with data from the System Bus. This serves to verify the functioning of the EDC. Any discrepancy between the injected checkbits and generated checkbits should result in assertion of the $\overline{ERR}$, $\overline{MERR}$ signals.

These modes and certain other features such as clear, buffer configuration, etc., can be selected by appropriately loading the Mode Register. The Mode Register can be written to by asserting $\overline{MEN}$. Then $SD_{0-15}$ is clocked into the mode register on the rising edge of SCLK.

## MODE REGISTER CONFIGURATION

| 15–7 | 6 | 5 | 4 | 3 | 2–0 |
|---|---|---|---|---|---|
| UNUSED | RMODE | PSEL | RWBD | CLEAR | EDCM0-2 |

| EDCM2 | EDCM1 | EDCM0 | OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | ERROR-DATA OUTPUT MODE |
| 0 | 0 | 1 | DIAGNOSTIC-OUTPUT MODE |
| 0 | 1 | 0 | GENERATE-DETECT MODE |
| 0 | 1 | 1 | NORMAL MODE |
| 1 | 0 | 0 | CHECKBIT-INJECTION MODE |

| RMODE | OPERATION |
|---|---|
| 0 | NOP |
| 1 | READ MODE REGISTER ON SD BUS |

| RWBD | OPERATION |
|---|---|
| 0 | DUAL FIFOS (8) |
| 1 | SINGLE FIFO (16) |

| CLEAR | OPERATION |
|---|---|
| 0 | NOP |
| 1 | CLEAR ALL DIAGNOSTIC REGISTERS |

| PSEL | OPERATION |
|---|---|
| 0 | EVEN PARITY |
| 1 | ODD PARITY |

## OPERATING MODE DESCRIPTION

| Mode | Description |
|---|---|
| **MODE 0** | **Error-Data Output Mode:** This mode allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by setting the mode register "'clear"-bit. |
| **MODE 1** | **Diagnostic-Output Mode:** In this mode, contents of latch and five internal registers are read by the system for diagnostic and error logging purposes. Internal data paths allow output from the CBI LATCH to be read directly by the system bus for diagnostic purposes. The contents of the internal diagnostic checkbit register, syndrome registers, error count register and error-type register are also output on the SD bus. |
| **MODE 2** | **Generate-Detect Mode:** (Detect-Only) The EDC performs checkbit generation during a memory write, and performs error detection only during a memory read. |
| **MODE 3** | **Normal Mode:** The EDC performs checkbit generation during memory writes and error detection and correction during memory reads. |
| **MODE 4** | **Checkbit-Injection Mode:** In this mode, the checkbit latch is loaded with desired 8-bit data from the SD bus.This eight bit data passes through SD Latch in or write FIFO to the MD check bit latch. By inserting various checkbit values, correct functioning of the EDC can be verified “on-board”. The rest of the operation is similar to regular memory reads. The EDC compares the injected checkbits against the internally generated checkbits. Any discrepancy in the injected checkbits and the internally generated checkbits will cause the $\overline{ERR}$ / $\overline{MERR}$ to go LOW. |

### Memory Initialization

Memory initialization involves clearing all memory data locations and writing the corresponding checkbits (checkbits corresponding to all zero data = $0C) to checkbit memory. This can be done using the 49C466 to first create an "all-zero-data" source. This is done by setting the CLEAR bit in the mode register. This clears all diagnostic registers. Then this data can be written back to memory in the Error-Data output (Mode 0) mode. In order to wrap the all-zero data back to the MD bus, BE0-7 should be high and WBSEL =0.

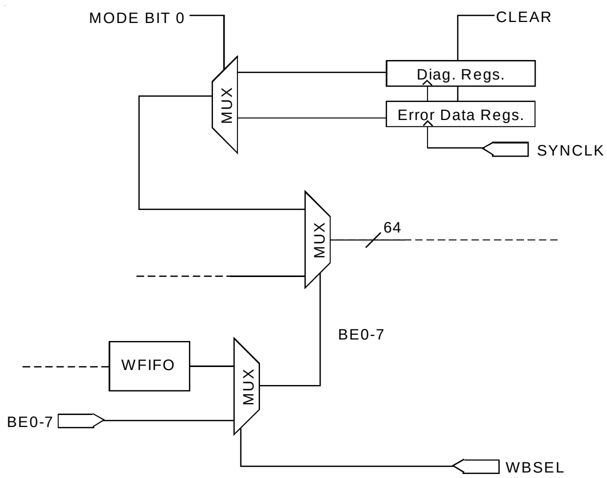
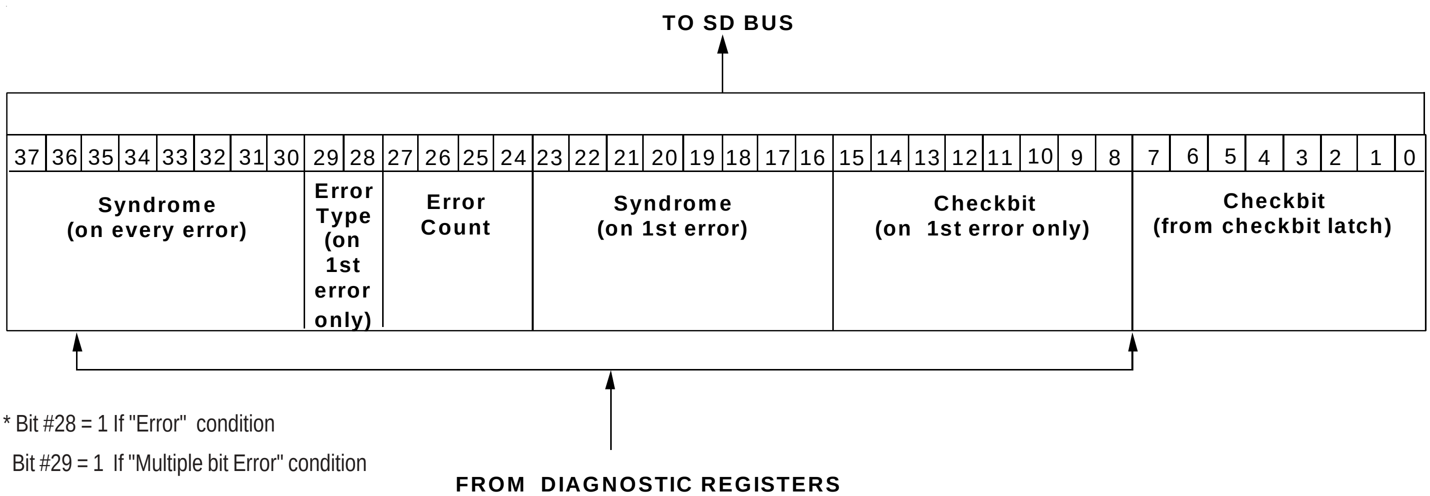



**Fig 3. Memory Initialization using Diagnostic Output/Error Data Output Mode**

## DIAGNOSTIC OUTPUT DATA FORMAT




* Bit #28 = 1 If "Error" condition

Bit #29 = 1 If "Multiple bit Error" condition

### Diagnostics

The diagnostic ability of the IDT49C466 rests on a set of 6 registers that provide error logging information. These include the checkbit register, error count register, error type register, two syndrome registers and the error data register. Data is clocked into each of these registers by SYNCLK. The error data register, checkbit register, error type register and one of the syndrome registers are reloaded only in the case of the first error after a clear. The other syndrome register and the error count register are reloaded on every error condition SYNCLK edge. The contents of the Error Data register can be read only in Error Data Output mode. The contents of the other diagnostic registers as well as the checkbit latch can be read in Diagnostic Output mode.

| DIAG. REGISTER | LOADED BY | CONDITION | OUTPUT |
|---|---|---|---|
| CHECKBIT | SYNCLK ↑ | ONLY ON 1st ERROR | SD8-15 |
| SYNDROME (On 1st ERR) | SYNCLK ↑ | ONLY ON 1st ERROR | SD16-23 |
| ERR CNT | SYNCLK ↑ | ON EVERY ERROR (Up to 15 ERRORS) | SD24-27 |
| ERR TYPE | SYNCLK ↑ | ONLY ON 1st ERROR | SD28-29 |
| SYNDROME (On every ERROR) | SYNCLK ↑ | ON EVERY ERROR | SD30-37 |

### Parity

The IDT49C466 provides a parity check and generation facility. On a memory read the EDC generates parity bits for each data byte and outputs the parity byte on the parity bus, P0-7. During a memory write, parity is checked by comparing the parity bits input on P0-7 and the parity bits generated from the input data word. A discrepancy between these two causes the $\overline{PERR}$ flag to be asserted. In the case of partial word writes, the $\overline{PERR}$ flag is based on the parity bits Px and data bytes input on SD bus.

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Rating | Com'l. | Unit |
|---|---|---|---|
| VCC | Power Supply Voltage | –0.5 to +7 | V |
| VTERM | Terminal Voltage with Respect to Ground | –0.5 to VCC + 0.5 | V |
| TBIAS | Temperature Under Bias | –55 to +125 | °C |
| TSTG | Storage Temperature | –55 to +125 | °C |
| IOUT | DC Output Current | 30 | mA |

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings for extended periods of time may affect reliability.

## CAPACITANCE (TA = +25°C, f = 1.0 MHz)

| Symbol | Parameter[1] | Conditions | | Typ. | Unit |
|---|---|---|---|---|---|
| CIN | Input Capacitance | VIN = 0V | PQFP | 5 | pF |
| COUT | Output Capacitance | VOUT = 0V | PQFP | 7 | pF |

NOTE:
1. This parameter is sampled and not 100% tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**The following conditions apply unless otherwise specified:**
**Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%**

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VIH | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| VIL | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| IIH | Input HIGH Current | VCC = Max., VIN = 2.7V | | — | 0.1 | 5 | µA |
| IIL | Input LOW Current | VCC = Max., VIN = 0.5V | | — | -0.1 | –5 | µA |
| IOZ | Off State (Hi-Z) Output Current | VCC = Max. | VO = 0V | — | -0.1 | –10 | µA |
| | | | VO = 3V | — | 0.1 | 10 | |
| IOS | Short Circuit Current | VCC = Max.[3], VOUT= 0V | | –20 | — | –150 | mA |
| VOH | Output HIGH Voltage | VCC = Min. VIN = VIH or VIL | IOH = –2mA | 2.4 | 3.6 | — | V |
| VOL | Output LOW Voltage | VCC = Min. VIN = VIH or VIL | IOL = 8mA | — | 0.3 | 0.5 | V |
| VH | Input Hysteresis on input control lines | | | — | 200 | — | mV |

NOTES:
1. For conditions shown as min. or max., use appropriate Vcc value.
2. Typical values are at VCC = 5.0V, +25°C ambient temperature.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (cont.)

**The following conditions apply unless otherwise specified:**
**Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%**

| Symbol | Parameter | Test Conditions[1] | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|
| ICCQC | Quiescent Power Supply Current | VIN = VCC, or VIN = GND<br>VCC = Max. | — | 3 | 15 | mA |
| ICCQT | Quiescent Power Supply Current TTL Input Levels | VIN = 3.4V<br>VCC = Max. | — | 0.3 | 1 | mA/ Input |
| ICCD | Dynamic Power Supply Current | VIN = VCC, or VIN = GND<br>VCC = Max., f = 10MHz Correct Mode | — | — | 100 | mA |

NOTES:
1. For conditions shown as Min. or Max., use appropriate Vcc value.
2. Typical values are at VCC = 5.0V, +25°C ambient temperature.

# AC PARAMETERS
## PROPAGATION DELAY TIMES

| Number | Parameter | Description: From Input[1] | Description: To Output | 49C466 Max. Com'l. | 49C466A (50MHz) Max. Com'l. | Unit |
|---|---|---|---|---|---|---|
| **GENERATE (WRITE) PARAMETERS** | | | | | | |
| **Without Write FIFO:** | | | | | | |
| 1 | $t_{BC}$ | BEn | CBSYN (chkbit) | 20 | 17 | ns |
| 2 | $t_{BM}$ | BEn | MDout | 16 | 13 | ns |
| 3 | $t_{PPE}$ | Pxin | $\overline{PERR}$ | 10 | 8 | ns |
| 4 | $t_{SC}$ | SDin | CBSYN (chkbit) | 22 | 15 | ns |
| **5** | **$t_{SM}$** | SDin | MDout | 22 | 15 | ns |
| 6 | $t_{SPE}$ | SDin | $\overline{PERR}$ | 16 | 12 | ns |
| **With Write FIFO:** | | | | | | |
| 7 | $t_{MC}$ | MCLK (Lo-Hi) | CBSYN (chkbit) | 25 | 18 | ns |
| 8 | $t_{MMD}$ | MCLK (Lo-Hi) | MDout | 25 | 18 | ns |
| 9 | $t_{WBSEL}$ | WBSEL | MDout | 18 | 13 | ns |
| **DETECT (READ) PARAMETERS** | | | | | | |
| **Without Read FIFO:** | | | | | | |
| 10 | $t_{WYC}$ | SYNCLK (Lo-Hi) | CBSYN (syndr) | 16 | 12 | ns |
| **11** | **$t_{ME}$** | MDin | $\overline{ERR}$ | 20 | 12 | ns |
| 12 | $t_{MME}$ | MDin | $\overline{MERR}$ | 22 | 14 | ns |
| 13 | $t_{CE}$ | CBI | $\overline{ERR}$ | 13 | 9 | ns |
| 14 | $t_{CME}$ | CBI | $\overline{MERR}$ | 13 | 9 | ns |
| **With Read FIFO:** | | | | | | |
| 15 | $t_{SSD}$ | SCLK (Lo-Hi) | SDout | 22 | 15 | ns |
| 16 | $t_{RBSEL}$ | RBSEL | SDout | 18 | 13 | ns |
| **CORRECT (READ) PARAMETERS** | | | | | | |
| **Without Read FIFO:** | | | | | | |
| 17 | $t_{CS}$ | CBI | SDout | 20 | 16 | ns |
| 18 | $t_{MP}$ | MDin | Pxout | 22 | 18 | ns |
| **19** | **$t_{MS}$** | MDin | SDout | 22 | 17 | ns |
| **With Read FIFO:** | | | | | | |
| 20 | $t_{SP}$ | SCLK (Lo-Hi) | Pxout | 22 | 15 | ns |

**NOTE:**
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

# PROPAGATION DELAY TIMES FROM LATCH ENABLES

| Number | Parameter | Description | | 49C466 Max. | 49C466A (50MHz) Max. | Unit |
|---|---|---|---|---|---|---|
| | | From Input(1) | To Output | Com'l. | Com'l. | |
| 21 | $t_{MLE}$ | MDILE (Lo-Hi) | $\overline{ERR}$ | 16 | 13 | ns |
| 22 | $t_{MLME}$ | MDILE (Lo-Hi) | $\overline{MERR}$ | 18 | 15 | ns |
| 23 | $t_{MLP}$ | MDILE (Lo-Hi) | Px | 24 | 18 | ns |
| 24 | $t_{MLS}$ | MDILE (Lo-Hi) | SDout | 22 | 19 | ns |
| 25 | $t_{MOLS}$ | $\overline{MDOLE}$ (Hi-Lo) | SDout | 18 | 9 | ns |
| 26 | $t_{MOLP}$ | $\overline{MDOLE}$ (Hi-Lo) | Px | 18 | 11 | ns |
| 27 | $t_{SLC}$ | SDILE (Lo-Hi) | CBSYN (chkbit) | 20 | 15 | ns |
| 28 | $t_{SLM}$ | SDILE (Lo-Hi) | MDout | 20 | 12 | ns |
| 29 | $t_{SOLC}$ | $\overline{SDOLE}$ (Hi-Lo) | CBSYN (chkbit) | 12 | 8 | ns |
| 30 | $t_{SOLM}$ | $\overline{SDOLE}$ (Hi-Lo) | MDout | 15 | 10 | ns |

**NOTE:**
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

# R/W FIFO TIMES

| Number | Parameter | Description | | 49C466 Com'l. | | 49C466A (50MHz) Com'l. | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | From Input(1) | To Output | Min. | Max. | Min. | Max. | |
| 31 | $t_{RSF}$ | RS1 (Hi-Lo) during SCLK LOW | $\overline{EF}$ (Hi-Lo)/$\overline{FF}$ (Lo-Hi) | — | 16 | — | 16 | ns |
| 32 | $t_{SKEW1}$ | RCLK (Lo-Hi) (SCLK or MCLK) | WCLK (Lo-Hi) (SCLK or MCLK) | 10 | — | 9 | — | ns |
| 33 | $t_{SKEW2}$ | WCLK (Lo-Hi) (SCLK or MCLK) | RCLK (Lo-Hi) (SCLK or MCLK) | 10 | — | 9 | — | ns |
| 34 | $t_{EF}$ | R/WCLK (Lo-Hi) (SCLK or MCLK) | $\overline{EF}$ | — | 15 | — | 12 | ns |
| 35 | $t_{FF}$ | R/WCLK (Lo-Hi) (SCLK or MCLK) | $\overline{FF}$ | — | 15 | — | 12 | ns |
| 39 | $t_{HFF}$ | R/WCLK (Lo-Hi) (SCLK or MCLK) | $\overline{HF}$ | — | 15 | — | 12 | ns |

**NOTE:**
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

## BYTE MERGE TIMES

| Number | Parameter | Description From Input(1) | Description To Output | 49C466 Max. Com'l. | 49C466A (50MHz) Max. Com'l. | Unit |
|---|---|---|---|---|---|---|
| 36 | tSCM | SCLK (Lo-Hi) | MDout | 25 | 18 | ns |
| 37 | tMDM | $\overline{\text{MDOLE}}$ (Hi-Lo) | MDout | 18 | 14 | ns |
| 38 | tRBM | RBSEL | MDout | 23 | 15 | ns |

**NOTE:**
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

## ENABLE AND DISABLE TIMES

| Number | Parameter | Description From Input(1) | | Description To Output | | 49C466 Com'l. Min. | 49C466 Com'l. Max. | 49C466A (50MHz) Com'l. Min. | 49C466A (50MHz) Com'l. Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| 40 | tBESZx | BEN = | High | SDout | * | — | 22 | — | 12 | ns |
| 41 | tBESxZ | | Low | | Hi-Z | — | 22 | — | 12 | |
| 42 | tBEPZx | BEN = | High | Pout | * | — | 15 | — | 10 | ns |
| 43 | tBEPxZ | | Low | | Hi-Z | — | 15 | — | 8 | |
| 44 | tSEPZx | $\overline{\text{SOE}}$ = | Low | Pout | * | — | 14 | — | 10 | ns |
| 45 | tSEPxZ | | High | | Hi-Z | — | 14 | — | 8 | |
| 46 | tCECZx | $\overline{\text{MOE}}$ = | Low | CBSYN | * | — | 12 | — | 10 | ns |
| 47 | tCECxZ | | High | | Hi-Z | — | 10 | — | 8 | |
| 48 | tMEMZx | $\overline{\text{MOE}}$ = | Low | MDout | * | — | 22 | — | 10 | ns |
| 49 | tMEMxZ | | High | | Hi-Z | — | 18 | — | 9 | |
| 50 | tSESZx | $\overline{\text{SOE}}$ = | Low | SDout | * | — | 16 | — | 10 | ns |
| 51 | tSESxZ | | High | | Hi-Z | — | 20 | — | 9 | |

**NOTES:**
1. (High-Z) indicates High-Impedence.
2. * indicates delay to both edges.

## SET-UP AND HOLD TIMES

| Number | Parameter | Description | | | 49C466 Min. | 49C466A (50MHz) Min. | Unit |
|---|---|---|---|---|---|---|---|
| | | From Input(1) | To Output | | Com'l. | Com'l. | |
| 52 | $t_{CMLS}$ | CBI Set-up | before MDILE = | Hi-Lo | 2 | 1.5 | ns |
| 53 | $t_{CMLH}$ | CBI Hold | after MDILE = | Hi-Lo | 6 | 1.5 | ns |
| 54 | $t_{MMLS}$ | MDIN Set-up | before MDILE = | Hi-Lo | 2 | 1.5 | ns |
| 55 | $t_{MMLH}$ | MDIN Hold | after MDILE = | Hi-Lo | 6 | 1.5 | ns |
| 56 | $t_{CMOLS}$ | CBI Set-up (Correct) | before $\overline{MDOLE}$ = | Lo-Hi | 12 | 8 | ns |
| 57 | $t_{CMOLH}$ | CBI Hold (Correct) | after $\overline{MDOLE}$ = | Lo-Hi | 2 | 0 | ns |
| 58a | $t_{MMOLS}$ | MDIN Set-up (Detect) | before $\overline{MDOLE}$ = | Lo-Hi | 10 | 5 | ns |
| 58b | $t_{MMOLS}$ | MDIN Set-up (Correct) | before $\overline{MDOLE}$ = | Lo-Hi | 12 | 12 | ns |
| 59a | $t_{MMOLH}$ | MDIN Hold (Detect) | after $\overline{MDOLE}$ = | Lo-Hi | 4 | 0 | ns |
| 59b | $t_{MMOLH}$ | MDIN Hold (Correct) | after $\overline{MDOLE}$ = | Lo-Hi | 4 | 0 | ns |
| 60 | $t_{MMCS}$ | MDIN Set-up | before MCLK = | Lo-Hi | 10 | 10 | ns |
| 61 | $t_{MMCH}$ | MDIN Hold | after MCLK = | Lo-Hi | 4 | 0 | ns |
| 62 | $t_{SSLS}$ | SDIN Set-up | before SDILE = | Hi-Lo | 5 | 1.5 | ns |
| 63 | $t_{SSLH}$ | SDIN Hold | after SDILE = | Hi-Lo | 3 | 1.5 | ns |
| 64 | $t_{SSCS}$ | SDIN Set-up | before SCLK = | Lo-Hi | 2 | 1 | ns |
| 65 | $t_{SSCH}$ | SDIN Hold | after SCLK = | Lo-Hi | 6 | 2 | ns |
| 66 | $t_{SSOLS}$ | SDIN Set-up | before $\overline{SDOLE}$ = | Lo-Hi | 8 | 6 | ns |
| 67 | $t_{SSOLH}$ | SDIN Hold | after $\overline{SDOLE}$ = | Lo-Hi | 0 | 0 | ns |
| 68 | $t_{SCSD}$ | SCLK (Lo-Hi) | before $\overline{SDOLE}$ = | Lo-Hi | 14 | 14 | ns |
| 69 | $t_{MCSD}$ | MCLK (Lo-Hi) | before $\overline{SDOLE}$ = | Lo-Hi | 14 | 10 | ns |
| 70 | $t_{ENS}$ | R/W FIFO Enable Set-up | before S/M CLK = | Lo-Hi | 4 | 2 | ns |
| 71 | $t_{ENH}$ | R/W FIFO Enable Hold | after S/M CLK = | Lo-Hi | 4 | 2 | ns |
| 72 | $t_{RSS}$ | RS1 (Lo-Hi) | R/WCLK = | Lo-Hi | 6 | 2 | ns |
| 73 | $t_{MODS}$ | Mode Data Set-up | before SCLK = | Lo-Hi | 4 | 2 | ns |
| 74 | $t_{MODH}$ | Mode Data Hold | after SCLK = | Lo-Hi | 4 | 2 | ns |
| 75 | $t_{MENS}$ | Mode Enable Set-up | before SCLK = | Lo-Hi | 4 | 2 | ns |
| 76 | $t_{MENH}$ | Mode Enable Hold | after SCLK = | Lo-Hi | 4 | 2 | ns |
| 77 | $t_{MSDS}$ | MDIN Set-up | before $\overline{SDOLE}$ = | Lo-Hi | 22 | 20 | ns |
| 78 | $t_{MSDH}$ | MDIN Hold | after $\overline{SDOLE}$ = | Lo-Hi | 0 | 0 | ns |
| 93 | $t_{BSCS}$ | BE Set-up | before SCLK = | Lo-Hi | 1 | 1 | ns |
| 94 | $t_{BSCH}$ | BE Hold | after SCLK = | Lo-Hi | 6 | 2 | ns |
| **DIAGNOSTIC SET-UP AND HOLD TIMES** | | | | | | | |
| 79 | $t_{CSCS}$ | CBI Set-up | before SYNCLK = | Lo-Hi | 4 | 2 | ns |
| 80 | $t_{MSCS}$ | MDIN Set-up | | | 10 | 8 | ns |
| 81 | $t_{MLSCS}$(2) | MDILE = Lo-Hi Set-up | | | 10 | 8 | ns |
| 82 | $t_{CSCH}$(2) | CBI Hold | After SYNCLK= | Lo-Hi | 6 | 2 | ns |
| 83 | $t_{MSCH}$(2) | MDIN Hold | | | 6 | 2 | ns |
| 84 | $t_{MLSCH}$(2) | MDILE = Lo-Hi Hold | | | 6 | 2 | ns |

**NOTE**:
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

## MINIMUM PULSE WIDTH

| Number | Parameter | Description From Input(1) | | Condition | 49C466 Min. Com'l. | 49C466A (50MHz) Min. Com'l. | Unit |
|---|---|---|---|---|---|---|---|
| 85 | $t_{RS}$ | Min. RS1 LOW time | to reset buffers | — | 6 | 5 | ns |
| 86 | $t_{MLE}$ | Min. MDILE HIGH time | to strobe new data | MD, CBI = Valid | 6 | 5 | ns |
| 87 | $t_{MDOLE}$ | Min. $\overline{\text{MDOLE}}$ LOW time | to strobe new data | — | 6 | 5 | ns |
| 88 | $t_{SLE}$ | Min. SDILE HIGH time | to strobe new data | SD = Valid | 6 | 5 | ns |
| 89 | $t_{CLK}$ | Min. S/MCLK HIGH time | to clock in new data | EN signal LOW | 6 | 6 | ns |
| 90 | $t_{SYNCLK}$ | Min. SYNCLK HIGH time | to clock in new data | — | 6 | 5 | ns |
| 91 | $t_{SDOLE}$ | Min. $\overline{\text{SDOLE}}$ LOW time | to clock in new data | — | 6 | 5 | ns |

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3V |
| Input Rise/Fall Times | 1V/ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Test Circuits for All Outputs |

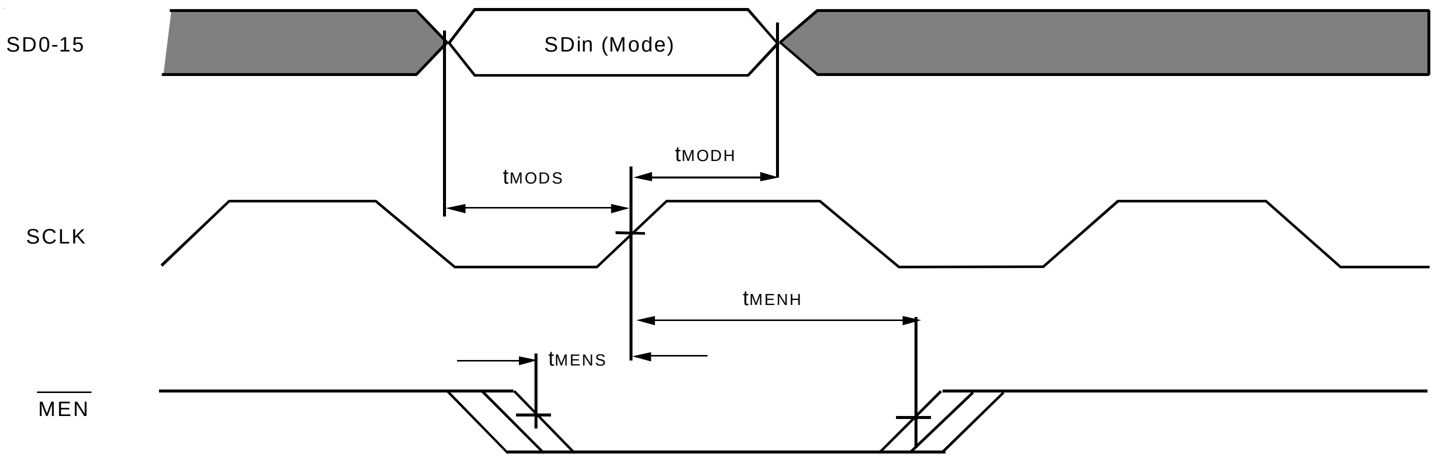



**Figure 4. Mode Enable Timing**

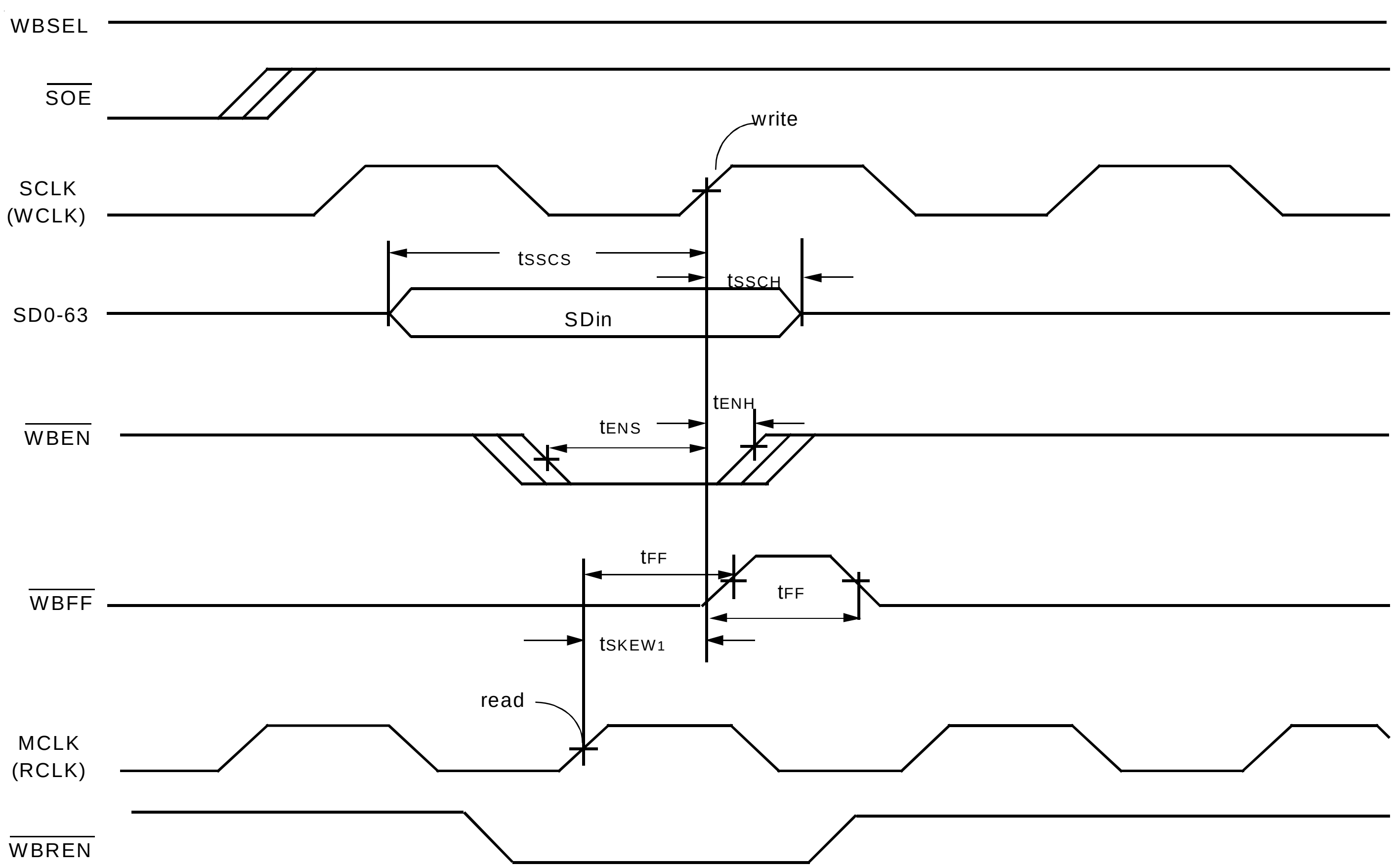



**Figure 5. WFIFO Write Timing (Write Cycle)**

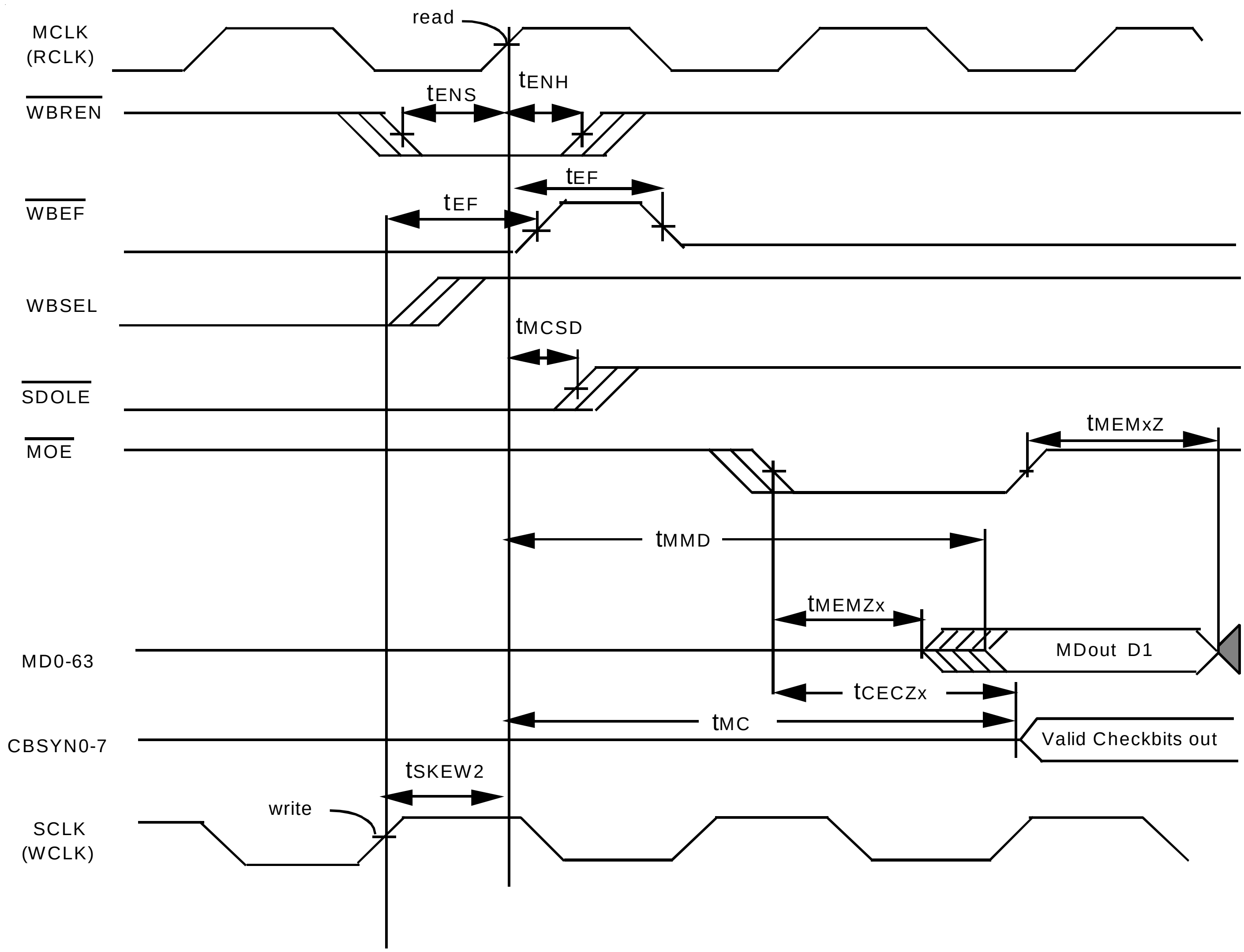



Figure 6. WFIFO Read and Checkbit Generate Timing (Write Cycle)

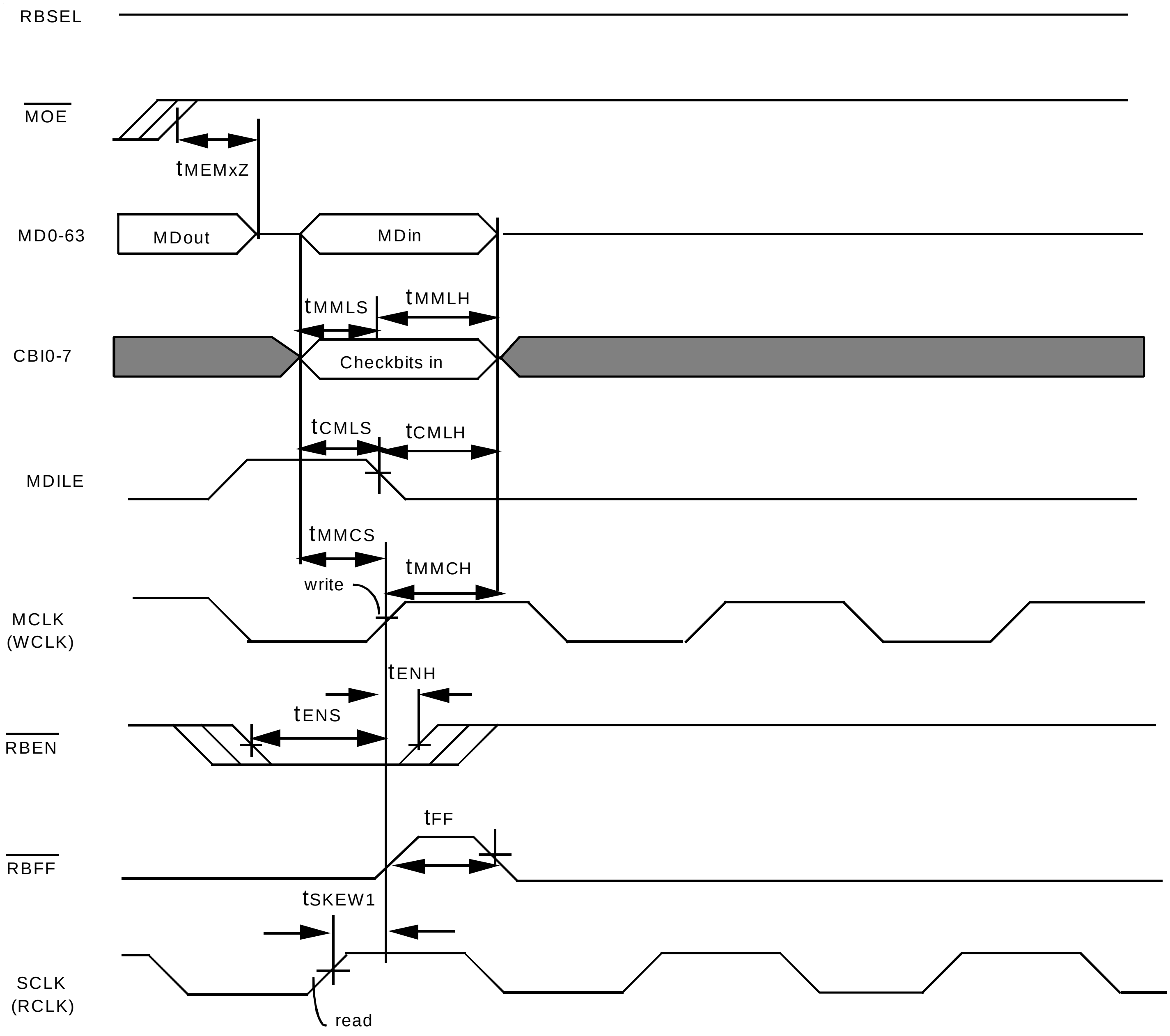



**Figure 7. RFIFO Write Timing (Read Cycle)**

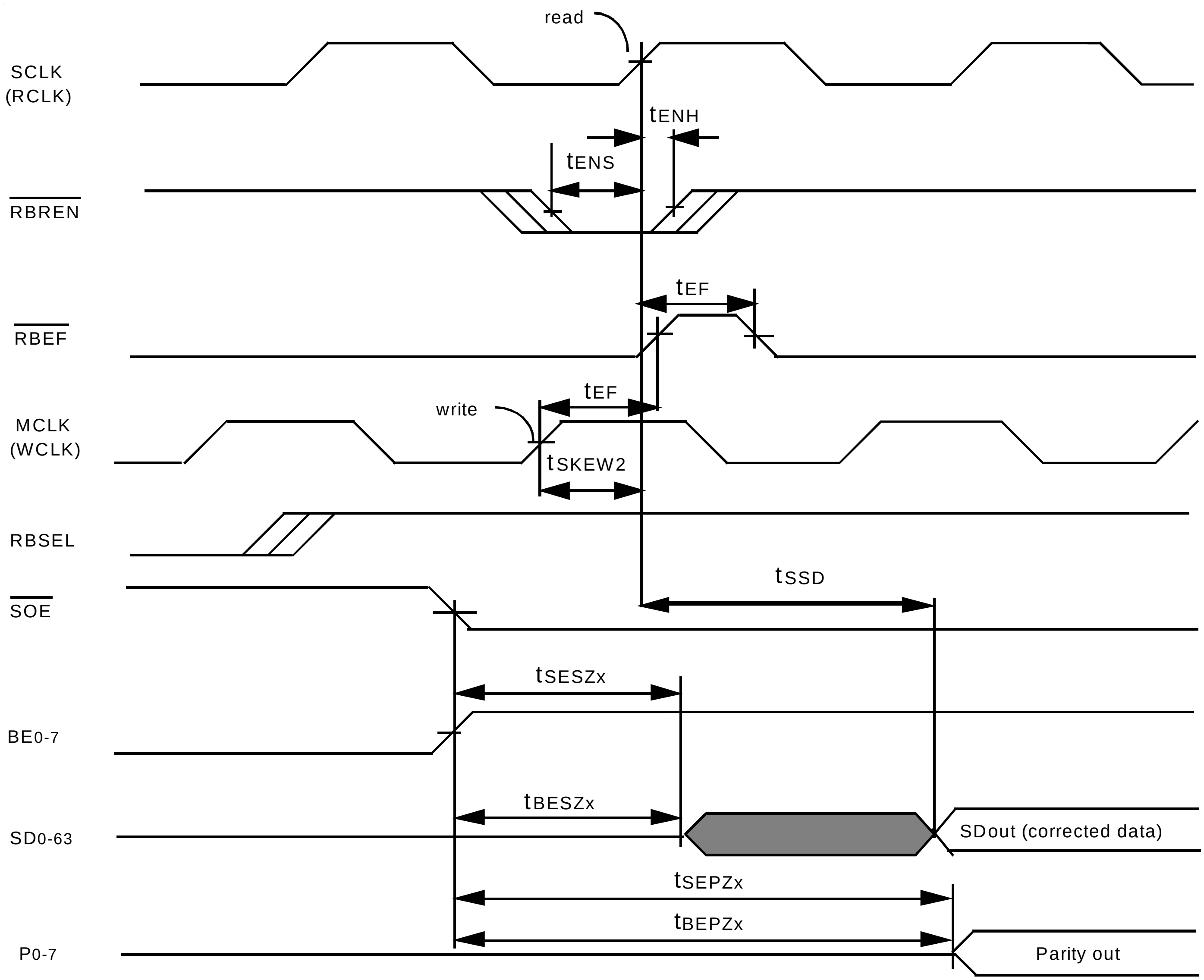



**Figure 8. RFIFO Read Timing (Read Cycle)**

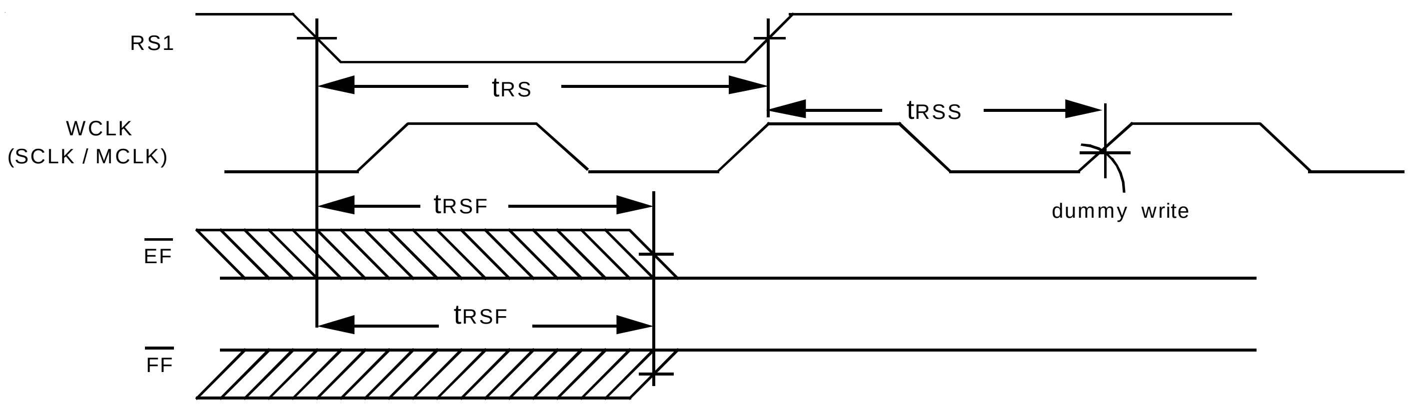



**Figure 9. FIFO (WFIFO/RFIFO) Reset Timing**

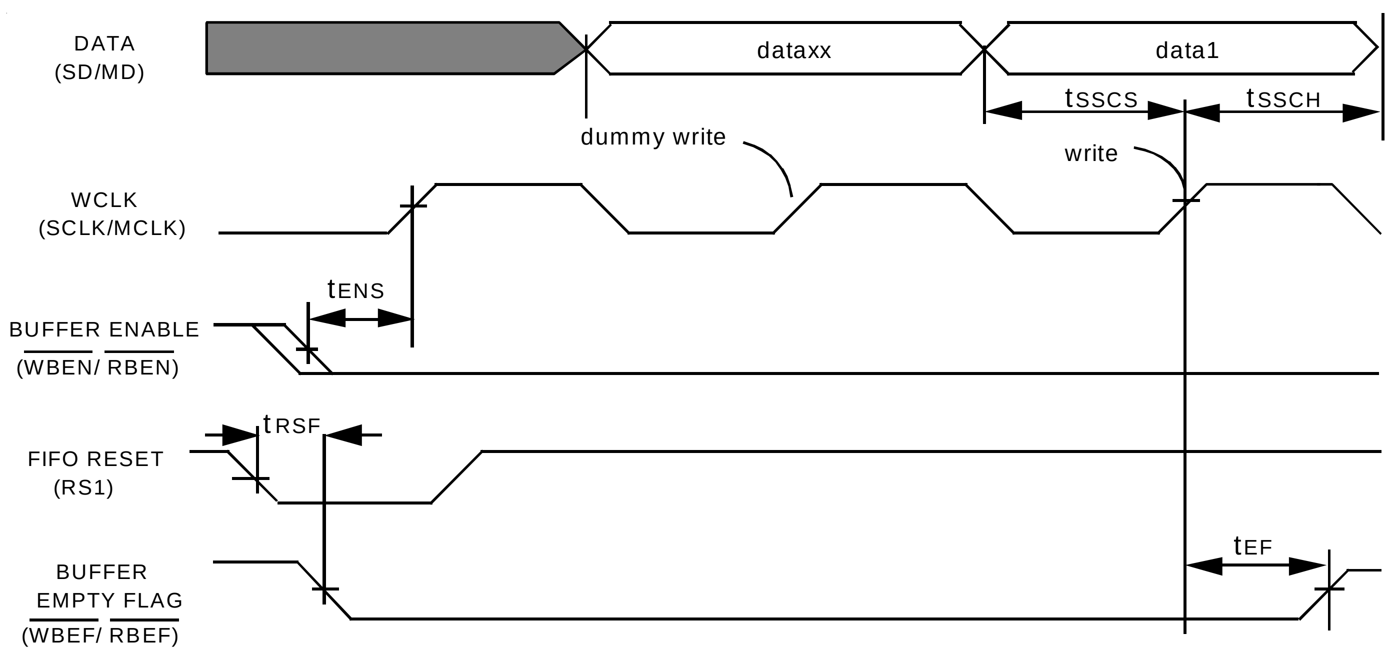



**Figure 10. FIFO (WFIFO/RFIFO) Write Latency Timing**

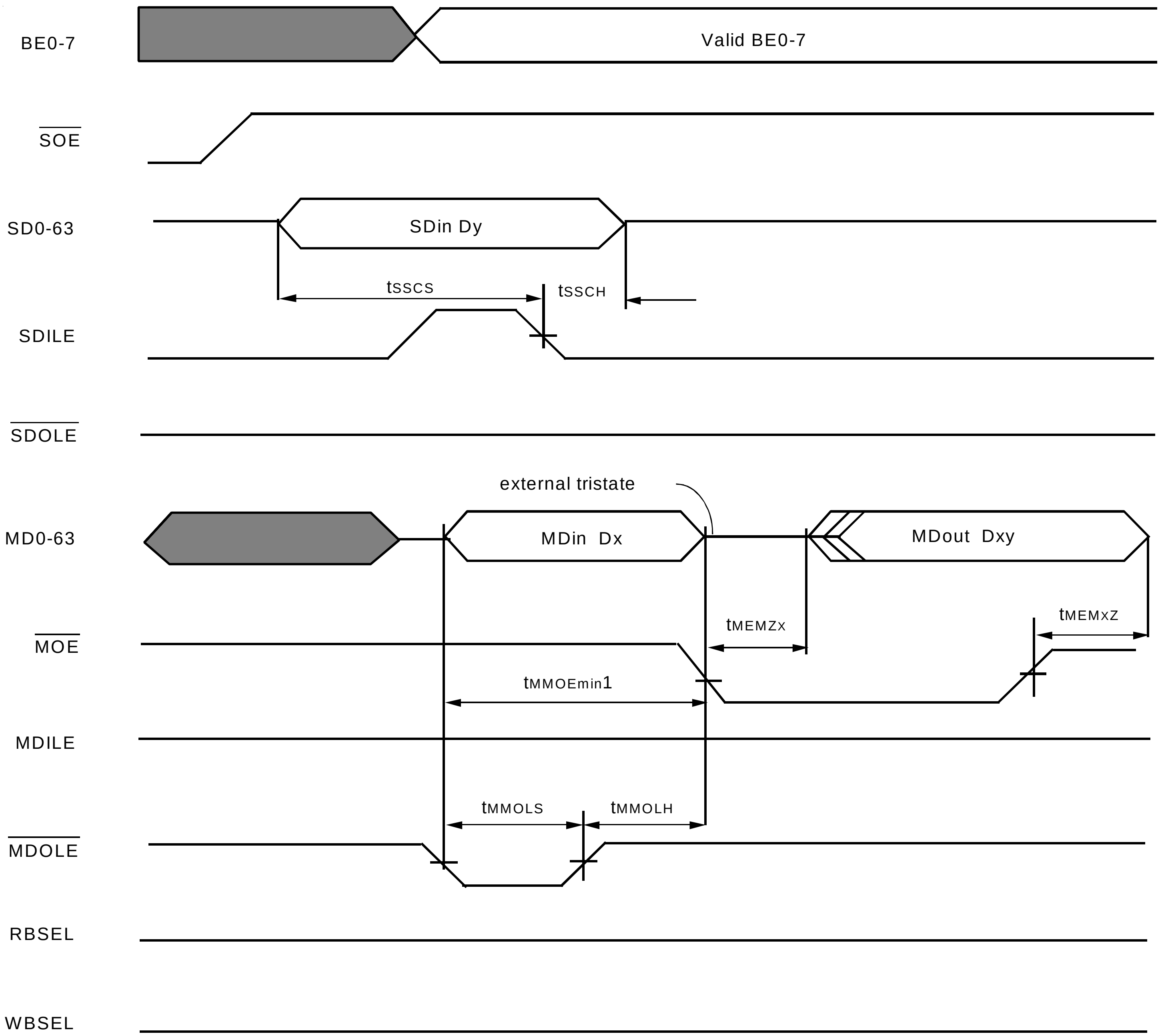



**Figure 11. Partial Word Write/Byte Merge Timing**

**NOTE:**
1. $t_{MMOE}$ is not a propagation delay. For partial word write operations $t_{MMOE\ MIN} = t_{MDM}$.

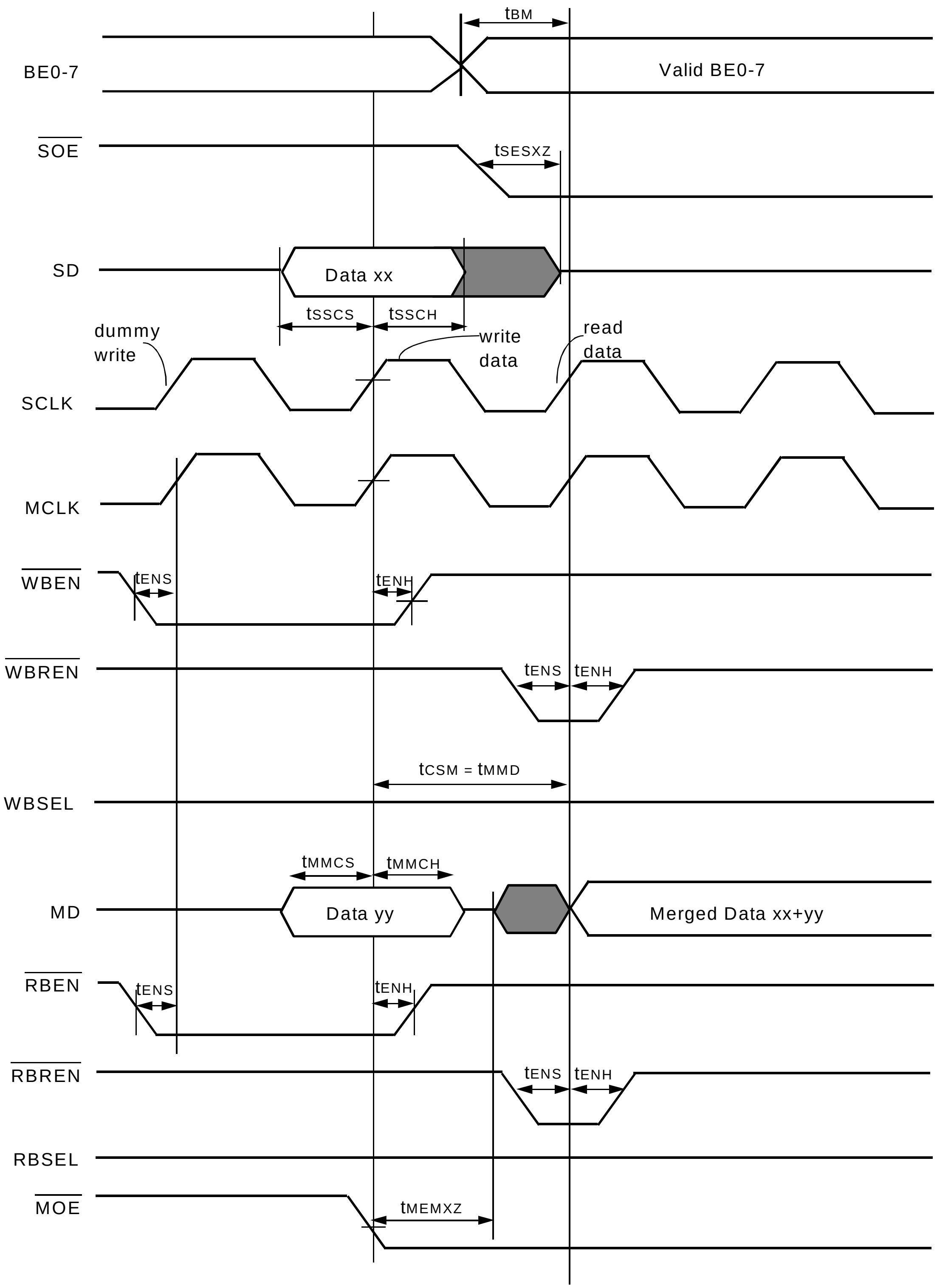



**Figure 12. Partial Word Write/Byte Merge Timing using both RFIFO and WFIFO**

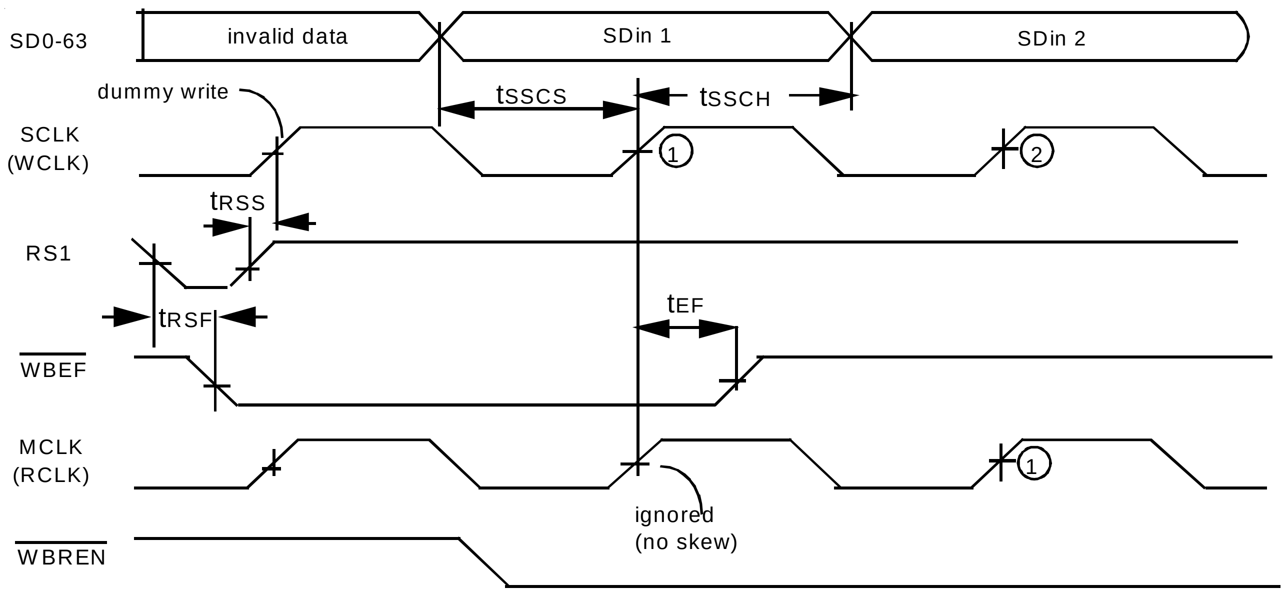



Figure 13. Write FIFO Write Timing with Clock Skew Violation

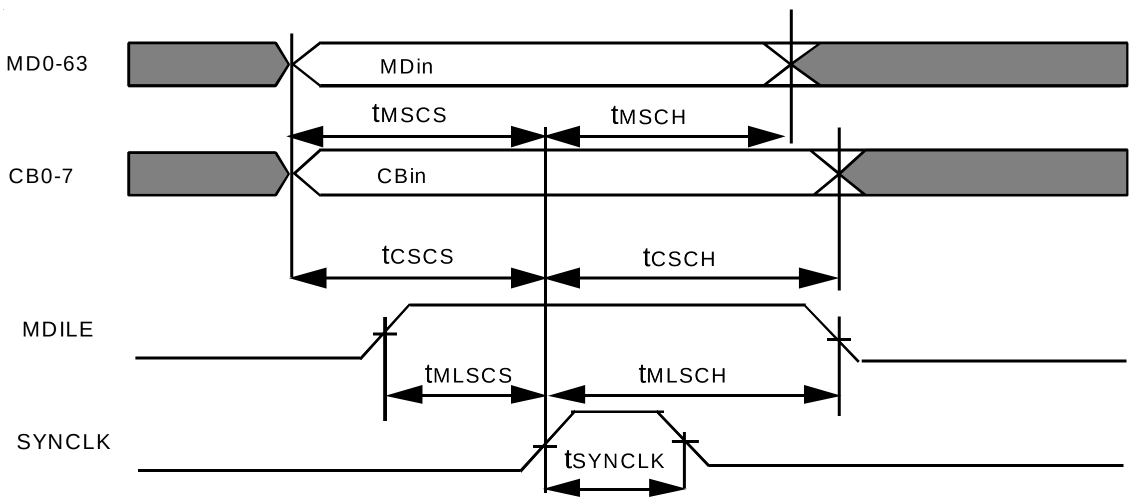
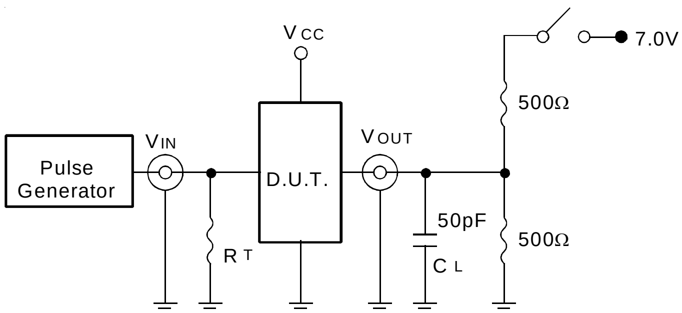



Figure 14. Diagnostic Timing

# TEST WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




## SWITCH POSITION

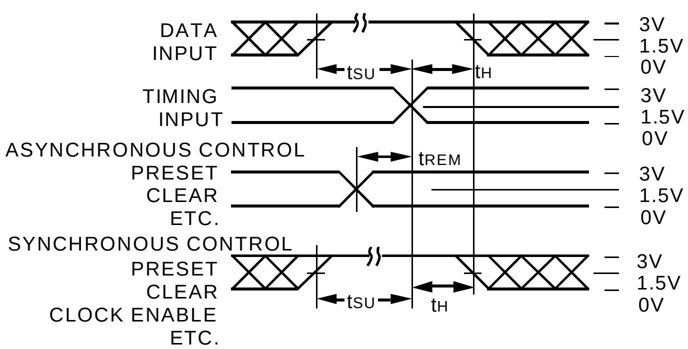
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

**DEFINITIONS:**

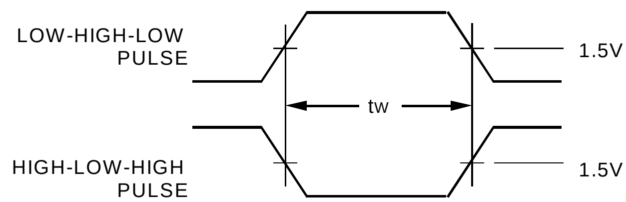
$C_L$= Load capacitance: includes jig and probe capacitance.

$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

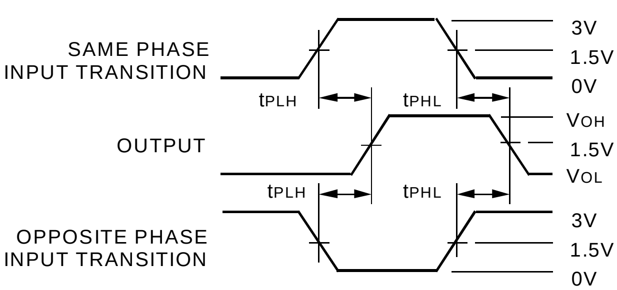
## SET-UP, HOLD, AND RELEASE TIMES



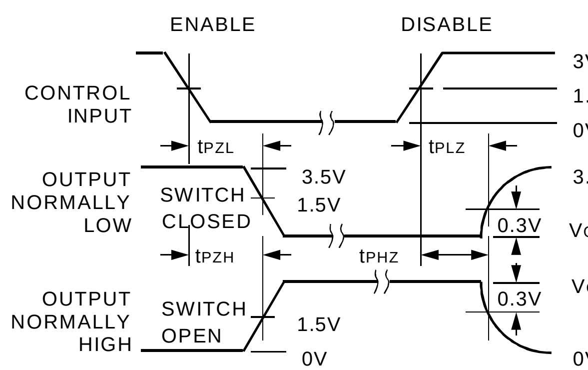

## PULSE WIDTH




## PROPAGATION DELAY




## ENABLE AND DISABLE TIMES




**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.

# ORDERING INFORMATION

| IDT | 49C466 | X | XX | X |
|---|---|---|---|---|
| | Device Type | Speed | Package | Process/ Temperature Range |

| | | |
|---|---|---|
| Process/Temperature Range | Blank | Commercial (0°C to +70°C) |
| Package | PQF | Plastic Quad Flatpack |
| Speed | Blank | Standard speed |
| | A | 50MHz speed |
| Device Type | 49C466 | 64-Bit Flow-thru™ EDC |

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