Agilent HDMP-0552 Quad Port Bypass Circuit with CDR and Data Valid Detection

For Fibre Channel Arbitrated Loops

Data Sheet

Description

The HDMP-0552 is a Quad Port Bypass Circuit (PBC) with Clock and Data Recovery (CDR) and data valid detection capability included. See Figure 1 for block diagram. This device minimizes part count, cost and jitter accumulation while repeating incoming signals. Port Bypass Circuits are used in hard disk arrays constructed in Fibre Channel Arbitrated Loop (FC-AL) configurations. By using Port Bypass Circuits, hard disks may be pulled out or swapped while other disks in the array are available to the system.

A PBC consists of multiple 2:1 multiplexers daisy chained along with a CDR. Each port has two modes of operation: “disk in loop” and “disk bypassed.” When the “disk in loop” mode is selected, the loop goes into and out of the disk drive at that port. For example, data goes from the HDMP-0552’s TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC (for example, an HDMP-263x) Rx± differential input pins. Data from the Disk Drive Transceiver IC Tx± differential output pins goes to HDMP-0552’s FM_NODE[n]± differential input pins. Figure 2 and Figure 3 show connection diagrams for disk drive array applications. When the “disk bypassed” mode is selected, the disk drive is either absent or nonfunctional, and the loop bypasses the hard disk.

Multiple HDMP-0552’s may be cascaded or connected to other members of the HDMP-04xx family through the FM_LOOP and TO_LOOP pins to create loops for arrays of disk drives greater than 4. See Table 3 to identify which of the 5 cells (0:4) provides FM_LOOP, TO_LOOP pins (cell connected to cable).

Features

- Supports 1.0625/2.125 GBd Fibre Channel operation
- Quad PBC/CDR in one package
- CDR location determined by choice of cable input/output
- Amplitude valid detection on FM_NODE[0] input
- Data valid detection on FM_NODE[0] input
  - Run length violation detection
  - Comma detection
  - Configurable for both single-frame and multi-frame detection
- Speed select pin for 1 or 2 GBd operation
- Single REFCLK for 1 or 2 GBd operation
- CDR selectable via external pin
- Enable/disable equalizers on all inputs
- Enable/disable selected high-speed output drivers
- High speed LVPECL I/O
- Buffered line logic (BLL) outputs (no external bias resistors required)
- 1.1 W typical power at V_{CC} = 3.3 V
- Advanced 0.35 μ BiCMOS technology
- 64 Pin, 10 mm, low cost plastic QFP package

Applications

- RAID, JBOD, BTS cabinets
- 1=> 1-4 serial buffer with or without CDR

CAUTION: As with all semiconductor ICs, it is advised that normal static precautions be taken in the handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).

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Combinations of Quad PBCs can be utilized to accommodate any number of hard disks. The unused cells in a quad may be bypassed with pulldown resistors on the BYPASS[n]- pins for these cells. Additional power savings possible by turning off unused output drives. Please refer to BLL output section on page 3. An HDMP-0552 can be wired as a single or double mux cell with a CDR. It may also be used as a single or double mux cell without a CDR. All TO_NODE outputs of the HDMP-0552 are of equal strength. Therefore, this part may be used as a 1=>1- 4 buffer.

The design of HDMP-0552 allows for placement of the CDR at any location with respect to hard disk slots. For example, if BYPASS[0]-pin is tied to V_{CC} and hard disk slots A to D are connected to PBC cells 1 to 4 in the same order, the CDR function is performed at entry to the HDMP-0552 (Figure 2). To achieve a CDR function at exit from the HDMP-0552, BYPASS[1]- must be tied to V_{CC} and hard disk slots A to D must be connected to PBC cells 2, 3, 4, 0 in that order (Figure 3). Table 3 shows all possible connections. In case of CDR at entry, a Signal Detect (SD) pin shows the status of the signal at the incoming cable. The recommended method of setting the BYPASS[i]- pins HIGH is to drive them with a high-impedance signal. Internal pull-up resistors force the BYPASS[i]- pins to V_{CC}.

HDMP-0552 Block Diagram

CDR

The Clock and Data Recovery (CDR) block is responsible for frequency and phase locking onto the incoming serial data stream and resampling the incoming data based on the recovered clock. An automatic locking feature allows the CDR to lock onto the input data stream without external training controls. It does this by continually frequency locking onto the reference clock (REFCLK) and then phase locking onto the input data stream. Once bit-locked, the CDR generates a high-speed sampling clock. This clock is used to sample or repeat the incoming data to produce the CDR output. The CDR jitter specifications listed in this data sheet assume an input that has been 8B/10B encoded.

Data Valid Output

The outgoing data from the CDR is checked for two types of errors. First, the data is checked for “Run Length Violations” (RLV), which are defined as a consecutive bit sequence greater than five. In addition, the data is checked for “No Comma Detected” (NCD), which is defined as no comma within a 2^{15} bit frame. If neither of these errors occur, the data is considered valid Fibre Channel data, and FM_NODE[0]_DV is driven HIGH.

For reporting errors, the data valid (DV) block contains a 2^{15}-bit counter to provide a frame clock. All errors are reported relative to the rising edge of this internally generated clock.

There are two LVTTL inputs for configuring the data validity checking. When MODE_DV is HIGH, the data input for the CDR comes from FM_NODE[0]. In this mode, the FM_NODE[0] input is checked for data validity. In addition, the FM_NODE[0]_DV LVTTL output can be used to drive BYPASS[0]- signal. In this configuration, when the data is invalid, the CDR output will be bypassed and the data from TO_NODE[0] will be passed on instead.

When MODE_DV is LOW, the data validity checking is still taking place on output of the CDR; however, this data may be from another input besides FM_NODE[0]. In addition, the CDR output data will always be passed on to TO_NODE[1] in this mode.

Lastly, the LVTTL input FSEL selects single versus multi-frame operation of the DV block. For example, when FSEL is LOW, the FM_NODE[0]_DV output will be driven HIGH after 2^{15} bits of good data. Similarly, FM_NODE[0]_DV will be driven LOW after one 2^{15} bit sequence containing errors. This is “single frame” operation.

When FSEL is HIGH, the DV block is operating in “multi-frame”, or four frame, mode. In this mode, the FM_NODE[0]_DV will be driven HIGH only after four consecutive frames of valid data. Once HIGH, FM_NODE[0]_DV will only be driven LOW after four consecutive 2^{15}-bit frames containing errors.

REFCLK Input and REF_RATE Control

The LVTTL REFCLK input provides a reference oscillator for frequency acquisition of the CDR. The REFCLK frequency should be 53.125 Mhz or 106.25 Mhz $\pm$100 ppm. Set REF_RATE = 0 for a 53 Mhz and set REF_RATE = 1 for 106 MHz references. Either reference frequency can be used for both 1 GBd or 2 GBd rates.

Amplitude Valid Output

The Amplitude Valid (AV) block detects if the incoming data on FM_NODE[0]$\pm$ is valid by examining the differential amplitude of that input. The incoming data is considered valid and FM_NODE[0]_AV is driven HIGH, as long as the amplitude is greater than 200 mV (differential peak-to-peak). FM_NODE[0]_AV is driven LOW as long as the amplitude of the input signal is less than 100 mV (differential peak-to-peak). When the amplitude of the input signal is between 100 and 200 mV (differential peak-to-peak), FM_NODE[0]_AV is unpredictable.

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Equalizer Input

All FM_NODE[n]± high-speed differential inputs have an equalization setting to offset the effects of skin loss and dispersion on PCBs. This function is independently controllable for each input port using the EQ_SEL and NDx (x = 0-4) pins. The default setting for the equalization is TRUE. Equalization maybe set to FAULT for individual inputs by forcing EQ_SEL low and NDx (where x = port number) low for each port that the equalization setting is desired to be false. It is a logic OR function. For instance, forcing EQ_SEL, ND2 & ND3 pins low will turn off the equalization setting at FM_NODE[2]± and FM_NODE[3]± while the equalization setting will remain on for ports 0, 1 and 4.

The EQ_SEL and NDx (x = 0-4) pins are LVTTL and contain internal pull-up circuitry. To force a pin low each pin should be connected to GND through a 1 kΩ resistor. Otherwise, these inputs should be left to float. In this case, the internal pull-up circuitry will force them high.

BYPASS[n]- Input

The active low BYPASS[n]- inputs control the data flow through the HDMP-0552. All BYPASS pins are LVTTL and contain internal pull-up circuitry. To bypass a port, the appropriate BYPASS[n]- pin should be connected to GND through a 1 kΩ resistor. Otherwise, the BYPASS[n]- inputs should be left to float. In this case, the internal pull-up circuitry will force them high.

BLL Output

All TO_NODE[n]+ high-speed differential outputs are driven by a Buffered Line Logic (BLL) circuit that has on-chip source termination. Therefore, no external bias resistors are required. The BLL outputs on the HDMP-0552 are of equal strength. **Unused outputs should be turned off independently. This reduces power and reduces the potential for crosstalk effects caused by incorrect terminations.** If the unused outputs are not turned off they should be differentially terminated. The value of the termination resistor should match the PCB trace differential impedance. Each output port is set to active or inactive by the OUT_SEL and NDx (x = 0-4) pins.

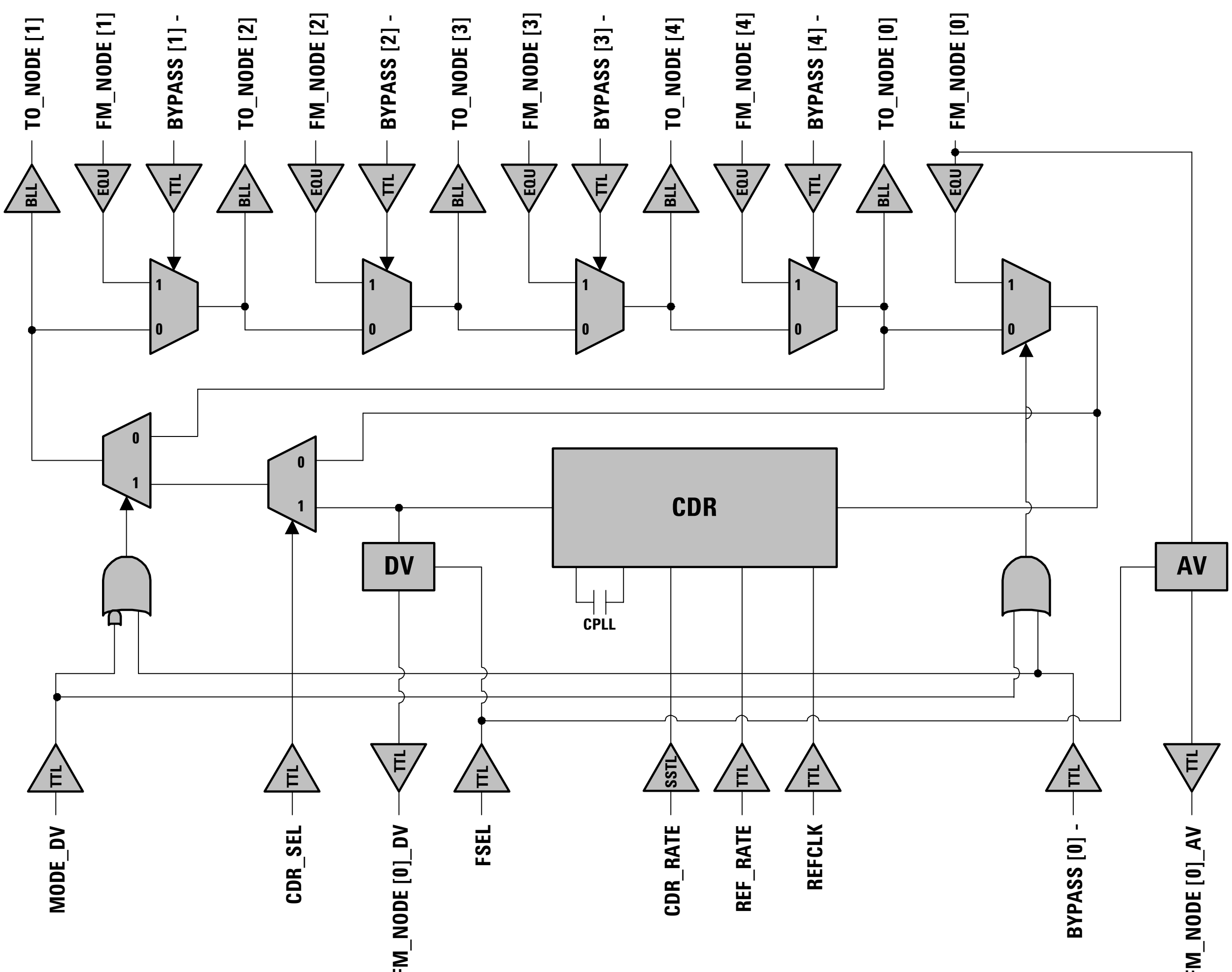

Figure 1 - Block Diagram of HDMP-0552

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Output port active is the default condition. Each output port may be set to inactive by forcing OUT_SEL low and NDx (where x = port number) low. It is a logic OR function. For instance, forcing OUT_SEL, ND1 & ND4 pins low will turn off output ports TO_NODE[1]± and TO_NODE[4]± while output ports 0,2 and 3 will remain on. When an output port is off both output terminals will pull high to approximately V_{CC}.

The OUT_SEL and NDx (x = 0-4) pins are LVTTL and contain internal pull-up circuitry. To force a pin low each pin should be connected to GND through a 1 kΩ resistor. Otherwise, these inputs should be left to float. In this case, the internal pull-up circuitry will force them high.

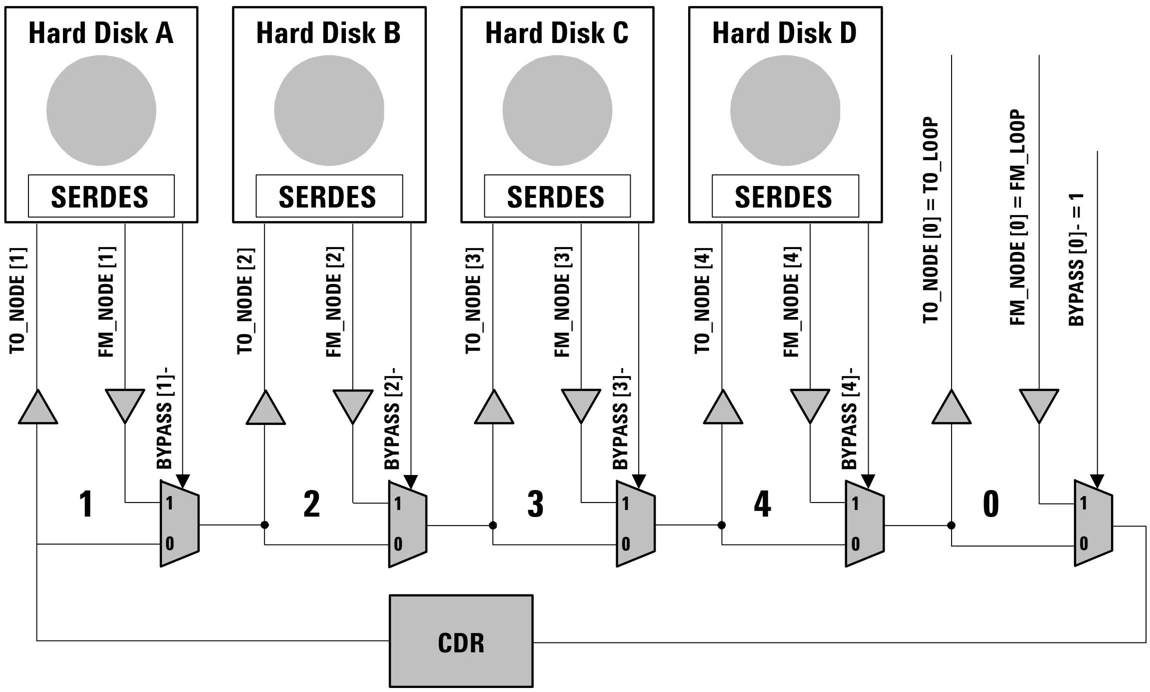

Figure 2 - Connection Diagram for CDR at First Cell

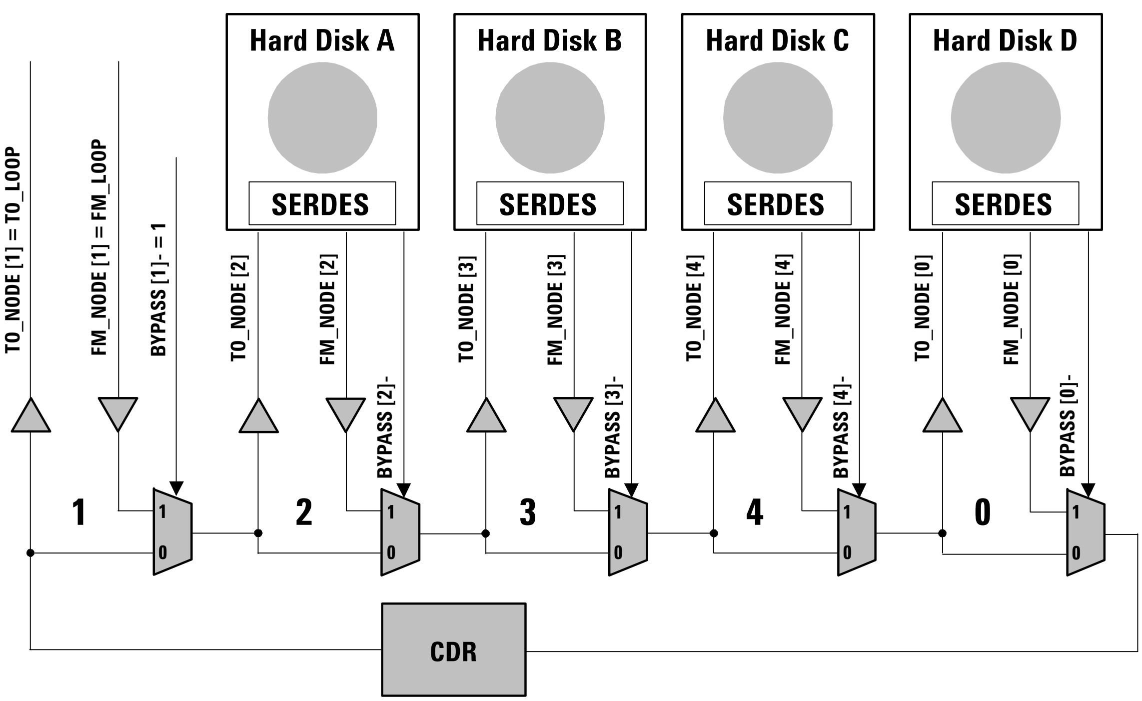

Figure 3 - Connection Diagram for CDR at Last Cell

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Table 1 - Pin Definitions for HDMP-0552. Refer to Figure 4 for pin layout

Pin Name	Pin	Pin Type	Pin Description
MODE_DV	24	I-LVTTL	**Data Valid Detect Mode**: To allow data valid detection, float MODE_DV HIGH. To configure chip for "CDR anywhere" capability, connect MODE_DV to GND through a 1 kΩ resistor.
FSEL	25	I-LVTTL	**Frame Select:** To configure single-frame operation of the data valid and amplitude valid detection circuits, connect FSEL to GND through a 1 kΩ resistor. To configure multi-frame (4-frame) operation of the data valid and amplitude valid detection circuits, float FSEL HIGH.
FM_NODE[0]_DV	23	O-LVTTL	**Data Valid:** Indicates valid Fibre Channel Data on the FM_NODE[0]± inputs when HIGH. Indicates either run length violation error or no comma detected when LOW.
FM_NODE[0]_AV	59	O-LVTTL	**Amplitude Valid:** Indicates acceptable signal amplitude on the FM_NODE[0]± inputs.
TO_NODE[0]+ TO_NODE[0]- TO_NODE[1]+ TO_NODE[1]- TO_NODE[2]+ TO_NODE[2]- TO_NODE[3]+ TO_NODE[3]- TO_NODE[4]+ TO_NODE[4]-	57 56 32 31 35 34 44 43 47 46	HS_OUT	**Serial Data Outputs:** High-speed outputs to a hard disk drive or to a cable input.
FM_NODE[0]+ FM_NODE[0]- FM_NODE[1]+ FM_NODE[1]- FM_NODE[2]+ FM_NODE[2]- FM_NODE[3]+ FM_NODE[3]- FM_NODE[4]+ FM_NODE[4]-	54 53 29 28 38 37 41 40 51 50	HS_IN	**Serial Data Inputs:** High-speed inputs from a hard disk drive or from a cable output.
BYPASS[0]- BYPASS[1]- BYPASS[2]- BYPASS[3]- BYPASS[4]-	55 30 36 42 49	I-LVTTL	**Bypass Inputs:** For "disk bypassed" mode, connect BYPASS[n]- to GND through a 1 kΩ resistor. For "disk in loop" mode, float HIGH.
CDR_SEL	10	I-LVTTL	**CDR Select:** To configure the chip with the CDR bypassed, connect CDR_SEL to GND through a 1 kΩ resistor. To configure the chip with the CDR in the loop, float CDR_SEL HIGH.
CDR_RATE	11	I-SSTL2	**CDR Rate:** To configure the chip for 1 GBd operation, connect CDR_RATE to GND through a 1 kΩ resistor. To configure the chip for 2 GBd operation, float CDR_RATE HIGH.
REF_RATE	12	I-LVTTL	**Reference Rate:** Float REF_RATE HIGH for a reference rate of 106.25 MHz and connect REF_RATE to GND via a 1 kΩ resistor for a reference rate of 53.125 MHz.
REFCLK	14	I-LVTTL	**Reference Clock:** A user-supplied clock reference used for frequency acquisition in the Clock and Data Recovery (CDR) circuit.
CPLL1 CPLL0	16 17	C C	**Loop Filter Capacitor:** A loop filter capacitor for the internal Clock and Data Recovery (CDR) circuit must be connected across the CPLL1 and CPLL0 pins. Recommended value is 0.1 µF.
EQ_SEL	61	I-LVTTL	**Equalizer Select:** Allows user to select/deselect equalization on any input.

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Table 1 (continued) - **Pin Definitions for HDMP-0552. Refer to Figure 4 for pin layout**

Pin Name	Pin	Pin Type	Pin Description
OUT_SEL	60	I-LVTTL	**Output Select:** Allows user to turn on/off any output driver.
ND0	64	I-LVTTL	**Node 0 Input:** In combination with EQ_SEL, allows the user to select/deselect equalization on FM_NODE[0]± inputs. In combination with OUT_SEL, allows the user to turn on/off the TO_NODE[0]± output driver. Float HIGH to select Node 0, or connect to GND through a 1 kΩ resistor to deselect Node 0.
ND1	63	I-LVTTL	**Node 1 Input:** In combination with EQ_SEL, allows the user to select/deselect equalization on FM_NODE[1]± inputs. In combination with OUT_SEL, allows the user to turn off/on the TO_NODE[1]± output driver. Float HIGH to select Node 1, or connect to GND through a 1 kΩ resistor to deselect Node 1.
ND2	62	I-LVTTL	**Node 2 Input:** In combination with EQ_SEL, allows the user to select/deselect equalization on FM_NODE[2]± inputs. In combination with OUT_SEL, allows the user to turn off/on the TO_NODE[2]± output driver. Float HIGH to select Node 2, or connect to GND through a 1 kΩ resistor to deselect Node 2.
ND3	20	I-LVTTL	**Node 3 Input:** In combination with EQ_SEL, allows the user to select/deselect equalization on FM_NODE[3]± inputs. In combination with OUT_SEL, allows the user to turn off/on the TO_NODE[3]± output driver. Float HIGH to select Node 3, or connect to GND through a 1 kΩ resistor to deselect Node 3.
ND4	21	I-LVTTL	**Node 4 Input:** In combination with EQ_SEL, allows the user to select/deselect equalization on FM_NODE[4]± inputs. In combination with OUT_SEL, allows the user to turn off/on the TO_NODE[4]± output driver. Float HIGH to select Node 4, or connect to GND through a 1 kΩ resistor to deselect Node 4.
TDO	2	O-LVTTL	JTAG
TDI	3	I-LVTTL	JTAG
nTRST	4	I-LVTTL	JTAG
TMS	5	I-LVTTL	JTAG
TCK	6	I-LVTTL	JTAG
NC	19	NC	**No Connect.**
GND	07 09 15 18 26 39 52	S	**Ground:** Normally 0 V.
V_{CC}	01 13 22 27 48	S	Digital Power Supply pin.
$V_{CC}A$	08	S	Analog Power Supply pin.
$V_{CC}HS$	33 45 58	S S S	Cells 1 and 2 High Speed Output Pins Power Supply. Cells 3 and 4 High Speed Output Pins Power Supply. Cell 0 High Speed Output Pins Power Supply.

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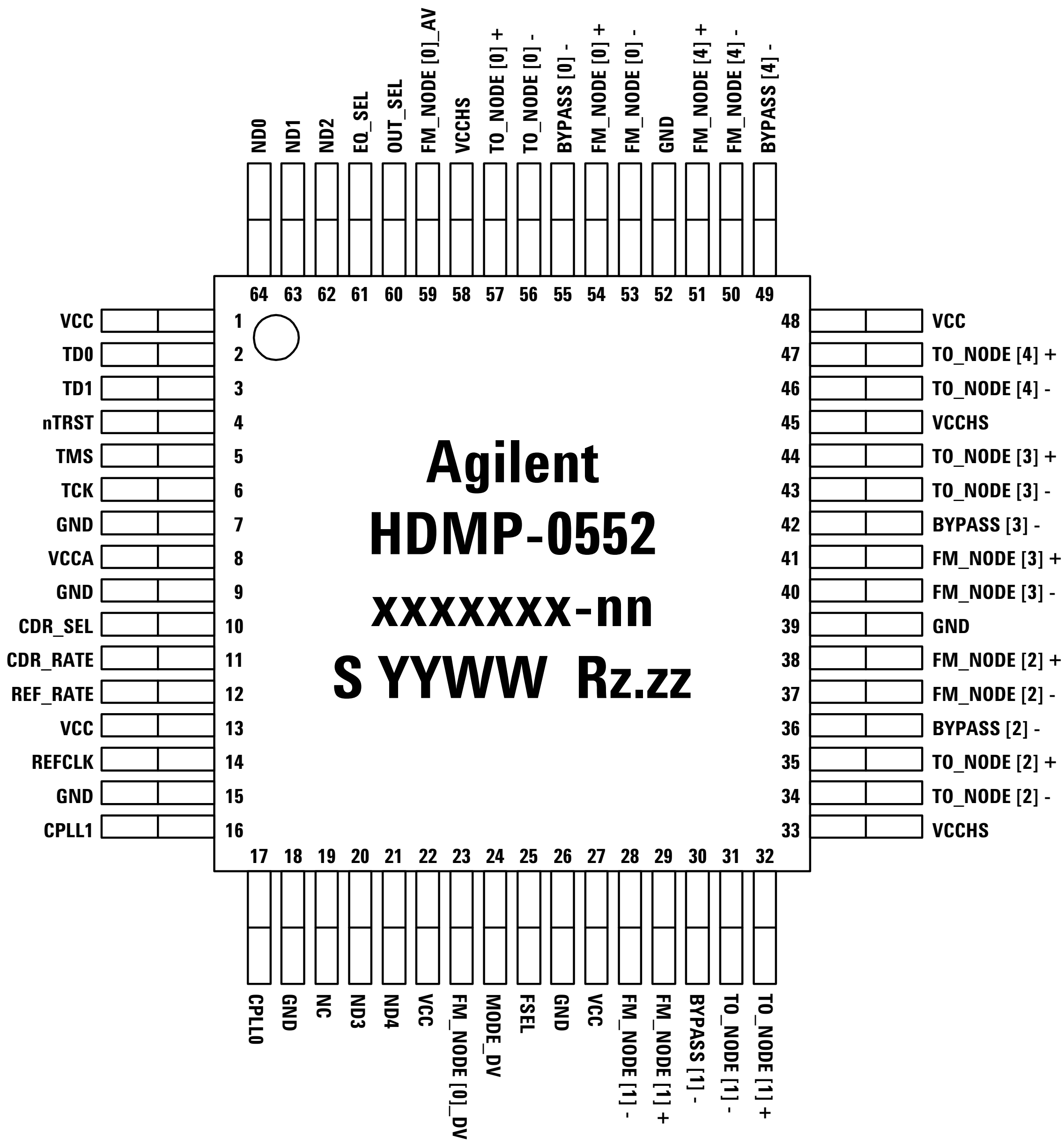

Figure 4 - HDMP-0552 package layout and marking, top view

xxxxxxx-nn = wafer lot - build number; S = Supplier Code; YYWW = Date Code (YY = year, WW = work week); Rz.zz = Die Revision; COUNTRY (on back side) = country of manufacture.

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Table 2 - I/O Type Definitions

I/O Type	Definition
I-LVTTL	LVTTL Input
O-LVTTL	LVTTL Output
HS_OUT	High Speed Output, BLL
HS_IN	High Speed Input
C	External circuit node
S	Power supply or ground
NC	No connect
I-SSTL2	SSTL2 compatible, non-terminated

Please refer to Figures 5 and 6 for simplified I/O diagrams.

Table 3 - Pin Connection Diagram to Achieve Desired CDR Location

Hard Disks	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
Connection to PBC cells	1	2	3	4	0	1	2	3	4	0	1	2	3	4	0	1	2	3	4	0
CDR position (x)	x A	B	C	D	A x	B	C	D	A	B x	C	D	A	B	C x	D	A	B	C	D x
Cell connected to Cable	0				4				3				2				1			

x denotes CDR position with respect to hard disks. For example A x B C D means the CDR is between disk A and disk B.

HDMP-0552 Electrical Specifications

Absolute Maximum Ratings

Ta = +25°C , except as specified.

Operation in excess of any of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Minimum	Maximum
VCC	Supply Voltage	V	-0.7	4.0
VIN, LVTTL	LVTTL Input Voltage	V	-0.7	5.0
VIN,HS_IN	HS_IN Input Voltage	V	2.0	VCC
IO,LVTTL	LVTTL Output Current	mA		+13
Tstg	Storage Temperature	°C	-65	+150
Tj	Junction Temperature	°C	0	+125

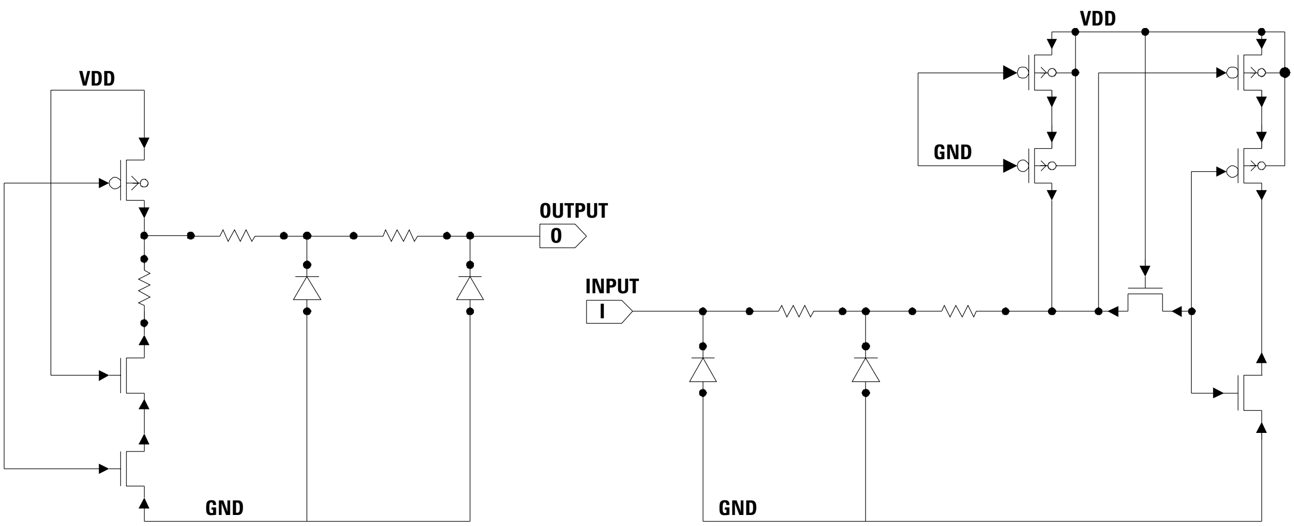

Figure 5 - Simplified Digital I/O Circuit Diagrams

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Guaranteed Operating Rates

Ta = 0°C to Tc = +80°C , VCC = 3.15 V to 3.45 V

Serial Clock Rate FC (MBd)	
Minimum	**Maximum**
1,040	1,080
2,080	2,160

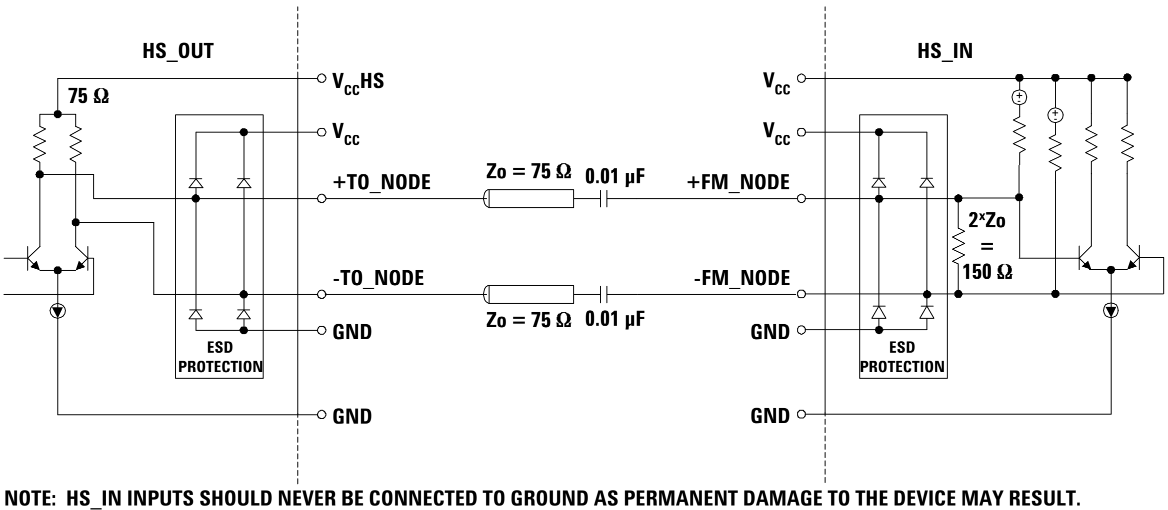

Figure 6 - O-BLL and I-BLL Simplified Circuit Schematic

Clock and Data Recovery Circuit (CDR) Reference Clock Requirements

Ta = 0°C to Tc = +80°C , VCC = 3.15 V to 3.45 V

Symbol	Parameter	Units	Minimum	Typical	Maximum
f	Nominal Frequency (REF_RATE = 1)	MHz		106.25	
f	Nominal Frequency (REF_RATE = 0)	MHz		53.125	
Ftol	Frequency Tolerance	ppm	-100		+100
Symm	Symmetry (duty cycle)	%	40		60

DC Electrical Specifications

Ta = 0°C to Tc = +80°C , VCC = 3.15 V to 3.45 V

Symbol	Parameter	Units	Minimum	Typical	Maximum
VIH[1],LVTTL	LVTTL Input High Voltage Range	V	2.0		Vcc
VIL,LVTTL	LVTTL Input Low Voltage Range	V	0		0.8
VOH[1],LVTTL	LVTTL Output High Voltage Range, IOH = -400 uA	V	2.2		Vcc
VOL,LVTTL	LVTTL Output Low Voltage Level, IOL = 1 mA	V	0		0.6
IIH,LVTTL	Input High Current (Magnitude), VIN = 2.4 V, VCC = 3.45 V	uA	0	5	40
IIL,LVTTL	Input Low Current (Magnitude), VIN = 0.4 V, VCC = 3.45 V	uA	0	65	300
ICC	Total Supply Current, Ta = +25°C	mA		320	

Note: 1. LVTTL I/Os 5 V tolerant.

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AC Electrical Specifications

Ta = 0°C to Tc = +80°C , VCC = 3.15 V to 3.45 V

Symbol	Parameter	Units	Minimum	Typical	Maximum
tdelay1	Total Loop Latency from FM_NODE[0] to TO_NODE[0]	ns		1.5	4.0
tdelay2	Per Cell Latency from FM_NODE[x] to TO_NODE[x+1]	ns		0.4	0.8
tr,LVTTLin	Input LVTTL Rise Time Requirement, 0.8 V to 2.0 V	ns		2	
tf,LVTTLin	Input LVTTL Fall Time Requirement, 2.0 V to 0.8 V	ns		2	
tr, LVTTLout	Output LVTTL Rise Time Range, 0.8 V to 2.0 V, 10 pF Load	ns		1.5	
tf, LVTTLout	Output LVTTL Fall Time Range, 2.0 V to 0.8 V, 10 pF Load	ns		2.0	
trs[2],HS_OUT	HS_OUT Single-Ended Rise Time	ps	44	65	110
tfs[2],HS_OUT	HS_OUT Single-Ended Fall Time	ps	44	65	110
trd[2],HS_OUT	HS_OUT Differential Rise Time	ps	44	65	110
tfd[2],HS_OUT	HS_OUT Differential Fall Time	ps	44	65	110
VIP,HS_IN	HS_IN Input Peak to Peak Required Differential Voltage Range	mV	200		2000
VOP,HS_OUT	HS_OUT Output Pk-Pk Diff. Voltage Range (Zo = 75 Ω)	mV	1100	1400	2000

Note: 2. Measured from 20% to 80% levels with trace length 3", Fr-4 board, Zo= 50 ohms and a 50 ohm and 200 fF termination. Please refer to Figure 6 for simplified circuit schematic.

Power Dissipation and Thermal Resistance

Ta = 0°C to Tc = +80°C , VCC = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typical	Maximum
PD	Power Dissipation	W	1.1	1.28
θjc	Thermal Resistance, Junction to Case	°C/W	2.5	

Output Jitter Characteristics

Ta = 0°C to Tc = +80°C , VCC = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typical
RJ	Random Jitter at TO_NODE pins (1 sigma rms)	ps	3.5
DJ	Deterministic Jitter at TO_NODE pins (pk-pk)	ps	10

Please refer to Figures 8 and 9 for jitter measurement setup information.

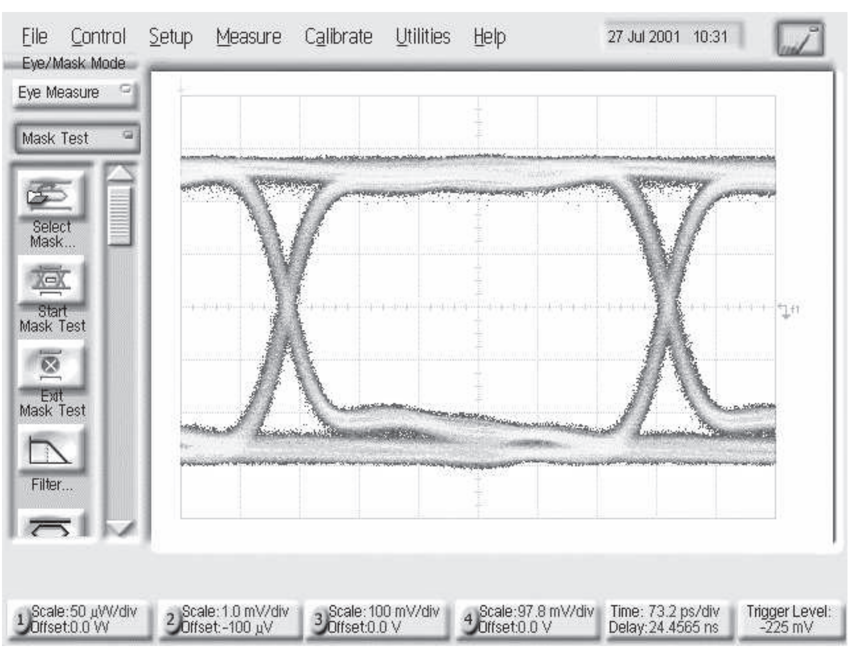

Figure 7 - Eye Diagram obtained differentially at 2.125 GBd FROM NODE(0) TO NODE(2) with 50 Ω termination

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Locking Characteristics

Ta = 0°C to Tc = +80°C , VCC = 3.15 V to 3.45 V

Parameter	Units	Maximum
Bit Sync Time (phase lock)	bits	2500
Frequency Lock at Powerup	μs	500

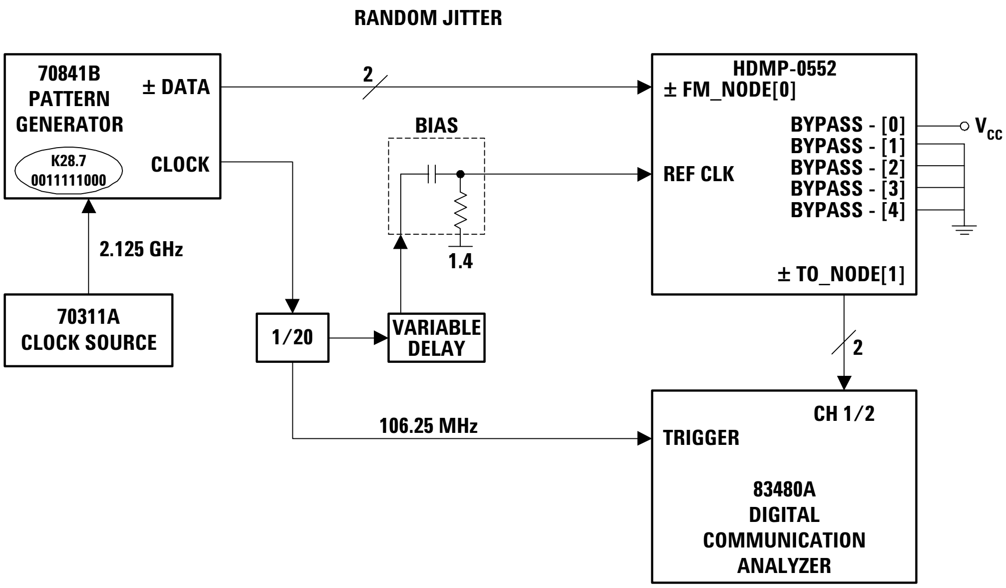

Figure 8 - Setup for Measurement of Random Jitter

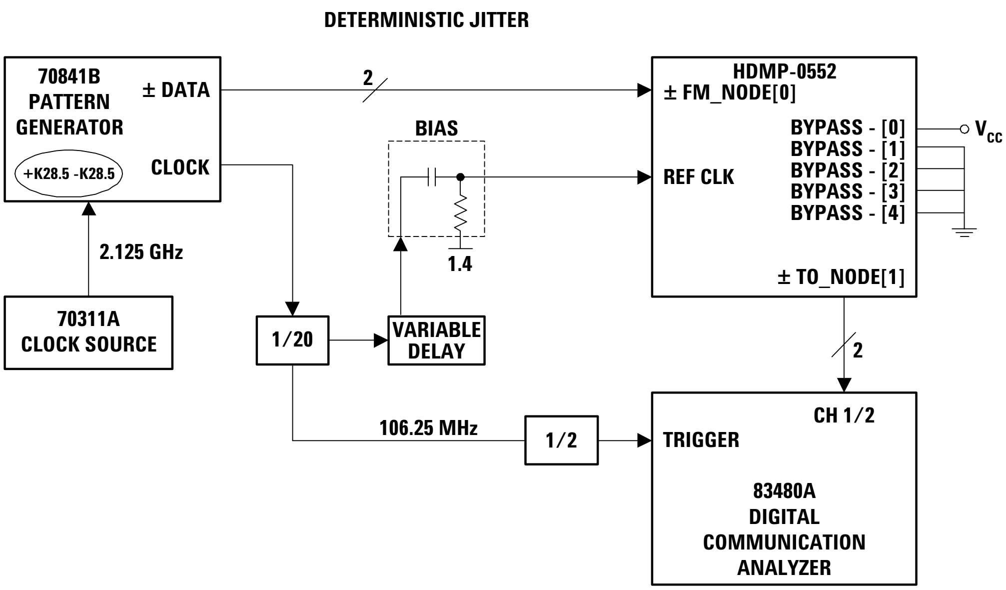

Figure 9 - Setup for Measurement of Deterministic Jitter

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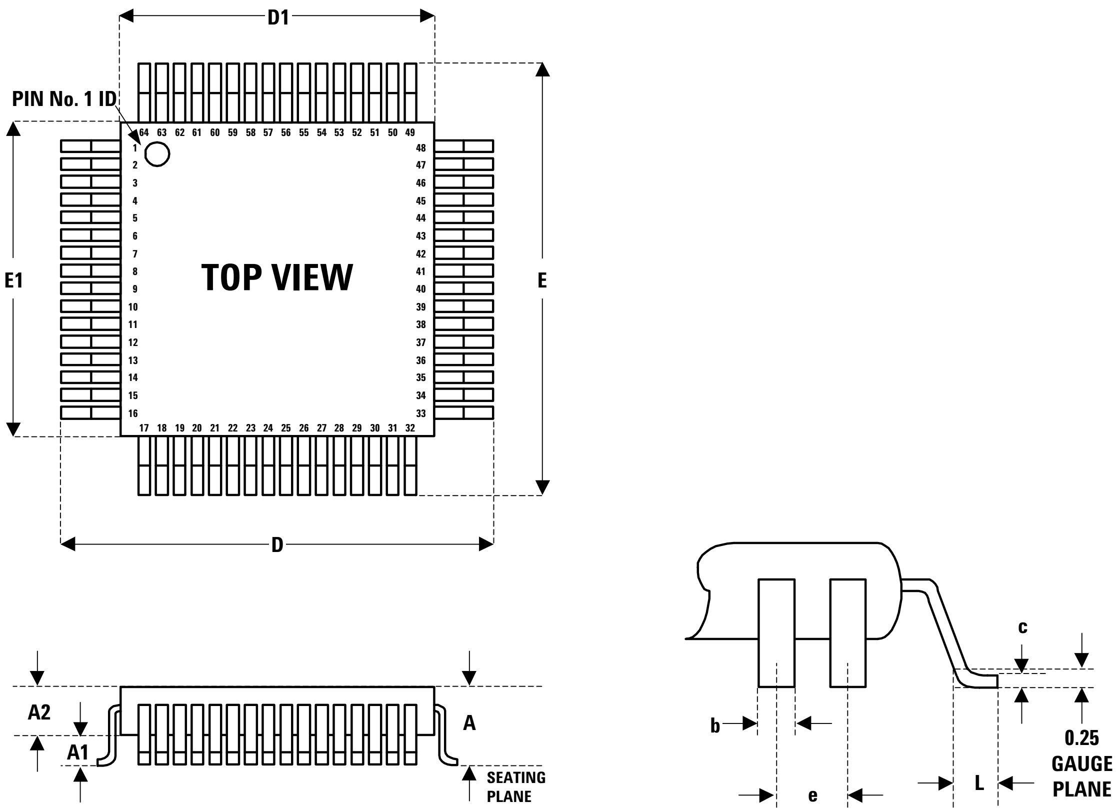
Package Information

Item	Details
Package Material	Plastic
Lead Finish Material	85% Tin, 15% Lead
Lead Finish Thickness	300-800 micro-inches
Lead Skew	0.08 mm maximum
Lead Coplanarity (Seating Plane Method)	0.08 mm maximum

Mechanical Dimensions



Dimensional Parameter (millimeters)	A	A1	A2	D/E	D1/E1	L	b	c	e
Value	2.45	0.25	2.00	13.20	10.00	0.88	0.22	0.17	0.50
Tolerance	MAX	MIN	+0.10, -0.05	±0.25	±0.10	+0.15, -0.10	±0.05	MAX	BASIC

Figure 10 - HDMP-0552 Package Drawing

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