SONET/SDH OC-3/12 TRANSMITTER AND RECEIVER

S3005/S3006

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports 139.264 Mbit/s (E4), 155.52 Mbit/s (OC-3), and 622.08 Mbit/s (OC-12) transmission rates
- Supports 139.264 Mbit/s and 155.52 Mbit/s Code Mark Inversion (CMI) interfaces
- Selectable reference frequencies of 19.44, 38.88, 51.84, and 77.76 MHz (OC-3/12) and 17.408, 34.816, 46.421, and 69.632 MHz(E4)
- Interface to both ECL and TTL logic
- 8-bit TTL/CMOS datapath
- Bypass mode for off-chip clocking
- Local and line loopback mode
- Lock detect
- Low jitter ECL interface
- Low power
- 80 PQFP or 68 LDCC package

APPLICATIONS

- SONET/SDH or E4-based transmission systems
- SONET/SDH or E4 modules
- SONET/SDH or E4 test equipment
- ATM over SONET
- Section repeaters
- Add drop multiplexors
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

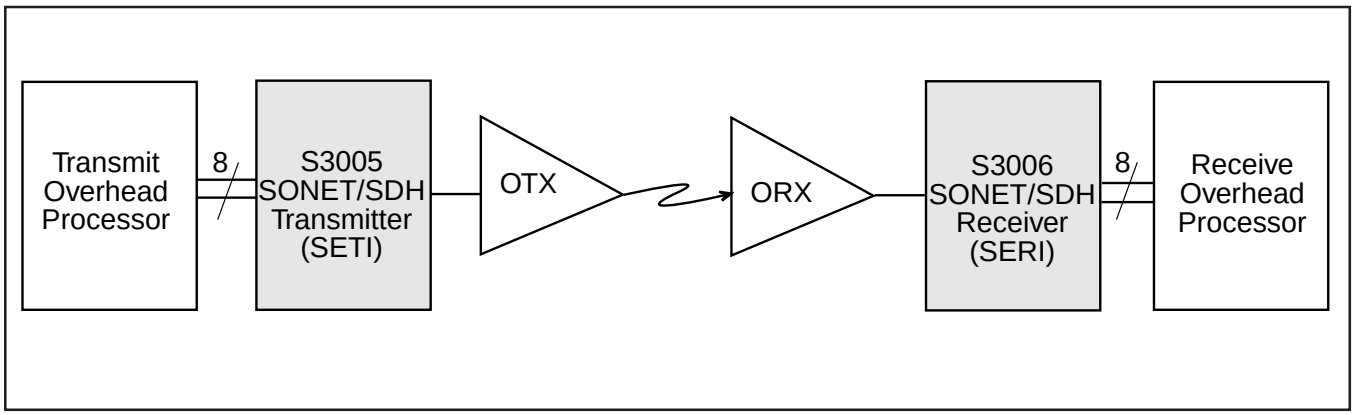
GENERAL DESCRIPTION

The S3005/S3006 Synchronous Electrical Transmit Interface, SETI, and Synchronous Electrical Receive Interface, SERI, SONET/SDH and E4 transmitter and receiver chips are the first fully integrated serialization/deserialization interface devices covering E4 (139.264 Mbit/s), SONET OC-3 (155.52 Mbit/s) and SONET OC-12 (622.08 Mbit/s). With architecture developed by PMC-Sierra, the chipset performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH and E4 transmissions standards. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3005 SETI transmitter chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the S3006 SERI receiver chip by synchronizing its on-chip VCO directly to the incoming data stream. The S3006 also performs SONET/SDH frame detection. The chipset can be used with 19.44, 38.88, 51.84, and 77.76 MHz reference clocks when operated in the SONET/SDH OC-3 or OC-12 modes. In the E4 mode the chipset can be operated with 17.408, 34.816, and 69.632 MHz reference clocks in support of existing system clocking schemes. On-chip code-mark-inversion (CMI) encoding and decoding is provided for 139.264 Mbit/s and 155.52 Mbit/s interfaces. If desired, both clock generation and recovery can be bypassed, allowing the use of externally generated and recovered clocks.

The very low jitter ECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3005/S3006 SETI and SERI chipset is packaged in a 50 mil pitch, 68-pin LDCC or 25 mil pitch, 80 PQFP package, offering designers a small package outline.

Figure 1. System Block Diagram



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SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3005/S3006 chipset supports OC-3 rates (155.52 Mbit/s) and OC-12 (622.08 Mbit/s) rates.

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-3 consists of nine transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 9 overhead and 261 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3)

For more details on SONET operations, refer to the ANSI SONET standard document.

Figure 2. SONET Structure

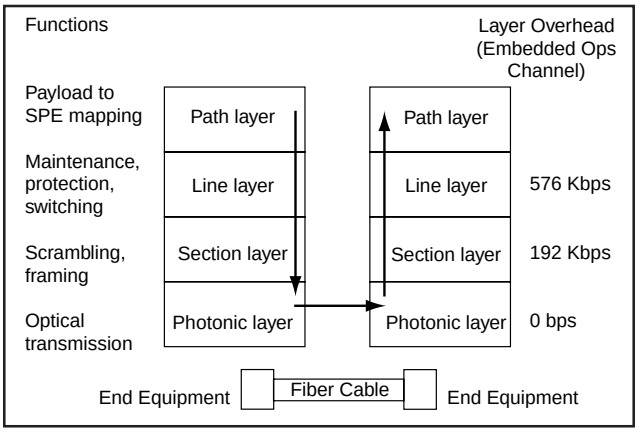
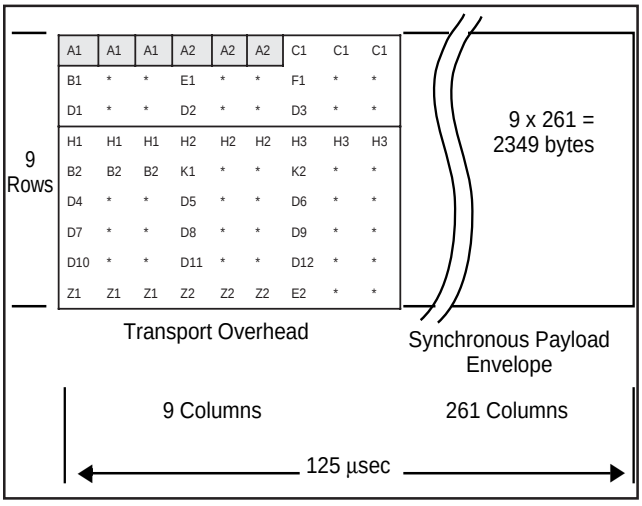


Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-9		OC-9	466.56
STS-12	STM-4	OC-12	622.08
STS-18		OC-18	933.12
STS-24		OC-24	1244.16
STS-36		OC-36	1866.24
STS-48	STM-16	OC-48	2488.32

Figure 3. STS–3/OC–3 Frame Format



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S3005/S3006 OVERVIEW

The S3005 SETI and S3006 SERI implement SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagrams in Figures 4 and 5 show basic operation of both chips. These chips can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface (S3005) and the serial receive interface (S3006). The chipset handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing, which includes management of the datastream, framing, and clock distribution throughout the front end.

Operation of the S3005/S3006 chips is straightforward. The sequence of operations is as follows:

Transmitter

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. CMI encoding (optional)
4. Serial output

Receiver

1. Clock and data recovery from serial input
2. CMI decoding (optional)
3. Frame detection
4. Serial-to-parallel conversion
5. 8-bit parallel output

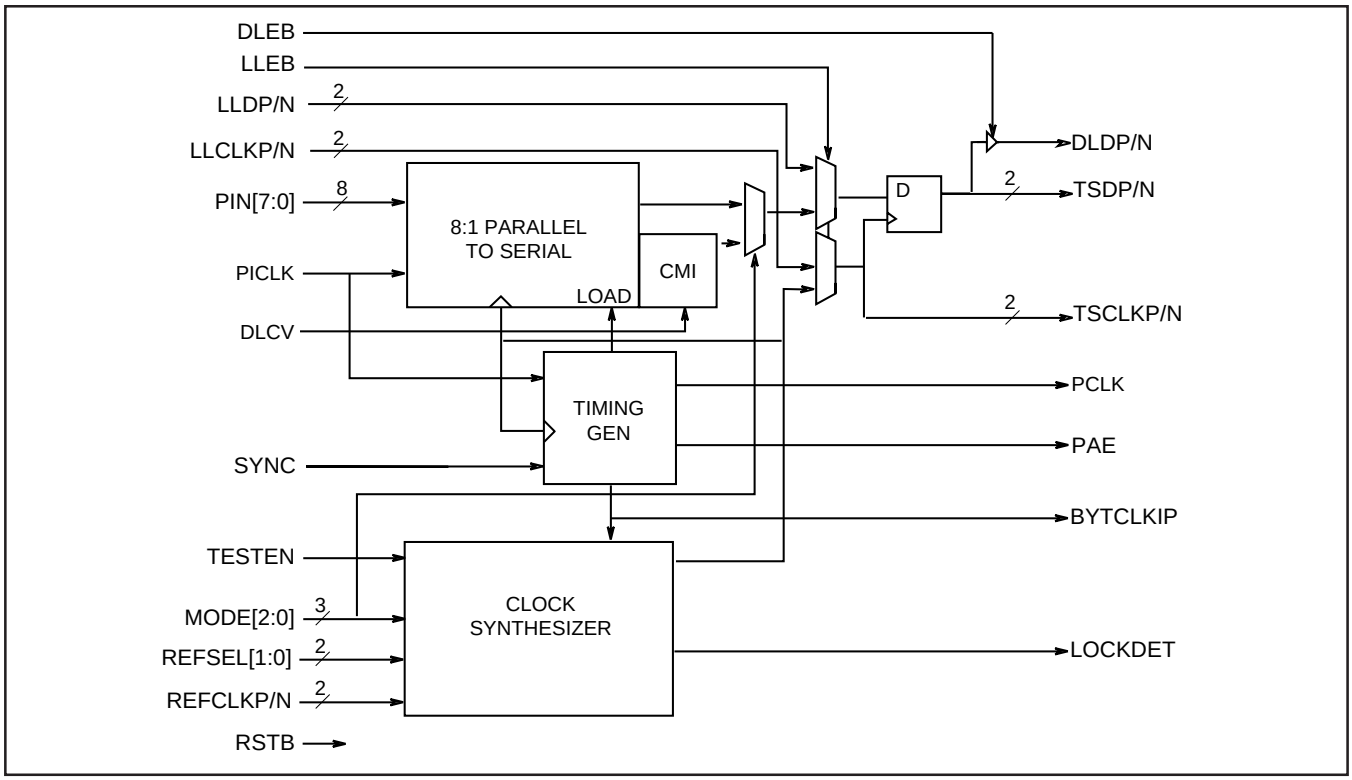
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 10 through 18. On-chip clock generation can be bypassed and an externally generated clock used in its place, providing an additional measure of design flexibility.

A lock detect feature is provided on both chips.

Suggested Interface Devices

PMC PM5345	SUNI	Saturn User Network Interface
PMC PM5355	SUNI-622	Saturn User Network Interface
IGT WAC–013–A		SONET LAN ATM Processor
Fujitsu MB86683B	NTC	Network Termination Controller
PMC PM5301	SSTX	Section Terminating Transceiver
PMC PM5312	STTX	Transport Terminating Transceiver
AT&T ASTROTEC1227/1230	650 Mbit/s	Fiber Optic Transmitter
Mitsubishi MF-622DF-T12-XXX	622 Mbit/s	Fiber Optic Transmitter
AT&T ASTROTEC 1310	650 Mbit/s	Fiber Optic Receiver
Mitsubishi MF-622DS-R1X-XXX	622 Mbit/s	Fiber Optic Receiver

Figure 4. SONET/SDH Transmitter Functional Block Diagram



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S3005 TRANSMITTER FUNCTIONAL DESCRIPTION

The S3005 SETI transmitter chip performs the serializing stage in the processing of a transmit SONET STS-12, STS-3, or ITU-T E4 bit serial data stream. It converts the byte serial data stream to bit serial format at 622.08, 155.52, or 139.264 Mbit/s depending on the control settings and reference frequency provided by the user. A Coded-Mark-Inversion (CMI) is available for use during 155.52 Mbit/s STS-3 (electrical) and 139.264 Mbit/s E4 operational modes. (See Other Operating Modes.)

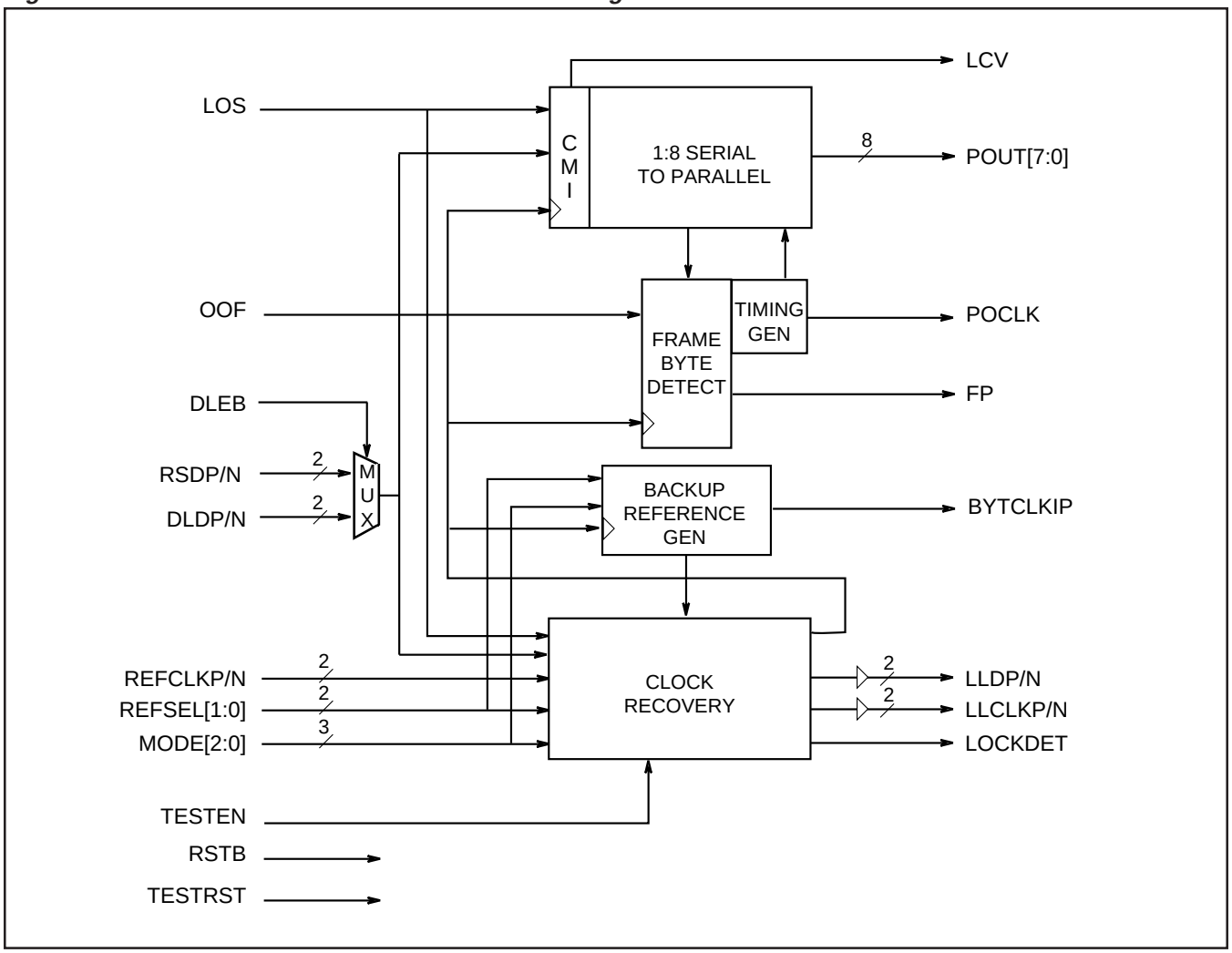
A high-frequency bit clock can be generated from a variety of lower frequency references by using the integral frequency synthesizer consisting of a phase-locked loop circuit with an adjustable divider in the loop.

For applications that provide a high-frequency bit clock externally, the internal synthesizer may be bypassed. Reference frequencies of 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz are selectable for SONET/SDH by the two reference select input pins. In E4 applications, these same pins can select the reference frequency from 17.408 MHz, 34.816 MHz, 46.421 MHz, or 69.632 MHz.

Loopback modes are provided for diagnostic loopback (transmitter to receiver), or line loopback (receiver to transmitter) when used with the compatible S3006. (See Other Operating Modes.)

The operating mode is selected by three mode programming inputs to be 622.08 Mbit/s, 155.52 Mbit/s, 155.52 Mbit/s with Coded-Mark-Inversion (CMI) encoding, or 139.264 Mbit/s with CMI encoding.

Figure 5. SONET/SDH Receiver Functional Block Diagram



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Clock Synthesizer

The Clock Synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCLK). There are three selectable output clock frequencies that are synthesizable from any of four selectable reference frequencies for SONET/SDH operation.

The MODE[2:0] inputs select the output serial clock frequency to be 622.08 MHz for STS-12, 311.04 MHz for CMI-encoded STS-3, 155.52 MHz for STS-3, or 278.528 MHz for CMI-encoded E4. Their frequencies are selected as shown in Table 2.

The REFSEL[1:0] inputs in combination with the MODE[2:0] inputs select the ratio between the output clock frequency and the reference input frequency, as shown in Tables 3 and 4. This ratio is adjusted for each of the four modes so that the reference frequency selected by the REFSEL[1:0] is the same for all modes.

The REFCLK input must be generated from a differential ECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system.

In order to meet the .01 UI SONET jitter specifications, the maximum reference clock jitter must be guaranteed over the 12KHz to 1MHz bandwidth. For details of reference clock jitter requirements, see Table 5.

The on–chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLK input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. The loop filter's corner frequency is optimized to minimize output phase jitter. The loop filter capacitor is included on the package.

Table 2. Clock Frequency Options

MODE[2:0]	OUTPUT CLOCK FREQUENCY	OPERATING MODE
100	622.08 MHz	STS–12
001	311.04 MHz	STS–3 CMI
010	155.52 MHz	STS–3
011	278.528 MHz	E4 CMI

Timing Generator

The Timing Generator function, seen in Figure 4, provides two separate functions. It provides a byte rate version of the TSCLK, and a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel-to-serial shift register.

The PCLK output is a byte rate version of TSCLK. For STS-12, the PCLK frequency is 77.76 MHz, and for NRZ or CMI coded STS-3, its frequency is 19.44 MHz. For CMI coded E4, its frequency is 17.408 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3005 device.

Table 3. Reference Frequency Options

REFSEL [1:0]	REFERENCE CLOCK FREQUENCY	OPERATING MODE
00	19.44 MHz	STS–12,STS–3
01	38.88 MHz	STS–12,STS–3
10	51.84 MHz	STS–12,STS–3
11	77.76 MHz	STS–12

Table 4. E4CMI Reference Frequency Options

REFSEL [1:0]	REFERENCE CLOCK FREQUENCY	OPERATING MODE
00	17.408 MHz	—
01	34.816 MHz	—
10	46.421 MHz	—
11	69.632 MHz	—

Table 5. Reference Jitter Limits

Maximum Reference Clock Jitter in 12 KHz to 1 MHz Band	Operating Mode
14 ps	STS–12
28 ps	STS–3 CMI
56 ps	STS–3

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In the parallel-to-serial conversion process, the incoming data is passed from the PICLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TSCLK. Although the frequency of PICLK and the internally generated byte clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated byte clock. Should the magnitude of the phase difference be less than one bit period, and if the SYNC input is high, the timing block inverts the internal byte clock.

Since the inversion of the internal byte clock will corrupt one byte of data, SYNC should be held low except when a phase correction is desired. When a timing domain phase difference of less than one bit period is detected, the Phase Alignment Event output (PAE) pulses high for one PCLK clock period. If the condition persists, PAE will remain high. When PAE conditions occur, SYNC should be activated until the condition is no longer present.

The Timing Generator also produces a feedback reference clock to the Clock Synthesizer (BYTCLKIP). A counter divides the synthesized clock down to the same frequency as the reference clock REFCLK. The PLL in the Clock Synthesizer maintains the stability of the synthesized clock by comparing the phase of the BYTCLKIP clock with that of the reference clock (REFCLK). The modulus of the counter is a function of the reference clock frequency and the operating frequency.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 4 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. In STS-12 and STS-3 NRZ modes, the serial data is shifted out of the second register at the TSCLK rate. In STS–3 CMI and E4 CMI modes, the serial data shifts out at the TSCLK/2 rate to the CMI encoder.

S3006 RECEIVER FUNCTIONAL DESCRIPTION

The S3006 SERI receiver chip provides the first stage of digital processing of a receive SONET STS-12, STS-3, or ITU-T E4 bit serial stream. It converts the bit-serial 622.08, 155.52, or 139.264 Mbit/s data stream into 78 Mbyte/s, 19 Mbyte/s, or 17 Mbyte/s byte-serial data format depending on the control settings and reference frequency provided by the user. A Coded Mark Inversion (CMI) decoder can be enabled during 155.52 Mbit/s and 139.264 Mbit/s operation for decoding STS-3 electrical and E4 signals. These modes are selected by three input pins.

Clock recovery is performed on the incoming scrambled NRZ or CMI–coded data stream. A reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference frequency to the nominal bit rate. Reference frequencies of 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz are selectable for SONET/SDH by the two reference select input pins. In E4 applications, these same pins can select the reference frequency from 17.408 MHz, 34.816 MHz, 46.421 MHz, or 69.632 MHz. For applications that provide a high-frequency bit clock externally, the internal synthesizer may be bypassed. (See Other Operating Modes.)

A loopback mode is provided for diagnostic loopback (transmitter to receiver). Signal pins are provided to allow for line loopback (receiver to transmitter) when used with the compatible S3005 device.

Clock Recovery

The Clock Recovery function, as shown in the block diagram in Figure 5, generates a clock that is frequency matched to the incoming data baud rate at the RSD or DLD differential inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) to which the PLL locks when data is lost.

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The MODE[2:0] inputs select the recovered serial clock frequency to be 622.08 MHz for STS-12, 311.04 MHz for CMI-encoded STS-3, 278.528 MHz for CMI-encoded E4, or 155.52 MHz for STS-3 NRZ. These frequencies are selected as shown in Table 2.

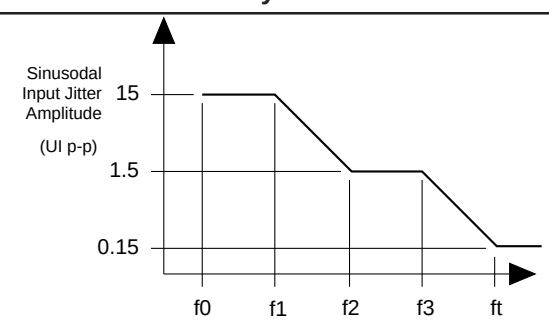
The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming encoded data stream has been low continuously for 4000 to 8000 recovered clock cycles, loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock. Alternatively, the loss-of-signal (LOS) input can be used to force a loss-of-signal condition. When active, LOS squelches the incoming data stream, and causes the PLL to switch its source of reference. Loss-of-signal condition is removed when LOS is inactive, and good data, with acceptable pulse density and run length, returns on the incoming data stream.

When the test clock enable (TESTEN) input is set high, the clock recovery block is disabled. The reference clock (REFCLK) is used as the bit rate clock input in place of the recovered clock. The frequency of the REFCLK should be appropriate for the desired data rate. The reference selection inputs REFSEL[1:0] have no effect when TESTEN is set high.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a typical capture time of 32 µs for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which meets, with ample margin, the minimum tolerance proposed for SONET equipment by the T1X1.6/91-022 document, shown in Figure 6.

Figure 6. Clock Recovery Jitter Tolerance



OC/STS Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
3	10	30	300	6.5	75
12	10	30	300	25	250

Backup Reference Generator

The Backup Reference Generator seen in Figure 5 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCLK. The modulus of the counter is a function of the reference clock frequency and the operating frequency. The frequency of the reference clock is selected by the REFSEL[1:0] inputs, as shown in Tables 3 and 4.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. This pattern occurs in both STS-3 and STS-12. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or DLD). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 or STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 µs, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

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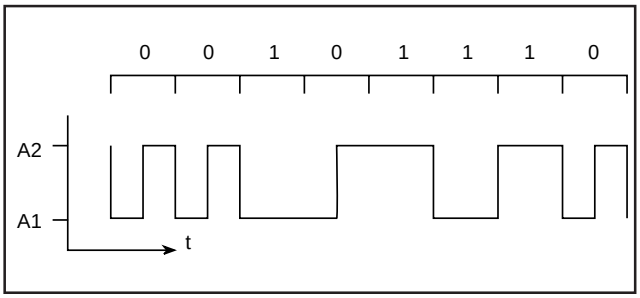
The Frame and Byte boundary Detection function is not utilized in the E4 operating mode. It is recommended that the OOF input remain low at all times for E4 operation to avoid spurious realignment of the byte boundary, and the FP output should be ignored.

Serial to Parallel Converter

The Serial to Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock generated by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial to Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

Figure 7. CMI Encoded Data



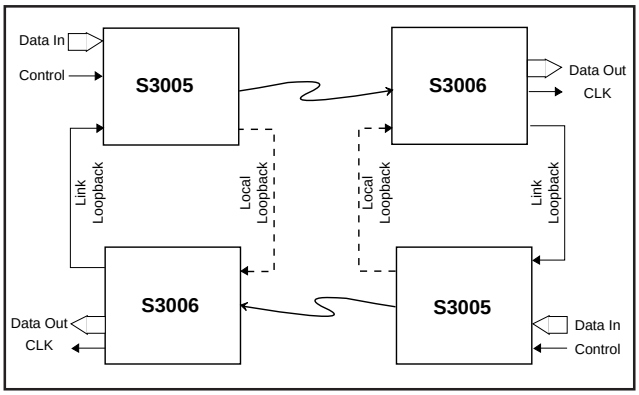
OTHER OPERATING MODES

CMI Encoding and Decoding

Coded Mark Inversion format (CMI) ensures at least one data transition per bit period, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the rest of that bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the ones bit period alternates at each occurrence of a one. Figure 7 shows an example of CMI-encoded data. The STS-3 electrical interface and the E4 interface are specified to have CMI-encoded data.

The CMI encoder on the S3005 SETI accepts serial data from the Parallel-to-Serial converter block at one half the TSCLK rate. The data is then encoded into CMI format, and the result is shifted out into the output selection logic at the TSCLK rate (311.04 MHz for STS-3 electrical, 278.528 MHz for E4). The MODE[2:0] inputs control whether the CMI encoder is in the data path. The encoder is only in the data path when the STS-3 CMI or the E4 CMI modes are selected. A single CMI violation can be inserted for diagnostic purposes by applying a low-to-high transition on DLCV. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

Figure 8. Loopback Diagram



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The CMI decoder block on the S3006 SERI accepts serial data from the RSDP/N input at the TSCLK rate (311.04 MHz or 278.528 MHz). The data is then decoded from CMI to NRZ format and converted from serial to parallel at one half the TSCLK rate.

Note that in CMI operating mode, the data bit rate is one half of the recovered clock rate.

Diagnostic Loopback

The Diagnostic Loopback path consists of alternate serial data outputs (in the case of the S3005) and inputs (in the case of the S3006).

On the S3005, the differential ECL output DLD provides Diagnostic Loopback serial data. When the Diagnostic Loopback Enable (DLEB) input is low, this data output is a replica of TSD. When DLD is connected to the S3006, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. When DLEB is high, DLD is held in the inactive state, with the positive output high and the negative output low. In the inactive state, there will be no interference from the transmitter to the receiver. The DLD outputs on the S3005 should be held inactive (DLEB high) when not in use to avoid potential crosstalk of the asynchronous DLD signals with the serial data signals.

On the receiver side, the differential ECL input DLD is the Diagnostic Loopback serial data input. When the Diagnostic Loopback Enable (DLEB) input is set low, the DLD input is routed in place of the normal data stream (RSD).

Line Loopback

The Line Loopback circuitry consists of alternate clock and data output drivers. For the S3005, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable input (LLEB) is high, it selects data and clock from the Parallel to Serial Converter block or the CMI Encoder block. When LLEB is low, it forces the output data multiplexor to select data and clock from the LLD and LLCLK inputs. When these inputs are connected to the Line Loop Clock (LLCLK) and Line Loop Data (LLD) outputs of a S3006 receiver, a receive-to-transmit loopback can be established at the serial data rate.

Test and Bypass Modes

The Test Clock Enable (TESTEN) inputs on both chips provide access to the PLL.

The PLL-generated clock source on both the S3005 and S3006 can be bypassed by setting TESTEN high. In this mode, an externally generated bit serial clock source must be applied at the REFCLK input. Table 6 lists the possible combinations allowed in bypass mode.

Table 6. Bypass Mode

TESTEN	MODE[2:0]	Reference Clock Frequency In Bypass Mode	Serial Data Rate (Mbit/s)
0	XXX	Normal Operating Mode (See Table 2)	—
1	100	622.08	622.08
1	101	311.04	155.52 CMI
1	101	278.528	139.264 CMI
1	110	155.52	155.52

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S3005 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin # (80 PQFP)	Pin # (68 LDCC)	Description
PIN7 PIN6 PIN5 PIN4 PIN3 PIN2 PIN1 PIN0	TTL	I	37 36 33 32 31 30 29 28	2 3 5 8 9 10 12 14	Parallel data input, a 77.76 Mbyte/s, 19.44 Mbyte/s, or 17.408 Mbyte/s word, aligned to the PICLK parallel input clock. PIN7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN(7-0) is sampled on the rising edge of PICLK.
PICLK	TTL	I	48	60	Parallel input clock, a 77.76 MHz, 19.44 MHz, or 17.408 MHz nominally 50% duty cycle input clock, to which PIN(7-0) is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN(7-0).
TESTEN	TTL	I	6	31	Test clock enable signal, set high to provide access to the PLL during production tests. (See Table 6.)
SYNC	TTL	I	50	58	Active high synchronization enable input that enables the timing generator to invert the internal byte transfer clock if transfers from the PIN(7-0) input holding register are occurring less than one bit period before or after clocking new data into the holding register. The SYNC pin is an asynchronous input.
REFCLKP REFCLKN	Diff. ECL	I	77 75	36 38	Inputs used as the reference for the internal bit clock frequency synthesizer, or used as an externally provided bit clock. (See Tables 3 and 4.)
REFSEL1 REFSEL0	TTL	I	10 11	28 27	Inputs used to select the reference frequency for the internal clock synthesizer. (See Tables 3 and 4.)
MODE2 MODE1 MODE0	TTL	I	43 45 44	66 63 65	Inputs used to select the operating mode of the device as 622.08 Mbit/s (STS-12); 155.52 Mbit/s (STS-3); 155.52 Mbit/s CMI (STS-3 electrical); or 139.764 Mbit/s (E4 CMI). (See Table 2.)
LLDP LLDN	Diff. ECL	I	64 62	49 51	Line loopback data inputs normally provided from a companion S3006 device. Used to implement a line loopback, in which the received bit serial data and clock signals are regenerated and passed through the S3005 transmitter. An internal 100-Ω resistor terminates LLDP to LLDN.
LLCLKP LLCLKN	Diff. ECL	I	68 66	45 47	Line loopback clock inputs normally provided from a companion S3006 device. Used to implement a line loopback, in which the received bit serial data and clock signals are regenerated and passed through the S3005 transmitter. An internal 100-Ω resistor terminates LLCLKP to LLCLKN.

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S3005 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin # (80 PQFP)	Pin # (68 LDCC)	Description
DLCV	TTL	I	49	59	Diagnostic line code violation input. A rising edge causes a CMI code violation in the serial output data. DLCV is an asynchronous input which is only valid when CMI is enabled.
DLEB	TTL	I	12	26	Diagnostic loopback enable signal. Enables the DLD output when low. When DLEB is high, the DLD output is held in the inactive state to prevent interference between the transmit and receive devices. Will not affect the TSD signals.
LLEB	TTL	I	51	57	Line loopback enable input. When low, the LLD and LLCLK inputs are connected to the TSD and TSCLK outputs to implement line loopback. When in normal mode (LLEB high), the internally generated data and clock signals are output at TSD and TSCLK.
RSTB	TTL	I	9	29	Reset input for the device, active low.
TSDP TSDN	Diff. ECL	O	74 72	39 41	High-speed source-terminated serial data stream signals, normally connected to an optical transmitter module. Updated on the falling edge of TSCLK.
DLDP DLDN	Diff. ECL	O	25 24	15 16	High-speed diff. ECL serial data stream signals, normally connected to a companion S3006 device for diagnostic loopback purposes. The DLD outputs are updated on the falling edge of TSCLK. They are held in the inactive state, except when DLEB is low.
TSCLKP TSCLKN	Diff. ECL	O	69 70	44 43	High-speed source-terminated diff. ECL transmit serial clock. Phase-aligned with the TSD and DLD output signals. TSCLK can be a buffered version of the internal frequency synthesizer clock, of the REFCLK inputs during clock bypass (TESTEN high), or of the LLCLK inputs during line loopback (LLEB low).
PCLK	TTL/ CMOS	O	16	23	A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3005 device.
PAE	TTL/ CMOS	O	18	20	Phase alignment event signal, that pulses high during each PCLK cycle for which there is less than one bit period between the internal byte clock and PICLK timing domains. PAE is updated on the falling edge of the PCLK outputs.
BYTCLKIP	TTL/ CMOS	O	17	21	Reference feedback clock. It is compared with the reference clock (REFCLK) to maintain stability of the clock synthesis PLL. BYTCLKIP is at the same frequency as REFCLK and is an asynchronous output.

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S3005 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin # (80 PQFP)	Pin # (68 LDCC)	Description
LOCKDET	TTL	O	52	56	Lock detect signal. Goes high after the PLL has had time to lock onto the clock provided on the REFCLK pins (approx. 2000 REFCLK cycles). LOCKDET is an asynchronous output.
CAP1 CAP2	–	I	1,2, 79, 80	– –	The loop filter capacitor is connected to these pins. The capacitor value should be 0.01µf ±10% tolerance, X7R dielectric. 50 V is recommended (16 V is acceptable).
AGND	GND	–	5, 56, 65, 71, 76	32, 37, 42, 48, 54	Analog Ground (0V)
AVEE	–4.5V	–	4, 57, 63, 67, 73	33, 40, 46, 50, 53	Power Supply (–4.5V)
ECLGND	GND	–	7, 15, 19, 22, 26, 35, 39, 42, 46, 54	4, 13, 18, 25, 34, 52, 61, 68	ECL Ground (0V)
VEE	–4.5V	–	8, 14, 27, 34, 47, 53	6, 7, 11, 24, 30, 62	Power Supply (–4.5V)
TTLGND	GND	–	20, 41	22, 64, 67	TTL Ground (0V)
VCC	+5V	–	21, 40	1, 17, 19	Power Supply (+5V)
NC	–	–	3, 13, 23, 38, 55, 58, 59, 60, 61, 78	35, 55	No connection

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S3006 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin # (80 PQFP)	Pin # (68 LDCC)	Description
RSDP RSDN	Diff. ECL	I	62 64	51 49	High-speed diff. ECL receive serial data stream signals, normally connected to an optical receiver module. When internal clock recovery is used, clock is recovered from transitions on the RSD inputs. When external clock recovery is used, the RSD inputs are sampled on the rising edge of the reference (REFCLK). An internal 100-Ω termination resistor is connected across RSDP and RSDN.
DLDP DLDN	Diff. ECL	I	66 68	47 45	High-speed diff. ECL diagnostic loopback data. Serial data stream signals, normally connected to a companion S3005 device for diagnostic loopback purposes. Clock is recovered from transitions on the DLD inputs while in diagnostic loopback. An internal 100- termination resistor is connected across DLDP and DLDN.
DLEB	TTL	I	51	57	Selects diagnostic loopback. When DLEB is high, the S3006 device uses the primary data (RSD) input. When low, the S3006 device uses the diagnostic loopback data (DLD) input.
TESTEN	TTL	I	6	31	Test clock enable signal, set high to provide access to the PLL during production tests. Can also be used to enable an external clock source in bypass mode (see Table 6).
OOF	TTL	I	50	58	Out of frame indicator used to enable framing pattern detection logic in the S3006. This logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 17 and 18.)
LOS	ECL	I	16	23	An active-high, single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power (Loss of Signal). When LOS is high, the data on the Serial Data In (RSDP/N) pins will be internally forced to a constant zero, LOCKDET will be forced low, and the PLL will lock to the REFCKINP/N inputs. This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. (This ensures that the PLL does not "wander" out of reacquisition range by tracking the random phase/frequency content of the optical detector's noise floor while monitoring "dark" fiber.) When LOS is low, data on the RSDP/N pins will be processed normally.

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S3006 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin # (80 PQFP)	Pin # (68 LDCC)	Description
REFCLKP REFCLKN	Diff. ECL	I	77 75	36 38	Input normally used as the reference for the integral clock recovery PLL. (See Tables 3 and 4.) When the test clock enable (TESTEN) input is set high, REFCLK replaces the bit rate recovered clock. (See Table 6.)
REFSEL1 REFSEL0	TTL	I	12 11	26 27	Inputs used to select the reference frequency for the internal clock synthesizer. (See Tables 3 and 4.)
MODE2 MODE1 MODE0	TTL	I	49 10 9	59 28 29	Inputs used to select the operating mode of the device as 622.08 Mbit/s (STS-12); 155.52 Mbit/s (STS-3); 155.52 Mbit/s CMI (STS-3 electrical); or 139.764 Mbit/s (E4 CMI). (See Table 2.)
TESTRST	TTL	I	18	20	Used to reset portions of the clock recovery PLL during production testing. Held low for normal operation.
RSTB	TTL	I	17	21	Reset input for the device, active low. After reset, frame boundary detection is disabled.
LLDP LLDN	Diff. ECL	O	72 74	41 39	High-speed source-terminated diff. ECL line loopback data. A regenerated version of either the incoming data stream (RSD) input in normal mode, or the diagnostic loopback data (DLD) input in diagnostic loopback mode (DLEB set high). LLD is updated on the rising edge of LLCLK.
LLCLKP LLCLKN	Diff. ECL	O	69 70	44 43	High-speed source-terminated diff. ECL line loopback clock, phase-aligned with the LLD output signals. LLCLK can be a buffered version of the internally recovered bit clock, or the reference clock (REFCLK) input when clock recovery is bypassed (TESTEN set high).
POUT7 POUT6 POUT5 POUT4 POUT3 POUT2 POUT1 POUT0	TTL/ CMOS	O	37 36 33 32 31 30 29 28	2 3 5 8 9 10 12 14	Parallel data output, a 77.76 Mbyte/s, 19.44 Mbyte/s, or 17.408 Mbyte/s word, aligned to the POCLK parallel output clock. POUT7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). POUT0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). POUT(7-0) is updated on the falling edge of POCLK.
LCV	TTL/ CMOS	O	44	65	Line code violation output signal, set high to indicate that one or more bits of the byte currently presented on POUT(7– 0) contains a CMI line code violation. LCV is only active in STS-3 CMI and E4 CMI modes. LCV is updated on the falling edge of POCLK.

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S3006 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin # (80 PQFP)	Pin # (68 LDCC)	Description
FP	TTL/ CMOS	O	24	16	Frame pulse, indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48-bit sequence matching the framing pattern is detected on the RSD inputs.
POCLK	TTL/ CMOS	O	48	60	Parallel output clock, a 77.76 MHz, 19.44 MHz, or 17.408 MHz nominally 50% duty cycle, byte rate output clock, that is aligned to POUT(7-0) byte serial output data. POUT(7-0), FP and LCV are updated on the falling edge of POCLK.
BYTCLKIP	TTL/ CMOS	O	45	63	Reference feedback clock, compared with the reference clock (REFCLK) to maintain stability of the clock recovery PLL when it is in loss of signal state. BYTCLKIP is at the same frequency as REFCLK and is an asynchronous output.
LOCKDET	TTL	O	52	56	Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET will go low if the incoming encoded data stream has been low continuously for 4000 to 8000 bit times. LOCKDET will go high if LOS is low and good data with acceptable run length and transition density returns on the incoming data stream. LOCKDET is an asynchronous output.
CAP1 CAP2	–	I	1, 2 79, 80	– –	The loop filter capacitor is connected to these pins. The capacitor value should be 0.01µf ±10% tolerance, X7R dielectric. 50 V is recommended (16 V is acceptable).
AGND	GND	–	5, 56, 65, 71, 76	32, 37, 42, 48, 54	Analog Ground (0V)
AVEE	–4.5V	–	4, 57, 63, 67, 73	33, 40, 46, 50, 53	Power Supply (–4.5V)
ECLGND	Gnd	–	7, 15, 19, 22, 26, 35, 39, 42, 46, 54	4, 13, 18, 25, 34, 52, 61, 68	ECL Ground (0V)
VEE	–4.5V	–	8, 14, 27, 34, 47, 53	6, 7, 11, 24, 30, 62	Power Supply (–4.5V)

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S3006 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin # (80 PQFP)	Pin # (68 LDCC)	Description
TTLGND	GND	–	20, 25, 41	22, 64, 67	TTL Ground (0V)
VCC	+5V	–	21, 38, 40	1, 17, 19	Power Supply (+5V)
NC	–	–	3, 13, 23, 43, 55, 58, 59, 60, 61, 78	35, 55	No connection

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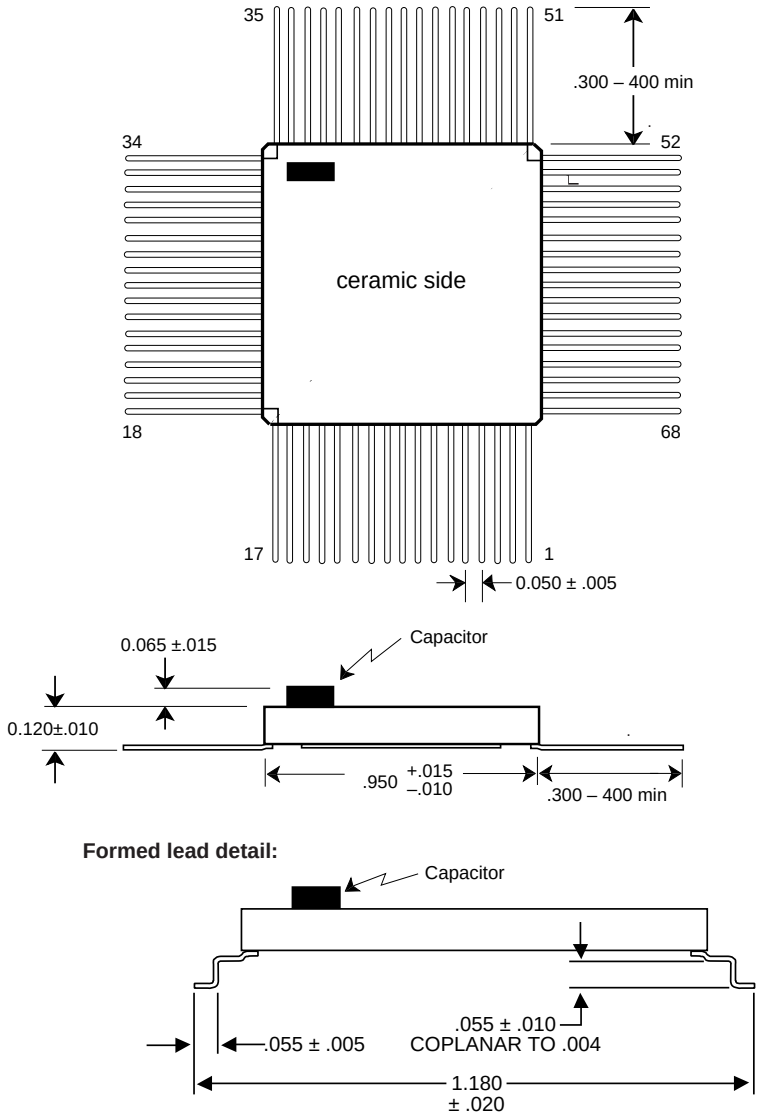
Figure 9. 68 LDCC Package



All dimensions nominal in inches.

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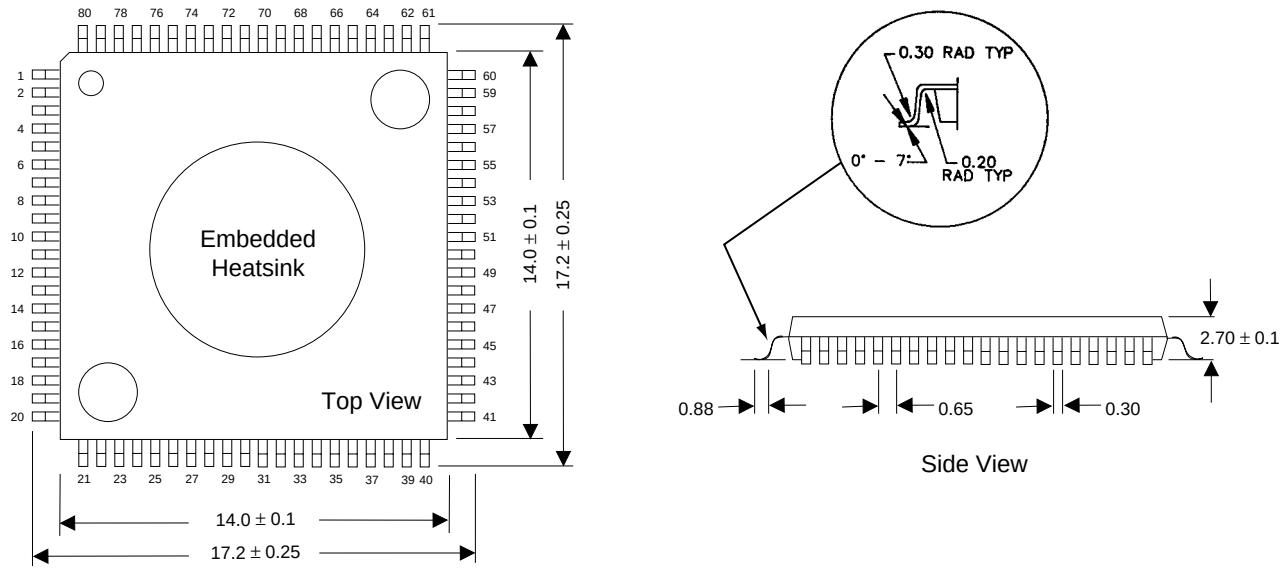
80 PQFP Package



All dimensions nominal in mm.

S3005 and S3006 80 PQFP Pinouts

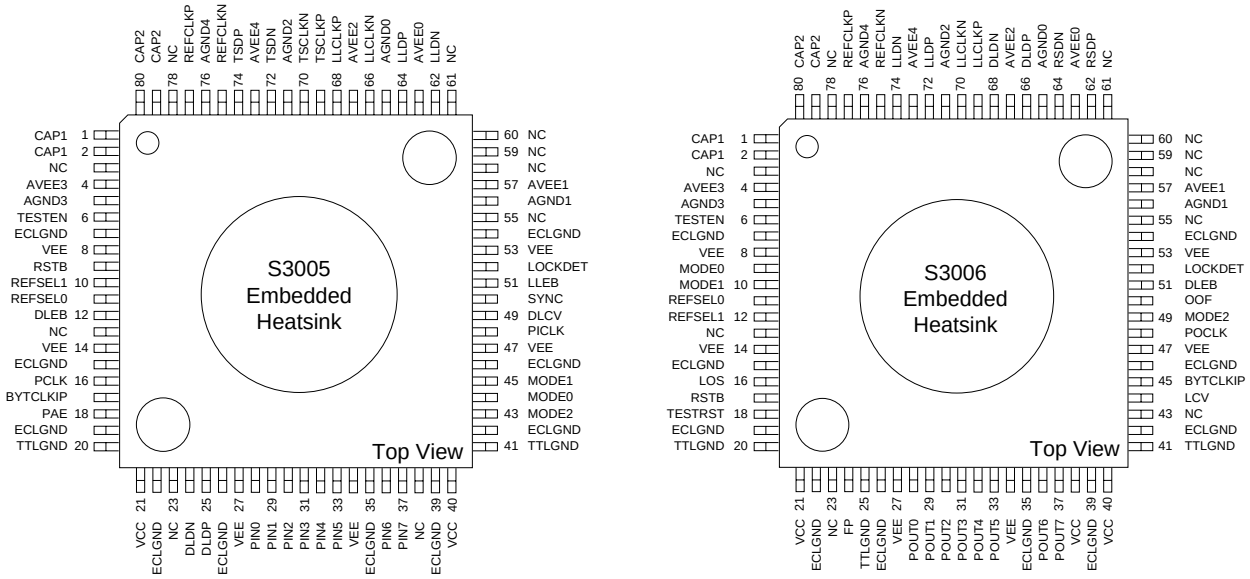


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Table 7. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	Given REFCLK = SERCLK ÷ 8, 12, 16 or 32 per REFSEL<1:0> settings
ECL Data Output Jitter (S3005 TSDP/N, DLDP/N) OC–3/STS–3 OC–STS–3 CMI OC–12/STS-12 [1]			 64 32 16	 ps (rms) ps (rms) ps (rms)	Given the jitter on REFCLK (12KHz to 1 MHz band) is less than: • 56 ps rms (OC–3) • 28 ps rms (OC–STS–3 CMI) • 14 ps rms (OC–12), REFCLK = 77.76 MHz
Reference Clock Frequency Tolerance Clock Synthesis S3005 REFCKINP/N S3006 REFCKINP/N	 -20 -100		 20 100	 ppm ppm	Required to meet SONET output frequency specification
OC–3/STS–3 & OC–12/STS–12 Capture Range Lock Range		 ±200 +8, -12		 ppm %	 With respect to fixed reference frequency Minimum transition density of 20%
Acquisition Lock Time [2] OC-3/STS-3 OC-STS-3 CMI OC-12/STS-12			 64 32 16	µsec	With device already powered up and valid REFCLK
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
ECL Output Rise & Fall Times (S3005 DLDP/N)			600	ps	20% to 80%, 50Ω to -2V equivalent load, as per Figure 19
Source Terminated Differential ECL Compatible Outputs Rise and Fall Times			450	ps	20% to 80%, 100Ω line to line, as per Figure 19

1. For REFCLK =19.44, 38.88 or 51.84 MHz, multiply the specified value by three.
2. Specifications based on design values. Not tested.

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Absolute Maximum Ratings

PARAMETER	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on VEE with Respect to GND	+0.5		-8.0	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any ECL Input Pin	-3		0	V
TTL/CMOS Output Sink Current			20	mA
TTL/CMOS Output Source Current			25	mA
High Speed ECL Output Source or Sink Current			50	mA
Static Discharge Voltage		500		V

Recommended Operating Conditions

PARAMETER		Min	Typ	Max	Unit
Ambient Temperature under Bias		-40		85	°C
Junction Temperature under Bias		-10		130	°C
Voltage on VCC with Respect to GND		4.75	5.0	5.25	V
Voltage on VEE with Respect to GND[1]		-4.2	-4.5/-5.2	-5.46	V
Voltage on Any TTL Input Pin		0		VCC	V
Voltage on Any ECL Input Pin		-2.0		0	V
TTL/CMOS Output Sink Current				8	mA
TTL/CMOS Output Source Current				20	mA
ECL Output Source Current				25	mA
Source Terminated Diff. ECL Compatible Output Source or Sink Current				10	mA
S3005	ICC IEE		41 314	52 402	mA mA
S3006	ICC IEE		54 324	69 414	mA mA

1. V_{EE} (min) = -4.2V for Ambient Temperature ≥ 0˚C, -4.5V for Ambient Temperature <0˚C.

Thermal Management

Device	Package	Θjc	Θja Still AIr	Power	Max Still Air	Air/70˚C	Air/85˚C	Air/70˚C for 100˚C Tj
S3005	68 LDCC	2.5˚C/W	33.9˚C/W	2.4W	49˚C	200 LFPM	500 LFPM	750 LFPM
	w/45-20 HS		26.4˚C/W	2.4W	66˚C	<50 LFPM	140 LFPM	210 LFPM
S3005	80 TEP	2.0˚C/W	30˚C/W	2.4W	58˚C	200 LFPM	700 LFPM	1050 LFPM
	w/45-28 HS		23˚C/W	2.4W	75˚C	N/A	200 LFPM	300 LFPM
S3006	68 LDCC	2.5˚C/W	33.9˚C/W	2.6W	42˚C	310 LFPM	600 LFPM	900 LFPM
	w/45-20 HS		26.4˚C/W	2.6W	61˚C	100 LFPM	150 LFPM	230 LFPM
S3006	80 TEP	2.0˚C/W	30˚C/W	2.6W	52˚C	300 LFPM	750 LFPM	1130 LFPM
	w/45-28 HS		23˚C/W	2.6W	70˚C	N/A	250 LFPM	380 LFPM

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TTL Input/Output DC Characteristics[1] (T_A = -40°C to +85°C, V_{CC} = 5 V ±5%, V_{EE} = -4.5 V ±7% or -5.2 ± 5%)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}[2]	Input LOW Voltage	Guaranteed Input LOW Voltage		0.8	Volts
V_{IH}[2]	Input HIGH Voltage	Guaranteed Input HIGH Voltage	2.0		Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	-400.0		uA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		50.0	uA
I_I	Input HIGH Current at Max VCC	V_{CC} = MAX, V_{IN} = 5.25V		1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V	-100.0	-25.0	mA
I_{OZL}	Output Three-State Current LOW	V_{CC} = MAX, V_{OL} = 0.4V	-50.0	50.0	uA
I_{OZH}	Output Three-State Current HIGH	V_{CC} = MAX, V_{OH} = 2.4V	-50.0	50.0	uA
V_{IK}	Input Clamp Diode Voltage	V_{CC} = MIN, I_{IN} = -18mA	-1.2		Volts
V_{OL}	TTL Output LOW Voltage	V_{CC} = MIN, I_{OL} = 8mA		0.5	Volts
V_{OH}	TTL Output HIGH Voltage	V_{CC} = MIN, I_{OH} = -1.0mA	2.4		Volts
V_{OL}	CMOS Compatible Output LOW Voltage	V_{CC} = MIN, I_{OH} = 100uA		0.4	Volts
V_{OH}	CMOS Compatible Output HIGH Voltage	V_{CC} = MIN, I_{OH} = -100uA	3.4		Volts

1. These conditions will be met with an airflow of 400 LFPM.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

ECL Input/Output DC Characteristics[7] (T_A = -40°C to +85°C, V_{CC} = 5 V ±5%, V_{EE} = -4.5 V ±7% or -5.2 ± 5%)

Symbol	Parameter	Conditions	Signal Name	Min	Max	Unit
V_{IL}[1]	Input LOW Voltage	Guaranteed Input LOW Voltage for all single ended inputs		-2.00	-1.47	Volts
V_{IH}[1]	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all single ended inputs		-1.18	-0.80	Volts
V_{IL}[2]	Input LOW Voltage	Guaranteed Input LOW Voltage for all differential inputs		-2.00	-0.70	Volts
V_{IH}[2]	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all differential inputs		-1.75	-0.45	Volts
V_{ID}[2]	Input DIFF Voltage	Guaranteed Input DIFF Voltage for all differential inputs		0.25	1.40	Volts
I_{IL}	Input LOW Current	V_{EE} = MAX, V_{IL} = -1.95V	LOS[6]	-0.50	20.00	uA
		V_{EE} = MAX, V_{DIFF} = 0.5V	LLDP[5],LLCLKP[5], RSDP[6], DLDP[6]	-7.00	-3.50	mA
		V_{EE} = MAX, V_{DIFF} = 0.5V	LLDN[5], LLCLKN[5], RSDN[6], DLDN[6]	-8.30	-2.80	mA
		V_{EE} = MAX, V_{DIFF} = 0.5V	REFCLKP[5,6], REFCLKN[5,6]	-1.00	20.00	uA
I_{IH}	Input HIGH Current	V_{EE} = MAX, V_{IH} = -0.80V	LOS[6]	-0.50	20.00	uA
		V_{EE} = MAX, V_{DIFF} = 0.5V	LLDP[5], LLCLKP[5], RSDP[6], DLDP[6]	3.50	7.00	mA
		V_{EE} = MAX, V_{DIFF} = 0.5V	LLDN[5], LLCLKN[5], RSDN[6], DLDN[6]	2.80	8.30	mA
		V_{EE} = MAX, V_{DIFF} = 0.5V	REFCLKP[5,6], REFCLKN[5,6]	-1.00	20.00	uA
V_{OL}[3]	Output LOW Voltage	50Ω to -2V termination		-2.00	-1.50	Volts
V_{OH}[3]	Output HIGH Voltage	50Ω to -2V termination		-1.11	-0.62	Volts
V_{OL}[4]	Output LOW Voltage	100Ω between differential outputs		-2.50	-0.80	Volts
V_{OH}[4]	Output HIGH Voltage	100Ω between differential outputs		-2.20	-0.50	Volts
V_{OD}[4]	Output DIFF Voltage	100Ω between differential outputs		0.30	1.00	Volts

1. Single Ended ECL Inputs
2. Differential ECL Inputs
3. Standard ECL Outputs
4. Source Terminated Differential ECL Compatible Outputs
5. S3005 Signals
6. S3006 Signals
7. These conditions will be met with an airflow of 400 LFPM.

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Table 8. S3005 AC Timing Characteristics

(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%, V_{EE} = -4.5 V ±7% or -5.2V ± 5%)

Symbol	Description	Min	Max	Units
	TSCLK Frequency (nom. 155, 311, or 622 MHz)		640	MHz
	TSCLK Duty Cycle	40	60	%
	PICLK Duty Cycle	33	67	%
tS_{PIN}	PIN [7.0] Set-up Time w.r.t. PICLK	2.0		ns
tH_{PIN}	PIN [7.0] Hold Time w.r.t. PICLK	1.0		ns
tS_{LLD}	LLD Set-Up Time w.r.t. LLCLK	100		ps
tH_{LLD}	LLD Hold Time w.r.t. LLCLK	100		ps
	LLCLK Duty Cycle	40	60	%
tP_{TSD}	TSCLK Low to TSD Valid Propagation Delay		440	ps
tS_{TSD}	TSD Set-Up Time w.r.t. TSCLK	400		ps
tH_{TSD}	TSD Hold Time w.r.t. TSCLK	400		ps
tP_{PAE1}	PCLK Low to PAE Valid Propagation Delay		3.0	ns
TSD^1_{ESK}	TSD ± Edge Skew		100	ps
$TSCLK^1_{ESK}$	TSCLK ± Edge Skew		100	ps

1 Guaranteed but not tested.

Figure 10. PIN AC Input Timing

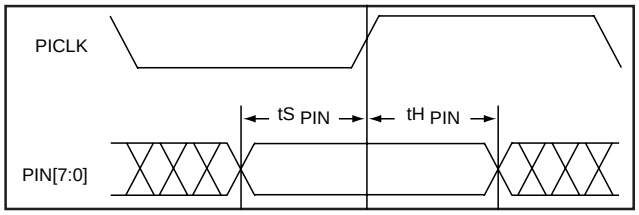
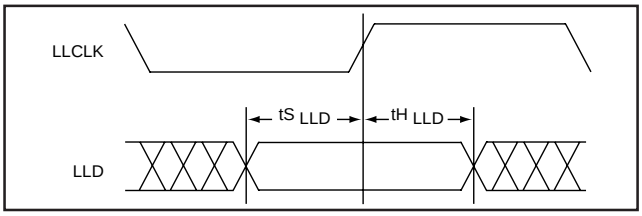
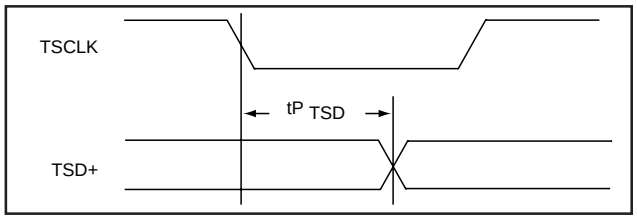


Figure 11. LLD AC Input Timing



1. When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in picoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in picoseconds from the 50% point of the clock to the 50% point of the input.
3. When a set-up time is specified on differential ECL signals between an input and a clock, the set-up time is the time in picoseconds from the cross-over point of the input to the cross-over point of the clock.
4. When a hold time is specified on differential ECL signals between an input and a clock, the hold time is the time in picoseconds from the cross-over point of the clock to the cross-over point of the input.

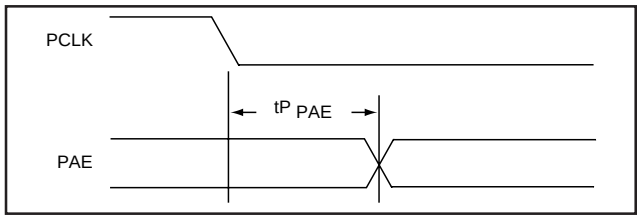
Figure 12. Output Timing



Notes on High-Speed PECL Output Timing

1. Output propagation delay time is the time in nanoseconds from the cross-over point of the reference signal to the cross-over point of the output.

Figure 13. PAE Output Timing



Notes on TTL Output Timing

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 15pF load on the outputs.

Table 9. S3005 External Clock Mode Timing

Description	Min	Max	Units
REFCLK in Bypass Mode (nom. 155, 311, or 622 MHz)		640	MHz
REFCLK in Bypass Mode duty cycle	33	67	%

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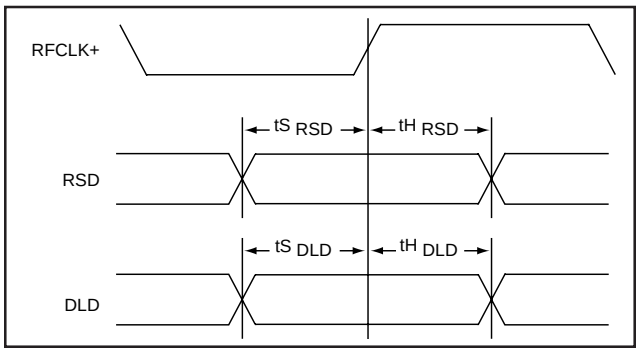
Table 10. S3006 AC Timing Characteristics

Symbol	Description	Min	Max	Units
	POCLK Duty Cycle [1]	40	60	%
tP_{POUT}	POCLK Low to POUT [7:0] Valid Prop. Delay @ STS-3 POCLK Low to POUT [7:0] Valid Prop. Delay @ STS-12	0 0	5 1.5	ns ns
tP_{FP}	POCLK Low to FP Valid Propagation Delay @ STS-3 POCLK Low to FP Valid Propagation Delay @ STS-12	0 0	5 1.5	ns ns
	LLCLK Frequency		640	MHz
	LLCLK Duty Cycle	40	60	%
tP_{LLD}	LLCLK Low to LLD Valid Propagation Delay @ STS-3 LLCLK Low to LLD Valid Propagation Delay @ STS-12	-800 -500	800 500	ps ps

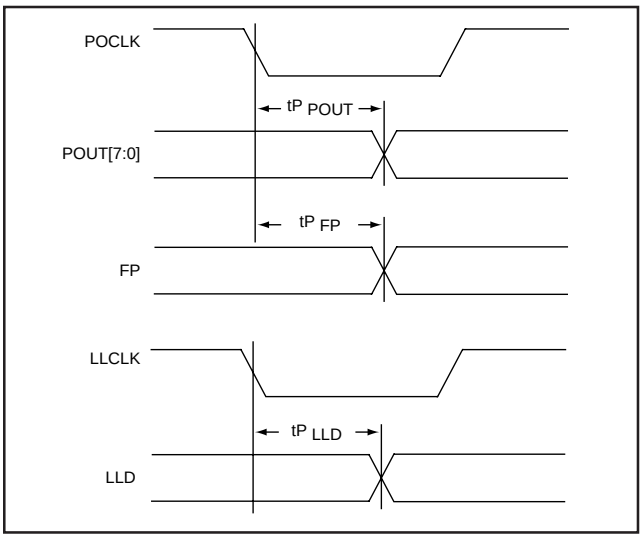
1 Driving CMOS with a 2.5V threshold and a 500Ω load, or driving TTL with a 1.4V threshold and a 150Ω load.

Figure 14. Input Timing - External Clock Mode



Notes on Input Timing:
1. When a set-up time is specified between a data input and a clock input, the set-up time is the time in picoseconds from the crossover point of the differential data input to the crossover point of the differential clock input.
2. When a hold time is specified between a data input and a clock input, the hold time is the time in picoseconds from the crossover point of the differential clock input to the crossover point of the differential data input.

Figure 15. Output Timing Diagram



Notes on Output Timing:
1. Output timing specification are valid when terminating all outputs with 500Ω to GND.
2. Output propagation delay time of TTL outputs is the time in picoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
3. Maximum output propagation delays of TTL outputs are measured with a 15 pF load on the outputs.
4. Output propagation delay time of high speed ECL outputs is the time in picoseconds from the cross-over point of the reference signal to the cross-over point of the output.
5. Maximum output propagation delays of TTL outputs are measured with a 50Ω transmission line on the outputs.

Table 11. S3006 External Clock Mode Timing

Symbol	Description	Min	Max	Units
	REFCLK Freq. (Nominally 622/311//155 MHz)		640	MHz
	REFCLK Duty Cycle	33	67	%
tS_{RSD}	RSD to REFCLK Set-up Time	300		ps
tH_{RSD}	REFCLK to RSD Hold Time @ STS-3 REFCLK to RSD Hold Time @ STS-12	1.0 100		ns ps
tS_{DLD}	DLD to REFCLK Set-up Time	300		ps
tH_{DLD}	REFCLK to DLD Hold Time @ STS-3 REFCLK to DLD Hold Time @ STS-12	1.0 100		ns ps

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RECEIVER FRAMING

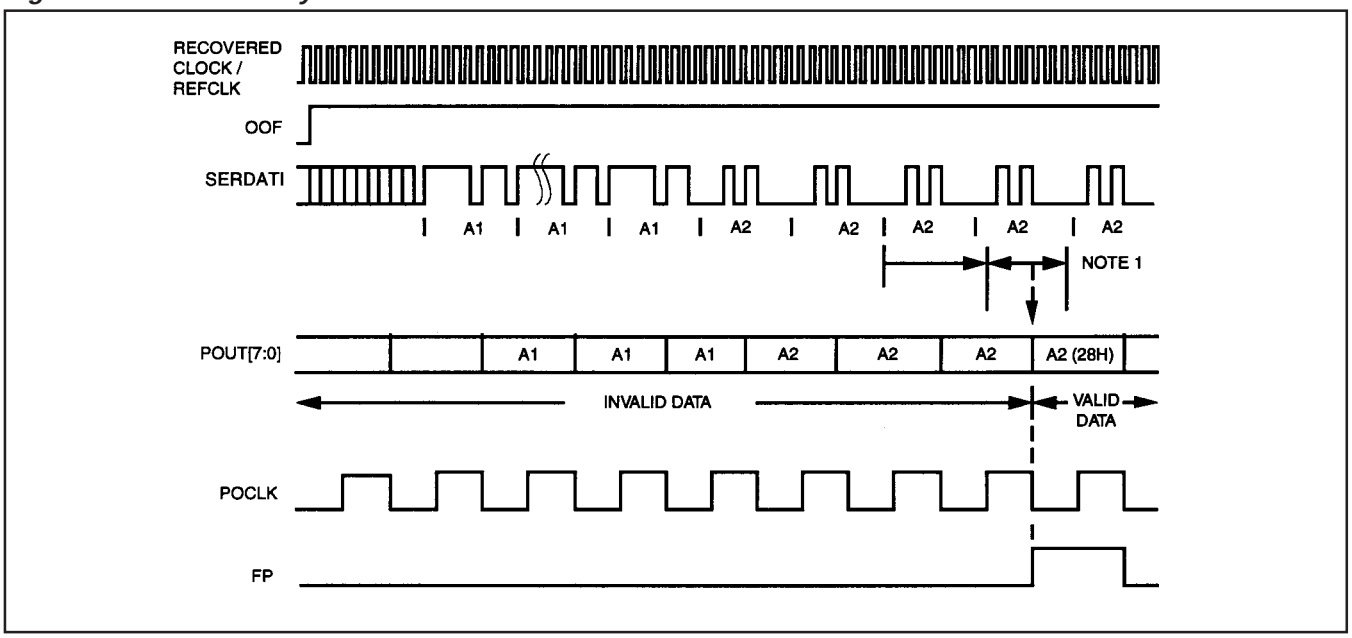
Figure 16 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 17. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 17 shows a typical OOF timing pattern which occurs when the S3006 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 18 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 16. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 17. OOF Operation Timing with SSTX

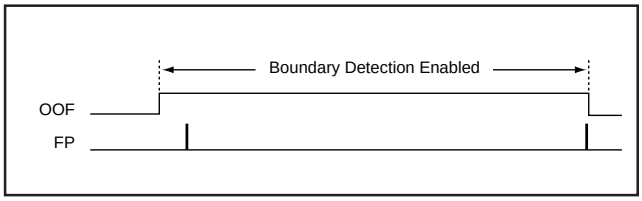


Figure 18. Alternate OOF Timing

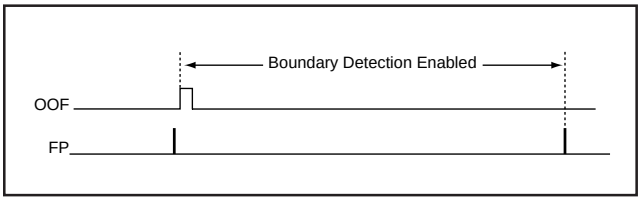


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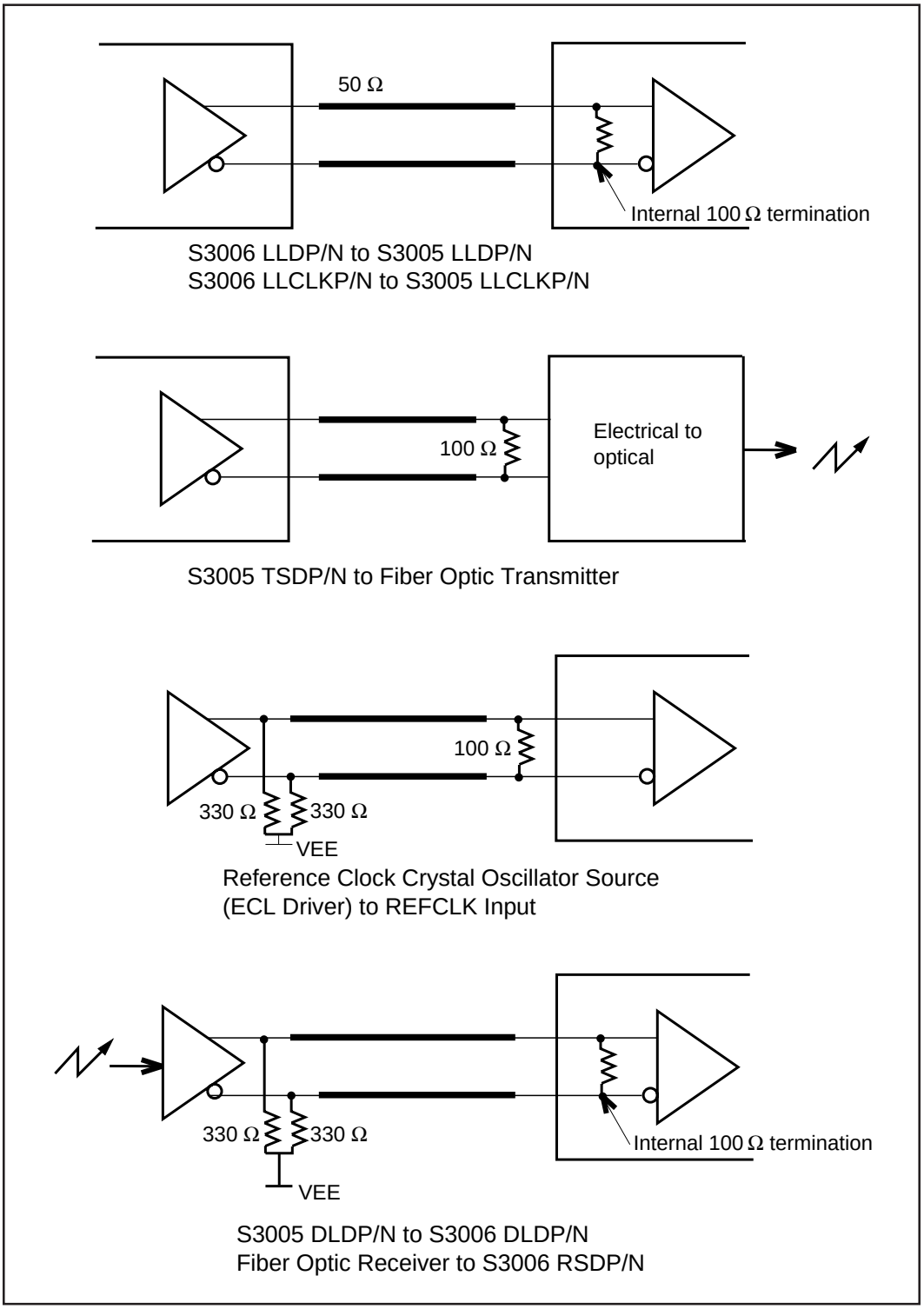
Figure 19. Differential ECL Input and Output Applications



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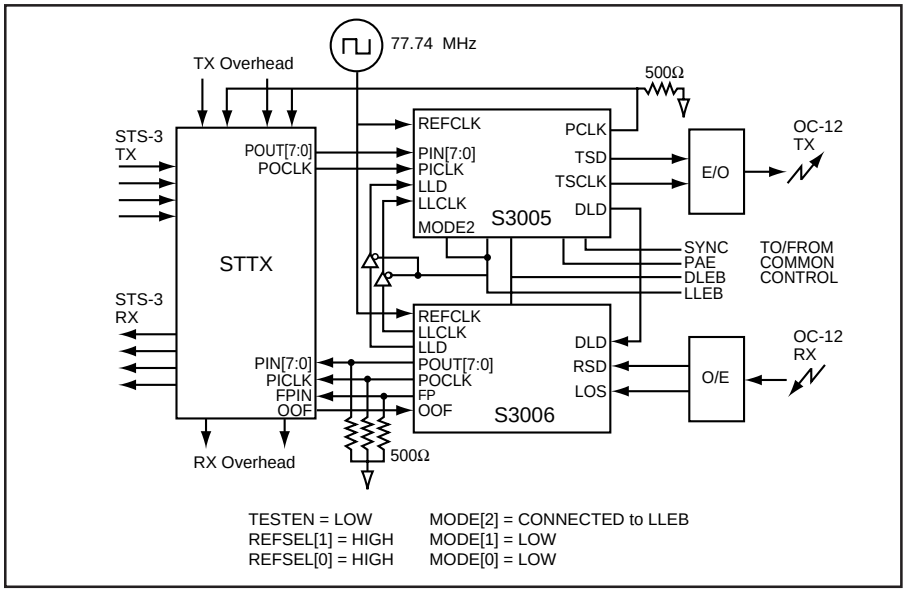
STS-12/STS-3 OPTICAL INTERFACE

The S3005 and S3006 devices are designed to interface seamlessly to make a SONET transceiver for STS-12, CMI-encoded STS-3, and STS-3. Figure 20 shows these two devices connected together with receive and transmit overhead processors on the equipment side and electrical-to-optical converters on the line side to realize the core of a typical SONET transceiver.

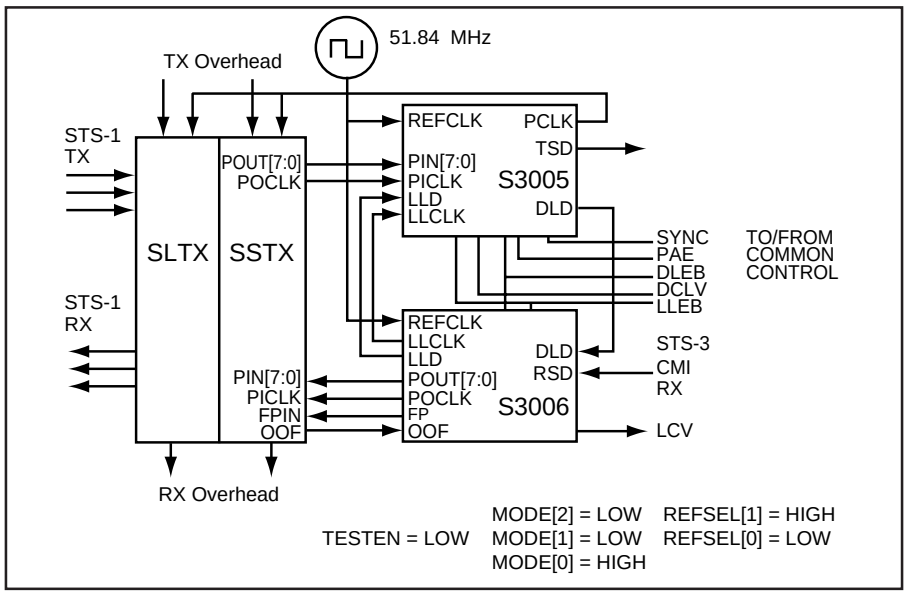
Figure 20. OC-12 Application



STS-3 CMI ELECTRICAL INTERFACE

With the S3006 devices optioned for CMI-coded STS-3, an electrical SONET transceiver can be implemented as shown in Figure 21 In this case, a clock reference of 51.84 MHz was selected. TSD would be coupled through a line driver and transformer to a coaxial cable for short span applications.

Figure 21. CMI Electrical Interface



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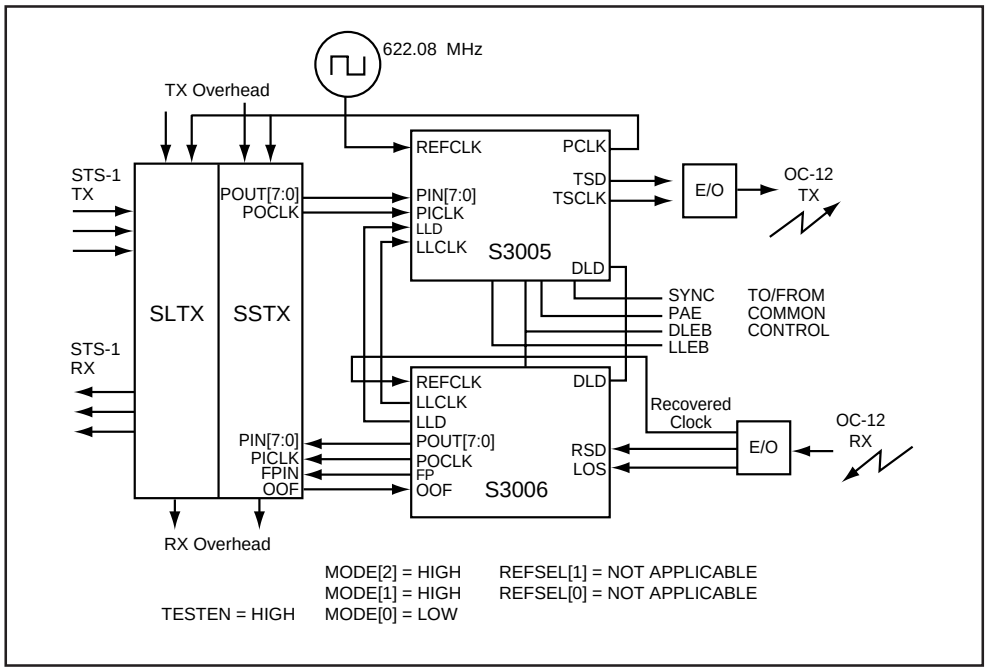
EXTERNAL CLOCK APPLICATION

The S3006 can receive data at SONET or other standard data rates by bypassing the internal clock recovery PLL and supplying the appropriate clock to the REFCLK input. Figure 22 shows an application for STS-12 with external clock recovery on the receive side, and an external transmit clock connected to REFCLK of the S3005 device.

Figure 22. OC-12 External Clock Application



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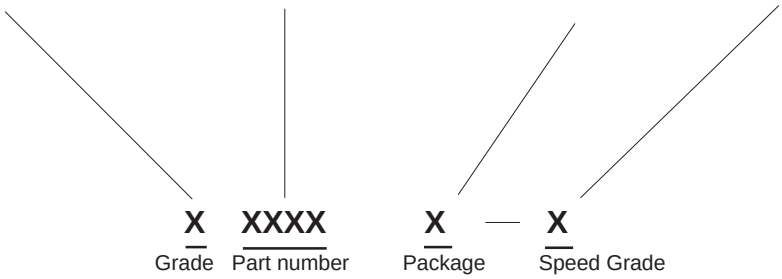
Ordering Information

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S – commercial	3005	A – 68 LDCC with straight leads B – Bare Die C – 68 LDCC lead formed D – 80 PQFP	1 – 139 Mbit/s 1 – 139 Mbit/s CMI 1 – 155 Mbit/s 1 – 155 Mbit/s CMI 6 – 622 Mbit/s

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S – commercial	3006	A – 68 LDCC with straight leads B – Bare Die C – 68 LDCC lead formed D – 80 PQFP	1 – 139 Mbit/s 1 – 139 Mbit/s CMI 1 – 155 Mbit/s 1 – 155 Mbit/s CMI 6 – 622 Mbit/s



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