RTL8801 PHY/IEEE 1394a

3 port 100/200/400 Mb/s Cable Transceiver/Arbiter Chip

1. Features

- Fully support provisions of IEEE1394-1995 for High- Performance Serial Bus and the P1394a draft 2.0 standard
- Provides three fully compliant cables ports at 100/200/400 Mbits/s and available with three ports
- Fully compliant with Open HCI requirements
- Full P1394a additional function support
- Support optional 1394 Annex J electrical isolation barrier at PHY-link interface
- Support power-down feature to conserve energy in battery–powered applications
- Cable power presence monitoring
- Separate cable bias (TPBIAS) and driver termination voltage supply for each port
- Encode and decode functions included for data-strobe bit level encoding
- Support LPS/link-on pin for PHY-link interface
- Incoming data resynchronized to local clock
- Single 24.576 MHZ crystal provide transmit/receive data at 100/200/400 Mbits/s and LLC clock at 49.152 MHZ
- Node power-class information signaling for system power management
- Adaptive equalizer
- Easy configured as a repeater
- Single 3.3V power supply
- 64 pin LQFP package

2. General Description

The RTL8801 provides three-port physical layer(PHY) function in a cable-based IEEE 1394-1995 and IEEE P1394a network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

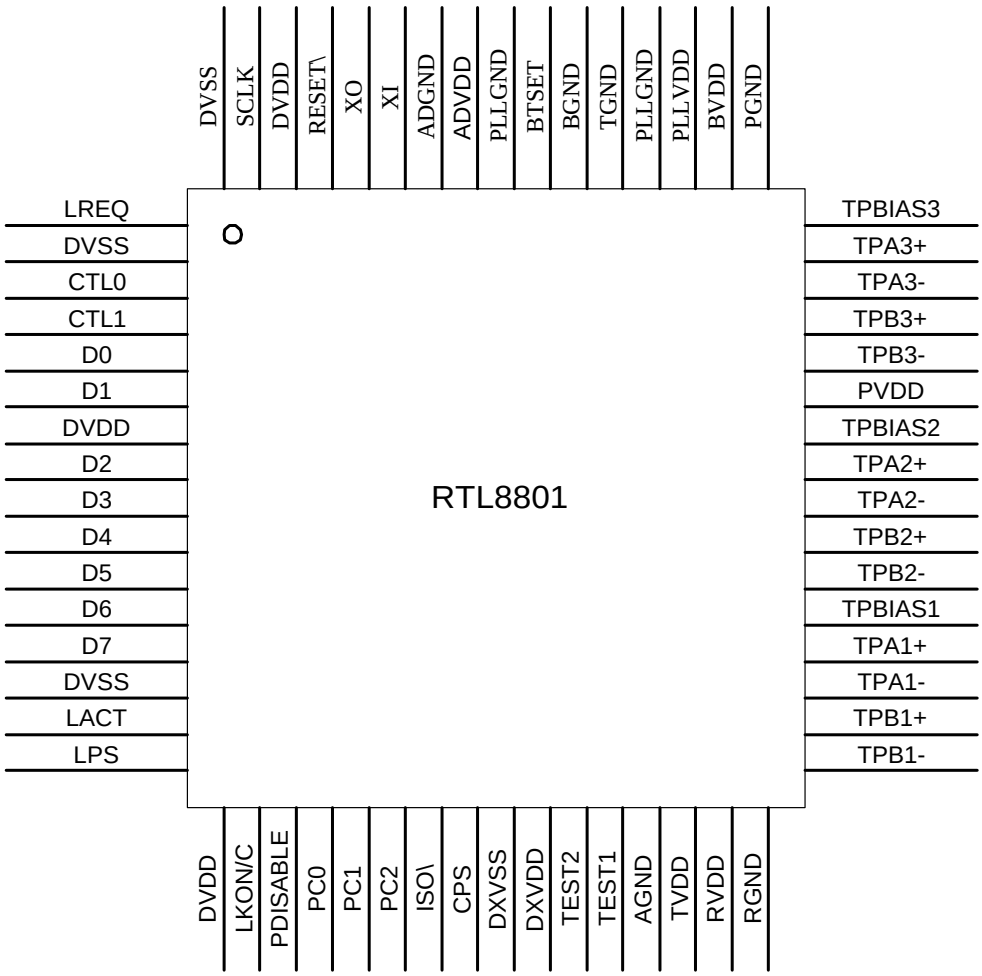
Data bits to be transmitted through the cable ports are received from the Link on 2/4/8 data lines (D0-D8), and are latched internally in the RTL8801 in synchronization with the 49.152 MHZ system clock these bits are combined serially, encoded, and transmitted at 98.304 , 196.608 or 393.216Mbps as the outbound data-strobe information stream. During transmission, the encoded

data transmitted differential on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded Strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the received clock signal and the serial data bits. The serial data bits are split into two or four parallel transmitted (repeated) out of the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The output of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable connection status. The cable connection status signal is internally debounced in the RTL8801 on a cable disconnect-to-connect. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect a debounce delay is incorporated. There is no delay on a cable disconnect.

3. Pin Assignment

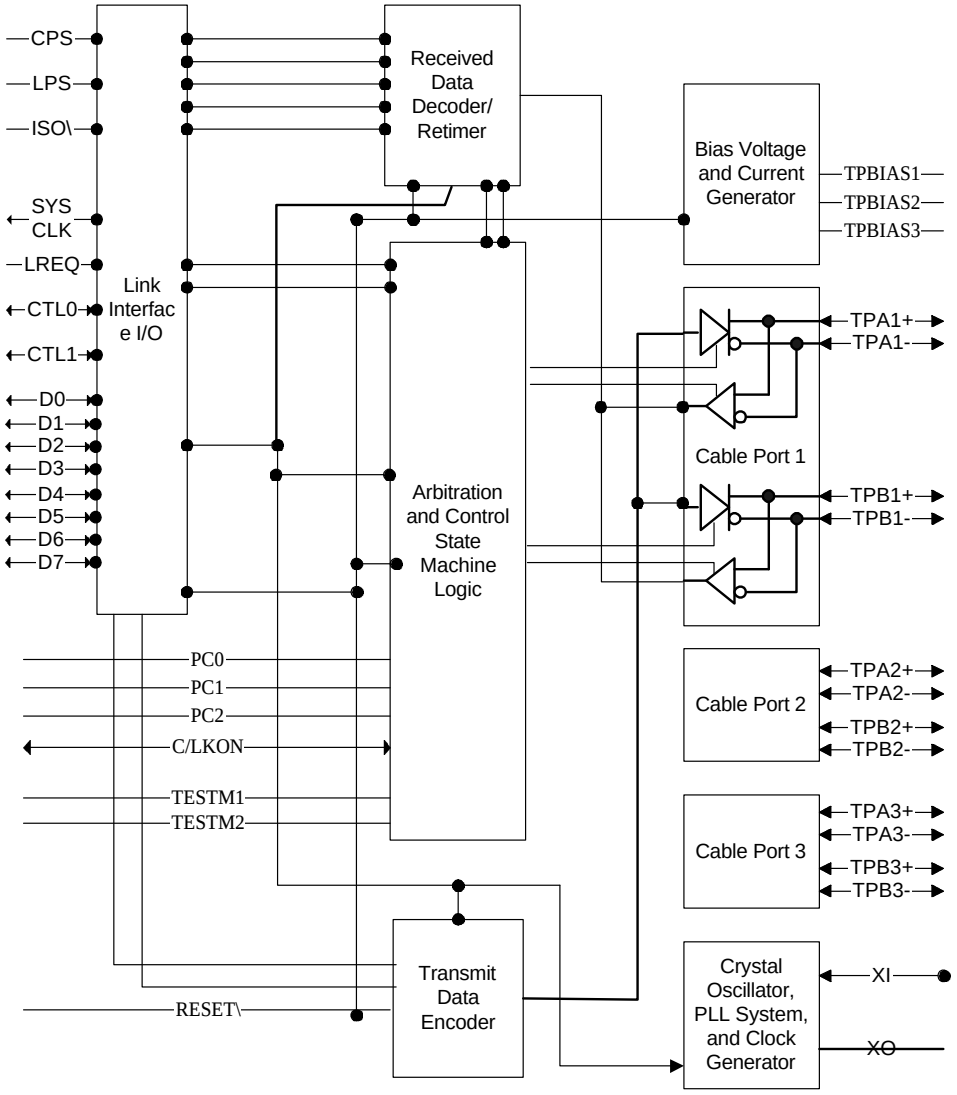


4. Pin Descriptions

Symbol	Type	Pin(s) No.	Description
C/LKON	I/O	18	(input) Bus manager capable. When set as input, C/LKON specifies in the Self-ID packet that the node is bus manager capable. (output) Link on. When set as an output, C/LKON indicates the reception of a link-on packet by asserting a 6.114 MHZ square wave signal.
CNA	O	15	CNA is asserted high when none of the PHY ports are connected to another active port. This circuit remains acitve during the power down mode.
CPS	I	24	Cable power status. CPS is normally connected to the cable power through a 400-Kohm resistor. This circuit drivers an internal comparator that detects the presence of cable power.
LPS	I	16	Link power status. LPS is connected to either the VDD supplying the LINK or to a pulsed output that is active when the LINK is powered for the purpose of monitoring the LINK power status.
LREQ	I	1	Link request. LREQ is an input from the LINK that requests the PHY to perform some service.
LACT\ISO	I	23	Link active. This pin direct the phy with link or not
CTL0 CTL1	I/O	3,4	Control I/O. the CTLn pins are bi-directional communications control signals between the PHY and LLC.
D0-D7	I/O	5,6,8,9,10,11, 12,13	Data I/O. The D terminals are bi-directional and pass data between the PHY and LLC.
SYSCLK	O	63	System clock. SYSCLK provides a 49.152 MHZ clock signal, which is synchronized with the data transfers to the LLC.
TPA1+ TPA1-	I/O	36,35	Port1, cable pair A. TPA1 is the port A connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA2+ TPA2-	I/O	41,40	Port2, cable pair A. TPA3 is the port A connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA3+ TPA3-	I/O	47,46	Port2, cable pair A. TPA3 is the port A connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB1+ TPB1-	I/O	34,33	Port1, cable pair B. TPB1 is the port B connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB2+ TPB2-	I/O	39,38	Port2, cable pair B. TPB2 is the port B connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB3+ TPB3-	I/O	45,44	Port3, cable pair B. TPB3 is the port B connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPBIAS1 TPBIAS2 TPBIAS3	O	37,42,48	Portn, twisted pair bias. It provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes.
PC0-PC2	I	20,21,22	Power class indicator. The PC signals set the bit values of the three power class bits in Self-ID packet . These bits can be programed by

			tying the terminals to VDD or GND.
XI XO		59,60	Crystal oscillator input and output.
PLLGND	-	52,56	PLL circuit ground. The pin should be tied together to the low impedance ground plane
PLLVDD	-	51	PLL circuit power. PLLVDD supplies power to the PLL circuit
AVDD	-	30,31,43,50	Analog power. AVDD supplies power to the analog port of the device.
AVSS	-	32,49,53,54	Analog ground. These pins should be tied together to the low impedance ground plane.
BTSET	I	55	Current setting resistor input. This pin is connected to an external resistor to set the internal operating current and cable driver output current.
PDISABLE	I	19	Port configuration monitor input. This pin is only active in power on stage and meets the requirement of OHCI.
DVDD	-	7,17,26,57,62	Digital power. DVDD supplies power to the digital part of the device.
DVSS	-	2,14,25,29,58,64	Digital ground. These pins should be tied together to the low impedance ground plane.
RESET\	I	61	Reset. An external capacitor is required for proper power-up operation.
TEST1	I	28	Test control pin. This pin is used in the manufacturing test of the device. For normal use it should be tied to DVSS.
TEST2	I	27	Test control pin. This pin is used in the manufacturing test of the device. For normal use it should be tied to DVDD.

5. Functional Block Diagram



6. Functional Description

The operation of the cable PHY can best be understood with reference to the 5.0 block diagram show before.

The main controller of the cable PHY is the block labeled “arbitration and control state machine logic” which responds to arbitration requests from the link layer and changes in the state of attached ports. It provides the management and timing signals for transmitting, receiving, and repeating packets. It also provides the bus reset and configuration . The cable environment supports the immediate, fair, isochronous, and cycle_master arbitration classes, where the cycle_master class is only available at the root node.

Cable arbitration has two parts: a three-phase initialization process (bus reset, tree identify, and self-identify), and a normal operation phase. Each of these four phases is described using a state machine, The state machine and the list of actions and conditions are the normative part of IEEE standard.

The “receive data decoder/retimer” block decodes the data-strobe signal and retimes the received data to a local fixed-frequency clock provided by the local clock. Since the clocks of receiving and transmitting nodes can be up to 100 ppm different from the nominal, the data resynch function has to be able to compensate for a difference of 200 ppm over the maximum packet length of 84.31 us (1024 byte isochronous packet at 98.304 Mbit/s). Data reception for the cable environment physical layer has three major functions: decoding the data-strobe signal to recover a clock, synchronizing the data to a local clock for use by the link layer, repeating the synchronized data out all other connected ports.

The “transmit data encoder” block provides a common interface to the link layer for both packet daa and arbitration signal (gaps and bus reset indicators). Data transmission is a straightforward function: the data bits are sent to the attached peer PHY along with the appropriately encoded strobe signal using the timing provided by the PHY transmit clock. If connected port cannot accept data at the requested speed, then no data is send (leaving the drivers in the “01” data prefix condition).

The “link interface” block provides a scalable, cost-effective method to connect one serial bus link chip to one serial bus PHY chip. The width of the data bus scales with the highest speed both chips can support, using two pins per 100 Mbit/s. The clock rate of the signals at this interface remains constant, independent of speed, to support galvanic isolation for implementations where it is

desirable.

The PHY has control over the bidirectional pins. The link only drives these pins when control is transferred to it by the PHY. The link performs all unsolicited activity through a dedicated request pin. The possible actions that may occur on the interface are categorized as transmit, receive, status, and request.

7. Register Definitions

Definitions and usage for each of the registers listed below are provided on this and the following pages:

7.1 PHY register map for the cable environment

address	0	1	2	3	4	5	6	7
0000b	Physical_ID						R	PS
0001b	RHB	IBR	Gap_count					
0010b	Extended(7)			reserved	Total_ports			
0011b	Max_speed			reserved	Delay			
0100b	Link_active	Contender	Jitter			Pwr_class		
0101b	Resume_int	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
0110b	Reserved							
0111b	Page_select			reserve	Port_select			
1000b	Register0(page_select)							
1111b	Register7(page_select)							

7.2 PHY register fields for the cable environment

	size	type	Power reset value	description
Physical_ID	6	r	-	The address of this node determined during self-identification. A value of 63 indicates a malconfigured bus; the link shall not transmit any packets.
R	1	r	-	When set to one, indicate that this node is the root.
PS	1	r	-	Cable Power status.
RHB	1	rw	0	Root hold-off bit. When set to one, instructs the PHY to attempt to become the root during the next tree identify process.
IBR	1	rw	0	Initiate bus reset. When set to one, instructs the PHY to initiate a bus reset immediately (without arbitration). This bit causes assertion of the reset state for 166 us and is self-clearing.
Gap_count	6	rw	3F	Used to configure the arbitration timer setting in order to optimize gap times according to the topology of the bus. IEEE 1394-1995 4.3.6
Extended	3	r	7	constant value of seven
Total_ports	5	r	3	the number of ports implemented by this PHY
Max_speed	3	r	010	Indicates the maximum speed this PHY supports; 000 - 98.304 Mbit/s 001 - 98.304 and 196.608 Mbit/s 010 – 98.304, 196.608 and 393.216 Mbit/s 011 - .98.304, 196.608, 393.216 and 786.43 Mbit/s 100 – 98.304, 196.608, 393.216, 786.43 and 1,572.864 Mbit/s 101 – 98.304, 196.608, 393.216, 786.43, 1,572,864 and 3,145.728 Mbit/s all other values are reserved for future definition
Delay	4	R	0	Worse case repeater delay, expressed as 144+(delay*20)ns.
Link_active	1	rw	1	Link enabled. Default value of one subsequent to a power reset. Otherwise cleared or set by software to control the value of the L bit transmitted in the self-ID packet. The transmitted L bit shall be the logical AND of this bit and the LPS signal.
Contender	1	rw	Pin C/LK ON	Contender. Cleared or set by software to control the value of the C bit transmitted in the self-ID packet.

Pwr_class	3	rw	Pin PC0-PC2	Power class. Controls the value of the pwr field transmitted in the self-ID packet. 000 - Node does not need power and does not repeat power 001 - Node is self-powered and provides a minimum of 15 W to the bus 010 - Node is self-powered and provides a minimum of 30 W to the bus. 011 - Node is self-powered and provides a minimum of 45 W to the bus 100 - Node may be powered from the bus and is using up to 1 W. 101 - Node is powered from the bus and is using up to 1 W. An additional 2 W is needed to enable the link and higher layers. 110 - Node is powered form the bus and is using up to 1 W. An additional 5 W is needed to enable the link and higher layers. 111 - Node is powered from the bus and is using up to 1 W. An additional 9 W is needed to enable the link and higher layers.
Jitter	3	R	0	The difference between the fastest and slowest repeater data delay, expressed as (jitter+1)*20ns
Resume_int	1	Rw	0	Resume interrupt enable. When set to one, the PHY shall set port_event to one if resume operations commence for any port.
ISBR	1	rw	0	Initiate short (arbitrated) bus reset. A write of one to this bit instructs the PHY to arbitrate and issue a short bus reset. This bit is self-clearing.
Loop	1	rw	0	Loop detect. A write of one to this bit clears it to zero.
Pwr_fail	1	rw	0	Cable power failure detect. Set to one when the PS bit changes from one to zero. A write of one to this bit clears it to zero.
Timeout	1	rw	0	Arbitration state machine timeout. A write of one to this bit clears it to zero.
Port_event	1	rw	0	Port event detect. The PHY sets this bit to one if any of connected, Bias, Disabled or Fault change for a port whose Int_enable bit is one. The PHY also sets this bit to one if resume

				operations commence for any port and Resume_int is one. A write of one to this bit clears it to zero.
Enab_accel	1	rw	0	Enable arbitration acceleration. When set to one, the PHY shall use the enhancements specification in P1394A.
Enab_multi	1	rw	0	Enable multi-speed packet concatenation. When set to one, the Link shall signal the speed of all packets to the PHY.
Page_select	3	rw	000	Selects which of eight possible PHY register pages are accessible through the window at PHY register address 1000b through 1111b, inclusive.
Port_select	4	rw	0000	If the page selected by Page_select presents per port information, this field selects which port's registers are accessible through the window at PHY register addressed 1000b through 1111b, inclusive.

7.3.PHY register page0: Port Status page

The port Status page is used to access configuration and status information for each of the PHY's port. The port is selected by writing zero to Page_select and the desired port number to Port_select in the PHY register at address 0111.

	0	1	2	3	4	5	6	7
1000b	AStat		BStat		Child	connected	Bias	Disabled
1001b	Negotiated_speed			Int_enable	Fault			
1010b								
1011b								
1100b								
1101b								
1110b								
1111b								

7.4 PHY register port status page fields

	Size	Type	Power reset value	Description
Astat	2	r	-	TPA line State for the port 00 = invalid 01 =1 10 =0 11 =z
Bstat	2	r	-	(same encoding as Astat)
Child	1	r	-	If equal to one, the port is a child, else a parent. The meaning of this bit is undefined from the time a bus reset is detected until the PHY transitions to state T1:Child Handshake during the tree identify process(see 4.4.2.2 in IEEE Std 1394-1995)
Conncted	1	r	0	If equal to one, the port is connected, else disconnected. The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.
Bias	1	r	-	If equal to one, bias voltage is detected(possible connection). The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.
Disabled	1	rw	0	When set to one, the port shall be disabled. The value of this bit subsequent to a power reset is implementation-dependent, but should be a strappable option.
Negotiated_ speed	3	r	-	Indicated the maximum speed negotiated between this PHY port and its immediately connected port; the encoding is 000 – 98.304Mbit/s 001 – 98.304 and 196.608 Mbit/s 010 – 98.304, 196.608 and 393.216 Mbit/s
Int_Enable	1	rw	0	Enable port event interrupts. When set to one, the PHY shall set Port_event to one if any of Connected, Bias, Disabled or Fault (for this port) change state.
Fault	1	Rw	0	Set to one if an error is detected during a suspend or

				resume operation. A write of one to this bit clears it to zero.

7.5 PHY register page 1: Vendor identification page

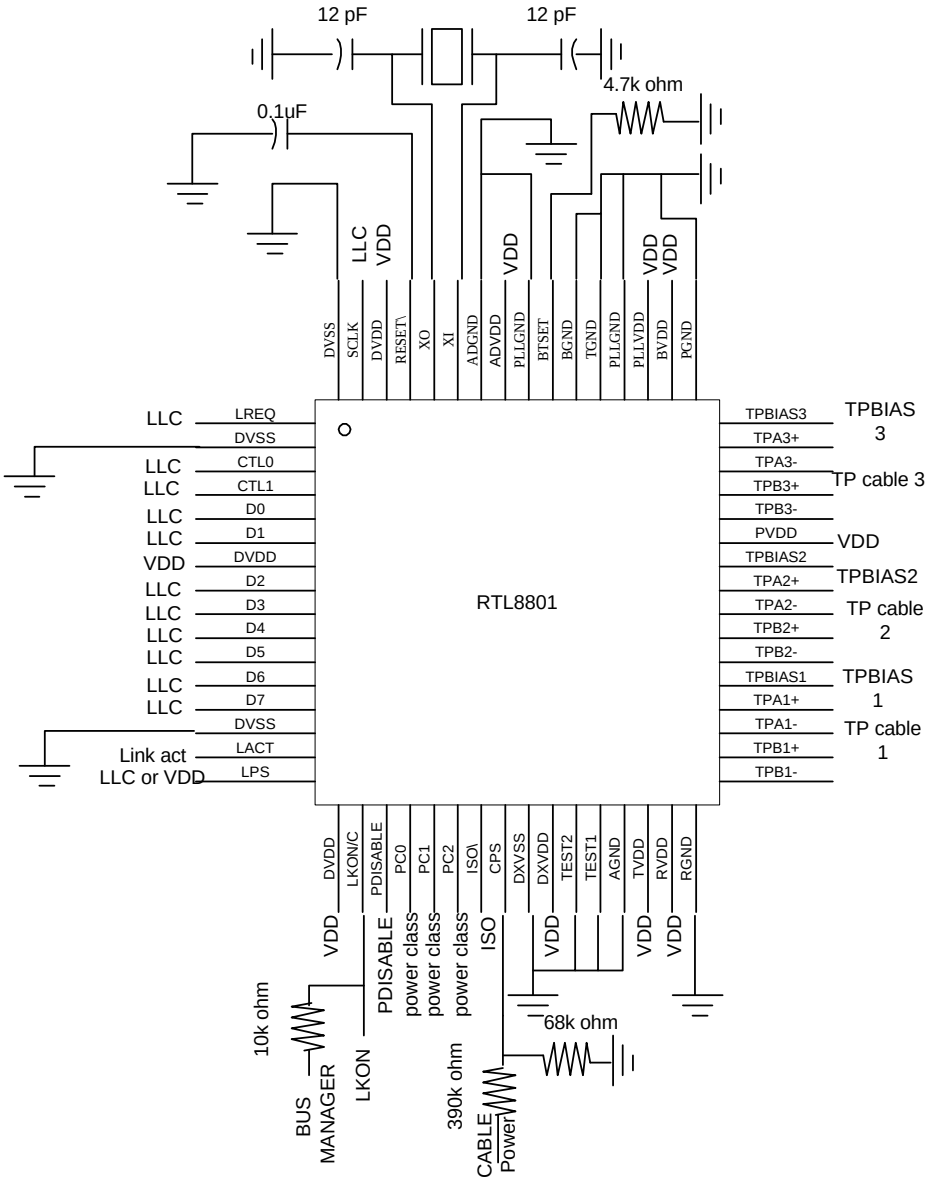
The Vendor Identification page is used to identify the PHY's vendor and compliance level. The page is selected by writing one to Page_select in the PHY register at address 0111.

	0	1	2	3	4	5	6	7
1000b	Compliance_level							
1001b	Reserved							
1010b	Vendor_ID							
1011b								
1100b								
1101b	Product_ID							
1110b								
1111b								

7.6 PHY register Vendor Identification page fields

	Size	Type	Description
Compliance _level	8	R	Standard to which the PHY implementation complies: 0 = not specified 1 = IEEE P1394a All other values reserved for future standardization. The default is "1".
Vendor_ID	24	R	The company ID or Organizationally Unique Identifier (OUI) of the manufacturer of the PHY. The most significant byte of Vendor_ID appears at PHY register location 1010 and the least significant at 1100. The default value is "00 e0 4c".
Product_ID	24	R	The meaning of this number is determined by the company or organization that has been granted Vendor_ID. The most significant byte of Product_ID appears at PHY register location 1101 and the least significant at 1111. The default value is "88 01 00".

8.0 Application information



9. ELECTRICAL CHARACTERISTICS

9.1 D.C. Electric Characteristics

9.1.1. Absolute Maximum Ratings

Symbol	Conditions	Min.	Type.	Max.
Supply Voltage		-0.3V		4V
Storage Temp.		-65¢ J		150¢ J

9.1.2. Operating Conditions

Symbol	Conditions	Min.	Type.	Max.
Vcc	Supply voltage	3.0V		3.6
TA	Operating Temperature	0¢ J		70¢ J

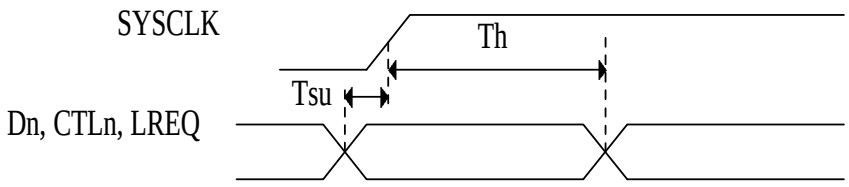
9.1.3. Power Dissipation

Max = 900 mW

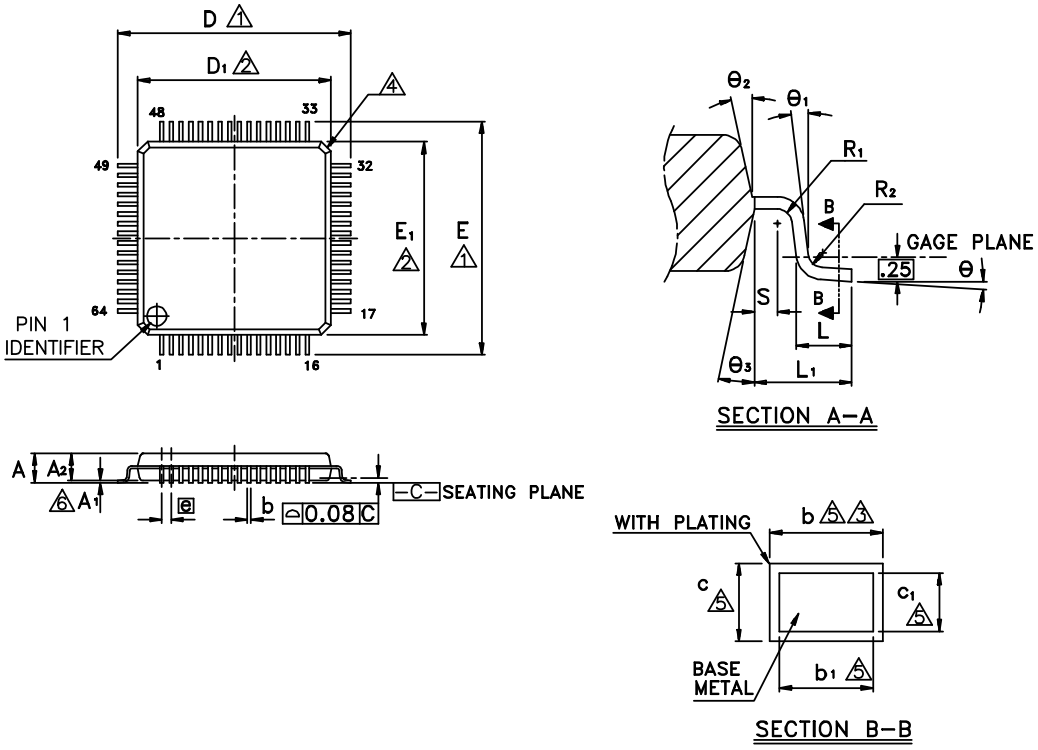
9.2 A.C. Electric Characteristics

A.C. Timing

9.2.1. Dn, CTLn, LREQ Input Setup and Hold Timing Waveforms



Symbol	Parameter	Min	Type.	Max.	Units
Tsu	Setup time, Dn, CTLn, LREQ to Sysclk	5			ns
Th	Hold time, Dn, CTLn, LREQ before Sysclk	2			ns



Note:

1.To be determined at seating plane -c-

2.Dimensions D_1 and E_1 do not include mold protrusion. D_1 and E_1 are maximum plastic body size dimensions including mold mismatch.

3.Dimension b does not include dambar protrusion. Dambar can not be located on the lower radius of the foot.

4.Exact shape of each corner is optional.

5.These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

6. A_1 is defined as the distance from the seating plane to the lowest point of the package body.

7.Controlling dimension : millimeter.

8. Reference document : JEDEC MS-026 , BBC

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A_1	0.000	0.004	0.008	0.00	**0.1**	0.20
A_2	0.051	0.055	0.059	1.30	**1.40**	1.50
b	0.006	0.009	0.011	0.15	**0.22**	0.29
b_1	0.006	0.008	0.010	0.15	**0.20**	0.25
c	0.004	-	0.008	0.09	-	0.20
c_1	0.004	-	0.006	0.09	-	0.16
D	0.472 BSC			12.00 BSC		
D_1	0.394 BSC			10.00 BSC		
E	0.472 BSC			12.00 BSC		
E_1	0.394 BSC			10.00 BSC		

TITLE : 64LD LQFP (10x10x1.4mm)
PACKAGE OUTLINE DRAWING , FOOTPRINT 2.0mm

e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L_1	0.039 REF			1.00 REF		
q	0°	3.5°	9°	0°	3.5°	9°
q_1	0°	-	-	0°	-	-
q_2	12° TYP			12° TYP		
q_3	12° TYP			12° TYP		

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		VERSION	1
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