SONET/SDH/ATM OC-3/12 TRANSCEIVER W/CDR S3032

FEATURES

- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports 155.52 Mbit/s (OC-3) and 622.08 Mbit/s (OC-12)
- Selectable reference frequencies of 19.44, 38.88, 51.84 or 77.76 MHz
- Interface to both LVPECL and LVTTL logic
- Simple interface with 3.3V or 5V optical modules
- Directly compatible with 3.3V or 5V network interface devices
- 8-bit LVTTL data path
- Compact 10 mm 64 PQFP package
- Diagnostic loopback mode
- Low jitter LVPECL serial interface
- Single 3.3 V supply

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

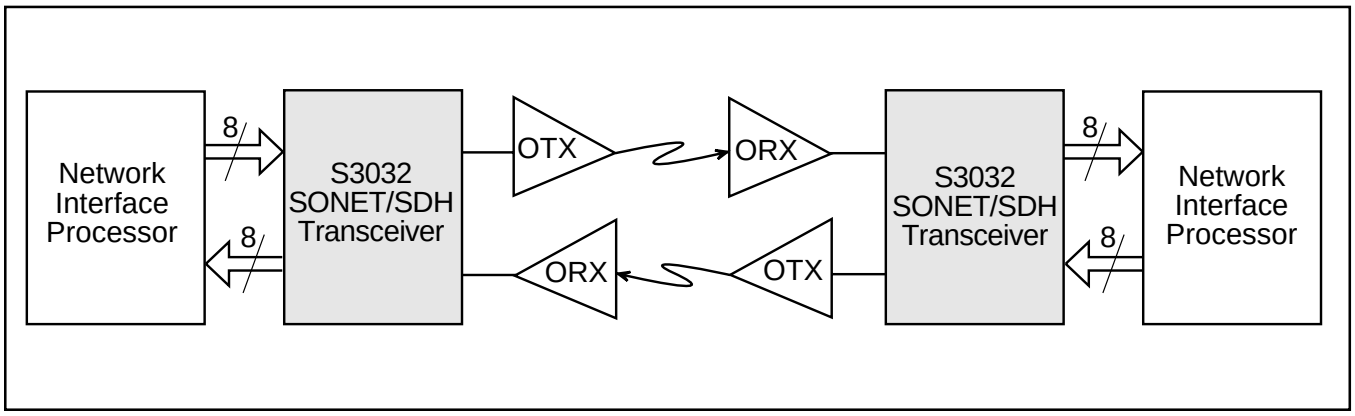
GENERAL DESCRIPTION

The S3032 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) and OC-3 (155.52 Mbit/s) interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3032 transceiver chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream. The S3032 also performs SONET/SDH frame detection. The chip can be used with a 19.44, 38.88, 51.84 or 77.76 MHz reference clock, in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3032 is packaged in a 10 mm 64 PQFP, offering designers a small package outline.

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3032 chip supports OC-3 and OC-12 rates (155.52 and 622.08 Mbit/s).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-12 consists of 36 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 36 overhead and 1044 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

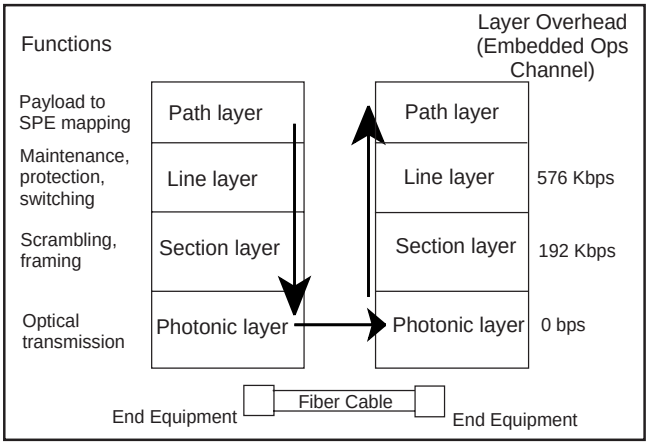


Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 3. STS–12/OC–12 Frame Format

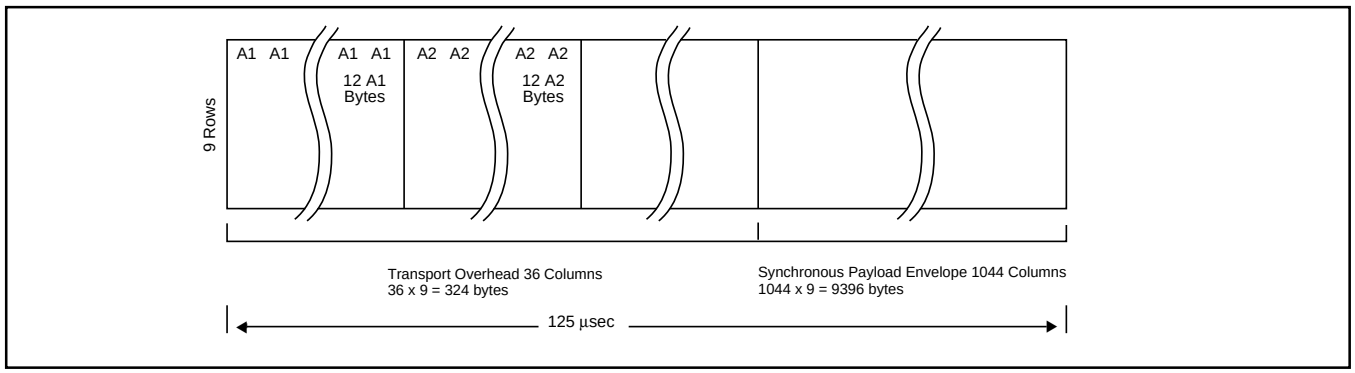
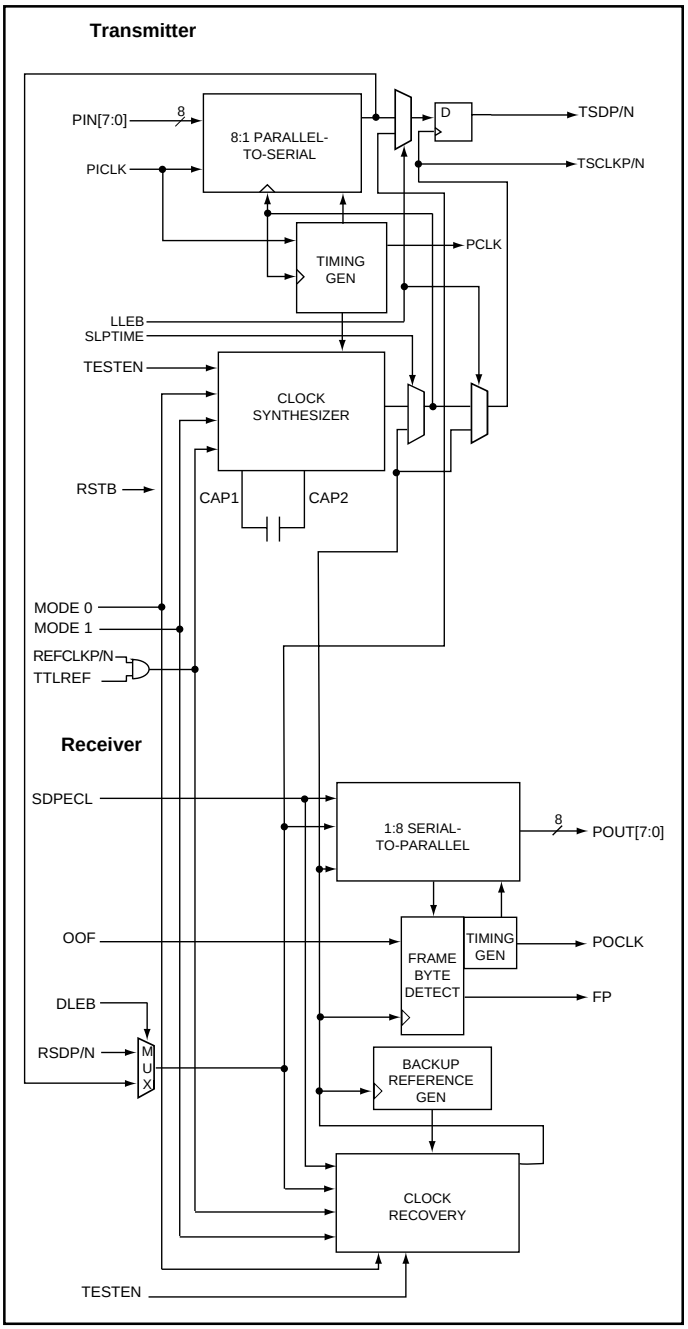


Figure 4. S3032 Transceiver Functional Block Diagram



S3032 OVERVIEW

The S3032 transceiver implements SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagram in Figure 4 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing. The system timing circuitry consists of management of the data stream, framing, and clock distribution throughout the front end.

The S3032 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 8 through 14.

Suggested Interface Devices

AMCC	CONGO (S1201)	POS/ATM SONET Mapper
AMCC	NILE (S1202)	ATM SONET Mapper

S3032 TRANSCEIVER FUNCTIONAL DESCRIPTION

TRANSMITTER OPERATION

The S3032 transceiver chip performs the serializing stage in the processing of a transmit SONET STS-3 or STS-12 bit serial data stream. It converts the 8-bit parallel 19.44 or 77.76 Mbps data stream into bit serial format at 155.52 or 622.08 Mbit/sec.

A high-frequency bit clock can be generated from a 19.44, 38.88, 51.84 or 77.76 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback is provided (transmitter to receiver). See Other Operating Modes on page 7.

Clock Synthesizer

The clock synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCLKP/N or TTLREF).

The REFCLKP/N input must be generated from an LVPECL crystal oscillator which has a frequency accuracy that meets the value stated in Table 8 in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH. TTLREF must be at logic "one" if REFCLKP/N are used.

For TTL reference operation, the TTLREF input should be driven with an LVTTL crystal oscillator output with the ppm accuracy specified in Table 8 for SONET compliance. In this mode, REFCLKP should be connected to LVPECL "High" and REFCLKN should be tied to LVPECL "Low."

Table 2. Reference Frequency Options

MODE [1:0]	REFERENCE CLOCK FREQUENCY	OPERATING MODE
00	19.44 MHz	STS-12
01	38.88 MHz	STS-12
10	51.84 MHz	STS-12
11	77.76 MHz	STS-12
0 NC	19.44 MHz	STS-3
1 NC	38.88 MHz	STS-3
NC 0	51.84 MHz	STS-3
NC 1	77.76 MHz	STS-3*

* Only valid in SLP mode.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLKP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generation

The timing generation function, seen in Figure 4, provides a byte rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PIN[7:0] data from the parallel input register to the serial shift register.

The PCLK output is a byte rate version of transmit serial clock at 19.44 or 77.76 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3032 device.

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 4 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

The load signal, which latches the data from the parallel to the serial shift register, has a fixed relationship to PCLK. If PICLK is tied to PCLK, the PIN[7:0] data latched into the parallel register will meet the timing specifications with respect to the load signal. If PICLK is not tied to PCLK, the delay must meet the timing requirements shown in Figure 9.

Table 3. Reference Jitter Limits

Frequency Band	Maximum Reference Clock Jitter	Operating Mode
12 kHz to 5 MHz	14 ps rms	STS–12
12 kHz to 1 MHz	56 ps rms	STS–3

RECEIVER OPERATION

The S3032 transceiver chip provides the first stage of digital processing of a receive SONET STS-3 or STS-12 bit-serial stream. It converts the bit-serial 155.52 or 622.08 Mbit/sec data stream into a 19.44 or 77.76 Mbps 8-bit parallel data format.

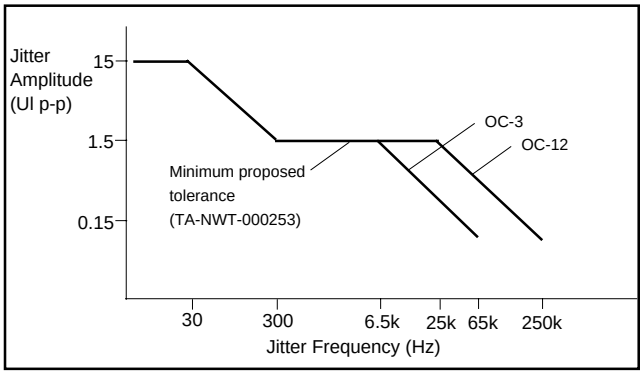
Clock recovery is performed on the incoming scrambled NRZ data stream. A 19.44, 38.88, 51.84 or 77.76 MHz reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

Clock Recovery

Clock recovery, as shown in the block diagram in Figure 4, generates a clock that is at the same frequency as the incoming data bit rate at the RSD input or, in loopback, the transmitter data output. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Figure 5. Clock Recovery Jitter Tolerance



The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields the typical capture time stated in Table 8 for random incoming NRZ data. A single external clean-up capacitor is utilized as part of the loop filter.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 5.

Lock Detect

The S3032 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the received serial data fails the run length or frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the POCLK output under loss of signal or loss of lock conditions. If the serial data inputs have a run length of 80-bit times with no transitions, the PLL will be declared out of lock. In addition, if the recovered clock frequency deviates from the local reference clock frequency by more than the specified ppm, the PLL will also be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the specified ppm and the run length check indicates valid data, the PLL will be declared in lock and the lock detect output will go active. The deassertion of SDPECL will also cause an out-of-lock condition. (See Table 8).

Backup Reference Generator

The backup reference generator seen in Figure 4 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock, REFCLKP/N.

Frame and Byte Boundary Detection

The frame and byte boundary detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is set High. It is disabled when a framing pattern is detected and OOF is no longer set High. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or looped transmitter data). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUTP/N[7:0]). The frame boundary is reported on the Frame Pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 or STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 μs, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set Low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial-to-parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial-to-parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the serial-to-parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial-to-parallel converter is that POCLK is neither truncated nor extended during reframe sequences. (See Figures 11 through 13.)

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes.

The differential serial output data from the transmitter is routed to the clock recovery unit and serial-to-parallel block in place of the normal Receive Serial Data (RSD). SDPECL must be High for diagnostic loopback.

Line Loopback

When Line Loopback Enable (LLEB) is active, a loopback from the receiver to the transmitter at the serial data rate can be set up for facility loopback testing. The recovered clock is used to retime the incoming data before driving the TSDP/N outputs. In line loopback mode, the TSCLKP/N outputs will be driven by the receiver recovered clock.

Serial Loop Timing

In Serial Loop Timing (SLPTIME) mode, the clock synthesizer PLL of the S3032 is bypassed, and the timing of the entire transmitter section is controlled by the recovered receive serial clock. This mode is entered by using the SLPTIME input.

In this mode the REFCLKP/N input is not used, and the MODE[1:0] inputs are ignored for all transmit functions.

Forward Clocking

For both 77.78 MHz and 38.88 MHz reference operation, the S3032 operates in the forward clocking mode. The PLL locks the PCLK output of the transmitter section to the REFCLK with a fixed and repeatable phase relation. This allows the transmitter data source to also be the timing source for the serial clock synthesis. (See Figures 14 and 15.)

The rising edge of PCLK is locked to the rising edge of REFCLKP, with a maximum delay of 8 to 10 nsec due to the PCLK TTL output driver.

For operation at 19.44 MHz and 51.84 MHz references, seperate timing paths are used for PLL control and PCLK generation, and forward clocking is not recommended.

Table 4. S3032 Transmitter Pin Assignment and Descriptions (Active High unless otherwise stated.)

Pin Name	Level	I/O	Pin #	Description
PIN7 PIN6 PIN5 PIN4 PIN3 PIN2 PIN1 PIN0	LVTTL	I	61 60 59 58 57 56 55 54	Parallel Data Input. A 77.76 Mbps or 19.44 Mbps, aligned to the PICLK parallel input clock. PIN[7] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN[0] is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PICLK.
PICLK	LVTTL	I	62	Parallel Input Clock. A 77.76 or 19.44 MHz, nominally 50% duty cycle input clock, to which PIN[7:0] is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN[7:0]. After a master reset, two rising edges of PICLK are required to fully initialize the internal datapath.
CAP1 CAP2	Analog	I	10 9	Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. The capacitor value should be 0.01µF ±10% tolerance, X7'R dielectric. 50 volt is recommended (16 volt is acceptable).
TSDP TSDN	Diff. LVPECL	O	15 16	Transmit Serial Data. Differential LVPECL serial data stream signals, normally connected to an optical transmitter module.
TSCLKP TSCLKN	Diff. LVPECL	O	19 18	Transmit Serial Clock. Clock that can be used to retime the TSD signal. This clock will be 622.08 MHz or 155.52 MHz, depending on the operating mode.
PCLK	LVTTL	O	64	Parallel Clock. A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3032 device.

Table 5. S3032 Receiver Pin Assignment and Descriptions (Active High unless otherwise stated.)

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Diff. LVPECL	I	25 26	Receive Serial Data stream signals. Normally connected to an optical receiver module. A clock is recovered from transitions on the RSD inputs.
OOF	LVTTL	I	33	Out Of Frame Indicator. Used to enable framing pattern detection logic in the S3032. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set Low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 11 through 13.)
SDPECL	LVPECL	I	20	Signal Detect. LVPECL with internal pull-down. Active High. A single-ended 10k LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDPECL is inactive, the data on the Serial Data In (RSDP/N) pins will be internally forced to a constant zero. When SDPECL is active, data on the RSDP/N pins will be processed normally.
POUT7 POUT6 POUT5 POUT4 POUT3 POUT2 POUT1 POUT0	LVTTL	O	45 44 43 41 40 39 37 36	Parallel Data Output bus. A 77.76 Mbps or 19.44 Mbps aligned to the POCLK parallel output clock. POUT[7] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT[0] is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT[7:0] is updated on the falling edge of POCLK.
FP	LVTTL	O	35	Frame Pulse. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses High for one POCLK cycle when a 48-bit sequence matching the framing is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses High when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.
POCLK	LVTTL	O	47	Parallel Output Clock. A 77.76 or 19.44 MHz, nominally 50% duty cycle, byte rate output clock that is aligned to POUT[7:0] byte serial output data. POUT[7:0] and FP are updated on the falling edge of POCLK.

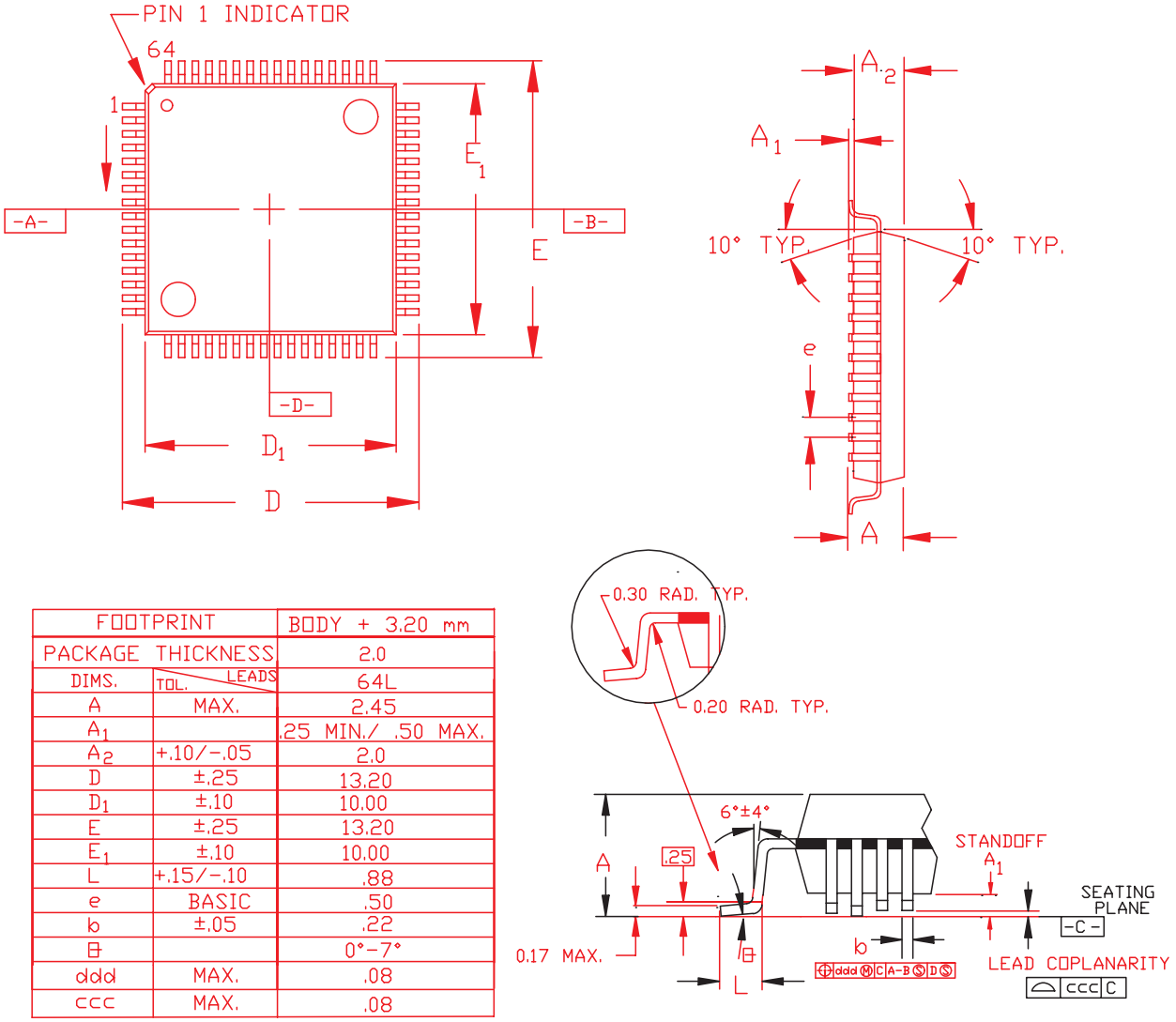
Table 6. S3032 Common Pin Assignment and Descriptions (Active High unless otherwise stated.)

Pin Name	Level	I/O	Pin #	Description
TESTEN	LVTTL	I	50	Test Clock Enable signal. Active High. Set High to provide access to the PLL during production tests.
REFCLKP REFCLKN	Diff. LVPECL	I	6 5	Reference Clock Input. Used as the reference for the internal bit clock frequency synthesizer. (Must be connected to a logic one state if TTL REF is used).
TTLREF	LVTTL	I	4	TTL Reference Clock Input. Can be used as the reference for the internal bit clock frequency synthesizer. (Must be tied High if REFCLKP/N is used).
DLEB	LVTTL	I	31	Diagnostic Loopback Enable. Active Low. Selects diagnostic loopback. When DLEB is High, the S3032 device uses the primary data (RSD) inputs. When Low, the S3032 device uses the diagnostic loopback data from the transmitter. SDPECL must be High for diagnostic loopback.
RSTB	LVTTL	I	32	Master Reset. Reset input for the device. Active Low. Initializes the device to a known state and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever the user wishes to force the PLL to re-acquire to the reference clock. The S3032 will also reacquire to the reference clock if the serial data input is held quiescent for at least 16 ms.
LLEB	LVTTL	I	13	Line Loopback Enable. Active Low. Selects line loopback. When LLEB is Low, the S3032 will route the retimed serial data from the receive section to the transmitter outputs.
MODE1 MODE0	LVTTL	I	51 52	Operating Mode select inputs. Used to select the reference clock frequency and the operating speed (see Table 2).
SLPTIME	LVTTL	I	53	Serial Clock Loop Time Select input. Active High. Used to enable the recovered clock from the receive section to be used in place of the synthesized transmit clock.

Table 7. S3032 Power and Ground Pin Assignments

Pin Name	Level	I/O	Pin #	Description
RXAVCC0,1	3.3V		21 24	Power Supply
RXAGND0,1	GND		22 23	Ground (0 V)
RSCLKGND	GND		27	Ground (0 V)
RSCLKVCC	3.3V		28	Power Supply
RXCOREVCC	3.3V		29	Power Supply
RXCOREGND	GND		30	Ground (0 V)
TTLGND	GND		34 42 49	Ground (0 V)
TTLVCC	3.3V		38 46 48	Power Supply
PCLKVCC	3.3V		63	Power Supply
PCLKGND	GND		1	Ground (0 V)
TXCOREVCC	3.3V		3	Power Supply
TXCOREGND	GND		2	Ground (0 V)
AGND0,1	GND		11 8	Ground (0 V)
AVCC0,1	3.3V		12 7	Power Supply
TXOUTVCC	3.3V		14	Power Supply
TXOUTGND	GND		17	Ground (0 V)

Figure 6. 64 PQFP Package



FOOTPRINT		BODY + 3.20 mm
PACKAGE THICKNESS		2.0
DIMS.	TOL. / LEADS	64L
A	MAX.	2.45
A_1		.25 MIN./ .50 MAX.
A_2	+.10/−.05	2.0
D	±.25	13.20
D_1	±.10	10.00
E	±.25	13.20
E_1	±.10	10.00
L	+.15/−.10	.88
e	BASIC	.50
b	±.05	.22
θ		0°−7°
ddd	MAX.	.08
ccc	MAX.	.08

Thermal Management

Max Package Power	Θja
1.25 W	48˚ C/W

Figure 7. Pinout Assignments

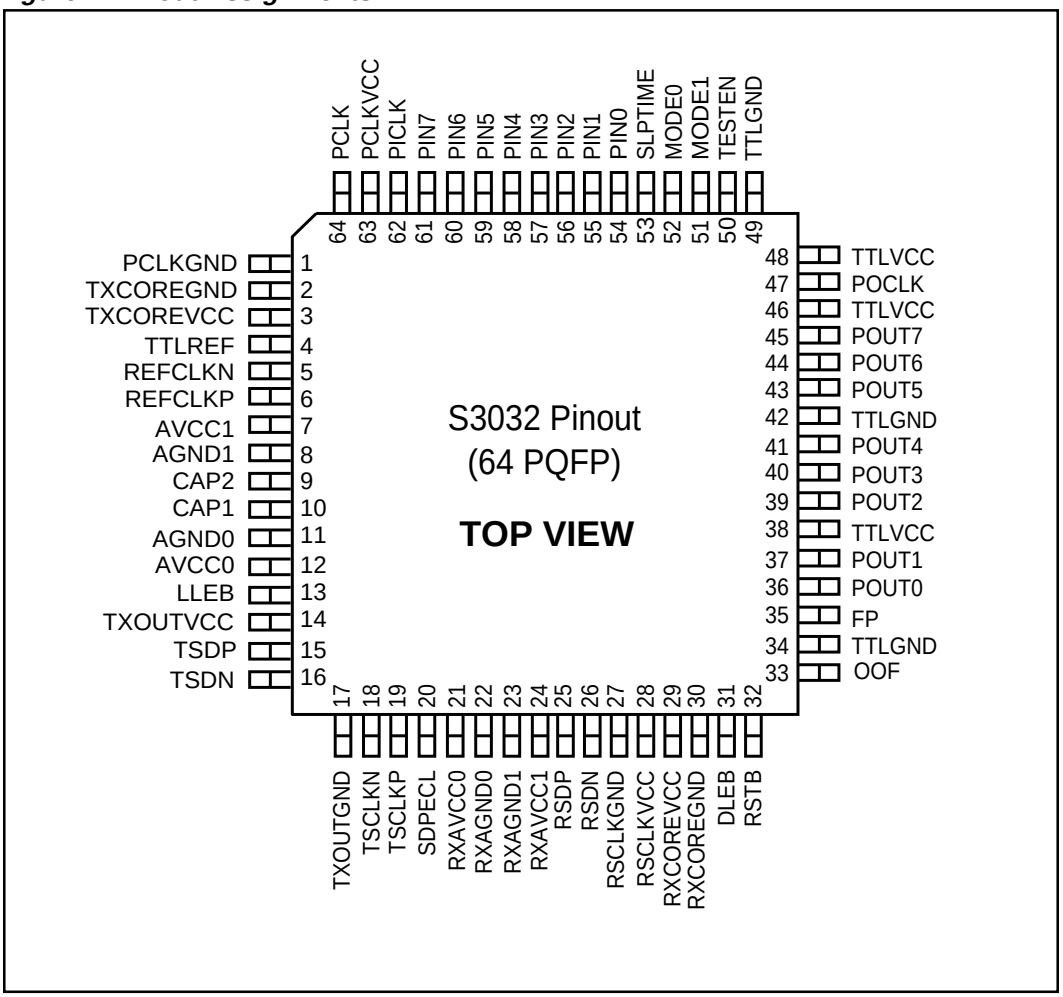


Table 8. Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Nominal VCO Center Frequency		622.08 ±12%		MHz	
TSCLK Clock Output Jitter OC-3/STS-3 OC-12/STS-12			 32 8	 ps(rms) ps(rms)	Given the jitter on REFCLKP/N (12 kHz to 1 MHz band) is less than: 56 ps rms (OC-3) 14 ps rms (OC-12)
Data Output Jitter **STS-12** -19.44 MHz Ref. Clk. -38.88 MHz Ref. Clk. -51.84 MHz Ref. Clk -77.76 MHz Ref. Clk. **STS-3** -19.44 MHz Ref. Clk -38.88 MHz Ref. Clk -51.84 MHz Ref. Clk.			 0.007 0.006 0.005 0.004 0.003 0.002 0.002	UI (rms)	rms jitter, in lock
Reference Clock Frequency Tolerance[1]	-20		+20	ppm	Required to meet SONET output frequency specification
OC-3/STS-3 and OC-12/STS-12 Capture Range Lock Range Capture Time		 ±200 ±12% 32		 ppm µs	 With respect to fixed reference frequency
Acquisition Lock Time			16	µsec	Minimum transition density of 20% With device already powered up and valid ref. clk.
Input Data Eye Opening	30			% of UI	Measured BER less than 1×10^{-12}
Reference Clock Input Duty Cycle	30		70	% of UI	
Reference Clock Rise & Fall Times			2.0	ns	20% to 80% of amplitude
LVPECL Output Rise & Fall Times			450	ps	20% to 80%, 51 Ω load, 5 pF cap
TSCLK Duty Cycle	40		60	%	% of UI
Frequency difference at which out of lock is declared (REFCLK compared to the divided down VCO clock).	250	290	330	ppm	
Frequency difference at which receive PLL is declared in lock (REFCLK compared to the divided down VCO clock).	250	290	330	ppm	
Maximum run length of serial data input before out of lock is declared		80		UI (Unit intervals)	
OC-12/STS-12 Jitter Tolerance[2]	0.4			UI	Sinusoidal input jitter. Amplitude on SERDATIP/N data inputs from 250 kHz to 5 MHz.

1. Noise on REFCLKP/N should be less than 14 ps rms in a jitter frequency band from 12 kHz to 5 MHz.
2. Guaranteed but not tested.

Table 9. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	–65		150	˚C
Voltgae on V_{CC} with Respect to GND	–0.5		+5.0	V
Voltage on any LVTTL Input Pin	–0.5		+5.5	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
LVTTL Output Sink Current			8	mA
LVTTL Output Source Current			8	mA
High Speed LVPECL Output Source Current			50	mA

ESD Ratings

The S3032 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500 V, except pin 9, pin 10, and pin 19.

Table 10. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias	–40		+130	˚C
Voltage on V_{CC} with Respect to GND 3.3 V Operation	3.135	3.3	3.465	V
Voltage on any LVTTL Input Pin	0		5.5	V
Voltage on any LVPECL Input Pin	V_{CC} –2		V_{CC}	V

Table 11. LVTTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL) –3.3 V Power Supply –3.3 V Power Supply	 2.1 2.2			 V V	 V_{CC} = min, I_{OH} = –2.4 mA V_{CC} = min, I_{OH} = –0.1 mA
V_{OL}	Output Low Voltage (TTL) –3.3 V Power Supply			 0.5	 V	 V_{CC} = min, I_{OL} = 2.4 mA
V_{IH}	Input High Voltage (TTL)	2.0		TTL V_{CC}	V	$I_H \leq 1$ mA at V_{IH} = 5.5 V
V_{IL}	Input Low Voltage (TTL)	0		0.8	V	
I_{IH}	Input High Current (TTL)			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current (TTL)	–500		–50	µA	V_{IN} = 0.5 V
I_{CC}	Supply Current		300	360	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		1.0	1.25	W	Outputs open, V_{CC} = V_{CC} max

Table 12. LVPECL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} –2.000		V_{CC} –1.441	V	Guaranteed Input Low Voltage for single-ended inputs.
V_{IH}	Input High Voltage	V_{CC} –1.225		V_{CC} –0.570	V	Guaranteed Input High Voltage for single-ended inputs.
V_{IL}	Input Low Voltage	V_{CC} –2.000		V_{CC} –0.700	V	Guaranteed Input Low Voltage for differential inputs.
V_{IH}	Input High Voltage	V_{CC} –1.750		V_{CC} –0.450	V	Guaranteed Input High Voltage for differential inputs.
V_{ID}	Input Differential Voltage	0.200	0.500	1.400	V	Differential Input Voltage.
I_{IHD}	Differential Input High Current	–0.500		20.000	µA	V_{ID} = 500 mV
I_{ILD}	Differential Input Low Current	–0.500		20.000	µA	V_{ID} = 500 mV
I_{IH}	Single Ended Input High Current			100	µA	SD Inputs have internal 24 kΩ to 1.8 V load resistor.
I_{IL}	Single Ended Input Low Current			–100	µA	SD Inputs have internal 24 kΩ to 1.8 V load resistor.
V_{OL}	Output Low Voltage	V_{CC} –2.000		V_{CC} –1.500	V	50 Ω termination to V_{CC} –2 V
V_{OH}	Output High Voltage	V_{CC} –1.110		V_{CC} –0.670	V	50 Ω termination to V_{CC} –2 V
V_{OD}	Output DIfferential Voltage	0.390		1.330	V	Differential Output Voltage.

Table 13. Transmitter AC Timing Characteristics

Parameter	Description	Min	Max	Units
tD_{PICLK}	PICLK Delay from PCLK	0	5.5	ns
tS_{PIN}	PIN [7:0] Setup Time w.r.t. PICLK	1.5		ns
tH_{PIN}	PIN [7:0] Hold Time w.r.t. PICLK	1.0		ns
tP_{TSD}	TSCLK Low to TSD Valid Propagation Delay	-200	600	ps
tS_{TSD}	TSD Setup Time w.r.t. TSCLK	200		ps
tH_{TSD}	TSD Hold Time w.r.t. TSCLK	200		ps

Table 14. Receiver AC Timing Characteristics

Parameter	Description	Min	Max	Units
	POCLK Duty Cycle	40	60	%
tP_{POUT}	POCLK Low to POUT [7:0] Valid Prop. Delay @ STS-3 POCLK Low to POUT [7:0] Valid Prop. Delay @ STS-12	-8 -3	0 1	ns ns
tS_{POUT}	POUT [7:0] and FP Setup Time w.r.t. POCLK[1]	4		ns
tH_{POUT}	POUT [7:0] and FP Hold Time w.r.t. POCLK[1]	3		ns

1. Setup and hold times are specified for an interface which directly connects the S3032 receiver parallel outputs to the data and clock inputs on an external register.

Figure 8. Transmitter Output Timing

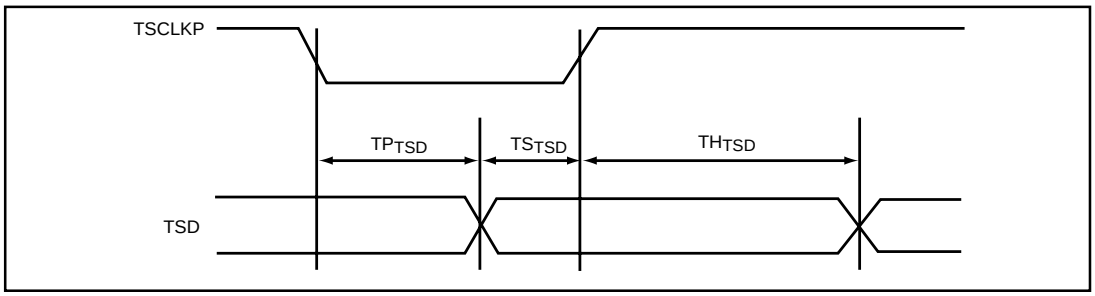
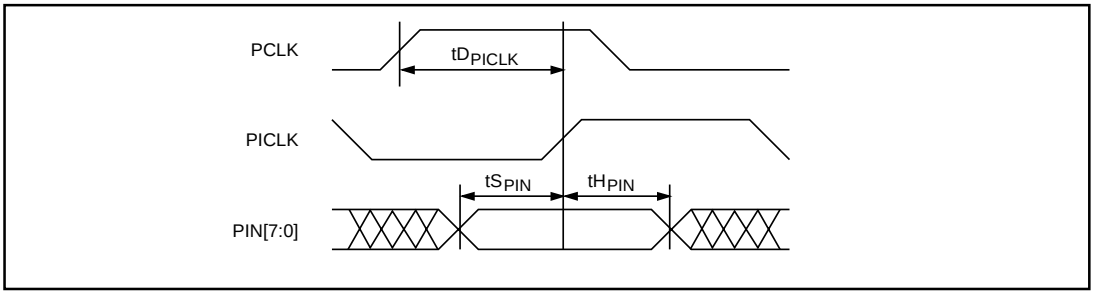
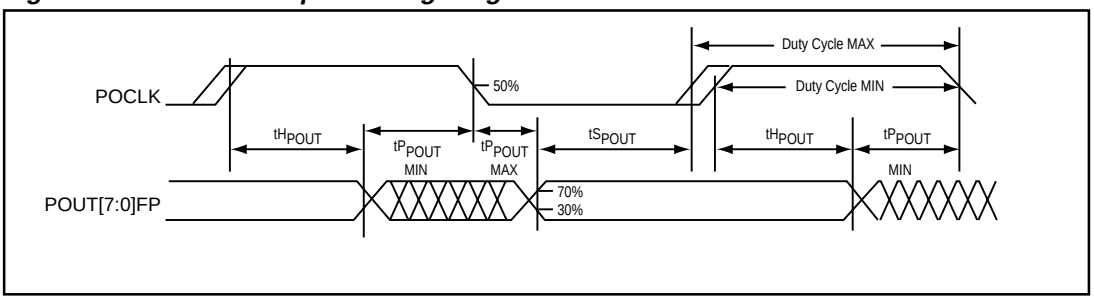


Figure 9. PIN AC Input Timing



1. When a setup time is specified on LVTTL signals between an input and a clock, the setup time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVTTL signals between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50%point of the input.

Figure 10. Receiver Output Timing Diagram



Notes on Output Timing:

1. Output propagation delay time of LVTTL outputs is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays of LVTTL outputs are measured with a 15 pF load on the outputs.

RECEIVER FRAMING

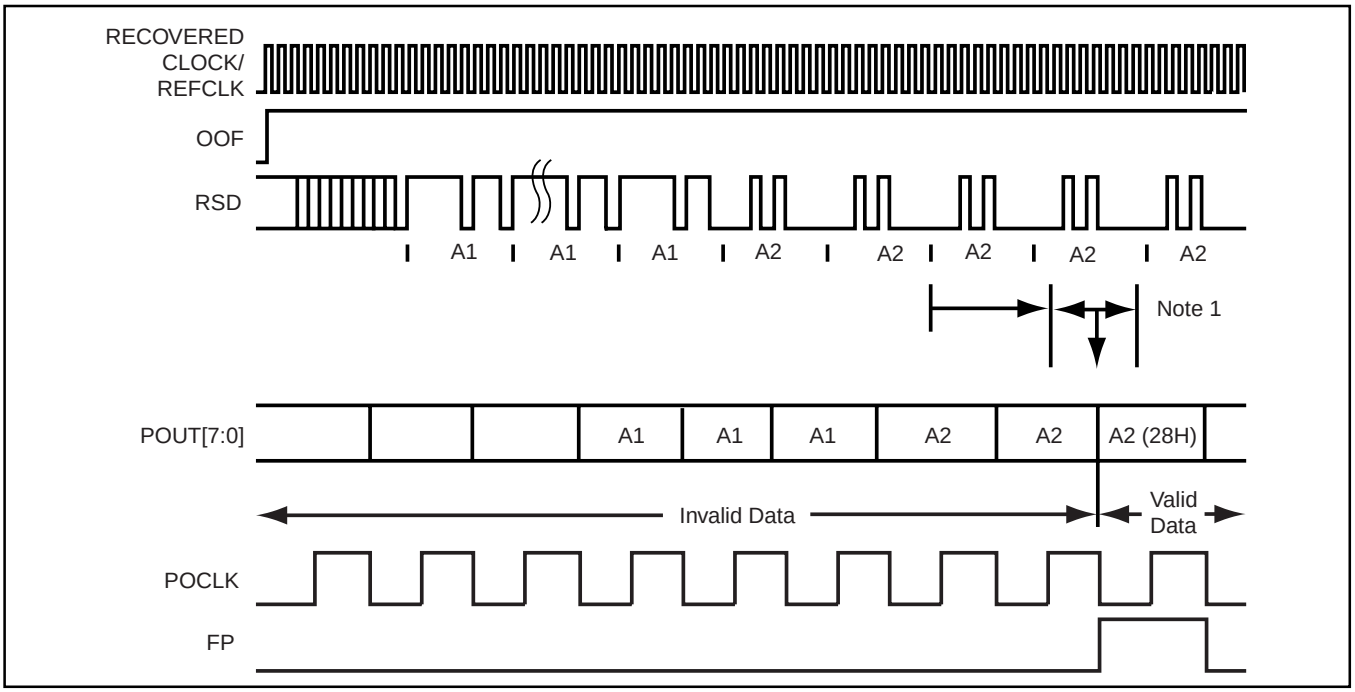
Figure 11 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is High. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set High for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains High for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 12. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set Low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes Low, whichever occurs last. Figure 11 shows a typical OOF timing pattern which occurs when the S3032 is connected to a down stream section terminating device. OOF remains High for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes Low.

Figure 13 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 11. Frame and Byte Detection



1. Range of input to output delay can be 1.5 to 2.5 POCLK cycles.

Figure 12. OOF Operation Timing

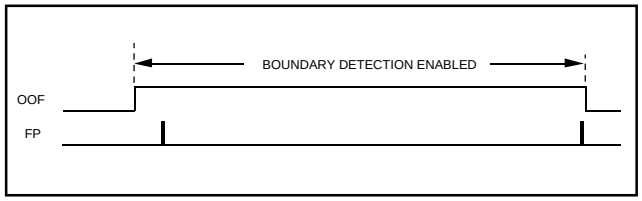
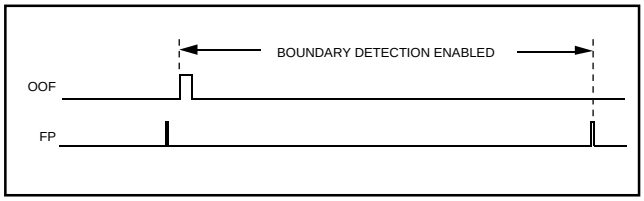


Figure 13. Alternate OOF Timing



S3032 WITH DATA CLOCK SYNCHRONOUS TO REFERENCE CLOCK

In some applications it is necessary to "forward clock" the data in a SONET/SDH system. In this application the reference clock from which the High speed serial clock is synthesized and the parallel data clock both originate from the same (usually TTL/CMOS) clock source. This application note explains how the AMCC S3032 can be configured to operate in this mode.

Clock Control Logic Description

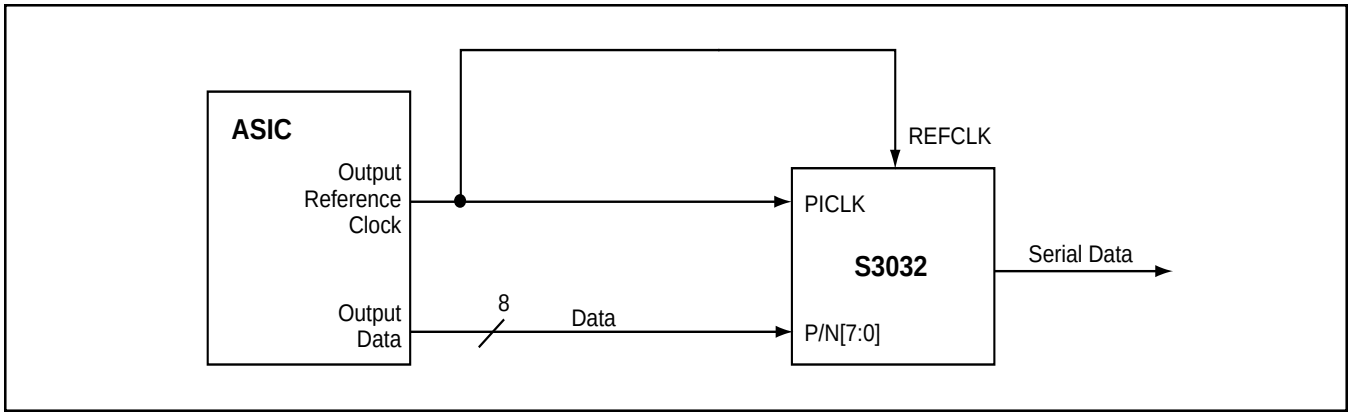
The timing control logic in the S3032 automatically generates an internal load signal which has a fixed relationship to the reference clock. The logic takes in to account the variation of the reference clock to the internal load signal over temperature and voltage.

The connections required to implement the design are shown in Figure 14. The setup and hold times for the PICLK to the data must be met by the controller ASIC. It is recommended that the data on the falling edge of the output reference clock be latched in order to meet the required specifications.

Possible Problems

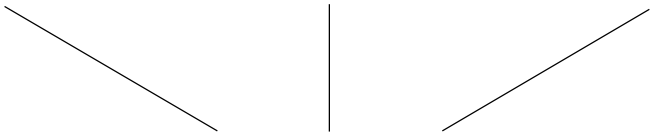
In order to meet the jitter generation specifications required by SONET, the jitter of the reference clock must be minimized. It may be difficult to meet the SONET jitter generation specifications using a reference clock input with a TTL reference source.

Figure 14. S3032 with Data Clocked by Reference Clock



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3032	A – 64 PQFP



X Prefix XXXX Device X Package

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