Data Sheet, DS2, Jan. 2001

Quad IEC AFE Quad ISDN Echocancellation Circuit Analogue Front End PEB 24902 Version 2.1

Quad IEC AFE Quad ISDN Echocancellation Circuit Analogue Front End PEF 24902 Version 2.1

Wired Communications

Infineon technologies

Never stop thinking.

Edition 2001-01-23

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Data Sheet, DS2, Jan. 2001

Quad IEC AFE

Quad ISDN Echocancellation Circuit Analogue Front End

PEB 24902 Version 2.1

Quad IEC AFE

Quad ISDN Echocancellation Circuit Analogue Front End

PEF 24902 Version 2.1

Wired Communications

Never stop thinking.

Revision History: **2001-01-23** DS2

Previous Version: none

Page	Subjects (major changes since last revision)
17, 20, 21	Pin ADDR has to be clamped to V_{DD} rather than to GND
11	XDNx pins removed from Logic Symbol

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

Table of Contents

List of Figures

Page

List of Tables

Page

1 Overview

The PEB 24902 Quad IEC AFE (Quadruple ISDN Echocancellation Circuit Analogue Front End) is part of a 2B1Q or 4B3T ISDN U-transceiver chip set. Up to four lines can be accessed simultaneously by the Quad IEC AFE. The Quad IEC AFE is optimized to work in conjunction with the PEB 24901 Quad IEC DFE-T and the PEB 24911 Quad IEC DFE-Q. An integrated PLL synchronizes the 15.36 MHz Master clock onto the 8 kHz or 2048 kHz PTT Clock. This specification describes the functionality for 2B1Q and 4B3T interfaces.

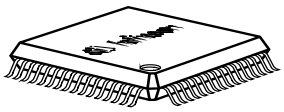
All technical descriptions are valid for PEF 24902 Quad IEC AFE, too. The only difference between PEB 24902 and PEF 24902 is the operating ambient temperature, which is extended for PEF 24902, see **Chapter 7.2**.

Quad ISDN Echocancellation Circuit Analogue Front End
Quad IEC AFE

PEB 24902

Version 2.1 **CMOS**

1.1 Features



P-MQFP-64-1,-2

- Digital to Analogue conversion (transmit pulse)
- Output buffering
- Analogue to digital conversion
- Detection of signal on the line
- Master clock generation by PLL
- P-MQFP-64 Package
- Compliant to ANSI T1.601 (1992), ETSI TS 102080 (1995)
- JTAG boundary scan path compliant to IEEE 1149.1

Type	Package
PEB 24902	P-MQFP-64-1

1.2 Logic Symbol

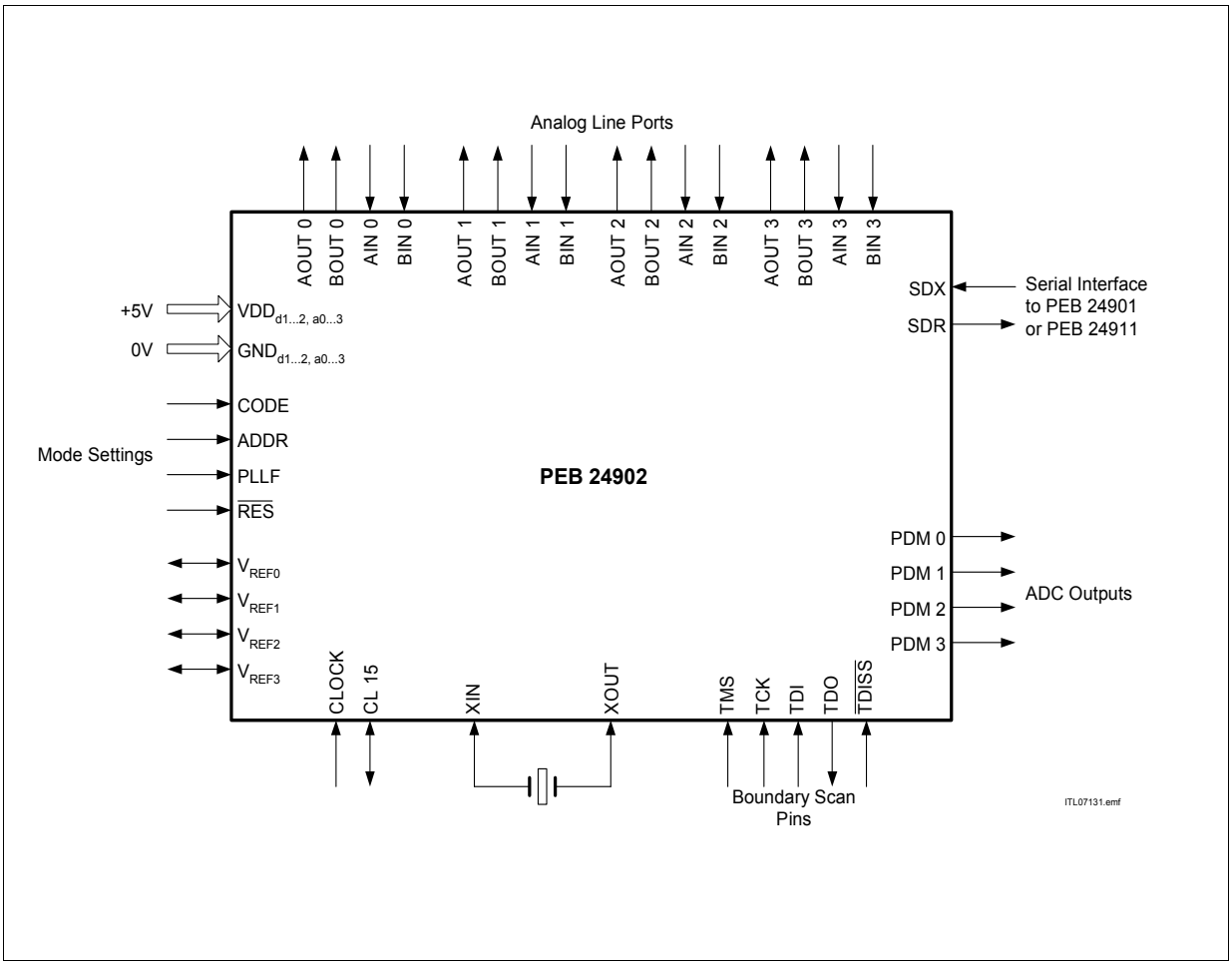


Figure 1 Logic Symbol

1.3 Functional Block Diagram

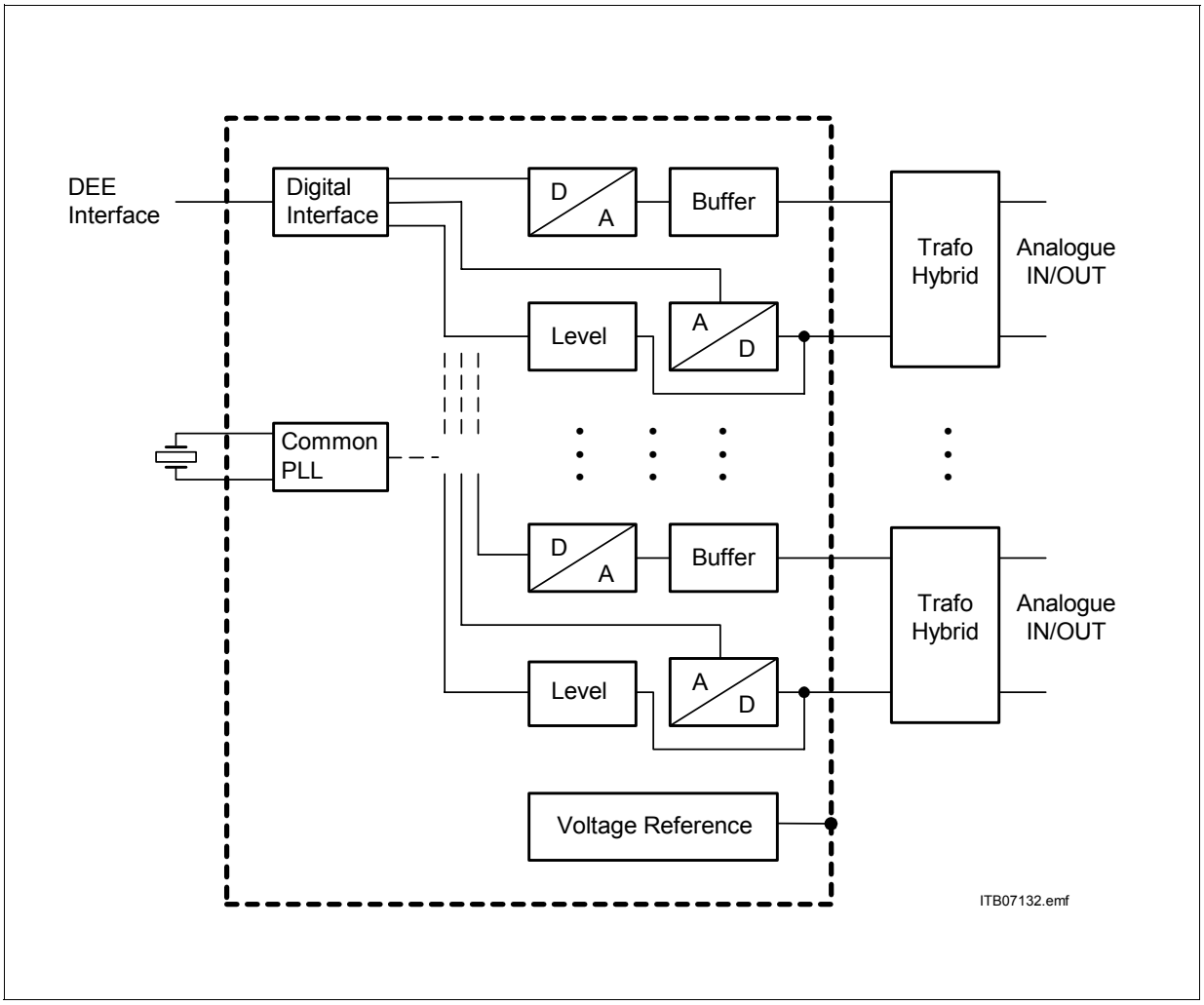


Figure 2 Block Diagram of the Quad IEC AFE

1.4 Pin Configuration

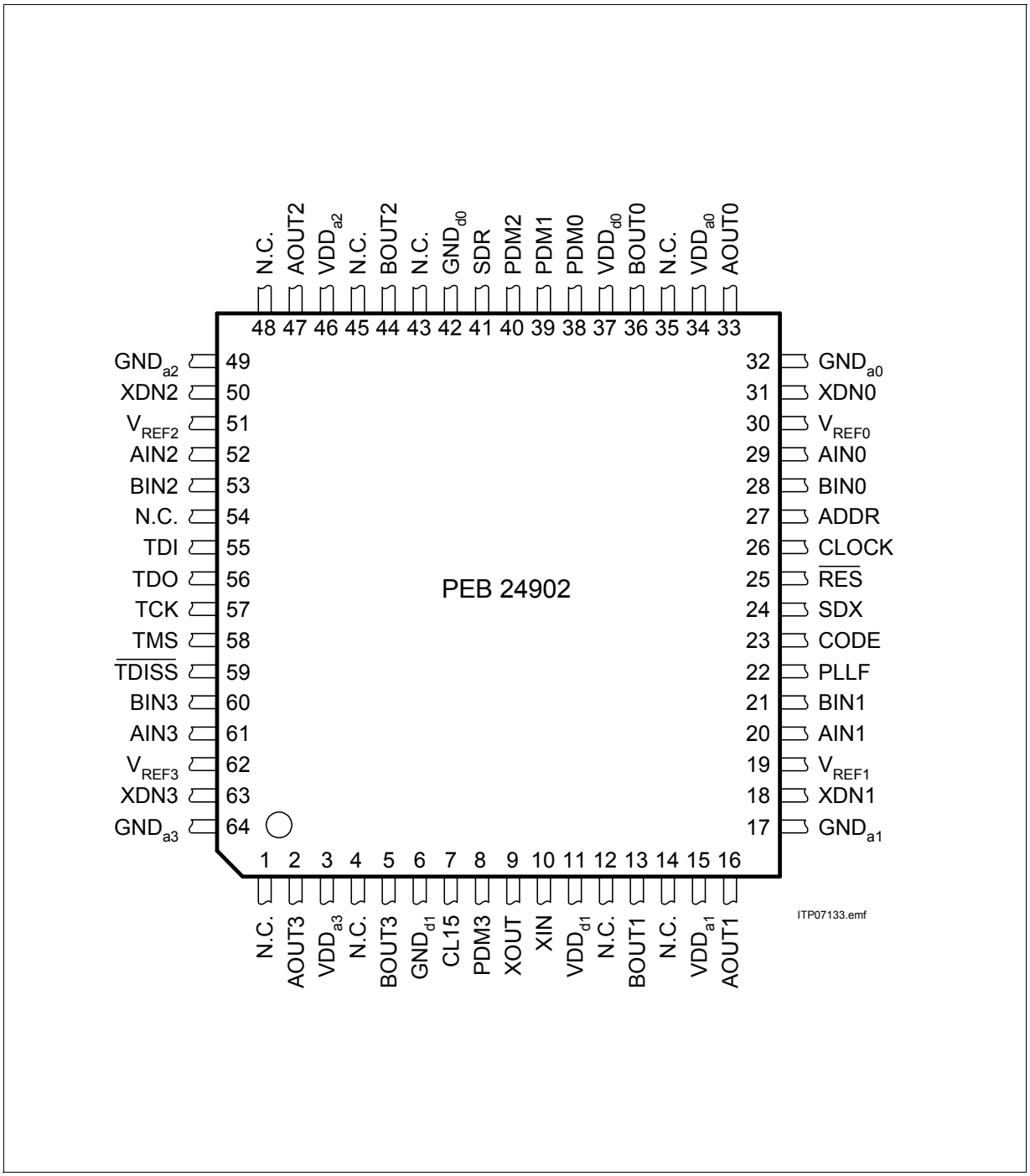


Figure 3 Pin Configuration (top view)

1.5 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type, a brief description of the function and cross-references referring to the sections in which the pin functions are discussed.

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Description	Reference Section
Power Supply Pins				
37	VDD_{d1}		5V +/-5% digital supply voltage	5.1
11	VDD_{d2}			
34	VDD_{a0}		5V +/-5% analogue supply voltage	5.1
15	VDD_{a1}			
46	VDD_{a2}			
3	VDD_{a3}			
42	GND_{d1}		0V digital	5.1
6	GND_{d2}			
32	GND_{a0}		0V analogue	5.1
17	GND_{a1}			
49	GND_{a2}			
64	GND_{a3}			
30	V_{REF0}	I/O	internally generated voltage may be left open or a capacitor, 100 nF, may be connected vs. GND to maintain compatibility with previous versions	
19	V_{REF1}	PD	no function, a capacitor, 100 nF, may be connected vs. GND to maintain compatibility with previous versions	
51	V_{REF2}	PD	no function, a capacitor, 100 nF, may be connected vs. GND to maintain compatibility with previous versions	

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference Section
62	V_{REF3}	PD	no function, a capacitor, 100 nF, may be connected vs. GND to maintain compatibility with previous versions	
JTAG Boundary Scan				
57	TCK	I	Test Clock.	4.2
58	TMS	I	Test Mode Select, internal pullup.	4.2
55	TDI	I	Test Data Input, internal pullup.	4.2
56	TDO	O	Test Data Output.	4.2
59	$\overline{\text{TDISS}}$	I	JTAG Boundary Scan Disable, active low, internal pullup (I_{TDISS} = -100µA (typ.)).	
Line Port Pins				
29	AIN0	I	Differential U interface input. Line port 0	3.2.1
28	BIN0	I	Differential U interface input. Line port 0	3.2.1
33	AOUT0	O	Differential U interface output. Line port 0	3.2.3
36	BOUT0	O	Differential U interface output. Line port 0	3.2.3
20	AIN1	I	Differential U interface input. Line port 1	3.2.1
21	BIN1	I	Differential U interface input. Line port 1	3.2.1
16	AOUT1	O	Differential U interface output. Line port 1	3.2.3
13	BOUT1	O	Differential U interface output. Line port 1	3.2.3
52	AIN2	I	Differential U interface input. Line port 2	3.2.1

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference Section
53	BIN2	I	Differential U interface input. Line port 2	3.2.1
47	AOUT2	O	Differential U interface output. Line port 2	3.2.3
44	BOUT2	O	Differential U interface output. Line port 2	3.2.3
61	AIN3	I	Differential U interface input. Line port 3	3.2.1
60	BIN3	I	Differential U interface input. Line port 3	3.2.1
2	AOUT3	O	Differential U interface output. Line port 3	3.2.3
5	BOUT3	O	Differential U interface output. Line port 3	3.2.3
Digital Interface				
7	CL15	I/O	Master Clock 15.36 MHz. All operations and the data exchange on the digital interface are based on this clock. CL 15 is set to an input at power-on. If a 15.36 MHz clock is generated by the internal PLL/ oscillator or if an external clock is provided at XIN then CL15 becomes an output and issues this clock. If the pin XIN is clamped to low or high then CL15 remains an input and an other device has to provide the 15.36 MHz clock.	3.2.1, 4.2
38	PDM0	O	Pulse density modulated output of the second-order sigma-delta ADC of line port 1	3.2.1, 4.2
39	PDM1	O	Pulse density modulated output of the second-order sigma-delta ADC of line port 2	3.2.1, 4.2

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference Section
40	PDM2	O	Pulse density modulated output of the second-order sigma-delta ADC of line port 3	3.2.1, 4.2
8	PDM3	O	Pulse density modulated output of the second-order sigma-delta ADC of line port 4.	3.2.1, 4.2
31	XDN0	I	For future use, leave pin open	
18	XDN1	I	For future use, leave pin open	
50	XDN2	I	For future use, leave pin open	
63	XDN3	I	For future use, leave pin open	
24	SDX	I	Interface for the transmit and control data. Up to eight lines can be multiplexed on SDX. Transmission and sampling is based on clock CL15 (15,36 MBit/sec).	3.3, 4.2
41	SDR	O	Level information for the detection of the awake tone. The four lines are multiplexed on SDR.	3.3, 4.2
27	ADDR	I	For future use, set to "1".	3.3
23	CODE	I	Select 2B1Q or 4B3T code. Code = low sets 2B1Q Code.	3.3, 3.2.3
25	$\overline{\text{RES}}$	I	Reset and power down of the entire IEC Quad AFE including PLL and all four line ports. Asynchronous signal, active low.	3.2.9
PLL				
9	XOUT	O	Crystal out. 15.36 MHz crystal is connected. Leave open if not used.	3.1.2
10	XIN	I	Crystal in. A synchronous 15.36 MHz clock signal or 15.36 MHz crystal is connected. Clamping XIN to either low or high sets CL15 to Input.	3.1, 3.1.2

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference Section
26	CLOCK	I	8 kHz or 2048 kHz clock as a time base of the 15.36 MHz clock.Connect to GND if not used.	3.1
22	PLLF	I	Select corner frequency of PLL Jitter Transfer function. Internal pullup resistor (I_{PLLF} = -100µA (typ.)).	3.1

2 System Integration

The Quad IEC AFE is optimized for line modules in the central office or access networks (LT function) together with the PEB 24901 Quad IEC DFE-T for 4B3T code or the PEB 24911 Quad IEC DFE-Q for 2B1Q code. The PEB 24911 Quad IEC DFE-Q is footprint compatible to the PEB 24901 Quad IEC DFE-T. This way, one board layout can be used for both line codes simply by putting the appropriate DFE.

2.1 Line Card Application

The Quad IEC AFE is controlled via the signal at pin SDX. The transmit data is transferred the same way.

The Quad IEC AFE can transmit either 2B1Q-data or 4B3T-data. Setting the pin CODE to low will result in 2B1Q code. For 4B3T code the pin CODE has to be tied to VDD.

The 15.36 MHz master clock is generated with a crystal oscillator and synchronized onto the PTT clock with an integrated PLL. Fig. 4 shows a 4 channel LT application for 2B1Q line code.

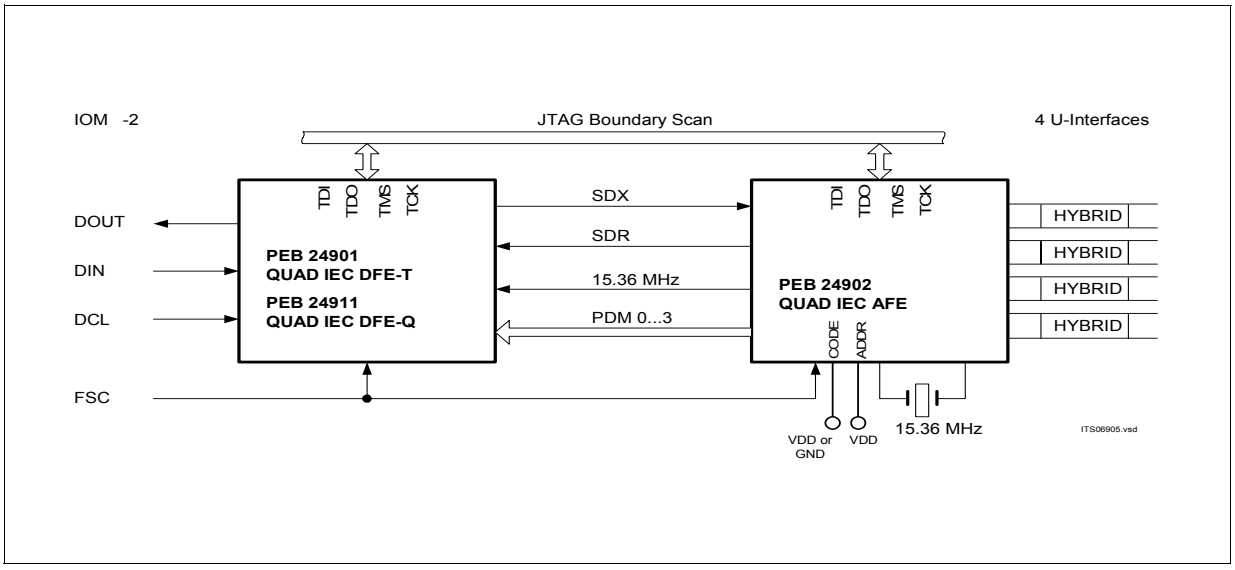


Figure 4 Connecting QAD IEC AFE/DFE-T or Q

Figure 5 gives an overview of an 8 channel linecard (2B1Q).

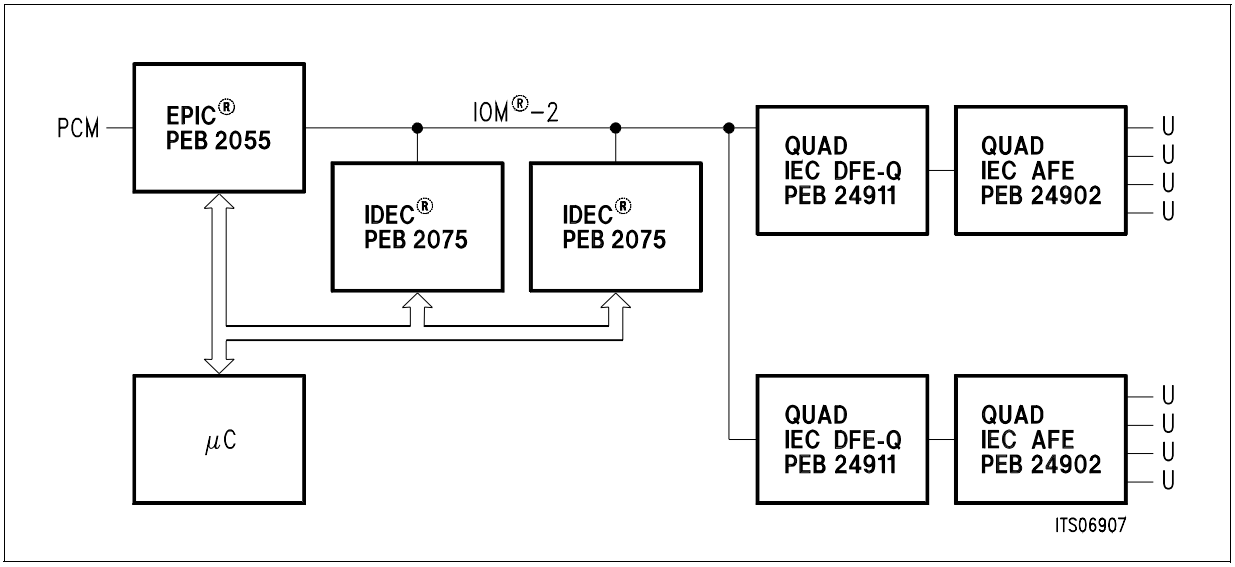


Figure 5 8 channel LT application (overview)

An 8 channel LT is built with two AFE/DFE sets. One Quad IEC AFE generates the master clock for all four devices. The PLL in the other Quad IEC AFE is passive.

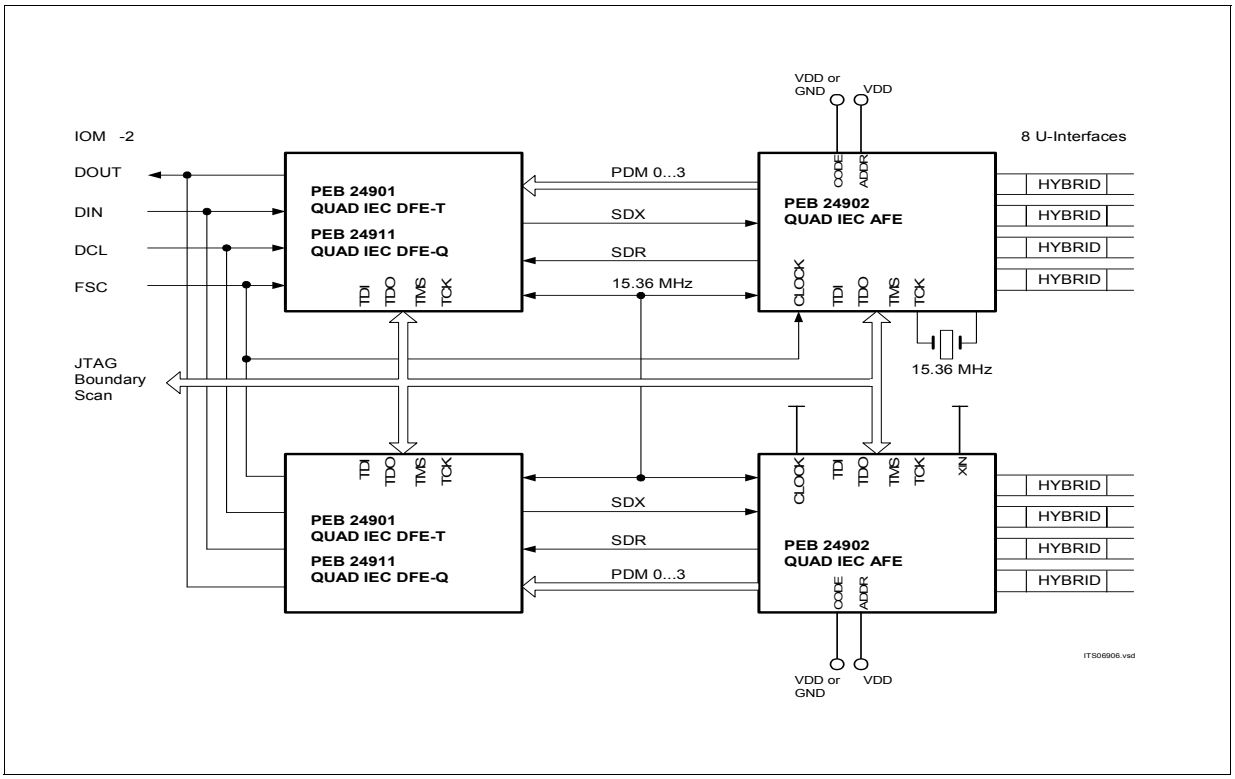


Figure 6 8 channel LT application

*Note: For linecards with 12 or more channels the 15.36 MHz Masterclock must not drive more than 3 inputs. The clocking scheme in **Figure 7** is recommended.*

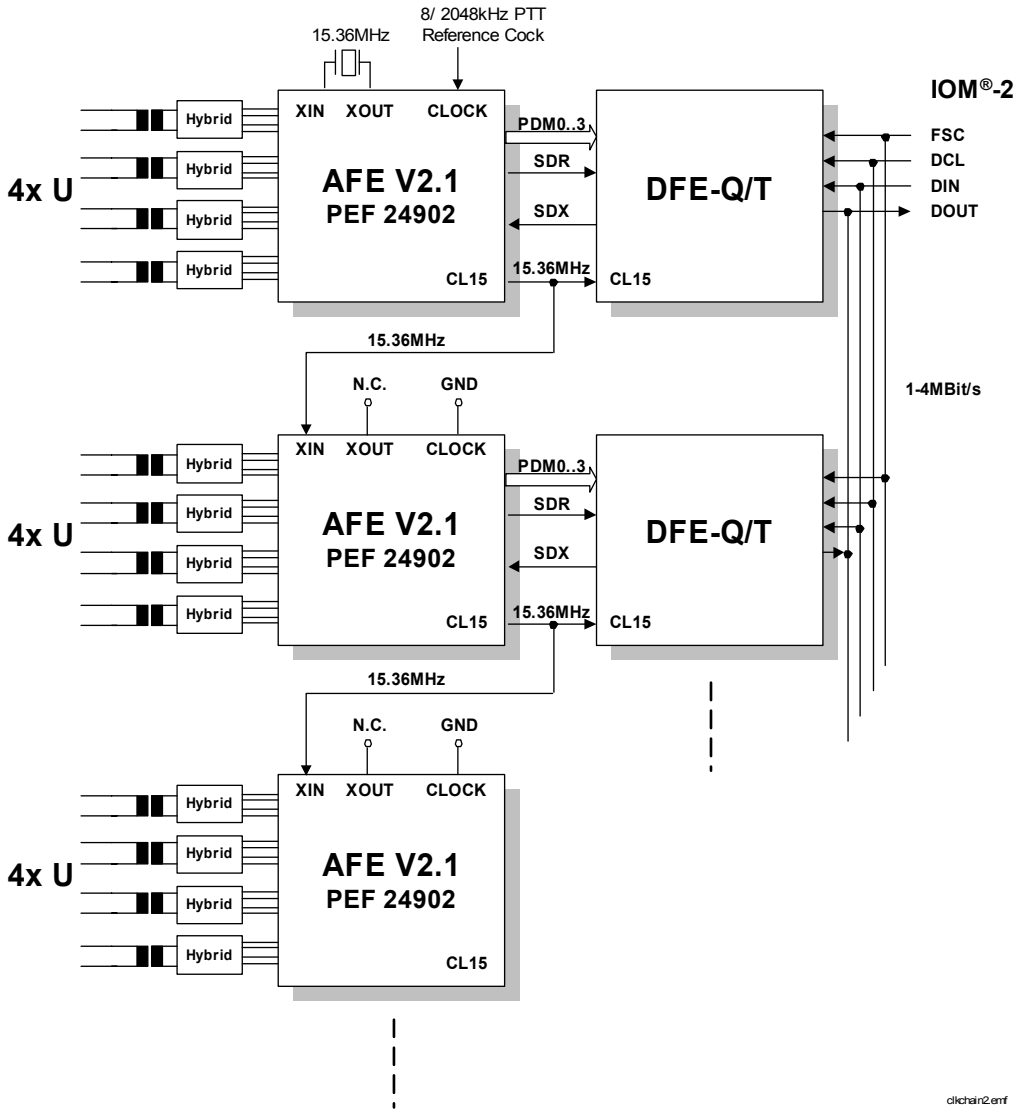


Figure 7 15.36 MHz Clock Distribution in Multichannel Linecards

3 Technical Description

3.1 Clock Generation

All timing signals are derived from a 15.36 MHz system clock. The 15.36 MHz clock can be provided by the Quad IEC AFE by a crystal-based PLL, which is synchronized to either an 8 kHz or a 2048 kHz clock at pin CLOCK. The frequency at pin CLOCK is detected automatically.

The PLL is set to the nominal frequency either by a POR or by a falling edge at the $\overline{\text{RES}}$ pin. When the reference clock (CLOCK) is applied, the PLL starts to synchronize.

The 15.36 MHz clock can also be provided externally at pin CL15 without making use of the internal PLL. In this mode the pin XIN must be tied to either VDD or GND. An internal power-on-reset circuitry assures that the pin CL15 is an input until a 15.36 MHz clock is detected at the output of the PLL/oscillator.

To enable error-free data transport to/from the Quad IEC DFE-T/Q, the clocks DCL and FSC from the IOM®-2-interface must be synchronous to the 15,36 MHz signal. Therefore it is recommended to use the same signal for FSC and as input to CLOCK pin at the Quad IEC AFE when the internal PLL is used to generate the 15.36 MHz clock.

If an other clock source is used for CLOCK, e.g. the 2048 kHz DCL, a common time base must be guaranteed. This is usually achieved if FSC is derived from DCL by dividing it directly by 256.

Any constant phase difference between the time bases of both clocks is possible, but the devices have currently been qualified and released only for using the same FSC signal for the Quad IEC DFE-T/Q and for Quad IEC AFE.

3.1.1 Specification of the PLL and the 15.36 MHz Master Clock (Pin CL15)

The PLL is based on a crystal connected to the pins XIN and XOUT. For synchronization of the 15.36 MHz clock up to 16 internal capacitances are connected to XIN and XOUT.

The loop filter of the PLL is of second order, therefore a sinusoidal input jitter with the angular frequency $\omega = 2\pi f$ at CLOCK is attenuated by the PLL according to the following formula:

$$H(j\omega) = \frac{\frac{2\delta}{\omega_r} j\omega + 1}{\left(\frac{j\omega}{\omega_r}\right)^2 + \frac{2\delta}{\omega_r} j\omega + 1}$$

H(jω) is the complex jitter transfer factor

$\omega_r = 2\pi f_r$ is the angular resonance-frequency of the PLL

δ is the damping factor of the PLL

The maximum phase difference between the external CLOCK and the internal reference, derived from the master clock, due to a sinusoidal input jitter with the angular frequency ω is given as 1 - H(jω). The magnitude of the jitter transfer function and of the phase difference are illustrated below:

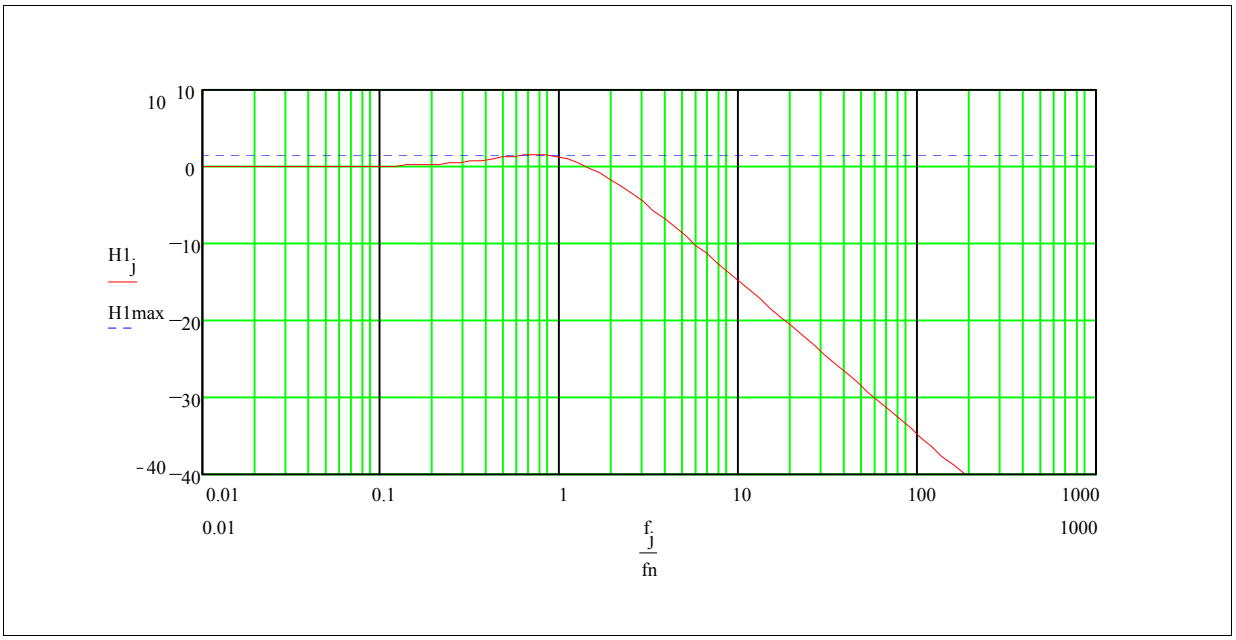


Figure 8 Jitter Transfer Gain in dB

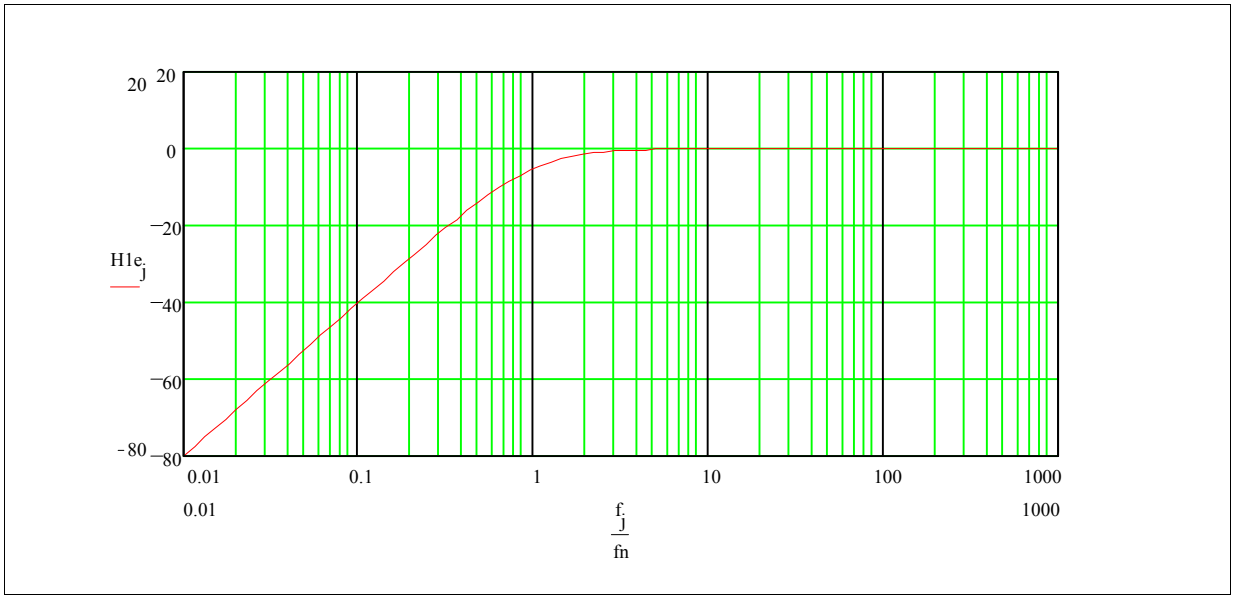


Figure 9 Maximum Phase Difference Due to Sinusoidal Input Jitter

If the input signal at pin CLOCK disappears being stuck to high or low, the PLL continues to generate the CL15 clock. In this case the PLL keeps the last setting. The accuracy of the frequency of CL15 degenerates in the long term only due to changes in temperature and ageing.

The resonance frequency can be set to two different values using the pin PLLF. PLLF tied to low sets the PLL to a low resonance frequency suited for applications in the Access Network. PLLF tied to high or left open results in a higher resonance frequency for accelerated synchronization. The PLLF pin has an internal pull-up resistor.

The PLL automatically determines whether the frequency at pin CLOCK is 8 kHz or 2048 kHz .

Table 2 PLL Characteristcs

Parameter	Limit Values			Unit
	min.	typ.	max.	
f_r resonance frequency, PLLF = low	1.7	2.0	2.3	Hz
f_r resonance frequency, PLLF = high	7	8	9	Hz
Damping factor	0.7	0.9	1.2	
H_{max} maximum jitter amplification	0.9	1.45	2.2	dB

Table 2 PLL Characteristcs (cont'd)

Parameter	Limit Values			Unit
	min.	typ.	max.	
Synchronization time of the PLL after power on and applying the reference at pin CLOCK, PLLF = low			8	sec
Synchronization time of the PLL after power on and applying the reference at pin CLOCK, PLLF = high			1	sec
Output Jitter at CL15 without any jitter in the CLOCK signal (peak-to-peak); jitter frequency > 800 Hz			2	ns
Output Jitter at CL15 with-out any jitter in the CLOCK signal (peak-to-peak) jitter frequency < 20 Hz			80	ns
Initial accuracy after the loss of the reference clock at CLOCK			0.5	ppm
Initial accuracy after power on	-50		50	ppm
Start-up time of the Oscillator with the crystal suggested below.		0.5	1	ms
Output current at XOUT during start-up		0.5	1	mA
Output current at XOUT after synchronization		0.5	1	mA

Table 3 PLL Input Requirements

Parameter	Limit Values			Unit
	min.	typ.	max.	
Accuracy of the reference at CLOCK to enable synchronization	-150	0	+150	ppm
Peak-to peak Jitter of the CLOCK signal during any 125 µsec period			70	ns
Peak-to-peak voltage of a sinusoidal external master clock provided at XIN	3.3			V_{pp}
Low time of the reference at CLOCK	130			ns
High time of the reference at CLOCK	130			ns
Pulse width of the 15MHz clock	26		39	ns

3.1.2 Specification of the Crystal

A crystal (serial resonance) has to be connected to XIN and XOUT which shall meet the following specification:

Table 4 Specification of the crystal

Parameter	Min	Typ	Max	Units
Nominal frequency		15.360000		MHz
Total frequency range	-150		+150	ppm
Operating frequency C_{Load} = 15 pF C_{Load} = 7 pF	 15.35770 -		 - 15.36230	 MHz MHz
Current		1	2	mA
Load capacitance	9.8		10.2	pF
Overall tolerance $\Delta f/f$			60	ppm
Resonance resistance R_r		30		Ohm
Shunt capacitance C_0			7	pF
Motional capacitance C_1	25			fF
Overall Pullability	+- 210			ppm

Note that the load capacitors are integrated in the PEB 24902. No additional capacitance has to be connected neither to XIN nor to XOUT. The crystal specifications shall meet the requirements given in **Table 4**.

A suitable type of crystal would be:

Vibrator:

Mode of vibration	DS	fundamental
Crystal cut	ATI	

Application hint: Parasitic capacitances at XIN and XOUT pin, e.g. due to board capacitances should be below 3 pF.

3.2 Analogue Line Port

The Quad IEC AFE Chip gives access to four line ports. The signal to be transmitted is issued differentially at pins AOUT0..3 and BOUT0..3. The input is differentially sampled at AIN0..3 and BIN0..3. Each line port consists of three main function blocks:

- the analogue-to-digital converter in the receive path
- the digital-to-analogue converter in the transmit path
- the output buffer in the transmit path

Furthermore a line port contains some special functions. These are:

- analogue test loop-back
- level detect function

3.2.1 Analogue-to-Digital Converter

A first order low pass anti alias filter is provided at the input of the ADC. The ADC is a sigma-delta modulator of second order using a clock rate of 15.36 MHz. During normal operation the ADC evaluates the signal at AINx and BINx. The ADC evaluates the signal at AOUTx and BOUTx while the analogue loop-back is activated.

The maximum peak input voltage between AINx and BINx is defined as the minimum input voltage that results in a continuous series of high or low at the PDMx pin. A larger input signal will be clipped. An increasing positive voltage at AINx - BINx will result in an increasing number of high states at the PDMx pin. Hence, the maximum positive voltage at AINx - BINx results in a series of high whereas the maximum negative voltage results in a series of low. The average percentage of high states obtained with a given input voltage is referred to as gain of the ADC. It is expressed in %/Volt. The ADC offset is the difference in % from the ideal 50 % high states with no input signal, transferred back to the input voltage using the ADC gain.

The maximum signal to noise ratio is achieved by signals of approximately 65% of the maximum peak input signal voltage. The signal to noise ratio is evaluated with a digital third order low pass filter applied to the digital data stream. The filter transfer function zeroes are at 80 kHz, 80 kHz and 160 kHz.

3.2.2 Range Function

In case the signal input is too high (low attenuation on short loops), the range function can be activated. The range function attenuates the received signal internally by 6 dB. The range function is activated by setting the RANGE bit on SDX to ONE.

Table 5 Specified Data of the Analogue-to-Digital Converter

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
Signal/Noise (sine wave 1.5 Vpp between AINx/BINx)	70	72		dB	range function deactivated, all line ports sending random 2B1Q pattern into 98 Ω load
Signal/(Noise+ Distortion) (sine wave 0.4 Vpp between AINx/BINx)	59.5	61.5		dB	range function deactivated, all line ports sending random 2B1Q pattern into 98 Ω load
Signal/(Noise+Distortion) (sine wave 1.5 Vpp between AINx/BINx)	65	68		dB	range function deactivated
Signal/(Noise+Distortion) (sine wave 2.0 Vpp between AINx/BINx)	60			dB	range function deactivated
Signal/(Noise + Distortion) (sine wave 3 Vpp between AINx/BINx)	60			dB	range function activated
Signal/Noise (sine wave 3 Vpp between AINx/BINx)	65	68		dB	range function activated, all line ports sending random 2B1Q pattern into 98 Ω load
Signal/(Noise + Distortion) (sine wave 4 Vpp between AINx/BINx)	50			dB	range function activated
Signal/(Noise+Distortion) (sine wave 4.6 Vpp between AINx/BINx)	35			dB	range function activated
DC offset voltage			35	mV	range function deactivated
DC offset voltage			70	mV	range function activated
ADC gain	28	33	38	%/V	range function deactivated
ADC gain	14	16.5	19	%/V	range function activated

Table 5 Specified Data of the Analogue-to-Digital Converter (cont'd)

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
Attenuation of the range function	5.45	6	6.25	dB	
Impedance between AINx and BINx	100			kΩ	
Input capacitance at AINx and BINx			3	pF	
Input voltage range at AINx and BINx	GND		VDD		
Common Mode Rejection Ratio	40			dB	f < 80 kHz
Power Supply Rejection Ratio	40			dB	f < 80 kHz
Power Supply Rejection Ratio	55			dB	80 kHz < f < 20 MHz
Anti Alias Filter Corner Frequency	1.1	1.6	2.3	MHz	

3.2.3 Digital-to-Analogue Converter

The output pulse is shaped by a special DAC. The DAC is optimized for excellent matching between positive and negative pulses and high linearity. It uses a fully differential switched capacitor approach. The staircase-like output signal of the DAC drives the output buffers. The shape of a DAC output signal is shown below, the peak amplitude is normalized to one. This signal is fed to an RC low pass of first order.

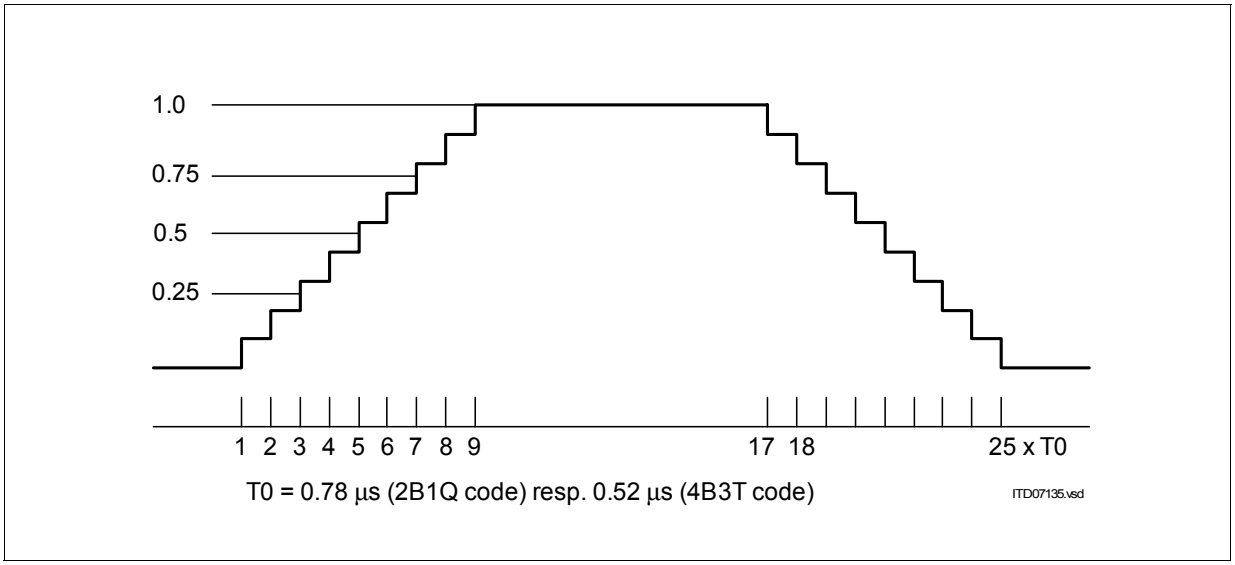


Figure 10 DAC Output for a Single Pulse

The duration of each pulse is 24 steps, with t = 0.78 µsec per step for 2B1Q code and 0.52 µsec per step for 4B3T code. The pulse rate is one pulse per 16 steps, e.g. 80 kHz for 2B1Q code and 120 kHz for 4B3T code. Thus, the subsequent pulses are overlapping for a duration of 8 steps.

The output stage consists of two identical buffers, operated in a differential mode. The buffers are optimized for:

– high output swing
– high linearity
– low quiescent current to minimize power consumption

The pulse mask for a single +3 2B1Q-pulse (+1 4B3T pulse) measured between AOUTx and BOUTx at a load of 98 Ω is given in **figure 11**. 98Ω represents the nominal load in a 2B1Q system when the line is substituted by a 135Ω register.

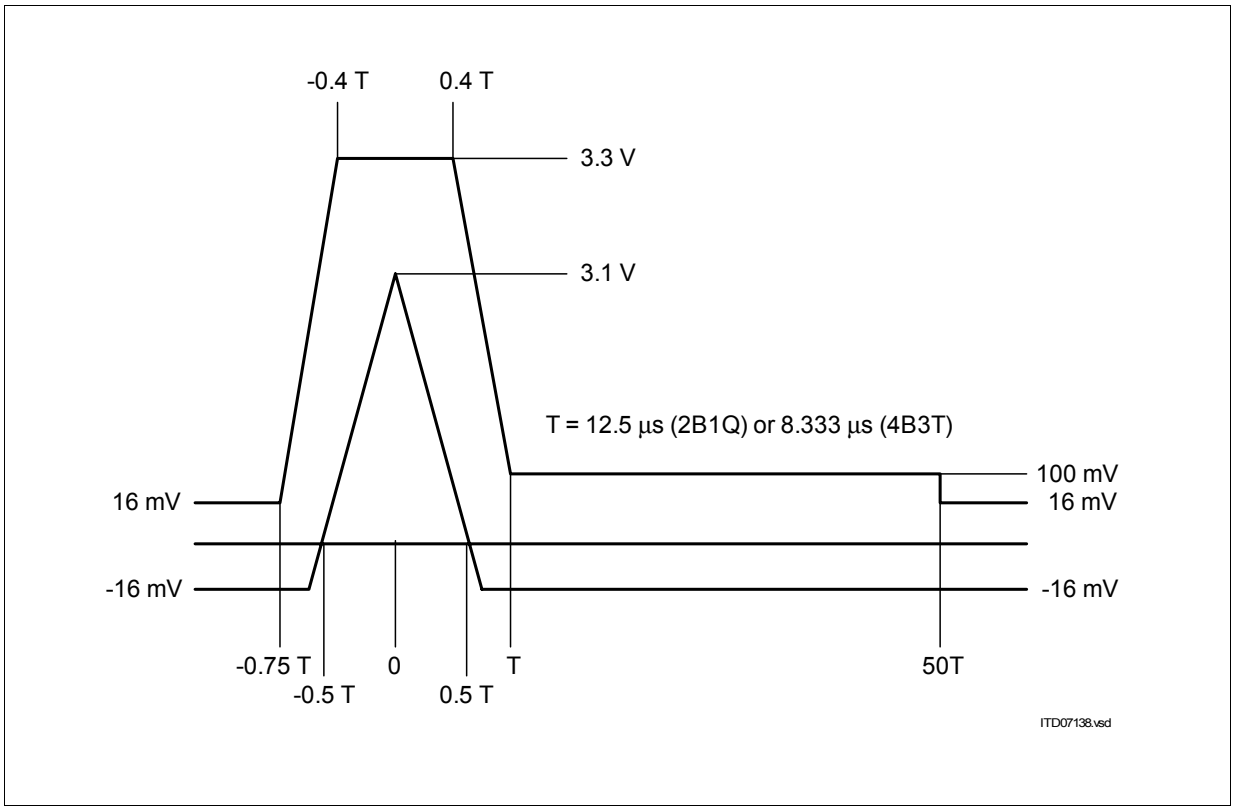


Figure 11 Pulse Mask for a Single +3 Pulse (not to scale)

The pulse mask for a +1 pulse is obtained by dividing all voltages in **figure 11** by 3. Negative pulses are described by the corresponding negative voltages.

The pulse as given in **figure 11** is passing a sample and hold circuit and a first order RC low pass filter. The sample period is 0.78 µs (2B1Q code) or 0.52 µs (4B3T code).

The switch is closed during 1/3 of the sample period. Hence, during 2 / 3 of the time, the output signal does not change. This way, a settling behavior is achieved which is slowed down by a factor of three compared to the cut-off frequency of the RC low pass filter.

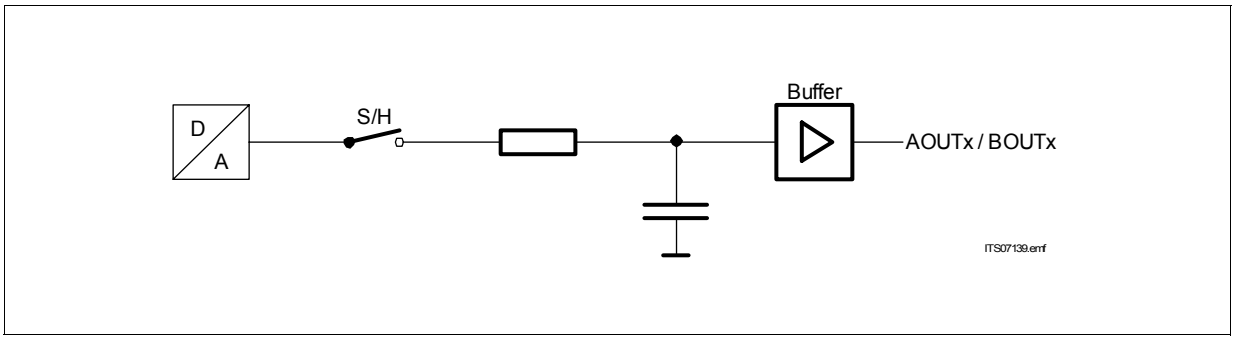


Figure 12 Output Pulse Sample and Hold with Filter

The relative amplitudes of the single steps of the pulse are given below. Step numbers are as referred to in **Figure 10**.

period after step no.	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
relative level	0	0.0625	0.1875	0.3125	0.4375	0.5625	0.6875	0.8125	0.9375

Steps 9 to 16 have a level of 1.0. The descending steps are defined as follows:

period after step no.	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**
relative level	0.9375	0.8125	0.6875	0.5625	0.4375	0.3125	0.1875	0.0625	0

Static tolerances of the step sizes are such that the pulse mask as given in **figure 11** is provided. Dynamic tolerances are such that the nonlinearity values as given in **table 6** are reached.

The signal to noise plus distortion ratio is measured using an evenly distributed but otherwise random sequence of +3, +1, -1, -3 (2B1Q code) or +1, 0, -1 (4B3T code) driving 98 Ω in series with a DC voltage. The output signal at AOUTx and BOUTx has to be weighted with a low pass filter from 0 to 80 kHz (2B1Q code) or 120 kHz (4B3T code), respectively, to get the specified sum of noise and total harmonic distortion as given in

Table 6 Specified Data of the Digital-to-Analogue-Converter

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
absolute peak voltage measured for a single +3 or -3 pulse between AOUTx and BOUTx	3.1	3.2	3.3	V	98 Ω load between AOUTx and BOUTx
absolute peak voltage measured for a single +1 or -1 pulse between AOUTx and BOUTx	1.033	1.067	1.1	V	98 Ω load between AOUTx and BOUTx
Common mode DC level	2.05	2.375	2.6	V	
Offset between AOUTx and BOUTx	- 35.5		35.5	mV	
ratio between ±1 and ±3 symbols	0.3283	0.3333	0.3383		
Variation of the signal amplitude measured over a period of 1 min.			1	%	
Peak-to-peak output jitter measured with a high-pass filter of 30 Hz cut-off frequency			1.3	nsec	jitter free 15.36 MHz clock
Peak-to-peak output jitter measured without the high-pass filter			6.5	nsec	
Signal / (Noise + Distortion) driving 98 Ω in series with ± 6.8 V DC	26			dB	
Signal / (Noise + Distortion) driving 98 Ω in series with ± 3.2 V DC	53			dB	
Signal / (Noise + Distortion) driving 98 Ω in series with ± 0.5 V DC	63	68		dB	
Corner frequency of the DAC RC low pass filter	420	620	900	kHz	
Output Impedance AOUTx/ BOUTx 1		2 6	4 12	Ω Ω	Power-Up Power-Down

table 6. Any linear mismatch between ±3 and ±1 symbols is cancelled for the S/N measurements.

3.2.4 External Hybrid and Transformer Parameters

For the 2B1Q-code and the 4B3T-code different external hybrids are suggested in **figures 13** and **14**. These hybrids will work correctly with an according transformer as described in **table 7**. Please note that table 7 gives typical transformer parameters and is not intended to be a complete transformer description. Transformer linearity must be such that no significant destortion is added to the signal passing the echo path from AOUTx/BOUTx to AINx/BINx.

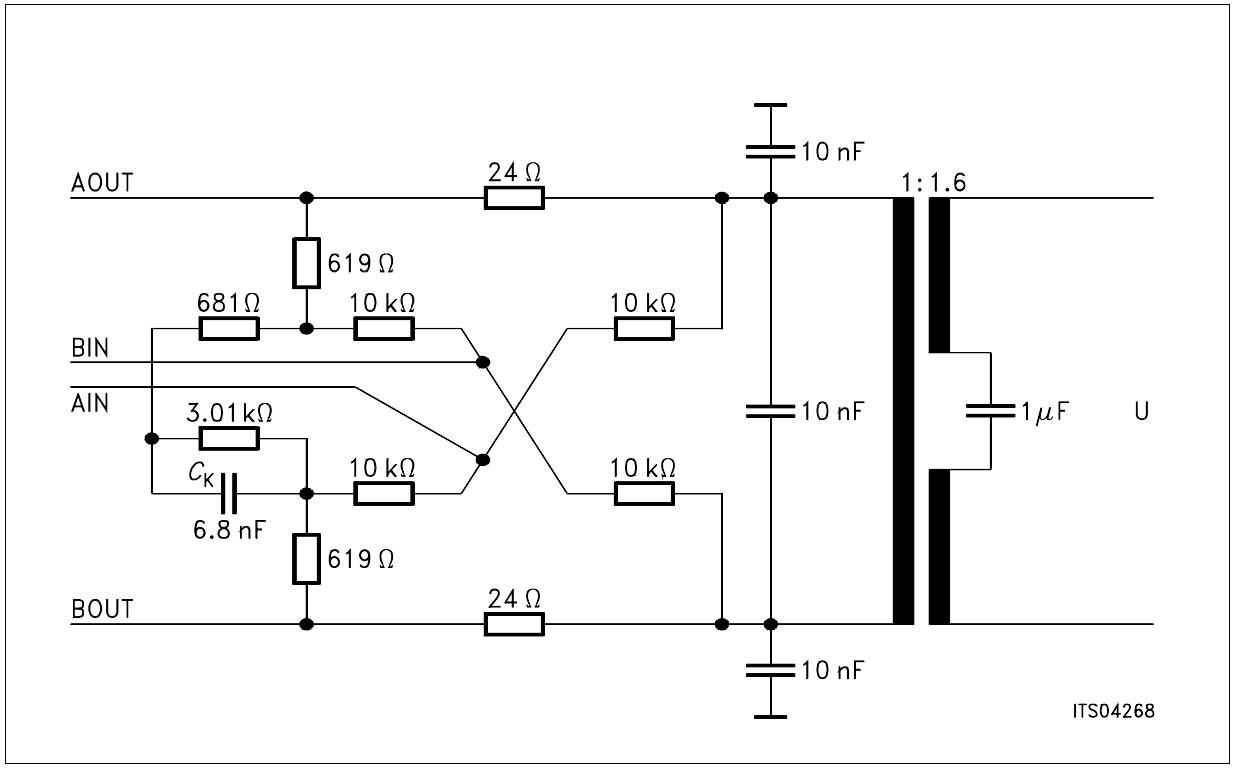


Figure 13 Example of External Hybrid Circuit for 2B1Q Code

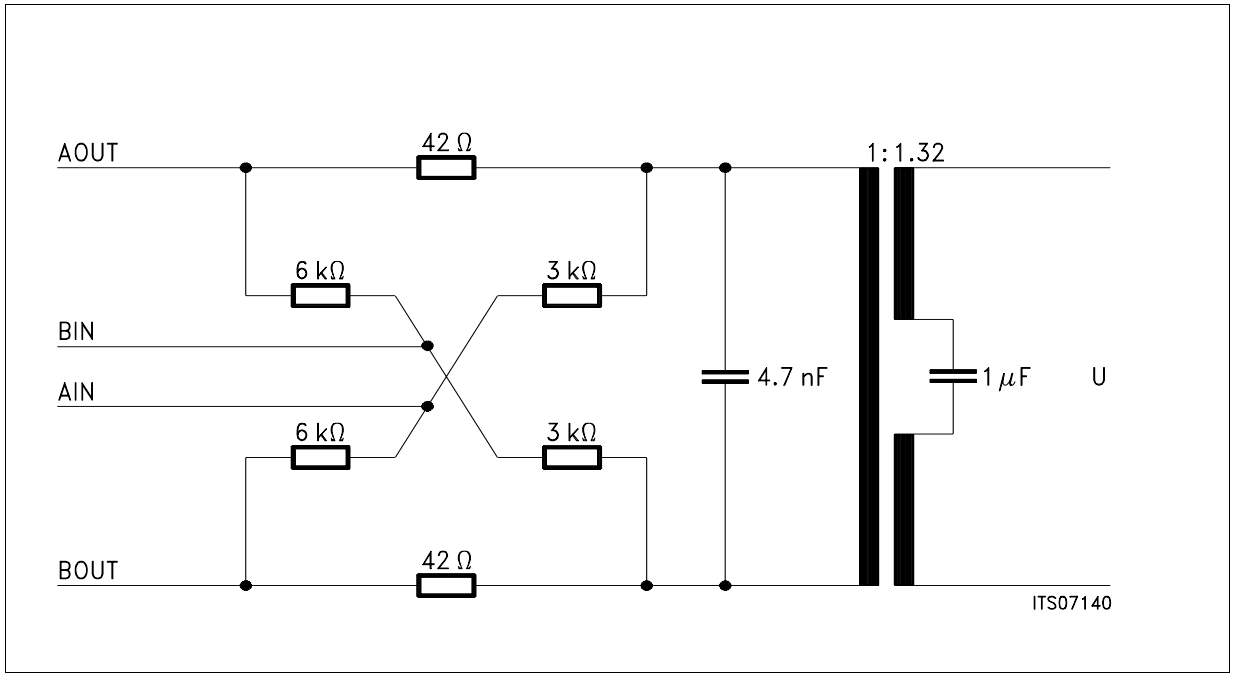


Figure 14 Example of External Hybrid Circuit for 4B3T Code

Table 7 Transformer Parameters

Parameter	Symbol	2B1Q	4B3T	Unit
Transformation ratio; Device side : Line side	n	1:1.6	1:1.32	
Main inductance of windings on the line side	L_H	14.5	7.9	mH
Leakage inductance of windings on the line side	L_S	≤ 90	≤ 50	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	≤ 100	≤ 75	pF
DC resistance of the windings on device side	$R_{Cu, B}$	2.8	1.9	Ω
DC resistance of the windings on line side	$R_{Cu, L}$	2.7	1.3	Ω

3.2.5 Analogue Loop-back Function

The loop-back bit (LOOP) set to ONE on SDX activates an internal analogue loop-back. This loop-back is closed near the U interface. Signals received on AINx / BINx will neither be evaluated nor recognized by the ADC. The output signal is attenuated by 17 dB and fed to the inputs of the ADC and level detect circuit instead. It is still available at AOUTx / BOUTx. **Figure 15** shows a schematic of the loop-back function.

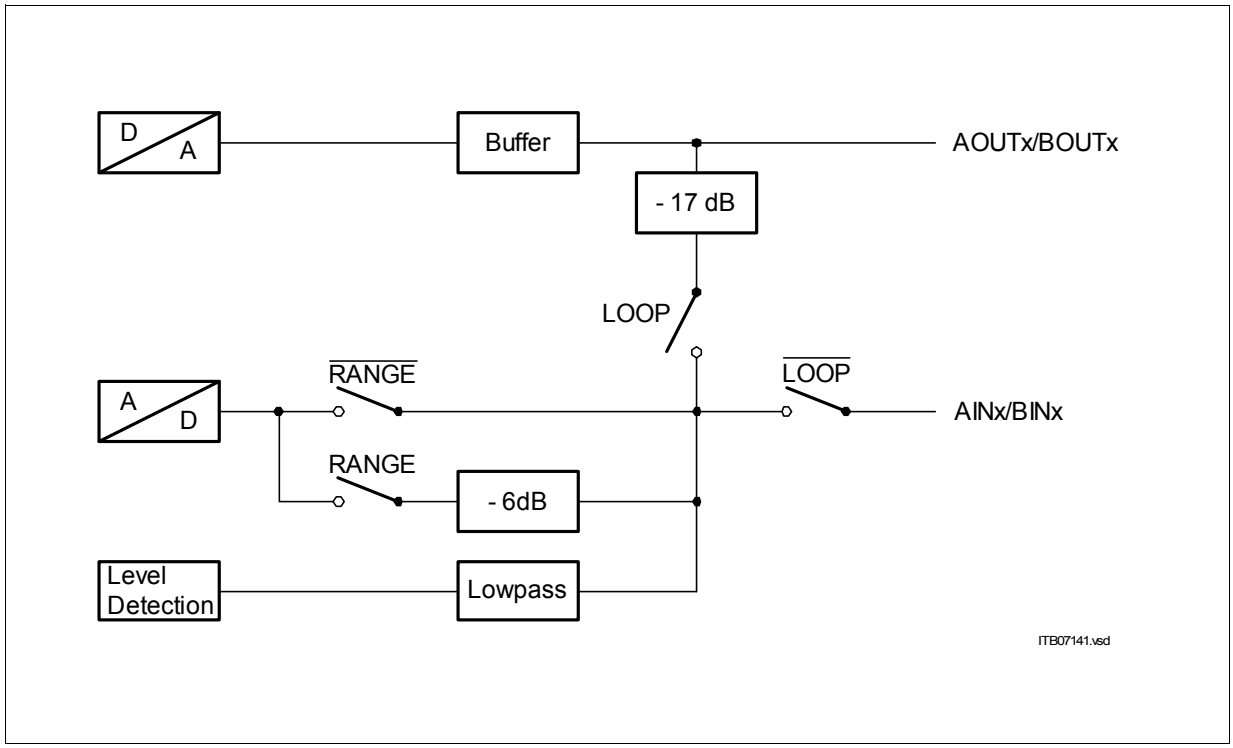


Figure 15 Block Diagram of Special Functions in the Quad IEC AFE

3.2.6 Level Detect

The level detect circuit evaluates the differential signal between AINx and BINx. Level detect is not affected by the range setting nor by the analog loop-back. It is also active during power down. The level detection is preceded by a first order low pass filter.

The detected level is communicated to the Quad IEC DFE on SDR. The detected level is updated every 12.5 µsec (2B1Q) or every 8.33 µsec (4B3T). If the input signal exceeds the threshold once during this time, the level bit is set to ONE, otherwise it is set to ZERO. The level bit is repeated on SDR during the whole time slot associated with the corresponding line port.

Table 8 Specified Data of the Level Detection Circuit

Parameter	Limit Values			Unit
	min.	typ.	max.	
Cut-off frequency of the input filter	90	160	230	KHz
Threshold of level detect (2B1Q)	4		20	mV
Threshold of level detect (4B3T)	10		30	mV
DC level of level detect (common mode level)	0		3	V

3.2.7 Power down

Transmit path, receive path and auxiliary functions of the analog line port are switched to a low power consuming mode when the power down function is activated. This implies the following:

– The ADC: The relevant pin PDMx is tied to GND.
– The DAC and the output buffer:The pins AOUTx BOUTx are tied to GND.
– The internal DC voltage reference is switched off.
– The range and the loop functions are deactivated.

The digital interface, the PLL, and the level detection are not affected by the powerdown.

3.2.8 Power-on-Reset (POR)

When applying power to the Quad IEC AFE an internal power-on-reset is generated to reset the PLL/oscillator* and to set CL15 to an input. If a 15.36 MHz clock is generated by the internal PLL/oscillator or if an external clock is provided at XIN then CL15 becomes an output and issues this clock.

If the supply voltage starts from a VDD voltage below 1.0V the AFE guarantees proper POR function with the restriction that the rising V_{DD} slope has to be minor 5V/4µs.
The POR function is enabled again if the supply voltage V_{DD} drops below 1.0V for a minimum period of 80ns (see figure 16 and table 9).

** Note: The RES pin must be at "1" level during POR to enable the reset of the PLL/oscillator.*

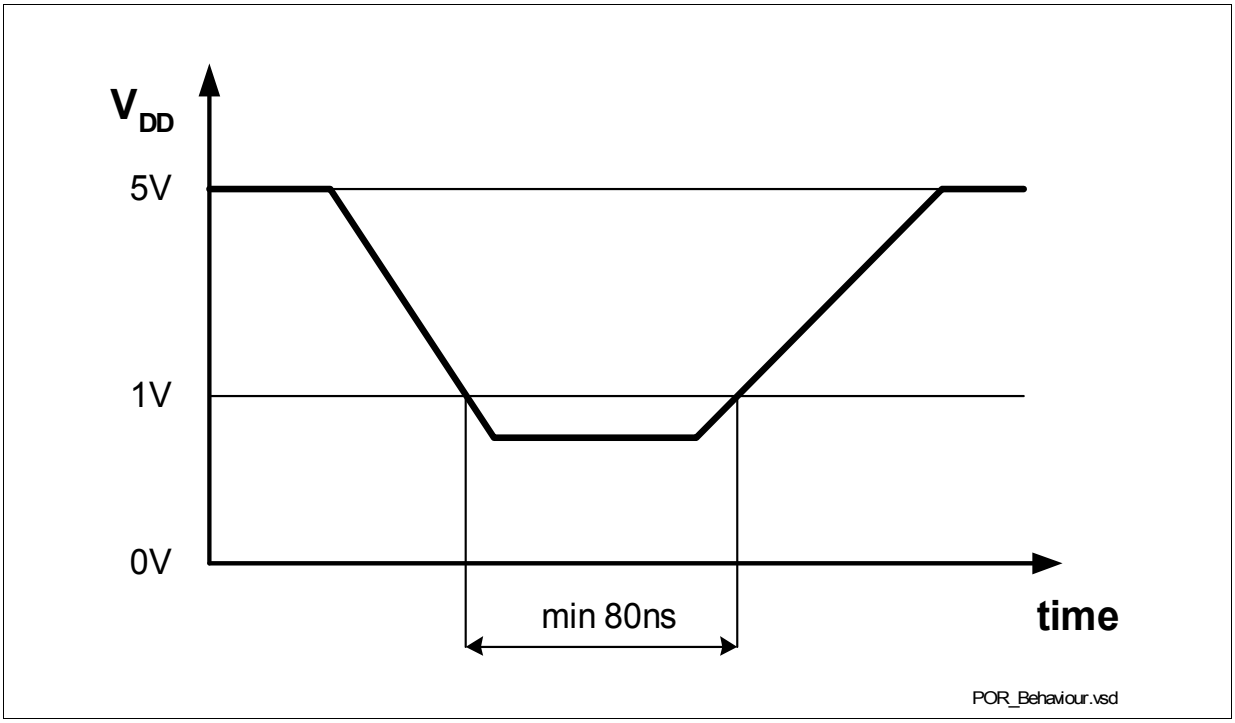


Figure 16 Power-on-reset behaviour of the AFE V1.2 after V_{DD} collapse

Table 9 Parameters for POR activation

Parameter	Limit Values			Unit
	min.	typ.	max.	
Maximum V_{DD} slope (rising or falling)			5V/ 4µs	
POR enable threshold	1.0		4.5	V
V_{DD} -below-1V-time	80			ns

3.2.9 Reset

The reset is activated by setting pin $\overline{\text{RES}}$ to low. The following functions are reset:

- The reset activates the powerdown of all line ports.
- The data on SDX is ignored during reset.
- SDR is set to low
- The range and the loop functions of all line ports are deactivated
- On a falling edge at the $\overline{\text{RES}}$ pin, the PLL is reset to it's nominal frequency and starts to resynchronize after 130 ns.
  Note: A running 15.36 MHz CL15 clock is required for this function.

All settings are maintained until $\overline{\text{RES}}$ is high and the digital interface is synchronized.

3.3 Digital Interface

On the digital interface transmit and receive data is exchanged as well as control information for the start-up procedure. The ADC output is transferred to the Quad IEC DFE T or Quad IEC DFE Q on the signals PDM0..PDM3. The timing of all signals in 2B1Q mode as well as 4B3T mode is based on the 15.36 MHz clock which is provided by the Quad IEC AFE.

The transmit data, powerup/down, range function and loopback are transferred on SDX, and the level status on SDR for all line ports. Eight time slots contain the data for up to eight line ports. The Quad IEC AFE operates in slots 0,2,4,6. The remaining slots are reserved for future use. The allocation of these time slots is done by the ninth time slot, a 24 bit synch. word on SDX, that consists of all ZEROs. The other time slots with transmission data start with a ONE. Therefore the first ONE after at least 24 subsequent ZEROs must be the first bit of time slot no. 0. This information is also used to determine the status of synchronization of the digital interface after reset.

The line code independent data on SDX:

$\overline{\text{NOP}}$: The no-operation-bit is set to ZERO if none of the control bits (PDOW, RANGE and LOOP) shall be changed. The values of the control bits of the assigned line port is latched. The states of the control bits on SDX are ignored, they should be set to ZERO to reduce any digital cross-talk to the analog signals.

The NOPQ bit is set to ONE if at least one of the control bits shall be changed. In this case all control bits are transmitted with their current values.

PDOW: If the PDOW bit is set to ONE, the assigned line port is switched to powerdown. Otherwise it is switched to powerup.

RANGE: RANGE = ONE activates the range function, otherwise the range function is deactivated. "Range function activated" refers to high input levels.

LOOP: LOOP = ONE activates the loop function, i.e. the loop is closed. Otherwise the line port is in normal operation.

SY: First bit of the time slots with transmission data. For synchronization and bit allocation on SDX and SDR, SY is set to ONE.

NT: This bit is for future use. It is set to"0" by the existing DFEs.

"0": reserved bit. Reserved bits are currently not defined and shall be set to ZERO. Some of these bits may be used for test purposes or can be assigned a function in later versions.

3.3.1 Frame structure on the Digital Interface in the 2B1Q Mode

The 192 available bits during a 80 kHz period (related to the 15.36 MHz clock) are divided into the 9 slots of which 8 slots are 21 bits long used for data transmission.

The status on SDR is synchronized to SDX. Each time slot on SDR carries the corresponding LD bit during the last 20 bits of the slot.

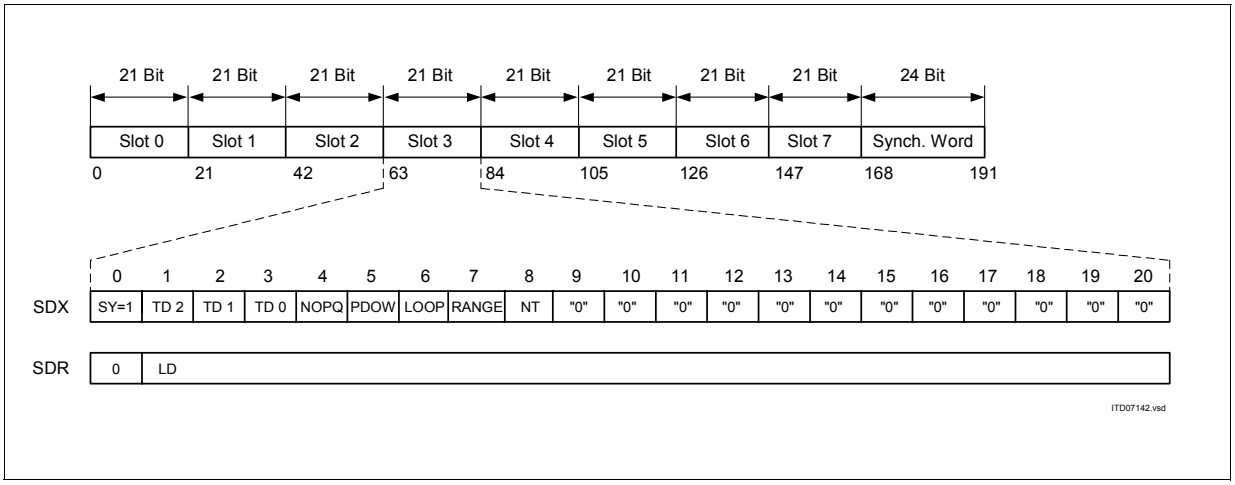


Figure 17 Frame Structure on SDX and SDR in 2B1Q Mode

The 2B1Q data is coded with the bits TD2, TD1, TD0:

Table 10 Coding of the 2B1Q data (AOUTx/BOUTx)

2B1Q Data	TD2	TD1	TD0
0	„1“	„don´t care“	„don´t care“
– 3	0	0	0
– 1	0	0	1
+ 3	0	1	0
+ 1	0	1	1

3.3.2 Frame structure on the Digital Interface in the 4B3T mode

The 128 available bits during a 120 kHz period (related to the 15.36 MHz clock) are divided into 9 slots of which 8 slots are 13 bits long used for data transmission. The status on SDR is synchronized to SDX. Each time slot on SDR carries the corresponding LD bit during the last 12 bits of the slot.

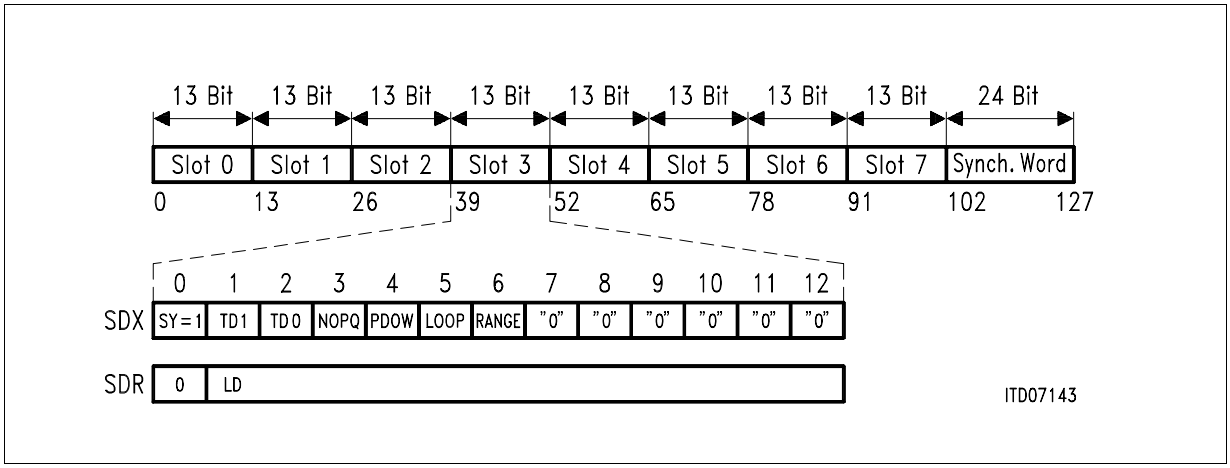


Figure 18 Frame Structure on SDX/SDR in 4B3T Mode

The 4B3T data is coded with the bits TD1, TD0:

Table 11 Coding of the 4B3T data pulse (AOUTx/BOUTx)

4B3T Data Pulse	TD1	TD0
0	0	0
+ 1	1	0
– 1	1	1

3.3.3 Propagation Delay in transmit direction

The start of the transmit pulse is defined as given in **Figure 19**:

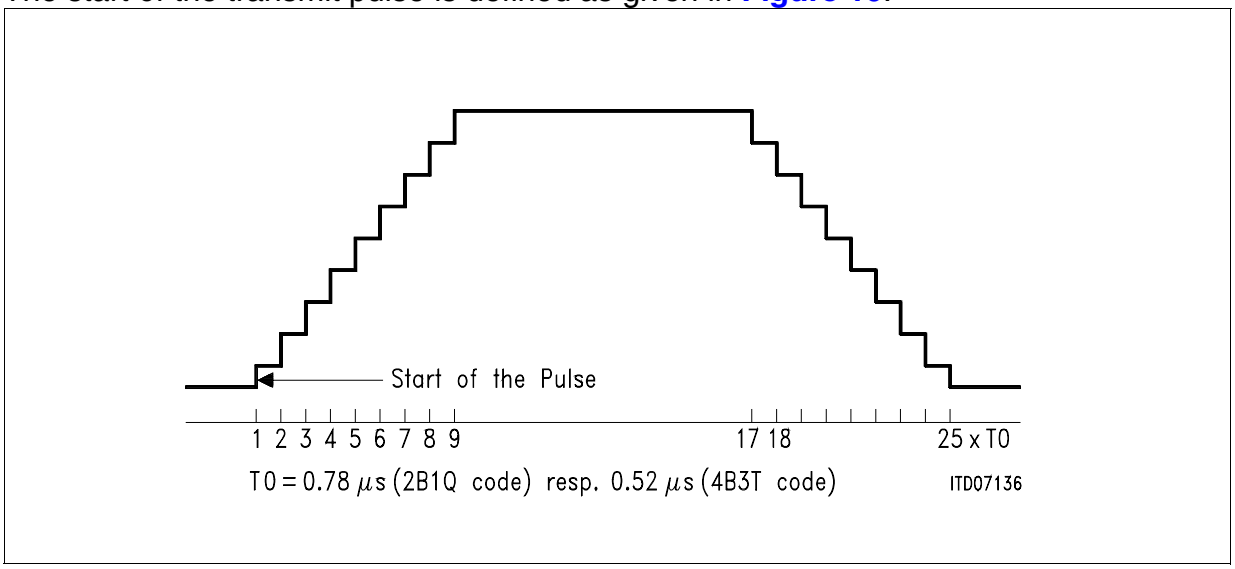


Figure 19 Definition of Transmit Pulse Start

The delay in transmit direction depends on the slot x on SDX. The pulses on the four lines are equally spaced in time while the transmit bits on SDX are not. The delay is defined as the time from the end of last bit of the slot x on SDX until the start of the pulse at AOUTx/BOUTx as given in figure 19. The delay is (3x + 27) *65 ns.

3.4 Boundary Scan Test Controller

The Quad IEC AFE provides a boundary scan support for a cost effective board testing. It consists of:

– Complete boundary scan for 11 signals (pins) according to IEEE Std. 1149.1 specification.
– Test access port controller (TAP)
– Four dedicated pins (TCK, TMS, TDI, TDO)
– One 32-bit IDCODE register
– pin $\overline{\text{TDISS}}$ tied to low disables the complete Boundary Scan Test Controller

Boundary Scan

The following pins are included in the boundary scan:
ADDR, CL15, CLOCK, CODE, PDM0, PDM1, PDM2, PDM3, $\overline{\text{RES}}$, SDR, SDX

Depending on the pin functionality one, two or three boundary scan cells are provided.

Table 12 Pin Types and Boundary Scan Cells

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	input
Output	2	output, enable
I/O	3	input, output, enable

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

Table 13 Sequence of Pins in the boundary scan

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells	Default value TDI —>
1	7	CL15	I/O	3	0 0 0
2	8	PDM3	O	2	1 0
3	23	CODE	I	1	0
4	24	SDX	I	1	0
5	25	$\overline{\text{RES}}$	I	1	0
6	26	CLOCK	I	1	0
7	27	ADDR	I	1	0

Table 13 Sequence of Pins in the boundary scan (cont'd)

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells	Default value TDI —>
8	38	PDM0	O	2	0 0
9	39	PDM1	O	2	0 0
10	40	PDM2	O	2	1 0
11	41	SDR	O	2	0 1

TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

The following instructions are executable.

Table 14 TAP controller instructions

Code	Instruction	Function
000	EXTEST	External testing
001	INTEST	Internal testing
010	SAMPLE/PRELOAD	Snap-shot testing
011	IDCODE	Reading ID code
11X	BYPASS	Bypass operation

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 001 (INTEST) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

Version	Device Code	Manufacturer Code		Output
0011	0000 0000 0010 0110	0000 1000 001	1	--> TDO

Note: Note:In the state "test logic reset" the code "0011" is loaded into the instruction code register.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

4 Digital Interface

Unless otherwise specified, the static and dynamic limits apply over a supply voltage range from 4.75 to 5.25 V and over the temperature range as specified in **section 7.2**.

4.1 Static Requirements

Table 15 Static Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High level input voltage	V_{IH}	2.4		V_{DD} + 0.3	V	
Low level input voltage	V_{IL}	– 0.3		0.8	V	
Low level input leakage current	V_{IL}	– 10			µA	V_{IN} = GND
High level input leakage current	I_{IH}			10	µA	V_{IN} = VDD
High level output voltage (Pin CL15)	V_{OH}	4.4			V	I_{OH} = 5 mA
High level output voltage (all other outputs)	V_{OH}	4.0			V	I_{OH} = 1 mA
Low level output voltage	V_{OL}			0.33	V	I_{OL} = 1 mA
Input capacitance	C_{IN}			10	pF	

The AC characteristics of the AFE-interface pins are optimized to fit to DFE-Q/T Versions 1.1/1.2/1.3/2.1 if the following loads are no exceeded. If DFE-Q/T of versions 1.x are used, it is required, that both devices are supplied by the same 5 Volt source (VDD/ GND).
No intermediating circuitry shall be inserted when connecting the AFE to DFE-Q/T.

Table 16 Interface Signals of AFE and DFE-Q/DFE-T

Pin	Signal Driving Device	Max. Capacitve load
CL15	AFE	50 pF
SDR	AFE	20 pF
PDM0..3	AFE	20 pF
SDX	DFE-T/DFE-Q	20 pF

4.2 Boundary Scan Timing

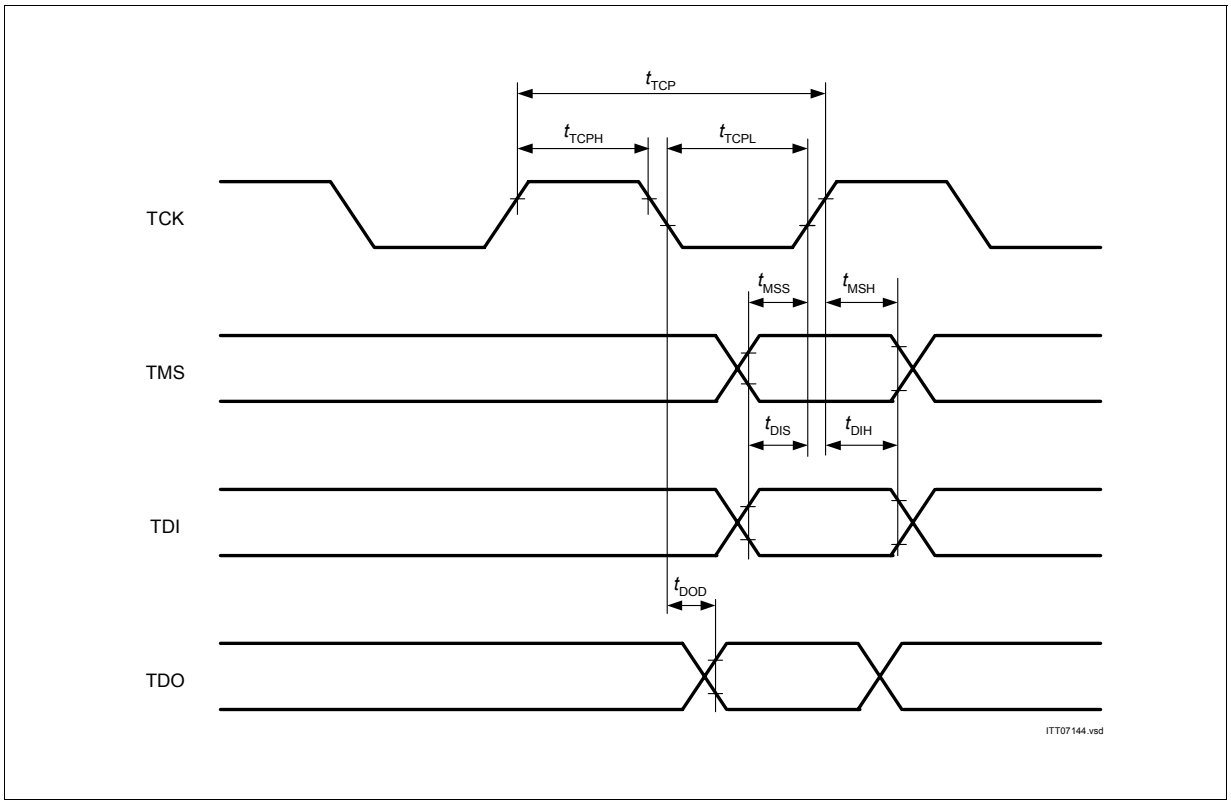


Figure 20 Boundary Scan Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
test clock period	t_{TCP}	160	-	ns
test clock period low	t_{TCPL}	70	-	ns
test clock period high	t_{TCPH}	70	-	ns
TMS set-up time to TCK	t_{MSS}	30	-	ns
TMS hold time from TCK	t_{MSH}	30	-	ns
TDI set-up time to TCK	t_{DIS}	30	-	ns
TDI hold time from TCK	t_{DIH}	30	-	ns
TDO valid delay from TCK	t_{DOD}	-	60	ns

5 Power Supply

5.1 Supply Voltages

VDD_{d1} to GND_{d1} = +5V ±0,25V
VDD_{d2} to GND_{d2} = +5V ±0,25V
VDD_{a1} to GND_{a1} = +5V ±0,25V
VDD_{a2} to GND_{a2} = +5V ±0,25V
VDD_{a3} to GND_{a3} = +5V ±0,25V
VDD_{a4} to GND_{a4} = +5V ±0,25V

The following blocking circuitry is suggested.

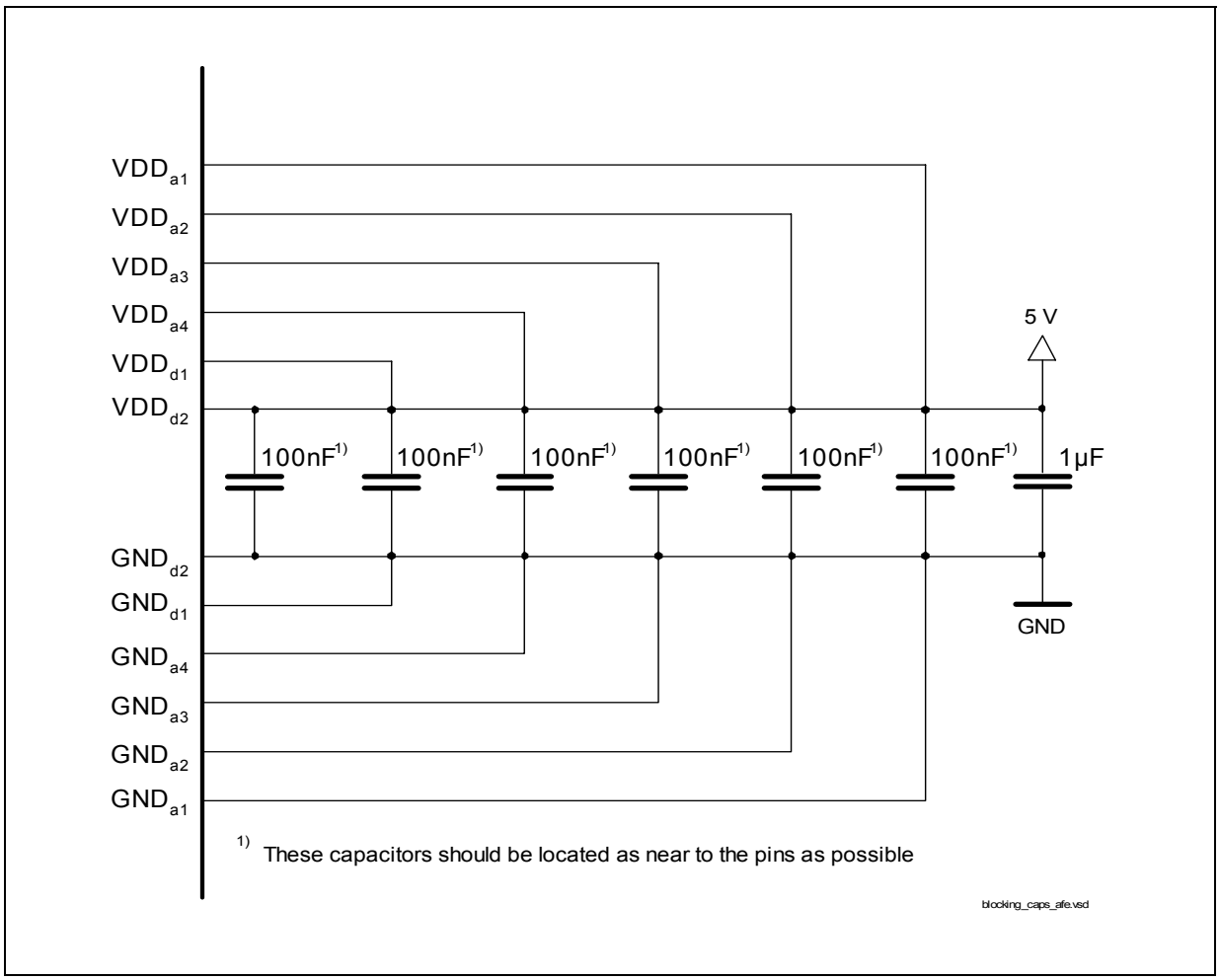


Figure 21 Power Supply Blocking

5.2 Power Consumption

All measurements with random 2B+D data in active states, 5V (0°C - 70°C).

Table 17 Power Consumption (2B1Q mode)

Parameter	Symbol	Limit Values			Unit	Comment
		min.	typ.	max.		
98 Ω load at AOUTx/BOUTx			725	840	mW	all line ports are in power up
98 Ω load at AOUTx/BOUTx			200	250	mW	one line port is in power up
All inputs are tied to V_{DD} or GND			25	50	mW	all line ports are in power-down

Table 18 Power Consumption (4B3T mode)

Parameter	Symbol	Limit Values			Unit	Comment
		min.	typ.	max.		
172 Ω load at AOUTx/BOUTx			665	775	mW	all line ports are in power up
172 Ω load at AOUTx/BOUTx			185	235	mW	one line port is in power up
All inputs are tied to V_{DD} or GND			25	50	mW	all line ports are in power-down

6 Maximum Ratings

Stresses above those listed in **table 19** may cause permanent damage to the device. Exposure to conditions beyond those indicated in **Section 5.1** of this specification may affect device reliability.

This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied. It is not implied, that more than one of these conditions can be applied simultaneously.

Table 19 Maximum ratings

Parameter	Limit Values		Unit
	min.	max.	
positive Supply Voltage		7.0	V
Voltage applied at any input	-0.3	VDD + 0.3 max. 7.0	V
Voltage applied at at the line port outputs	-0.3	VDD + 0.3 max. 7.0	V
Voltage between GNDx to any other GNDx		0.3	V
Voltage between VDDx to any other VDDx		0.3	V
Maximum surge Voltage applied at the line port inputs		ESD hardness according to MIL-Standard 883d Method 3015.7	

Line Overload Protection

The maximum input current (under over-voltage conditions) is given as a function of the width of a rectangular input current pulse. For the destruction current limits refer to **figure 22**:

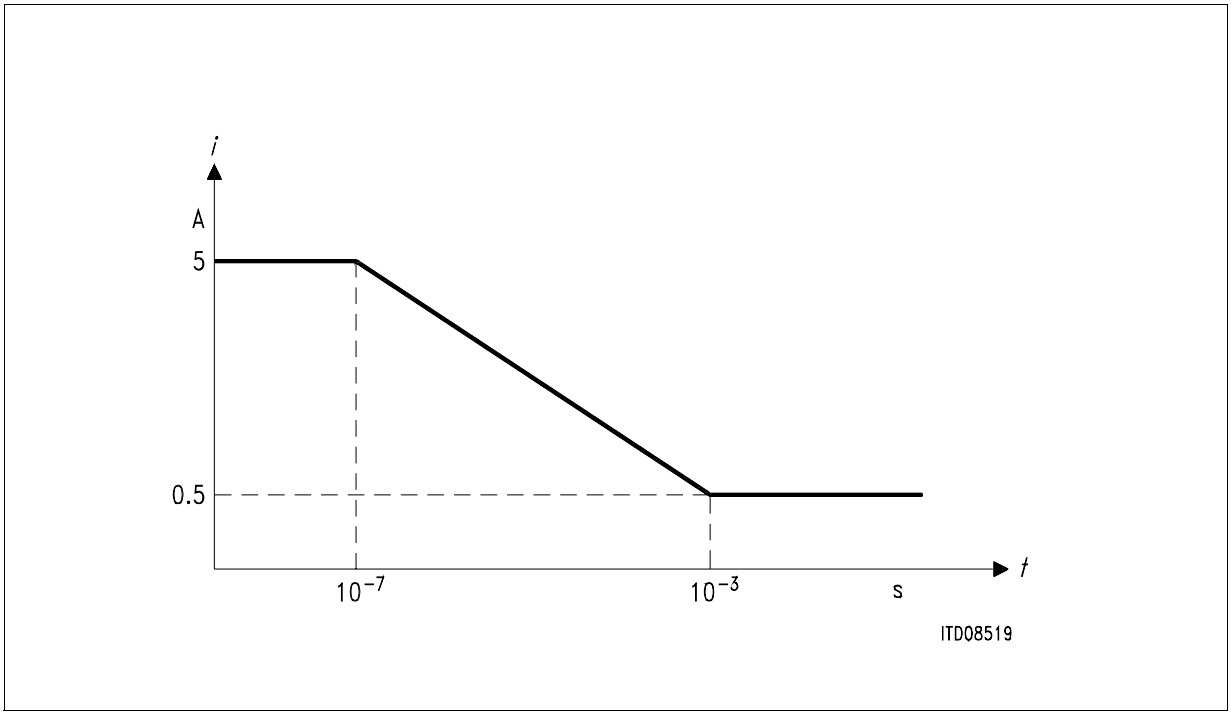


Figure 22 Maximum Line input current

7 Environmental Requirements

7.1 Storage and Transportation

The rated (limited capability) storage and transportation temperature range prior to printed board assembly shall be as follows:

- 65 to +150°C (without supply voltage)

7.2 Operating Ambient

The operating ambient temperature for standard and extended temperature versions shall be within the limits as follows:

PEB 24902	0 °C to +70 °C	(standard version)
PEF 24902	– 40 °C to +85 °C	(extended temperature range version)

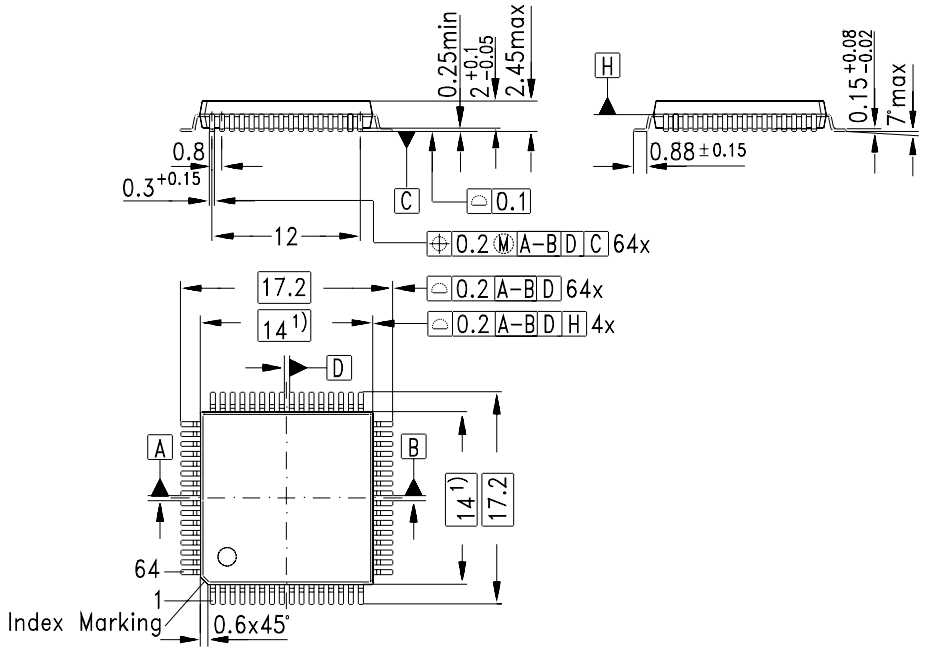
7.3 Thermal Contact Resistance

The thermal contact resistance is:

R_{THU} (silicon -environment): 55 Kelvin/Watt

8 Package Outlines

Plastic Package, P-MQFP-64-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

Published by Infineon Technologies AG