HIGH-SPEED 4K x 9 SYNCHRONOUS DUAL-PORT RAM

IDT7099S

Integrated Device Technology, Inc.

FEATURES:

- High-speed clock-to-data output times
  — Military: 20/25/30ns (max.)
  — Commercial: 15/20/25ns (max.)
- Low-power operation
  — IDT7099S
   Active: 900 mW (typ.)
   Standby: 50 mW (typ.)
- Architecture based on Dual-Port RAM cells
  — Allows full simultaneous access from both ports
  — Independent bit/byte Read and Write inputs for control functions
- Synchronous operation
  — 4ns setup to clock, 1ns hold on all control, data, and address inputs
  — Data input, address, and control registers
  — Fast 15ns clock to data out
  — 20ns cycle times, 50MHz operation
- Clock enable feature
- Guaranteed data output hold times
- Available in 68-pin PGA, 68-pin PLCC, and 80-pin TQFP
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7099 is a high-speed 4K x 9 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short realized cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts. Changing data direction from reading to writing normally requires one dead cycle.

These Dual-Ports typically operate on only 900mW of power at maximum high-speed clock-to-data output times as fast as 15ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT7099 is packaged in a 68-pin PGA, 68-pin PLCC, and a 80-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM
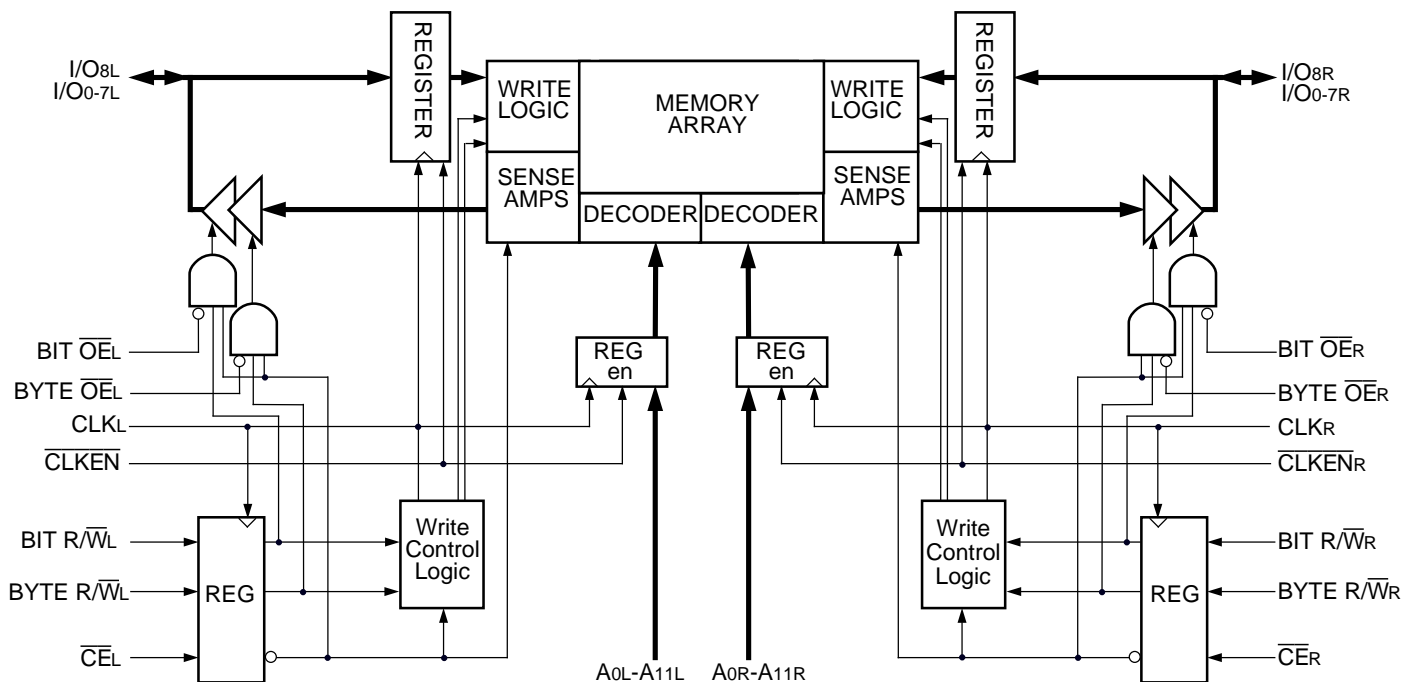
3007 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

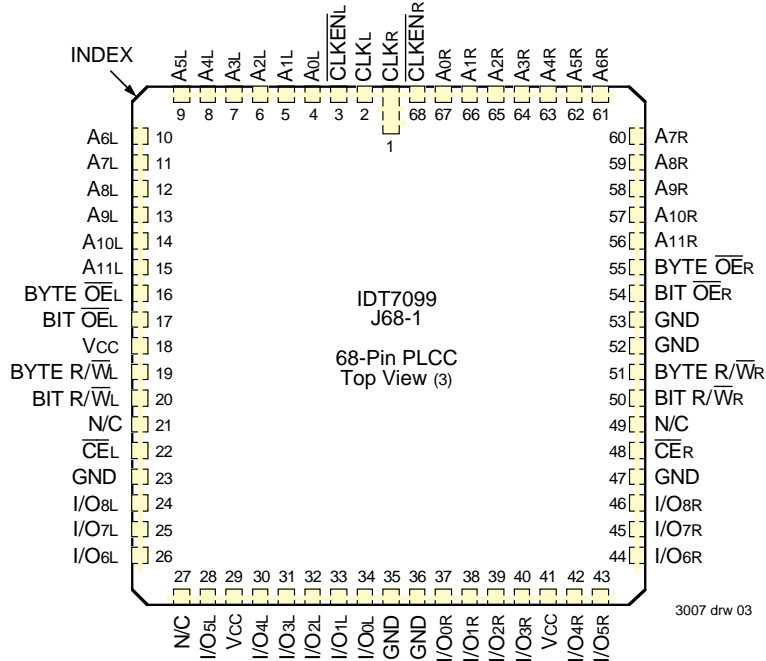**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

OCTOBER 1996

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PIN CONFIGURATIONS [1,2]

INDEX

A5L A4L A3L A2L A1L A0L CLKENL CLKL CLKR CLKENR A0R A1R A2R A3R A4R A5R A6R

9 8 7 6 5 4 3 2 68 67 66 65 64 63 62 61

1

A6L 10
A7L 11
A8L 12
A9L 13
A10L 14
A11L 15
BYTE $\overline{OE}$L 16
BIT $\overline{OE}$L 17
VCC 18
BYTE R/$\overline{W}$L 19
BIT R/$\overline{W}$L 20
N/C 21
$\overline{CE}$L 22
GND 23
I/O8L 24
I/O7L 25
I/O6L 26

IDT7099
J68-1

68-Pin PLCC
Top View (3)

60 A7R
59 A8R
58 A9R
57 A10R
56 A11R
55 BYTE $\overline{OE}$R
54 BIT $\overline{OE}$R
53 GND
52 GND
51 BYTE R/$\overline{W}$R
50 BIT R/$\overline{W}$R
49 N/C
48 $\overline{CE}$R
47 GND
46 I/O8R
45 I/O7R
44 I/O6R

27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43

N/C I/O5L VCC I/O4L I/O3L I/O2L I/O1L I/O0L GND GND I/O0R I/O1R I/O2R I/O3R VCC I/O4R I/O5R

3007 drw 03

| 51 A5L | 50 A4L | 48 A2L | 46 A0L | 44 CLKL | 42 $\overline{CLKEN}$R | 40 A1R | 38 A3R | 36 A5R | |
53 A7L	52 A6L	49 A3L	47 A1L	45 $\overline{CLKEN}$L	43 CLKR	41 A0R	39 A2R	37 A4R	35 A6R	34 A7R
55 A9L	54 A8L								32 A9R	33 A8R
57 A11L	56 A10L								30 A11R	31 A10R
59 BIT $\overline{OE}$L	58 BYTE $\overline{OE}$L			IDT7099					28 BIT $\overline{OE}$R	29 BYTE $\overline{OE}$R
61 BYTE R/$\overline{W}$L	60 VCC			G68-1					26 GND	27 GND
63 NC	62 BIT R/$\overline{W}$L			68-Pin PGA Top View (3)					24 BIT R/$\overline{W}$R	25 BYTE R/$\overline{W}$R
65 GND	64 $\overline{CE}$L								22 $\overline{CE}$R	23 NC
67 I/O7L	66 I/O8L								20 I/O8R	21 GND
68 I/O6L	1 NC	3 VCC	5 I/O3L	7 I/O1L	9 GND	11 I/O0R	13 I/O2R	15 VCC	18 I/O6R	19 I/O7R
	2 I/O5L	4 I/O4L	6 I/O2L	8 I/O0L	10 GND	12 I/O1R	14 I/O3R	16 I/O4R	17 I/O5R	

INDEX

A B C D E F G H J K L

3007 drw 02

NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONT'D) [1,2]

Reference

IDT7099
PN80-1

80-Pin TQFP
Top View [3]
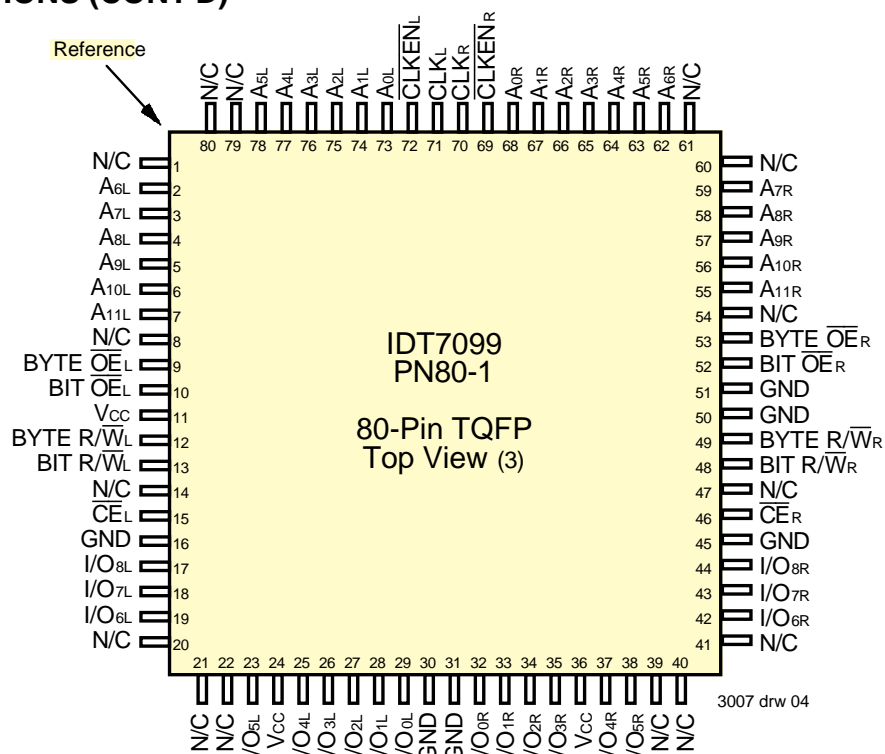
3007 drw 04

NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate the orientaion of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM} [2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM} [3]	Terminal Voltage	–0.5 to VCC	–0.5 to VCC	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

3007 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3007 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0 [2]	V
V_{IL}	Input Low Voltage	–0.5 [1]	—	0.8	V

3007 tbl 03

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE[1]

(T_A = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter	Condition[2]	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT	Output Capacitance	VOUT = 3dV	10	pF

3007 tbl 04

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V$_{CC}$ = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7099S Min.	IDT7099S Max.	Unit
|I$_{LI}$|	Input Leakage Current [1]	V$_{CC}$ = 5.5V, V$_{IN}$ = 0V to V$_{CC}$	—	10	µA
|I$_{LO}$|	Output Leakage Current	$\overline{CE}$ = V$_{IH}$, VOUT = 0V to V$_{CC}$	—	10	µA
V$_{OL}$	Output Low Voltage	I$_{OL}$ = 4mA	—	0.4	V
V$_{OH}$	Output High Voltage	I$_{OL}$ = –4mA	2.4	—	V

3007 tbl 05

NOTE:
1. Input leakages are undefined at V$_{CC}$ ≤ 2.0V.

DC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4] (V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	Test Conditions	Version	IDT7099S15 Com'l. Only Typ.	Max.	IDT7099S20 Typ.	Max.	IDT7099S25 Typ.	Max.	IDT7099S30 Mil Only Typ.	Max.	Unit
I$_{CC}$	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V$_{IL}$ Outputs Open f = fmAX[1]	Mil.	—	—	170	310	160	290	160	270	mA
			Com'l.	180	300	170	290	160	270	—	—	
I$_{SB1}$	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}$L and $\overline{CE}$R = V$_{IH}$ f = fmAX[1]	Mil.	—	—	85	140	80	130	80	110	mA
			Com'l.	90	140	85	130	80	110	—	—	
I$_{SB2}$	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}$'A' = V$_{IL}$ and $\overline{CE}$'B' = V$_{IH}$ [3] Active Port Outputs Open, f = fmAX[1]	Mil.	—	—	150	210	140	200	140	180	mA
			Com'l.	160	210	150	200	140	180	—	—	
I$_{SB3}$	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE}$R and $\overline{CE}$L ≥ V$_{CC}$ – 0.2V V$_{IN}$ ≥ V$_{CC}$ – 0.2V or V$_{IN}$ ≤ 0.2V, f = 0[2]	Mil.	—	—	10	20	10	20	10	20	mA
			Com'l.	10	15	10	—	10	—	—	—	
I$_{SB4}$	Full Standby Current (One Port—CMOS Level Inputs)	$\overline{CE}$'A'≤0.2V and $\overline{CE}$'B' ≥ V$_{CC}$ -0.2V[3], V$_{IN}$ ≥ V$_{CC}$ – 0.2V or V$_{IN}$ ≤ 0.2V, Active Port Outputs Open, f = fmAX[1]	Mil.	—	—	145	200	135	190	135	170	mA
			Com'l.	155	200	145	190	135	170	—	—	

3007 tbl 06

NOTES:
1. At f = fmax, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of the 1/t$_{CLK}$, using "AC TEST CONDITIONS" of input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
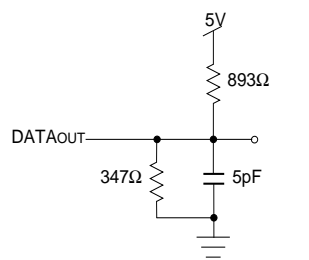4. Vcc = 5V, TA = 25°C for Typ, and are not production tested. I$_{CC}$ $_{DC}$ = 150mA (Typ).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

3007 tbl 07

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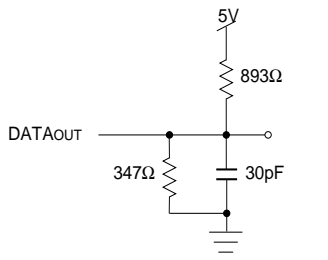
Figure 1.　AC Output Test load.

3007 drw 05

Figure 2.　Output Test Load
(For t_{CLZ}, t_{CHZ}, t_{OLZ}, and t_{OHZ}).
Including scope and jig.

3007 drw 06

☐ - 10pF is the I/O capacitance of this device, and 3pF is the AC Test Load Capacitance

Δt_{CD} (Typical, ns)

Capacitance (pF)
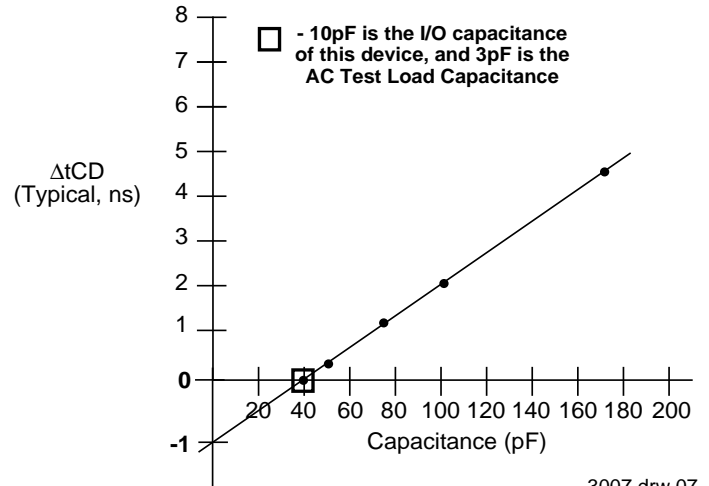
3007 drw 07

Figure 3.　Typical Output Derating (Lumped Capacitive Load).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGE — (READ AND WRITE CYCLE TIMING)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

| | | Commercial | | | | | | Military | | | | | | |
| | | 7099S15 | | 7099S20 | | 7099S25 | | 7099S20 | | 7099S25 | | 7099S30 | | |
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Clock Cycle Time	20	—	20	—	25	—	20	—	25	—	30	—	ns
t_{CH}	Clock High Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
t_{CL}	Clock Low Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
t_{CD}	Clock High to Output Valid	—	15	—	20	—	25	—	20	—	25	—	30	ns
t_S	Registered Signal Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
t_H	Registered Signal Hold Time	1	—	1	—	1	—	2	—	2	—	2	—	ns
t_{DC}	Data Output Hold After Clock High	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{CKLZ}	Clock High to Output Low-Z[1,2]	2	—	2	—	2	—	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1,2]	—	7	—	9	—	12	—	9	—	12	—	15	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	—	10	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1,2]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High-Z[1,2]	—	7	—	9	—	11	—	9	—	11	—	14	ns
t_{SCK}	Clock Enable, Disable Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
t_{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	2	—	3	—	3	—	3	—	ns
t_{CWDD}	Write Port Clock High to Read Data Delay	—	30	—	35	—	45	—	35	—	45	—	55	ns

NOTES:　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　3007 tbl 08
1. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.

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TIMING WAVEFORM OF READ CYCLE, EITHER SIDE
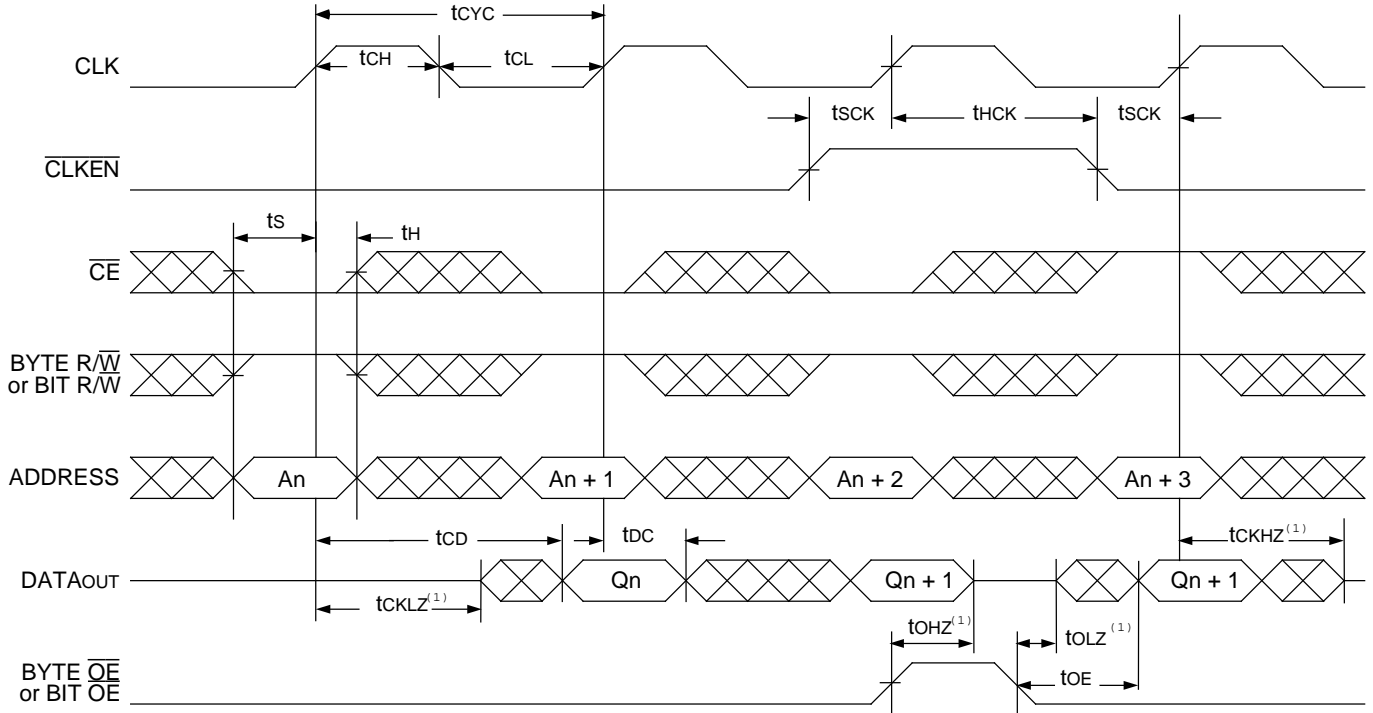
3007 drw 08

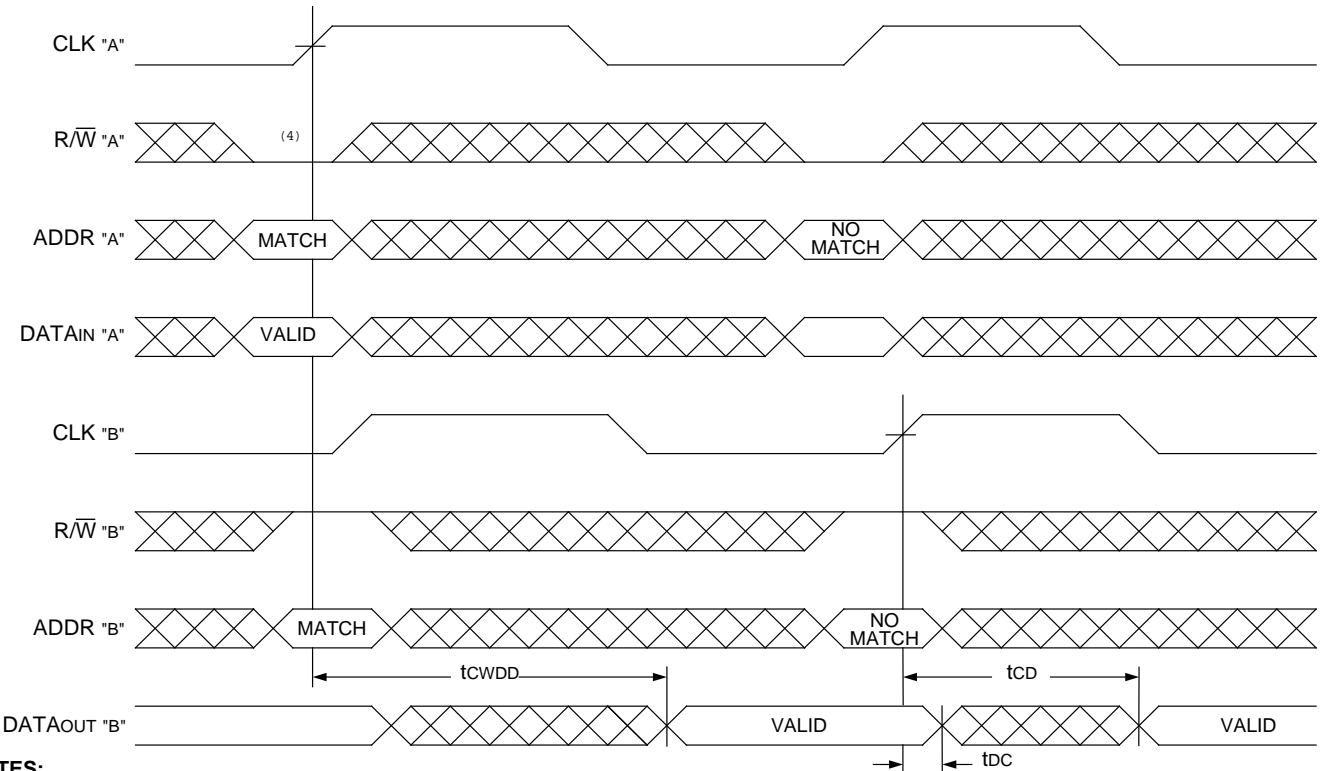**NOTE:**

1. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).

## TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ [1,2,3]

3007 drw 09

NOTES:

1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, $\overline{CLKEN}_L = \overline{CLKEN}_R = V_{IL}$
2. $\overline{OE} = V_{IL}$ for the reading port, port 'B'.
3. All timing is the same for left and right ports. Ports "A" may be either the left or right port. Port "B" is opposite from port "A".
4. R/$\overline{W}$'A' was active (V_{IL}) during the previous CLK'A', when enabled the write path.
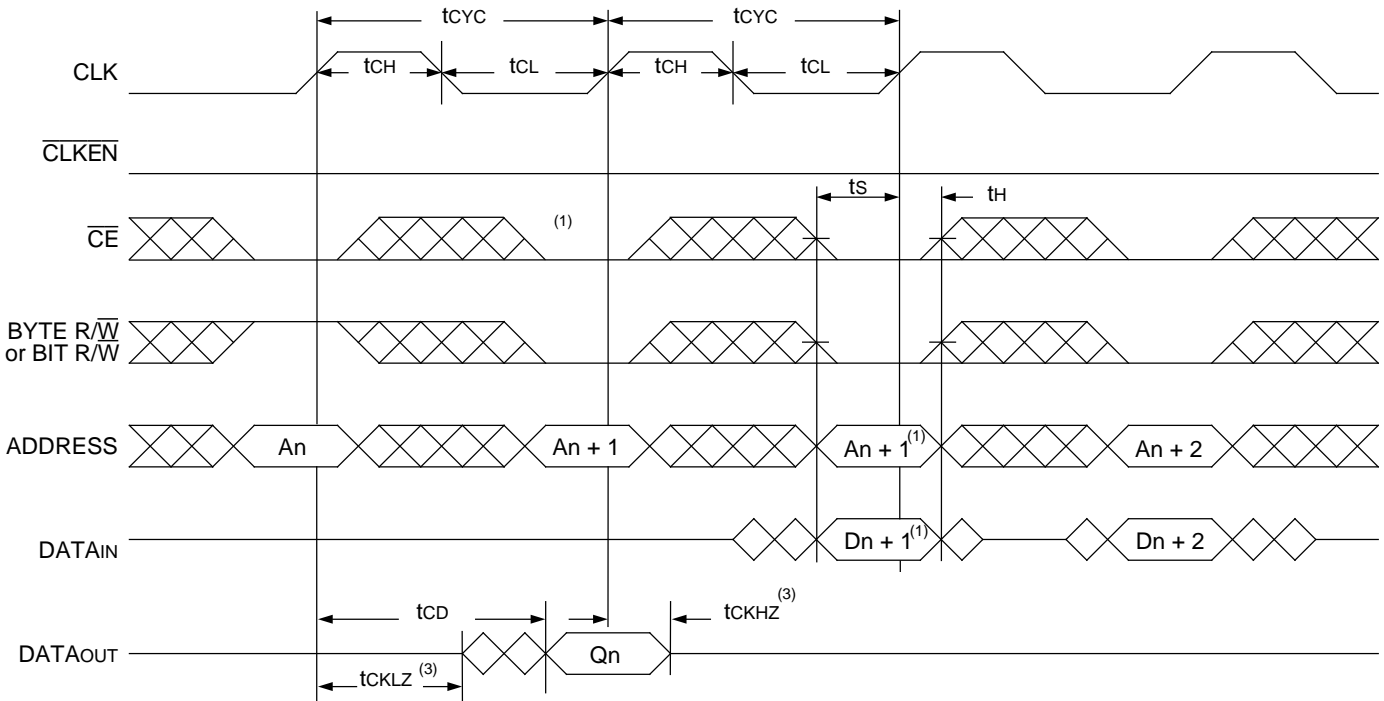
TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ = V$_{IH}$ [2]
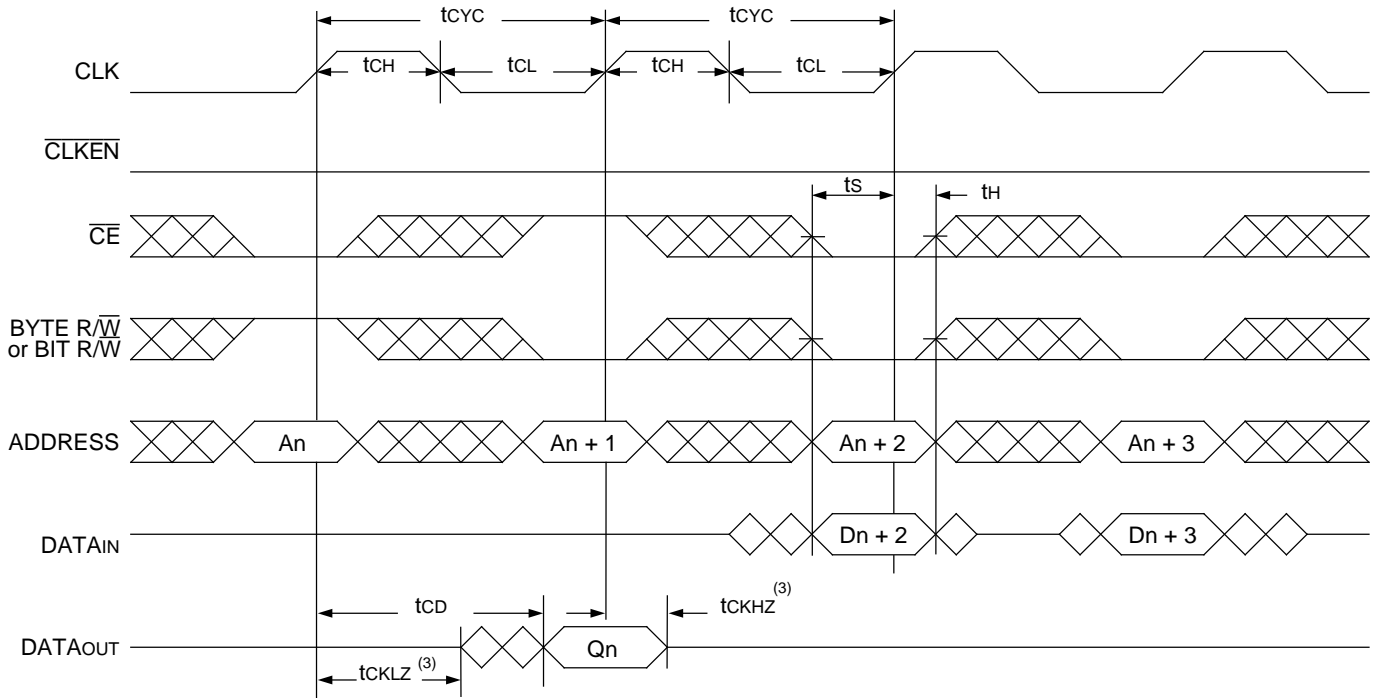
3007 drw 10

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 2, $\overline{CE}$ = V$_{IL}$ [2]

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NOTES:
1. During dead cycle, if $\overline{CE}$ = V$_{IL}$, then invalid data will be written into array. The An+1 must be rewritten on the following cycle.
2. $\overline{OE}$ low throughout.
3. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).

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FUNCTIONAL DESCRIPTION

The IDT7099 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent on the low to high transitions of the clock signal allowing the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

The data inputs are gated to control on-chip noise in bussed applications. The user must guarantee that the BYTE R/$\overline{W}$ and BIT R/$\overline{W}$ pins are low for at least one clock cycle before any write is attempted. A High on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

The device has separate Bit Write, Byte Write, Bit Enable, and Byte Enable pins to allow for independent control.

TRUTH TABLE I – READ/WRITE CONTROL[1]

Inputs						Outputs		
Synchronous[3]				Asynchronous		Outputs		
CLK	$\overline{CE}$	Byte R/$\overline{W}$	Bit R/$\overline{W}$	Byte $\overline{OE}$	Bit $\overline{OE}$	I/O0-7	I/O8	Mode
⌁	h	h	h	X	X	High-Z	High-Z	Deselected, Power Down, Data I/O Disabled
⌁	h	l	h	X	X	DATAIN	High-Z	Deselected, Power Down, Byte Data Input Enabled
⌁	h	h	l	X	X	High-Z	DATAIN	Deselected, Power Down, Bit Data Input Enabled
⌁	h	l	l	X	X	DATAIN	DATAIN	Deselected, Power Down, Data Input Enabled
⌁	l	l	h	X	L	DATAIN	DATAOUT	Write Byte, Read Bit
⌁	l	l	h	X	H	DATAIN	High-Z	Write Byte Only
⌁	l	h	l	L	X	DATAOUT	DATAIN	Read Byte, Write Bit
⌁	l	h	l	H	X	High-Z	DATAIN	Write Bit Only
⌁	l	l	l	X	X	DATAIN	DATAIN	Write Byte, Write Bit
⌁	l	h	h	L	L	DATAOUT	DATAOUT	Read Byte, Read Bit
⌁	l	h	h	H	L	High-Z	DATAOUT	Read Bit Only
⌁	l	h	h	L	H	DATAOUT	High-Z	Read Byte Only
⌁	l	h	h	H	H	High-Z	High-Z	Data I/O Disabled

3007 tbl 09

TRUTH TABLE II – CLOCK ENABLE FUNCTION TABLE[1]

Operating Mode	Inputs		Register Inputs		Register Outputs	
	CLK[3]	$\overline{CLKEN}$[2]	ADDR	DATAIN	ADDR	DATAOUT
Load "1"	⌁	l	h	h	H	H
Load "0"	⌁	l	l	l	L	L
Hold (do nothing)	⌁	h	X	X	NC	NC
	X	H	X	X	NC	NC

3007 tbl 10

NOTES:
1. 'H' = High voltage level steady state, 'h' = High voltage level one set-up time prior to the low-to-high clock transition, 'L' = Low voltage level steady state 'l' = Low voltage level one set-up time prior to the Low-to-High clock transition, 'X' = Don't care, 'NC' = No change
2. $\overline{CLKEN}$ = VIL must be clocked in during Power-Up.
3. Control signals are initialted and terminated on the rising edge of the CLK, depending on their input level. When R/$\overline{W}$ and $\overline{CE}$ are low, a write cycle is initiated on the low-to-high transition of the CLK. Termination of a write cycle is done on the next low-to-high transistion of the CLK.

ORDERING INFORMATION

IDT   XXXX   A   999   A   A

Device Type   Power   Speed   Package   Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class C
J	68-pin PLCC (J68-1)
G	68-pin PGA (G68-1)
PF	80-pin TQFP (PN80-1)
15	Commercial Only
20	
25	
30	Military Only
	Speed in nanoseconds
S	Standard Power
7099	36K (4K x 9-Bit) Synchronous Dual-Port RAM

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