Agilent HDMP-0452 Quad Port Bypass Circuit with CDR for Fibre Channel Arbitrated Loops

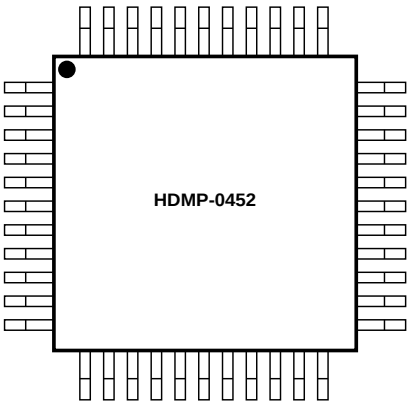
Data Sheet

Features

- **Supports 1.0625 GBd fibre channel operation**
- **Supports 1.25 GBd Gigabit Ethernet (GE) operation**
- **Quad PBC/CDR in one package**
- **CDR location determined by choice of cable input/output**
- **Valid amplitude detection on FM_NODE[0] input**
- **Equalizers on all inputs**
- **High speed LVPECL I/O**
- **Buffered Line Logic (BLL) outputs (no external bias resistors required)**
- **0.66 W typical power at V_{CC} = 3.3 V**
- **44 pin, 10 mm, low cost plastic QFP package**

Applications

- **RAID, JBOD, BTS cabinets**
- **1 => 1-4 serial buffer with or w/o CDR**



Description

The HDMP-0452 is a Quad Port Bypass Circuit (PBC) with a Clock and Data Recovery (CDR) circuit included. This device minimizes part count, cost and jitter accumulation while repeating incoming signals. Port Bypass Circuits are used in hard disk arrays constructed in Fibre Channel Arbitrated Loop (FC-AL) configurations. By using Port Bypass Circuits, hard disks may be pulled out or swapped while other disks in the array are available to the system.

A Port Bypass Circuit (PBC) consists of multiple 2:1 multiplexers daisy chained along with a CDR. Each port has two modes of operation: “disk in loop” and “disk bypassed”. When the “disk in loop” mode is selected, the loop goes into and out of the disk drive at that port. For example, data goes from the HDMP-0452’s TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC’s (e.g., an HDMP-1536A) Rx± differential input pins. Data from the Disk Drive Transceiver IC’s Tx± differential outputs goes to the HDMP-0452’s FM_NODE[n]± differential input pins. Figures 3 and 4 show connection diagrams for disk drive array applications. When the “disk bypassed” mode is selected, the disk drive is either absent or nonfunctional and the loop bypasses the hard disk.

The “disk bypassed” mode is enabled by pulling the BYPASS[n]– pin low. Leave BYPASS[n]– floating to enable the “disk in loop” mode. HDMP-0452s may be cascaded with other members of the HDMP-04XX/HDMP-05XX family through the FM_LOOP and TO_LOOP pins to accommodate any number of hard disks. See Table 2 to identify which of the 5 cells (0:4) will provide FM_LOOP and TO_LOOP pins (cable connections). The unused cells in this PBC may be bypassed by using pulldown resistors on the BYPASS[n]– pins for these cells.

CAUTION: As with all semiconductor ICs, it is advised that normal static precautions be taken in the handling and assembly of this component to prevent damage and/or degradation which may be induced by Electrostatic Discharge (ESD).

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An HDMP-0452 may also be used as five 1:1 buffers, one with a CDR and four without. For example, an HDMP-0452 may be placed in front of a CMOS ASIC to clean the jitter of the outgoing signal (CDR path) and to better read the incoming signal (non-CDR path). In addition, the HDMP-0452 may be configured as two 2:1 multiplexers or as two 1:2 buffers.

The HDMP-0452 design allows for CDR placement at any location with respect to the hard disk slots. For example, if the BYPASS[0]– pin is floating and hard disk slots A to D are connected to PBC cells 1 to 4 respectively (see Figure 3), the CDR function will be performed before entering the hard disk at slot A. To obtain a CDR function after slot D (see Figure 4), BYPASS[1]– must be floating and hard disk slots A to D must be connected to PBC cells 2,3,4, and 0 respectively. Table 2 shows all possible connections. For configurations where the CDR is before slot A, a Signal Detect (SD) pin shows the status of the signal at the incoming cable.

HDMP-0452 Block Diagram

CDR

The Clock and Data Recovery (CDR) block is responsible for frequency and phase locking onto the incoming serial data stream and resampling the incoming data based on the recovered clock. An automatic locking feature allows the CDR to lock onto the input data stream without external training controls. It does this by continually frequency locking onto the 106.25 MHz reference clock (REFCLK) and then phase locking onto the input data stream. Once bit locked, the CDR generates a high-speed sampling clock. This clock is used to sample or repeat the incoming data to produce the CDR output. The CDR jitter specifications listed in this data sheet assume an input that has been 8B/10B encoded.

SD OUTPUT

The Signal Detect (SD) block detects if the incoming data on FM_NODE[0]± is valid by examining the differential amplitude of that input. The incoming data is considered valid, and SD is driven high, as long as the amplitude is greater than 400 mV (differential peak-to-peak). SD is driven low as long as the amplitude of the input signal is less than 100 mV (differential peak-to-peak). When the amplitude of the input signal is between 100-400 mV (differential peak-to-peak), SD is unpredictable.

BLL OUTPUT

All TO_NODE[n]± high-speed differential outputs are driven by a Buffered Line Logic (BLL) circuit that has on-chip source termination, so no external bias resistors are required. The BLL Outputs on the HDMP-0452 are of equal strength and can drive in excess of 120 inches of FR-4 PCB trace.

Unused outputs should not be left unconnected. Ideally, unused outputs should have their differential pins shorted together with a short PCB trace. If transmission lines are connected to the output pins, the lines should be differentially terminated with an appropriate resistor. The value of the termination resistor should match the PCB trace differential impedance.

EQU INPUT

All FM_NODE[n]± high-speed differential inputs have an Equalization (EQU) buffer to offset the effects of skin loss and dispersion on PCBs. An external termination resistor is required across all high-speed inputs.

BYPASS[N]– INPUT

The active low BYPASS[n]– inputs control the data flow through the HDMP-0452. All BYPASS pins are LVTTL and contain internal pull-up circuitry. To bypass a port, the appropriate BYPASS[n]– pin should be connected to GND through a 1 kΩ resistor. Otherwise, the BYPASS[n]– inputs should be left to float. In this case, the internal pull-up circuitry will force them high.

REFCLK INPUT

The LVTTL REFCLK input provides a reference oscillator for frequency acquisition of the CDR. The REFCLK frequency should be within ± 100 ppm of one-tenth of the incoming data rate in baud (106.25 MHz ± 100 ppm for FC-AL running at 1.0625 GBd).

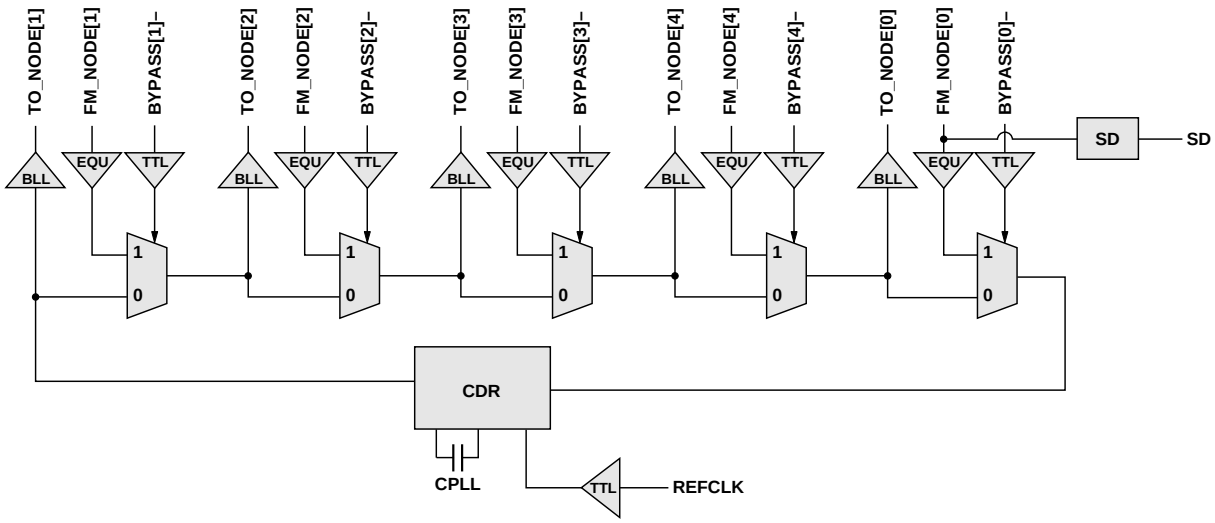


Figure 1. Block diagram of HDMP-0452.

Table 1. Truth Table for CDR at Entry Configuration.

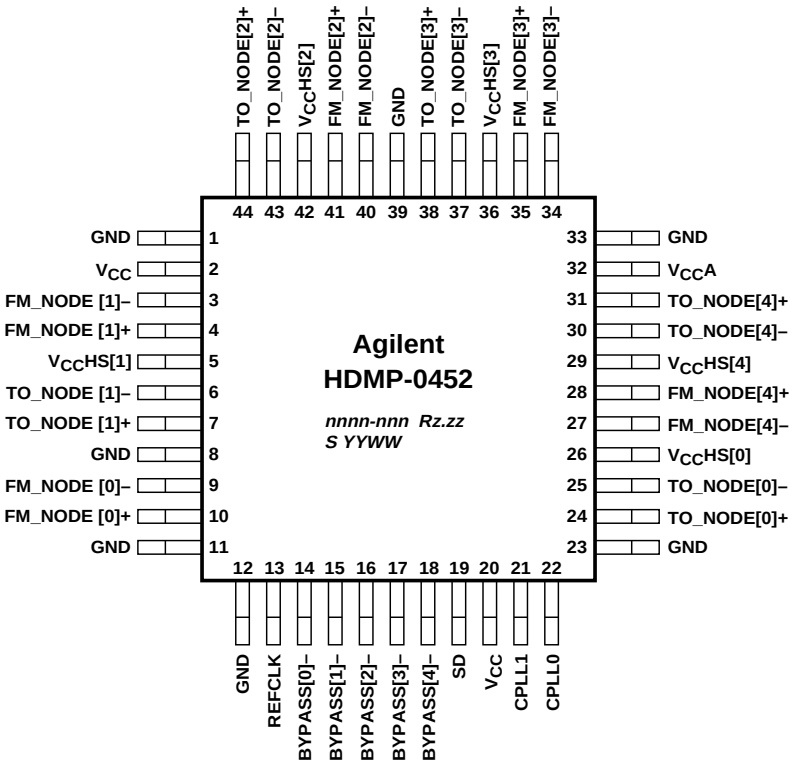
TO_LOOP	TO_NODE[4]	TO_NODE[3]	TO_NODE[2]	TO_NODE[1]	BYPASS[4]–	BYPASS[3]–	BYPASS[2]–	BYPASS[1]–
FM_LOOP	FM_LOOP	FM_LOOP	FM_LOOP	FM_LOOP	0	0	0	0
FM_NODE[1]	FM_NODE[1]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	0	0	0	1
FM_NODE[2]	FM_NODE[2]	FM_NODE[2]	FM_LOOP	FM_LOOP	0	0	1	0
FM_NODE[2]	FM_NODE[2]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	0	0	1	1
FM_NODE[3]	FM_NODE[3]	FM_LOOP	FM_LOOP	FM_LOOP	0	1	0	0
FM_NODE[3]	FM_NODE[3]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	0	1	0	1
FM_NODE[3]	FM_NODE[3]	FM_NODE[2]	FM_LOOP	FM_LOOP	0	1	1	0
FM_NODE[3]	FM_NODE[3]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	0	1	1	1
FM_NODE[4]	FM_LOOP	FM_LOOP	FM_LOOP	FM_LOOP	1	0	0	0
FM_NODE[4]	FM_NODE[1]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	1	0	0	1
FM_NODE[4]	FM_NODE[2]	FM_NODE[2]	FM_LOOP	FM_LOOP	1	0	1	0
FM_NODE[4]	FM_NODE[2]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	1	0	1	1
FM_NODE[4]	FM_NODE[3]	FM_LOOP	FM_LOOP	FM_LOOP	1	1	0	0
FM_NODE[4]	FM_NODE[3]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	1	1	0	1
FM_NODE[4]	FM_NODE[3]	FM_NODE[2]	FM_LOOP	FM_LOOP	1	1	1	0
FM_NODE[4]	FM_NODE[3]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	1	1	1	1

Note: FM_LOOP = FM_NODE[0], TO_LOOP = TO_NODE[0], BYPASS[0]– = 1.

Table 2. Pin Connection Diagram to Achieve Desired CDR Location (see Figures 3, 4).

Hard Disks	A B C D	A B C D	A B C D	A B C D	A B C D
Connection to PBC Cells	1 2 3 4	0 1 2 3	4 0 1 2	3 4 0 1	2 3 4 0
CDR Position (x)	xA B C D	AxB C D	A BxC D	A B CxD	A B C Dx
Cell Connected to Cable	0	4	3	2	1

Note: x denotes CDR position with respect to hard disks.



nnnn-nnn = WAFER LOT – BUILD NUMBER
Rz.zz = DIE REVISION
S = SUPPLIER CODE
YYWW = DATE CODE (*YY* = YEAR, *WW* = WORK WEEK)
COUNTRY = COUNTRY OF MANUFACTURE
(ON BACK SIDE)

Figure 2. HDMP-0452 package layout and marking, top view.

I/O Type Definitions

I/O Type	Definition
I-LVTTL	LVTTL Input
O-LVTTL	LVTTL Output
HS_OUT	High-Speed Output, LVPECL Compatible
HS_IN	High-Speed Input
C	External Circuit Node
S	Power Supply or Ground

Table 3. Pin Definitions for HDMP-0452.

Pin Name	Pin	Pin Type	Pin Description
TO_NODE[0]+ TO_NODE[0]– TO_NODE[1]+ TO_NODE[1]– TO_NODE[2]+ TO_NODE[2]– TO_NODE[3]+ TO_NODE[3]– TO_NODE[4]+ TO_NODE[4]–	24 25 07 06 44 43 38 37 31 30	HS_OUT	**Serial Data Outputs:** High-speed outputs to a hard disk drive or to a cable input.
FM_NODE[0]+ FM_NODE[0]– FM_NODE[1]+ FM_NODE[1]– FM_NODE[2]+ FM_NODE[2]– FM_NODE[3]+ FM_NODE[3]– FM_NODE[4]+ FM_NODE[4]–	10 09 04 03 41 40 35 34 28 27	HS_IN	**Serial Data Inputs:** High-speed inputs from a hard disk drive or from a cable output.
BYPASS[0]– BYPASS[1]– BYPASS[2]– BYPASS[3]– BYPASS[4]–	14 15 16 17 18	I-LVTTL	**Bypass Inputs:** For "disk bypassed" mode, connect BYPASS[n]– to GND through a 1 kΩ resistor. For "disk in loop" mode, float HIGH.
REFCLK	13	I-LVTTL	**Reference Clock:** A user-supplied clock reference used for frequency acquisition in the Clock and Data Recovery (CDR) circuit.
CPLL1 CPLL0	21 22	C	**Loop Filter Capacitor:** A loop filter capacitor for the internal Clock and Data Recovery (CDR) circuit must be connected across the CPLL1 and CPLL0 pins. Recommended value is 0.1 μF.
SD	19	O-LVTTL	**Signal Detect:** Indicates acceptable signal amplitude on the FM_NODE[0]± inputs. If (FM_NODE[0]+ – FM_NODE[0]–) >= 400 mV peak-to-peak, SD = 1 If 400 mV > (FM_NODE[0]+ – FM_NODE[0]–) > 100 mV, SD = unpredictable If 100 mV >= (FM_NODE[0]+ – FM_NODE[0]–), SD = 0
GND	01 08 11 12 23 33 39	S	**Ground:** Normally 0 volts. See Figure 11 for Recommended Power Supply Filtering.
VCCA	32	S	**Analog Power Supply:** Normally 3.3 volts. Used to provide a clean supply line for the Clock and Data Recovery (CDR) circuit. See Figure 11 for Recommended Power Supply Filtering.
VCCHS[0] VCCHS[1] VCCHS[2] VCCHS[3] VCCHS[4]	26 05 42 36 29	S S S S S	**High Speed Supply:** Normally 3.3 volts. Used only for high-speed outputs (TO_NODE[n]). See Figure 11 for Recommended Power Supply Filtering.
VCC	02 20	S	**Logic Power Supply:** Normally 3.3 volts. Used for internal logic. See Figure 11 for Recommended Power Supply Filtering.

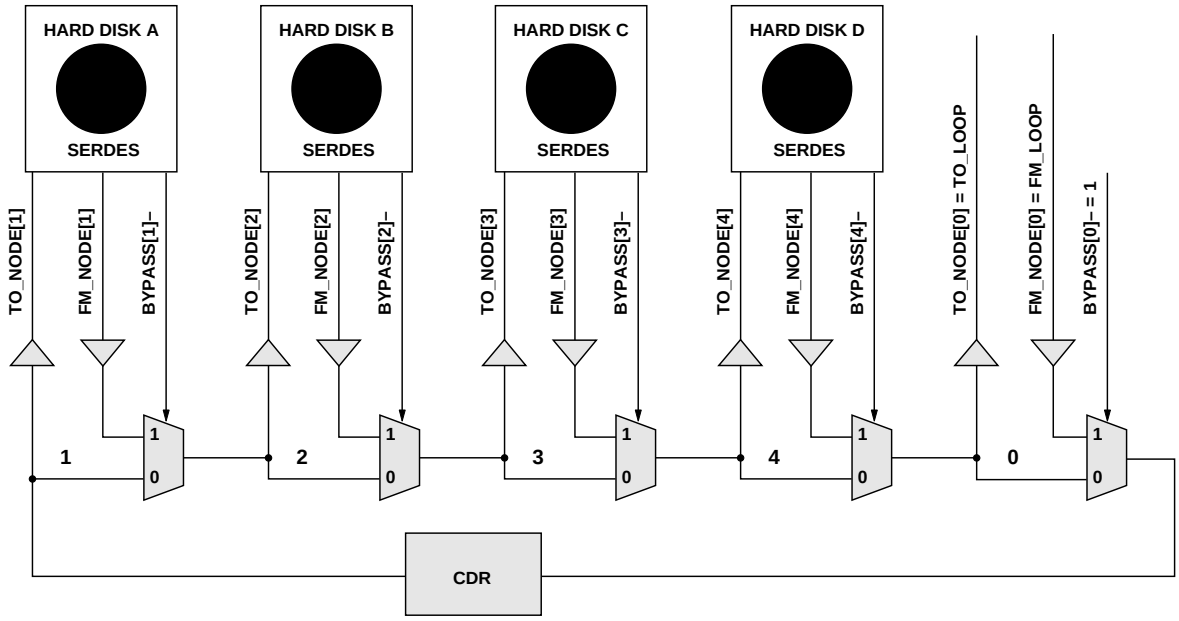


Figure 3. Connection diagram for CDR at first cell.

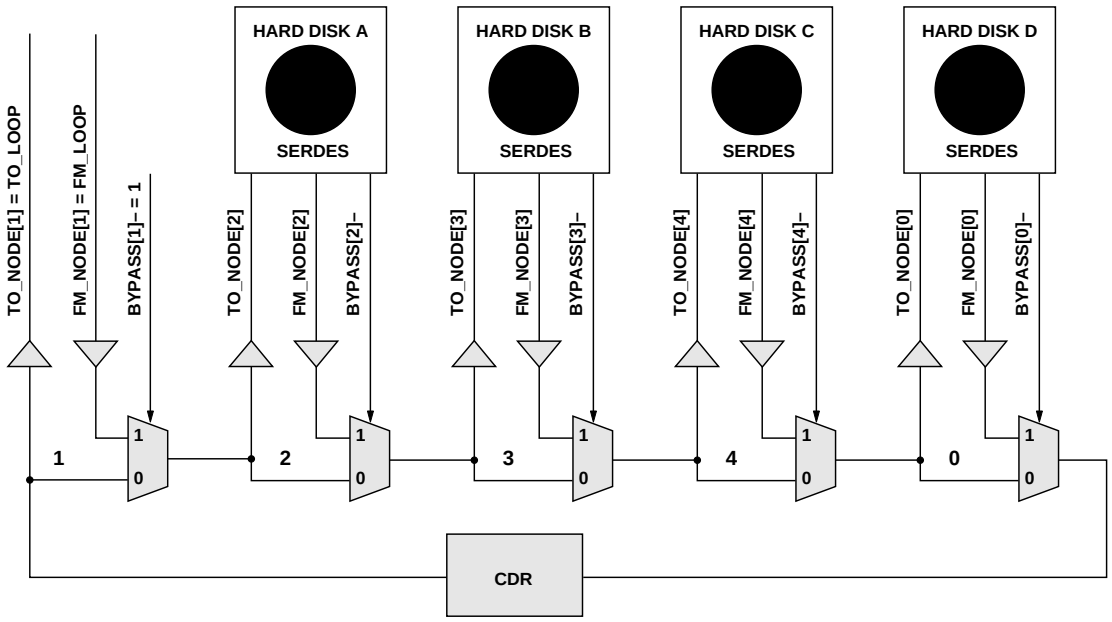


Figure 4. Connection diagram for CDR at last cell.

HDMP-0452 Absolute Maximum Ratings

T_A = 25°C, except as specified. Operation in excess of any of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	–0.7	4.0
$V_{IN,LVTTL}$	LVTTL Input Voltage	V	–0.7	4.0
V_{IN,HS_IN}	HS_IN Input Voltage	V	1.3	V_{CC}
$I_{O,LVTTL}$	LVTTL Output Voltage	mA		±13
T_{stg}	Storage Temperature	°C	–65	+150
T_j	Junction Temperature	°C	0	+125

HDMP-0452 Guaranteed Operating Rates

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Serial Clock Rate FC (MBd)		Serial Clock Rate GE (MBd)	
Min.	Max.	Min.	Max.
1040	1080	1240	1260

HDMP-0452 CDR Reference Clock Requirements

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.	Min.	Typ.	Max.
f	Nominal Frequency	MHz		106.25			125.00	
F_{tol}	Frequency Tolerance	ppm	–100		+100	–100		+100
Symm	Symmetry (Duty Cycle)	%	40		60	40		60

HDMP-0452 DC Electrical Specifications

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$V_{IH,LVTTL}$	LVTTL Input High Voltage Range	V	2.0		4.0
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Range	V	0		0.8
$V_{OH,LVTTL}$	LVTTL Output High Voltage Range, I_{OH} = –400 µA	V	2.2		3.45
$V_{OL,LVTTL}$	LVTTL Output Low Voltage Level, I_{OL} = 1 mA	V	0		0.6
$I_{IH,LVTTL}$	Input High Current (Magnitude), V_{IN} = 2.4 V, V_{CC} = 3.45 V	µA		0.003	40
$I_{IL,LVTTL}$	Input Low Current (Magnitude), V_{IN} = 0.4 V, V_{CC} = 3.45 V	µA		300	600
I_{CC}	Total Supply Current, T_A = 25°C	mA		200	

HDMP-0452 AC Electrical Specifications
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{delay1}	Total Loop Latency from FM_NODE[0] to TO_NODE[0]	ns		4.0	
t_{delay2}	Per Cell Latency from FM_NODE[4] to TO_NODE[0]	ns		0.8	
$t_{r,LVTTLin}$	Input LVTTL Rise Time Requirement, 0.8 V to 2.0 V	ns		2	
$t_{f,LVTTLin}$	Input LVTTL Fall Time Requirement, 2.0 V to 0.8 V	ns		2	
t_{rs,HS_OUT}	HS_OUT Single-Ended Rise Time, 20%-80%	ps		200	350
t_{fs,HS_OUT}	HS_OUT Single-Ended Fall Time, 20%-80%	ps		200	350
t_{rd,HS_OUT}	HS_OUT Differential Rise Time, 20%-80%	ps		200	350
t_{fd,HS_OUT}	HS_OUT Differential Fall Time, 20%-80%	ps		200	350
V_{IP,HS_IN}	HS_IN Input Peak-to-Peak Required Differential Voltage Range	mV	200	1200	2000
V_{OP,HS_OUT}	HS_OUT Output Pk-Pk Diff. Voltage Range (Z0 = 75 Ohm, Fig. 9)	mV	1100	1400	2000

HDMP-0452 Power Dissipation and Thermal Resistance
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typ.	Max.
P_D	Power Dissipation	mW	660	950
Θ_{jc}	Thermal Resistance, Junction to Case	°C/W	7	

HDMP-0452 Output Jitter Characteristics
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typ.	Max.
RJ	Random Jitter at TO_NODE pins (1 sigma rms)	ps	5	
DJ	Deterministic Jitter at TO_NODE pins (pk-pk)	ps	20	

Please refer to Figures 6 and 7 for jitter measurement setup information.

HDMP-0452 Locking Characteristics
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Parameter	Units	Max.
Bit Sync Time (phase lock)	bits	2500
Frequency Lock at Powerup	µs	500

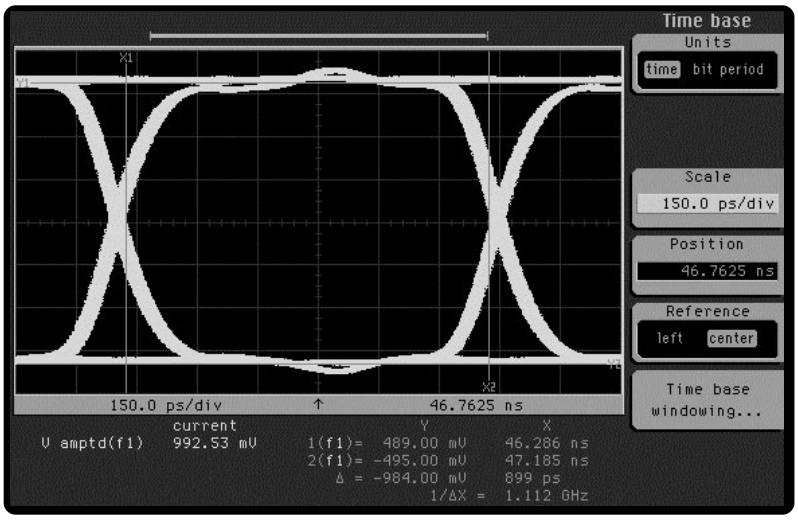


Figure 5. Eye diagram of FM_NODE[1]± high-speed differential output.
Note: Measurement taken with a 2^7-1 PRBS input to FM_NODE[0]±.

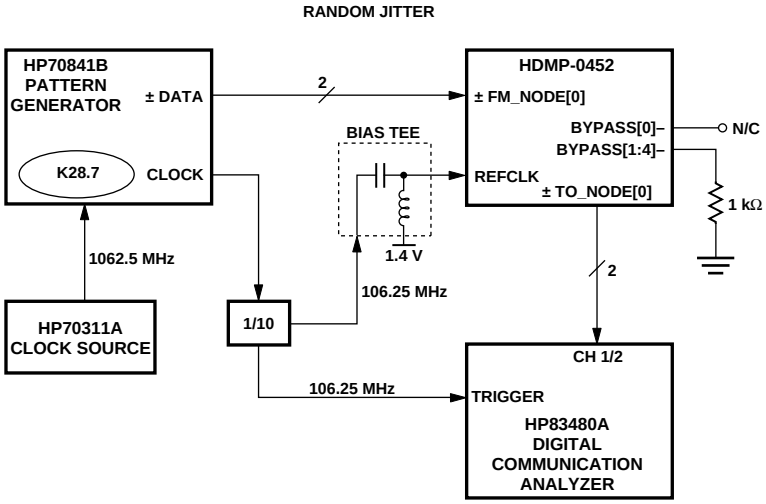


Figure 6. Setup for measurement of random jitter.

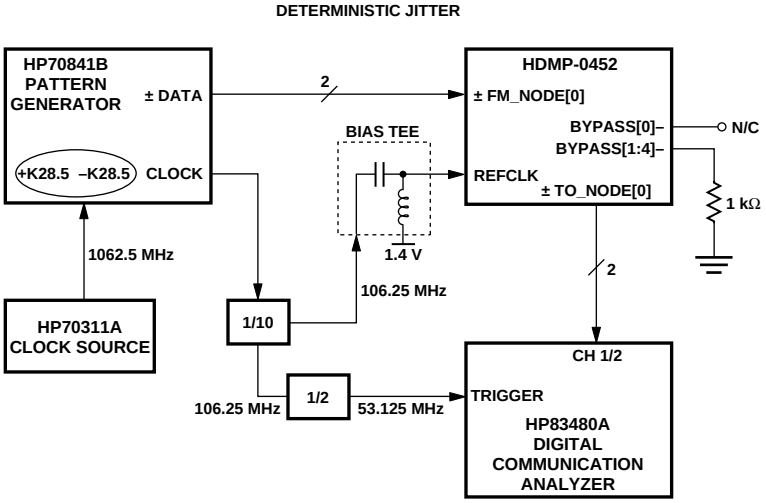


Figure 7. Setup for measurement of deterministic jitter.

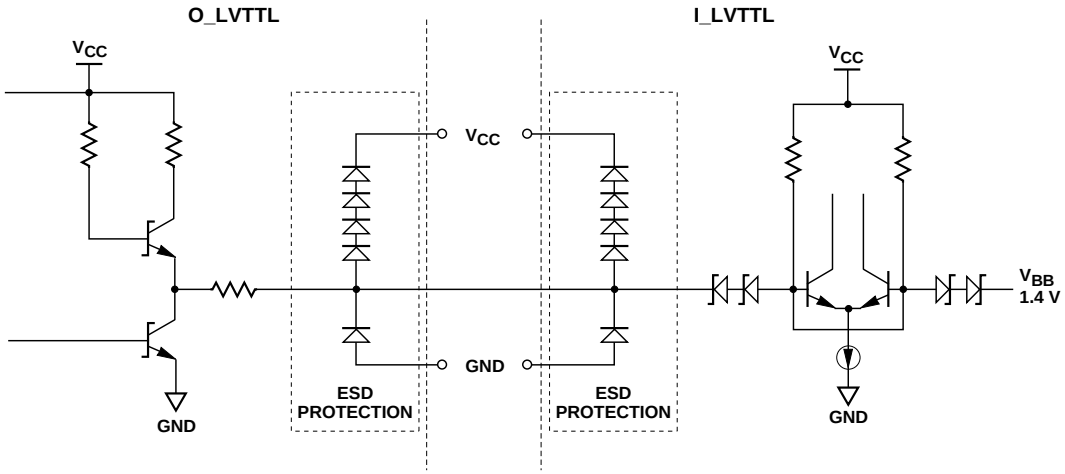
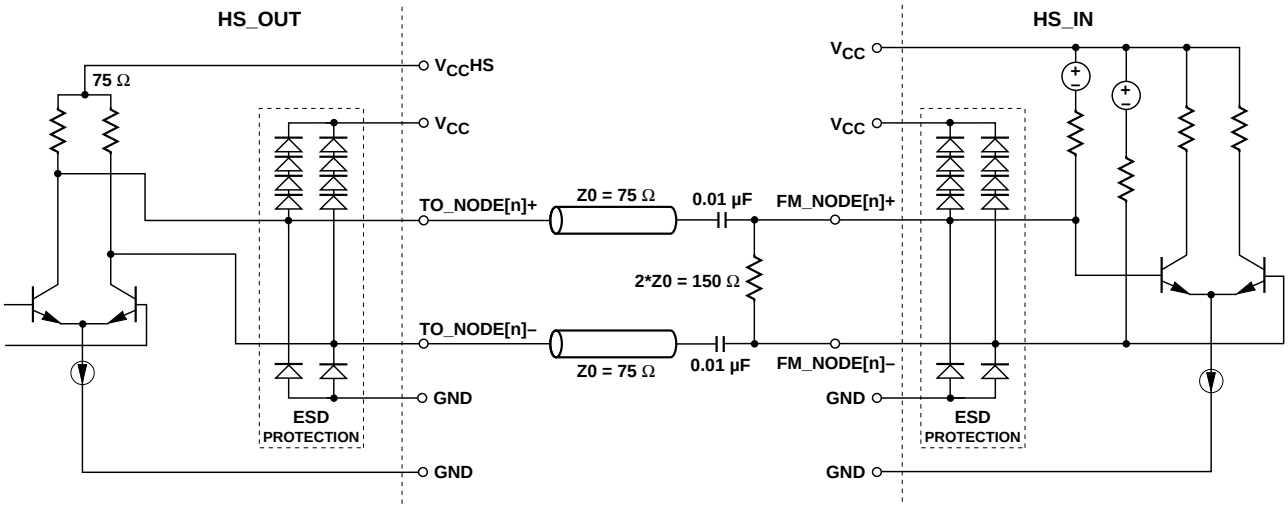


Figure 8. O-LVTTL and I-LVTTL simplified circuit schematic.



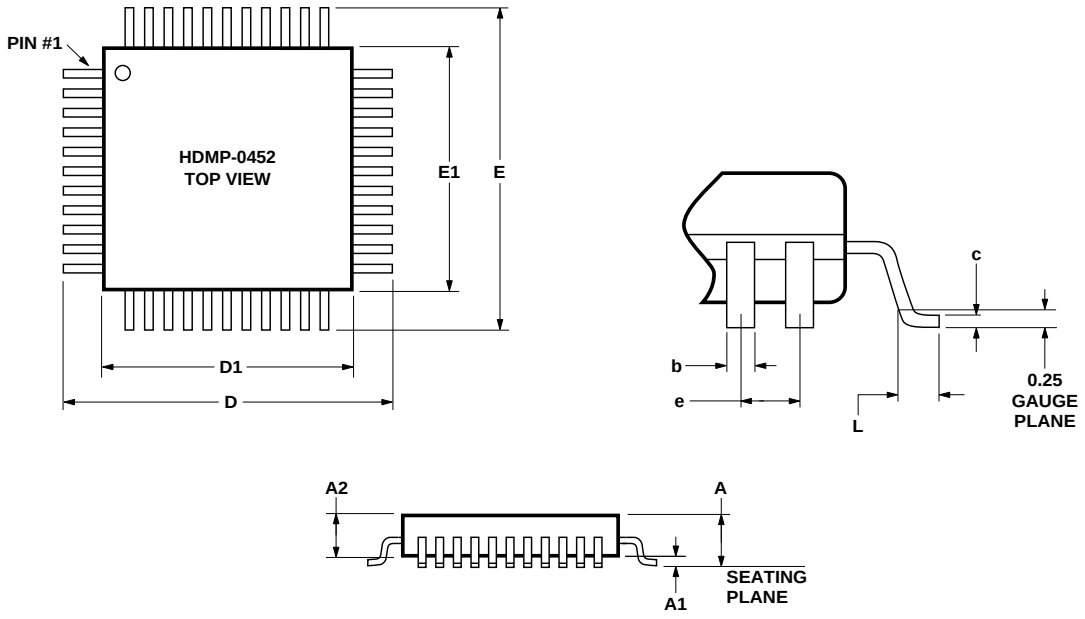
NOTE:
FM_NODE[n] INPUTS SHOULD NEVER BE CONNECTED TO GROUND AS PERMANENT DAMAGE TO THE DEVICE MAY RESULT.

Figure 9. HS_OUT and HS_IN simplified circuit schematic.

Package Information

Item	Details
Package Material	Plastic
Lead Finish Material	85% Tin, 15% Lead
Lead Finish Thickness	200-800 micro-inches
Lead Skew	0.33 mm max.
Lead Coplanarity (Seating Plane)	0.10 mm max.

Mechanical Dimensions

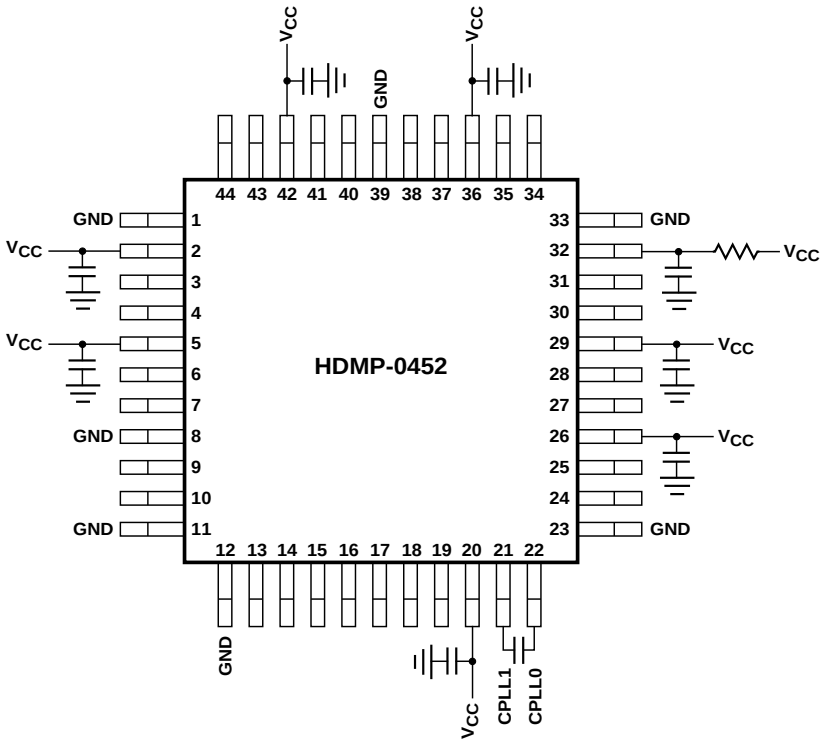


ALL DIMENSIONS ARE IN MILLIMETERS

PART NUMBER	E1/D1	E/D	b	e	L	c	A2	A1	A
HDMP-0452	10.00	13.20	0.35	0.80	0.88	0.23	2.00	0.25	2.45
TOLERANCE	± 0.10	± 0.20	± 0.05	BASIC	+ 0.15/ – 0.10	MAX.	+ 0.10/ – 0.05	± 0.25	MAX.

Figure 10. HDMP-0452 package drawing.

Supply Filtering



NOTE: CAPACITORS = 0.1 µF, RESISTORS = 10 Ω

Figure 11. Recommended power supply filtering.

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