## DATA SHEET



BUS

## SAA7108E; SAA7109E PC-CODEC

Product specification
File under Integrated Circuits, IC22

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## 1 FEATURES

### 1.1 Video decoder

- Six analog inputs, internal analog source selectors, e.g. $6 \times$ CVBS or $(2 \times \mathrm{Y} / \mathrm{C}$ and $2 \times \mathrm{CVBS})$ or $(1 \times \mathrm{Y} / \mathrm{C}$ and $4 \times$ CVBS)
- Two analog preprocessing channels in differential CMOS style for best S/N-performance
- Fully programmable static gain or Automatic Gain Control (AGC) for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 9-bit video CMOS Analog-To-Digital Converters (ADCs), digitized CVBS or Y/C signals are available on the IPD (Image Port Data) port under ${ }^{2} \mathrm{C}$-bus control
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal sync processing and clock generation, horizontal and vertical sync detection
- Requires only one crystal (either 24.576 MHz or 32.11 MHz ) for all standards
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, combination PAL N, PAL M, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Brightness Contrast Saturation (BCS) and hue control on-chip
- Two multi functional real-time output pins controlled by $I^{2} \mathrm{C}$-bus
- Multi-standard VBI data slicer decoding World Standard Teletext (WST), North-American Broadcast Text System (NABTS), Closed Caption (CC), Wide Screen Signalling (WSS), Video Programming System (VPS), Vertical Interval Time Code (VITC) variants (EBU/SMPTE) etc.
- Standard ITU 656 Y- $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2 format (8-bit) on IPD output bus

- Enhanced ITU 656 output format on IPD output bus containing:
- active video
- raw CVBS data for INTERCAST applications ( 27 MHz data rate)
- decoded VBI data
- Detection of copy protected input signals according to the macrovision standard. Can be used to prevent unauthorized recording of pay-TV or video tape signals.


### 1.2 Video scaler

- Both up and downscaling
- Conversion to square pixel format
- NTSC to 288 lines (video phone)
- Phase accuracy better than $1 / 64$ pixel or line, horizontally or vertically
- Independent scaling definitions for odd and even fields
- Anti-alias filter for horizontal scaling
- Provides output as
- scaled active video
- raw CVBS data for INTERCAST, WAVE-PHORE, POPCON applications or general VBI data decoding ( 27 MHz or sample rate converted)
- Local video output for $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2 format (VMI, VIP, ZV).


### 1.3 Video encoder

- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 45 MHz at double edged clocking, synthesized on-chip or from external source
- Up to $800 \times 600$ graphics data at 60 Hz or 50 Hz with programmable underscan range
- Three Digital-to-Analog Converters (DACs) at 27 MHz sample rate for CVBS (BLUE, $\mathrm{C}_{\mathrm{B}}$ ), VBS (GREEN, CVBS) and $C$ (RED, $C_{R}$ ) (signals in parenthesis are optional); all at 10-bit resolution


## PC-CODEC

- Selectable cross-colour reduction to improve CVBS output
- Non-interlaced $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ or RGB input at maximum 4:4:4 sampling
- Downscaling from $1: 1$ to $1: 2$ and up to $20 \%$ upscaling
- Optional interlaced $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ input Digital Versatile Disk (DVD)
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode, maximum 45 MHz )
- $3 \times 256$ bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- Programmable border colour of underscan area
- On-chip 27 MHz crystal oscillator (3rd-harmonic or fundamental 27 MHz crystal)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Optional support of various VBI data insertion as
- WST-625, WSS, VPS
- WST-525, NABTS
- Closed Caption, Copy Generation Management System (CGMS)
- Macrovision Pay-per-View copy protection system rev. 7.01 and rev. 6.1 as option; this applies to SAA7108E only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.


### 1.4 Common features

- 5 V tolerant digital I/O ports
- $I^{2} \mathrm{C}$-bus controlled (full read-back ability by an external controller, bit rate up to 400 kbits/s)
- Versatile power-save modes
- Boundary scan test circuit complies with the "IEEE Std. 1149.b1-1994" (separate ID codes for decoder and encoder)
- Monolithic CMOS 3.3 V device
- BGA156 package
- Moisture Sensitive Level (MSL): e3.


## 2 APPLICATIONS

- Notebook (low-power consumption)
- PCMCIA card application
- AGP based graphics cards
- PC editing
- Image processing
- Video phone applications
- INTERCAST and PC teletext applications
- Security applications
- Hybrid satellite set-top boxes.


## 3 GENERAL DESCRIPTION

The SAA7108E; SAA7109E is a new multi-standard video decoder and encoder chip, offering high quality video input and TV output processing as required by PC-99 specifications. It enables hardware manufacturers to implement versatile video functions on a significantly reduced printed-circuit board area at very competitive costs.

Separate pins for supply voltages as well as for $\mathrm{I}^{2} \mathrm{C}$-bus control and boundary scan test have been provided for the video encoder and decoder sections to ensure both flexible handling and optimized noise behaviour.

The video encoder is used to encode PC graphics data at maximum $800 \times 600$ resolution to PAL ( 50 Hz ) or NTSC $(60 \mathrm{~Hz})$ video signals. A programmable scaler and interlacer ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V -syncs as well, thereby serving as an auxiliary monitor at maximum $800 \times 600$ resolution $/ 60 \mathrm{~Hz}$ (PIXCLK < 45 MHz ).

The video decoder, a 9-bit video input processor, is a combination of a 2-channel analog pre-processing circuit
including source selection, anti-aliasing filter and Analog-to-Digital Converter (ADC), automatic clamp and gain control, a Clock Generation Circuit (CGC), and a digital multi-standard decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM).
The decoder includes a brightness, contrast and saturation control circuit, a multi-standard VBI data slicer and a 27 MHz VBI data bypass. The pure 3.3 V (5 V compatible) CMOS circuit SAA7108E; SAA7109E, consisting of an analog front-end and digital video decoder, a digital video encoder and analog back-end, is a highly integrated circuit especially designed for desktop video applications.

The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU-R BT. 601 compatible colour component values.

The encoder can operate fully independently at its own variable pixel clock, transporting graphics input data, and at the line-locked, single crystal-stable video encoding clock.

As an option, it is possible to slave the video PAL/NTSC encoding to the video decoder clock with the encoder FIFO acting as a buffer to decouple the line-locked decoder clock from the crystal-stable encoder clock.

## 4 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{V}_{\text {DDD }}$ | digital supply voltage |  | 3.0 | 3.3 | 3.6 | V |
| $\mathrm{~V}_{\mathrm{DDA}}$ | analog supply voltage |  | 3.15 | 3.3 | 3.45 | V |
| $\mathrm{~T}_{\mathrm{amb}}$ | ambient temperature |  | 0 | - | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{P}_{\mathrm{A}+\mathrm{D}}$ | analog and digital power dissipation | note 1 | - | - | 1.4 | W |

## Note

1. Power dissipation is extremely dependent on programming and selected application.

## 5 ORDERING INFORMATION

| TYPE <br> NUMBER | PACKAGE |  |  |
| :---: | :---: | :---: | :---: |
|  | NAME | DESCRIPTION | VERSION |
| SAA7108E | BGA156 | plastic ball grid array package; 156 balls; body $15 \times 15 \times 1.15 \mathrm{~mm}$ | SOT472-1 |
| SAA7109E |  |  |  |

## 6 BLOCK DIAGRAMS



Fig. 1 Simplified block diagram.


Fig. 2 Block diagram (video encoder part).


The pins RTCO and ALRCLK are used for configuration of the ${ }^{12} \mathrm{C}$-bus interface
and the definition of the crystal oscillator frequency at RESET (pin strapping).
Fig. 3 Block diagram (video decoder part).

## 7 PINNING

| SYMBOL | PIN | TYPE ${ }^{(1)}$ | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| PD7 | A2 | I | MSB of encoder input bus with $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$; see Tables 25 to 31 for pin assignment |
| PD4 | A3 | I | MSB - 3 of encoder input bus with $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2; see Tables 25 to 31 for pin assignment |
| $\overline{\text { TRSTe }}$ | A4 | 1/pu | test reset input for Boundary Scan Test (BST) (encoder); active LOW; with internal pull-up; notes 2 and 3 |
| XTALIe | A5 | I | 27 MHz crystal input (encoder) |
| XTALOe | A6 | 0 | 27 MHz crystal output (encoder) |
| DUMP | A7 | 0 | DAC reference pin (encoder), $12 \Omega$ resistor connected to $\mathrm{V}_{\text {SSAe }}$ |
| $\mathrm{V}_{\text {SSXe }}$ | A8 | S | ground for oscillator (encoder) |
| RSET | A9 | 0 | DAC reference pin (encoder), $1 \mathrm{k} \Omega$ resistor connected to $\mathrm{V}_{\text {SSAe }}$ |
| $\mathrm{V}_{\text {DDAe }}$ | A10 | S | 3.3 V analog supply voltage (encoder) |
| HPD0 | A11 | I/O | MSB - 7 of Host Port Data (HPD) output bus |
| HPD3 | A12 | I/O | MSB - 4 of HPD output bus |
| HPD7 | A13 | I/O | MSB of HPD output bus |
| PD9 | B1 | I | see Tables 25, 30 and 31 for pin assignment with different encoder input formats |
| PD8 | B2 | I | see Tables 25, 30 and 31 for pin assignment with different encoder input formats |
| PD5 | B3 | I | MSB - 2 of encoder input bus with $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2; see Tables 25 to 31 for pin assignment |
| PD6 | B4 | I | MSB - 1 of encoder input bus with $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2; see Tables 25 to 31 for pin assignment |
| TDIe | B5 | 1/pu | test data input for BST (encoder); note 4 |
| $\mathrm{V}_{\text {DDAe }}$ | B6 | S | 3.3 V analog supply voltage (encoder) |
| DUMP | B7 | 0 | DAC reference pin (encoder); connected to A7 |
| $\mathrm{V}_{\text {SSAe }}$ | B8 | S | analog ground (encoder) |
| $\mathrm{V}_{\text {DDAe }}$ | B9 | S | 3.3 V analog supply voltage (encoder) |
| TEST1 | B10 | 1 | scan test input 1, do not connect |
| HPD1 | B11 | I/O | MSB - 6 of HPD output bus |
| HPD4 | B12 | I/O | MSB - 3 of HPD output bus |
| IPD0 | B13 | 0 | MSB - 7 of IPD output bus |
| IPD4 | B14 | 0 | MSB - 3 of Image Port Data (IPD) output bus |
| PD11 | C1 | I | see Tables 25,30 and 31 for pin assignment with different encoder input formats |
| PD10 | C2 | I | see Tables 25, 30 and 31 for pin assignment with different encoder input formats |
| TTX_SRES | C3 | 1 | teletext input or sync reset input (encoder) |
| TTXRQ_XCLKO2 | C4 | O | teletext request output or 13.5 MHz clock output of the crystal oscillator (encoder) |
| $\mathrm{V}_{\text {SSIe }}$ | C5 | S | digital ground core (encoder) |
| BLUE_CB_CVBS | C6 | 0 | BLUE or $\mathrm{C}_{\mathrm{B}}$ or CVBS output |


| SYMBOL | PIN | TYPE ${ }^{(1)}$ | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| GREEN_VBS_CVBS | C7 | O | GREEN or VBS or CVBS output |
| RED_CR_C | C8 | 0 | RED or $\mathrm{C}_{\mathrm{R}}$ or C output |
| $\mathrm{V}_{\text {DDAe }}$ | C9 | S | 3.3 V analog supply voltage (encoder) |
| TEST2 | C10 | I | scan test input 2, do not connect |
| HPD2 | C11 | I/O | MSB - 5 of HPD output bus |
| HPD5 | C12 | I/O | MSB - 2 of HPD output bus |
| IPD1 | C13 | 0 | MSB - 6 of IPD output bus |
| IPD5 | C14 | 0 | MSB - 2 of IPD output bus |
| TDOe | D1 | 0 | test data output for BST (encoder); note 4 |
| RESET | D2 | I | reset input (encoder); active LOW |
| TMSe | D3 | I/pu | test mode select input for BST (encoder); note 4 |
| $\mathrm{V}_{\text {DDle }}$ | D4 | S | 3.3 V digital supply voltage for core (encoder) |
| $\mathrm{V}_{\text {SSIe }}$ | D5 | S | digital ground core (encoder) |
| $\mathrm{V}_{\text {DDXe }}$ | D6 | S | 3.3 V supply voltage for oscillator (encoder) |
| VSM | D7 | 0 | vertical synchronization output to VGA monitor (non-interlaced) |
| HSM_CSYNC | D8 | 0 | horizontal synchronization output to VGA monitor (non-interlaced) or composite sync for RGB-SCART |
| $\mathrm{V}_{\text {DDAe }}$ | D9 | S | 3.3 V analog supply voltage (encoder) |
| $V_{\text {DDEd }}$ | D10 | S | 3.3 V digital supply voltage for peripheral cells (decoder) |
| $\mathrm{V}_{\text {DDId }}$ | D11 | S | 3.3 V digital supply voltage for core (decoder) |
| HPD6 | D12 | I/O | MSB - 1 of HPD output bus |
| IPD2 | D13 | 0 | MSB - 5 of IPD output bus |
| IPD6 | D14 | O | MSB - 1 of IPD output bus |
| TCLKe | E1 | I/pu | test clock input for BST (encoder); note 4 |
| SCLe | E2 | I | $\mathrm{I}^{2} \mathrm{C}$-bus serial clock input (encoder) |
| HSVGC | E3 | I/O | horizontal synchronization output to Video Graphics Controller (VGC) (optional input) |
| $\mathrm{V}_{\text {SSEe }}$ | E4 | S | digital ground peripheral cells (encoder) |
| $\mathrm{V}_{\text {SSId }}$ | E11 | S | digital ground core (decoder) |
| n.c. | E12 | - | not connected |
| IPD3 | E13 | 0 | MSB - 4 of IPD output bus |
| IPD7 | E14 | 0 | MSB of IPD output bus |
| VSVGC | F1 | I/O | vertical synchronization output to VGC (optional input) |
| PIXCLKI | F2 | 1 | pixel clock input (looped through) |
| PD3 | F3 | I | MSB - 4 of encoder input bus with $C_{B}-Y-C_{R} 4: 2: 2$; see Tables 25 to 31 for pin assignment |
| $\mathrm{V}_{\text {DDEe }}$ | F4 | S | 3.3 V digital supply voltage for peripheral cells (encoder) |
| $\mathrm{V}_{\text {DDId }}$ | F11 | S | 3.3 V digital supply voltage for core (decoder) |
| n.c. | F12 | - | not connected |
| IGPV | F13 | 0 | multi-purpose vertical reference output with IPD output bus |
| IGP0 | F14 | 0 | general purpose output signal 0 with IPD output bus |


| SYMBOL | PIN | TYPE ${ }^{(1)}$ | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| FSVGC | G1 | I/O | frame synchronization output to VGC (optional input) |
| SDAe | G2 | I/O | $1^{2} \mathrm{C}$-bus serial data input/output (encoder) |
| $\overline{\mathrm{CBO}}$ | G3 | 0 | composite blanking output to VGC; active LOW |
| PIXCLKO | G4 | 0 | pixel clock output to VGC |
| $V_{\text {DDEd }}$ | G11 | S | 3.3 V digital supply voltage for peripheral cells (decoder) |
| IGPH | G12 | 0 | multi-purpose horizontal reference output with IPD output bus |
| IGP1 | G13 | 0 | general purpose output signal 1 with IPD output bus |
| ITRI | G14 | I/(0) | programmable control signals for IPD output bus |
| PD2 | H1 | I | MSB - 5 of encoder input bus with $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}} 4$ : $2: 2$; see Tables 25 to 31 for pin assignment |
| PD1 | H2 | I | MSB - 6 of encoder input bus with $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$; see Tables 25 to 31 for pin assignment |
| PD0 | H3 | I | MSB - 7 of encoder input bus with $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$; see Tables 25 to 31 for pin assignment |
| $\mathrm{V}_{\text {SSEd }}$ | H4 | S | digital ground for peripheral cells (decoder) |
| $\mathrm{V}_{\text {SSEd }}$ | H11 | S | digital ground for peripheral cells (decoder) |
| ICLK | H12 | I/O | clock for IPD output bus (optional clock input) |
| TEST0 | H13 | O | scan test output, do not connect |
| IDQ | H14 | $\bigcirc$ | data qualifier for IPD output bus |
| TEST4 | J1 | 0 | scan test output, do not connect |
| TEST5 | J2 | I | scan test input, do not connect |
| TEST3 | J3 | I | scan test input, do not connect |
| $\mathrm{V}_{\text {DDId }}$ | J4 | S | 3.3 V digital supply voltage for core (decoder) |
| $\mathrm{V}_{\text {DDId }}$ | J11 | S | 3.3 V digital supply voltage for core (decoder) |
| AMXCLK | J12 | 1 | audio master external clock input |
| ALRCLK | J13 | (I/)O | audio left/right clock output; can be strapped to supply via a $3.3 \mathrm{k} \Omega$ resistor to indicate that the default 24.576 MHz crystal (ALRCLK = 0; internal pull-down) has been replaced by a 32.110 MHz crystal (ALRCLK = 1); notes 5 and 6 |
| ITRDY | J14 | I | target ready input for IPD output bus |
| XTRI | K1 | 1 | control signal for all X port pins |
| XPD7 | K2 | I/O | MSB of XPD bus |
| XPD6 | K3 | I/O | MSB - 1 of XPD bus |
| $\mathrm{V}_{\text {SSId }}$ | K4 | S | digital ground core (decoder) |
| $\mathrm{V}_{\text {SSId }}$ | K11 | S | digital ground core (decoder) |
| AMCLK | K12 | 0 | audio master clock output, must be less than $50 \%$ of crystal clock |
| RTS0 | K13 | 0 | real-time status or sync information line 0 |
| ASCLK | K14 | 0 | audio serial clock output |
| XPD5 | L1 | I/O | MSB - 2 of XPD bus |
| XPD4 | L2 | I/O | MSB - 3 of XPD bus |
| XPD3 | L3 | I/O | MSB - 4 of XPD bus |
| $\mathrm{V}_{\text {DDId }}$ | L4 | S | 3.3 V digital supply voltage for core (decoder) |
| XRV | L5 | I/O | vertical reference for XPD bus |


| SYMBOL | PIN | TYPE ${ }^{(1)}$ | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {SSEd }}$ | L6 | S | digital ground for peripheral cells (decoder) |
| $\mathrm{V}_{\text {DDEd }}$ | L7 | S | 3.3 V digital supply voltage for peripheral cells (decoder) |
| $\mathrm{V}_{\text {DDXd }}$ | L8 | S | 3.3 V supply voltage for oscillator (decoder) |
| $V_{\text {DDEd }}$ | L9 | S | 3.3 V digital supply voltage for peripheral cells (decoder) |
| RTS1 | L10 | 0 | real-time status or sync information line 1 |
| V ${ }_{\text {DDId }}$ | L11 | S | 3.3 V digital supply voltage for core (decoder) |
| SDAd | L12 | I/O | $\mathrm{I}^{2} \mathrm{C}$-bus serial data input/output (decoder) |
| RTCO | L13 | (I/) O | real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence (see external document "RTC Functional Description", available on request); the RTCO pin is enabled via ${ }^{2}{ }^{2} \mathrm{C}$-bus bit RTCE; see notes 5 and 7 and Table 146 |
| LLC2 | L14 | 0 | line-locked $1 / 2$ clock output (13.5 MHz nominal) |
| XPD2 | M1 | I/O | MSB - 5 of XPD bus |
| XPD1 | M2 | I/O | MSB - 6 of XPD bus |
| XCLK | M3 | I/O | clock for XPD bus |
| XDQ | M4 | I/O | data qualifier for XPD bus |
| TMSd | M5 | I/pu | test mode select input for BST (decoder); note 4 |
| TCLKd | M6 | I/pu | test clock input for BST (decoder); note 4 |
| $\mathrm{V}_{\text {SSAd }}$ | M7 | S | analog ground (decoder) |
| $\mathrm{V}_{\text {DDAd }}$ | M8 | S | 3.3 V analog supply voltage (decoder) |
| $\mathrm{V}_{\text {DDAd }}$ | M9 | S | 3.3 V analog supply voltage (decoder) |
| AOUT | M10 | 0 | analog test output (do not connect) |
| SCLd | M11 | 1 | $\mathrm{I}^{2} \mathrm{C}$-bus serial clock input (decoder) |
| $\overline{\text { RES }}$ | M12 | 0 | reset output signal; active LOW (decoder) |
| $\mathrm{V}_{\text {SSEd }}$ | M13 | S | digital ground for peripheral cells (decoder) |
| LLC | M14 | 0 | line-locked clock output (27 MHz nominal) |
| XPD0 | N1 | I/O | MSB - 7 of XPD bus |
| XRH | N2 | I/O | horizontal reference for XPD bus |
| XRDY | N3 | O | data input ready for XPD bus |
| TRSTd | N4 | 1/pu | test reset input for BST (decoder); active LOW; with internal pull-up; notes 2 and 3 |
| TDOd | N5 | O | test data output for BST (decoder); note 4 |
| TDId | N6 | 1/pu | test data input for BST (decoder); note 4 |
| $\mathrm{V}_{\text {SSAd }}$ | N7 | S | analog ground (decoder) |
| $\mathrm{V}_{\text {SSAd }}$ | N8 | S | analog ground (decoder) |
| $\mathrm{V}_{\text {SSAd }}$ | N9 | S | analog ground (decoder) |
| AGND | N10 | S | analog ground (decoder) connected to substrate |
| $\mathrm{V}_{\text {DDAd }}$ | N11 | S | 3.3 V analog supply voltage (decoder) |
| $\mathrm{V}_{\text {SSAd }}$ | N12 | S | analog ground (decoder) |
| $\mathrm{V}_{\text {SSAd }}$ | N13 | S | analog ground (decoder) |
| CE | N14 | 1 | chip enable or reset input (with internal pull-up) |


| SYMBOL | PIN | TYPE $^{(1)}$ ) | DESCRIPTION |
| :--- | :---: | :---: | :--- |
| XTALId | P2 | I | 27 MHz crystal input (decoder) |
| XTALOd | P3 | O | 27 MHz crystal output (decoder) |
| XTOUTd | P4 | O | crystal oscillator output signal (decoder); auxiliary signal |
| V $_{\text {SSXd }}$ | P5 | S | ground for crystal oscillator (decoder) |
| Al24 | P6 | I | analog input 24 |
| Al23 | P7 | I | analog input 23 |
| Al2D | P8 | I | differential analog input for channel 2; connect to ground via a capacitor |
| Al22 | P9 | I | analog input 22 |
| Al21 | P10 | I | analog input 21 |
| Al12 | P11 | I | analog input 12 |
| Al1D | P12 | I | differential analog input for channel 1; connect to ground via a capacitor |
| Al11 | P13 | I | analog input 11 |

## Notes

1. Pin type: $I=$ input, $O=$ output, $S=$ supply, $p u=$ pull-up.
2. For board design without boundary scan implementation connect TRSTe and TRSTd to ground.
3. This pin provides easy initialization of the Boundary Scan Test (BST) circuit. TRSTe and TRSTd can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.
4. In accordance with the "IEEE1149.1" standard the pads TDIe (TDId), TMSe (TMSd), TCLKe (TCLKd) and TRSTe (TRSTd) are input pads with an internal pull-up resistor and TDOe (TDOd) is a 3-state output pad.
5. Pin strapping is done by connecting the pin to supply via a $3.3 \mathrm{k} \Omega$ resistor. During the power-up reset sequence the corresponding pins are switched to input mode to read the strapping level. For the default setting no strapping resistor is necessary (internal pull-down).
6. Pin ALRCLK: $0=24.576 \mathrm{MHz}$ crystal (default); $1=32.110 \mathrm{MHz}$ crystal.
7. Pin RTCO: operates as $1^{2} \mathrm{C}$-bus slave address pin; RTCO $=0$ slave address $42 \mathrm{H} / 43 \mathrm{H}$ (default); RTCO $=1$ slave address $40 \mathrm{H} / 41 \mathrm{H}$.

|  | мнвв |
| :---: | :---: |
|  | $\bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc 00000$ |
|  | $\bigcirc 0000000000000$ |
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|  | $\bigcirc 0000$ |
|  | ○○○ O O O O |
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|  | $\bigcirc \bigcirc \bigcirc \bigcirc$ SAA7109E ○ ○ ○ ○ |
|  | $\bigcirc 000000$ |
|  | 0000000 |
|  | $\bigcirc 0000000000000$ |
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|  | $\bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc 000000$ |

Fig. 4 Pin configuration.
Table 1 Pin assignment (top view)


## 8 FUNCTIONAL DESCRIPTION OF DIGITAL VIDEO ENCODER PART

The digital video encoder encodes digital luminance and colour difference signals ( $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ ) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or $\mathrm{C}_{\mathrm{R}}-\mathrm{Y}-\mathrm{C}_{\mathrm{B}}$ signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7108E; SAA7109E can be directly connected to a PC video graphics controller with a maximum resolution of $800 \times 600$ at a 50 or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : $2 \mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ input format (using 8 pins with double edge clocking), other $C_{B}-Y-C_{R}$ and RGB formats are also supported; see Tables 25 to 31 .

A complete $3 \times 256$ bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port PD (Pixel Data) or via the $I^{2} \mathrm{C}$-bus.
The SAA7108E; SAA7109E supports a $32 \times 32 \times 2$-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the $\mathrm{I}^{2} \mathrm{C}$-bus.

It is also possible to encode interlaced 4:2:2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

Besides the applications for video output, the SAA7108E; SAA7109E can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.
The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal $4: 2: 2$ bandwidth in the luminance/colour difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of "RS-170-A" and "ITU-R BT.470-3".

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figs 5 to 10. All three DACs are realized with full 10-bit resolution. The $C_{R}-Y-C_{B}$ to RGB dematrix can be bypassed (optionally) in order to provide the upsampled $\mathrm{C}_{\mathrm{R}}-\mathrm{Y}-\mathrm{C}_{\mathrm{B}}$ input signals.
The 8-bit multiplexed $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ formats are "ITU-R BT.656" (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in slave mode. For assignment of the input data to the rising or falling clock edge see Tables 25 to 31.
In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.
The SAA7108E; SAA7109E synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals from that clock.
Wide screen signalling data can be loaded via the $\mathrm{I}^{2} \mathrm{C}$-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the $\mathrm{I}^{2} \mathrm{C}$-bus.

The IC also contains Closed Caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Fig.50). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.

(1) $\mathrm{SCBW}=1$
(2) $\mathrm{SCBW}=0$.

Fig. 5 Chrominance transfer characteristic 1.


(1) $\mathrm{CCRS} 1=0 ; \mathrm{CCRS}=1$.
(2) $\mathrm{CCRS} 1=1 ; \mathrm{CCRS} 0=0$.
(3) $\mathrm{CCRS} 1=1 ; \mathrm{CCRS} 0=1$.
(4) $\mathrm{CCRS} 1=0 ; \mathrm{CCRS} 0=0$.

Fig. 7 Luminance transfer characteristic 1 (excluding scaler).

(1) $\mathrm{CCRS} 1=0 ; \mathrm{CCRS} 0=0$.

Fig. 8 Luminance transfer characteristic 2 (excluding scaler).


Fig. 9 Luminance transfer characteristic in RGB (excluding scaler).


Fig. 10 Colour difference transfer characteristic in RGB (excluding scaler).

### 8.1 Reset conditions

To activate the reset a pulse at least of 2 crystal clocks duration is required.

During reset (RESET = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{\mathrm{CBO}}, \mathrm{HSVGC}$ and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3 -state. A reset also forces the $I^{2} \mathrm{C}$-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an $\mathrm{I}^{2} \mathrm{C}$-bus access redefines the corresponding registers; see Table 2.

Table 2 Strapping pins

| PIN | TIED | PRESET |
| :---: | :---: | :---: |
| FSVGC (pin G1) | LOW | NTSC M encoding, PIXCLK fits to $640 \times 480$ graphics input |
|  | HIGH | PAL B/G encoding, PIXCLK fits to $640 \times 480$ graphics input |
| VSVGC (pin F1) | LOW | 4 : 2 : $2 \mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ graphics input (format 0) |
|  | HIGH | 4:4:4 RGB graphics input (format 3) |
| $\overline{\mathrm{CBO}}$ (pin G3) | LOW | input demultiplex phase: LSB = LOW |
|  | HIGH | input demultiplex phase: $\mathrm{LSB}=\mathrm{HIGH}$ |
| HSVGC (pin E3) | LOW | input demultiplex phase: MSB = LOW |
|  | HIGH | input demultiplex phase: $\mathrm{MSB}=\mathrm{HIGH}$ |
| $\begin{aligned} & \hline \text { TTXRQ_XCLKO2 } \\ & \text { (pin C4) } \end{aligned}$ | LOW | slave (FSVGC, VSVGC and HSVGC are inputs, internal colour bar is active) |
|  | HIGH | master (FSVGC, VSVGC and HSVGC are outputs) |

### 8.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or $Y-C_{B}-C_{R}$, to a common internal $R G B$ or $Y-C_{B}-C_{R}$ data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the $\mathrm{I}^{2} \mathrm{C}$-bus control bits EDGE1 and EDGE2 for correct operation.

If $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ is being applied as a 27 Mbyte /s data stream, the output of the input formatter can be used directly to feed the video encoder block.

### 8.3 RGB LUT

The three 256-byte RAMs of this block can be addressed by three 8 -bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed colour data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an $\mathrm{I}^{2} \mathrm{C}$-bus write access or can be part of the pixel data input through the PD port. In the latter case, $256 \times 3$ bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

### 8.4 Cursor insertion

A $32 \times 32$ dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an $\mathrm{I}^{2} \mathrm{C}$-bus write access to specific registers or in the pixel data input via the PD port. In the latter case the 256 bytes defining the cursor bit map ( 2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceeding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE ${ }^{2}$ C-bus register as described in Table 5.
Transparent means that the input pixels are passed through, the 'cursor colours' can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1 , the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 3 Layout of a byte in the cursor bit map

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| pixel $\mathrm{n}+3$ |  | pixel $\mathrm{n}+2$ |  | pixel $\mathrm{n}+1$ |  | pixel $n$ |  |
| D1 | D0 | D1 | D0 | D1 | D0 | D1 | D0 |

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the 'hot spot', the other register controls the insertion position. The hot spot is the 'tip' of the pointer arrow.

It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 4 Cursor bit map

| BYTE | D7 D6 | D5 D4 | D3 D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | row 0 column 3 | row 0 column 2 | row 0 column 1 | row 0 column 0 |  |
| 1 | row 0 column 7 | row 0 column 6 | row 0 column 5 | row 0 column 4 |  |
| 2 | row 0 column 11 | row 0 column 10 | row 0 column 9 | row 0 column 8 |  |
| ... | $\ldots$ | $\ldots$ | ... | ... |  |
| 6 | row 0 column 27 | row 0 column 26 | row 0 column 25 | row 0 column 24 |  |
| 7 | row 0 column 31 | row 0 column 30 | row 0 column 29 | row 0 column 28 |  |
| ... | ... | ... | ... | ... |  |
| 254 | row 31 column 27 | row 31 column 26 | row 31 column 25 | row 31 column 24 |  |
| 255 | row 31 column 31 | row 31 column 30 | row 31 column 29 | row 31 column 28 |  |

Table 5 Cursor modes

| CURSOR <br> PATTERN | CURSOR MODE |  |
| :--- | :--- | :--- |
|  | CMODE = 0 | CMODE = 1 |
| 00 | second cursor colour | second cursor colour |
| 01 | first cursor colour | first cursor colour |
| 10 | transparent | transparent |
| 11 | inverted input | auxiliary cursor <br> colour |

### 8.5 RGB Y- $C_{B}-C_{R}$ matrix

RGB input signals to be encoded to PAL or NTSC are converted to the $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ colour space in this block. The colour difference signals are fed through low-pass filters and formatted to a ITU-R BT. 601 like 4 : 2 : 2 data stream for further processing.

The matrix and formatting blocks can be bypassed for $Y-C_{B}-C_{R}$ graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

### 8.6 Horizontal scaler

The high quality horizontal scaler operates on the $4: 2: 2$ data stream. Its control engines compensate the colour phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC $=0$, this sets the scaling factor to 1 .

If the SAA7108E; SAA7109E input data is in accordance with "ITU-R BT.656", the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1 . With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a $4: 2$ : 2 data stream at the scaler output.

### 8.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 129.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC $=0$ sets the scaling factor to 1 ; YIWGTO and YIWGTE must not be 0 .

Due to the re-interlacing, the circuit can perform upscaling. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 8.17.

### 8.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the $\mathrm{I}^{2} \mathrm{C}$-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor. It is suggested to refer to Tables 6 to 23 for some representative combinations.

### 8.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true colour tint.

### 8.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd-harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the $I^{2} \mathrm{C}$-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 18 and 44 MHz .

### 8.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

### 8.12 Encoder

### 8.12.1 VIDEO PATH

The encoder generates luminance and colour subcarrier output signals from the $Y, C_{B}$ and $C_{R}$ baseband signals, which are suitable for use as CVBS or separate $Y$ and $C$ signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT. 656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7108E only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 7 and 8. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for $\mathrm{C}_{\mathrm{B}}$ and $\mathrm{C}_{\mathrm{R}}$ ), and a standard dependent burst is inserted, before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be used for the $Y$ and $C$ output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 5 and 6.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, colour is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the $Y$ and $C$ outputs is in accordance with the standards.

### 8.12.2 TELETEXT INSERTION AND ENCODING (NOT SIMULTANEOUSLY WITH REAL-TIME CONTROL)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Fig. 50.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz .

### 8.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the $I^{2} \mathrm{C}$-bus and will be encoded in the appropriate format into line 16.

### 8.12.4 Closed Caption encoder

Using this circuit, data in accordance with the specification of Closed Caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

### 8.12.5 ANTI-TAPING (SAA7108E ONLY)

For more information contact your nearest Philips Semiconductors sales office.

### 8.13 RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before $Y, C_{B}$ and $C_{R}$ signals are de-matrixed, individual gain adjustment for $Y$ and colour difference signals and 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed.

The transfer curves of luminance and colour difference components of RGB are illustrated in Figs 9 and 10.

### 8.14 Triple DAC

Both Y and C signals are converted from digital-to-analog in a 10-bit resolution at the output of the video encoder. Y and C signals are also combined into a 10 -bit CVBS signal.

The CVBS output signal occurs with the same processing delay as the $\mathrm{Y}, \mathrm{C}$ and optional $R G B$ or $\mathrm{C}_{\mathrm{R}}-\mathrm{Y}-\mathrm{C}_{\mathrm{B}}$ outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $15 / 16$ with respect to $Y$ and C DACs to make maximum use of the conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 10-bit resolution.

The reference currents of all three DACs can be adjusted individually in order to adapt for different output signals. In addition, all reference currents can be adjusted commonly to compensate for small tolerances of the on-chip band gap reference voltage.

Alternatively, all currents can be switched off to reduce power dissipation.

All three outputs can be used to sense for an external load (usually $75 \Omega$ ) during a pre-defined output. A flag in the $\mathrm{I}^{2} \mathrm{C}$-bus status byte reflects whether a load is applied or not.

If the SAA7108E; SAA7109E is required to drive a second (auxiliary) VGA monitor, the DACs receive the signal directly from the cursor insertion block. In this event, the DACs are clocked at the incoming PIXCLKI instead of the 27 MHz crystal clock used in the video encoder.

### 8.15 Timing generator

The synchronization of the SAA7108E; SAA7109E is able to operate in two modes; slave mode and master mode.
In slave mode, the circuit accepts sync pulses on the bidirectional FSVGC (frame sync), VSVGC (vertical sync) and HSVGC (horizontal sync) pins: the polarities of the signals can be programmed. The frame sync signal is only necessary when the input signal is interlaced, in other cases it may be omitted. If the frame sync signal is present, it is possible to derive the vertical and the horizontal phase from it by setting the HFS and VFS bits. HSVGC and VSVGC are not necessary in this case, so it is possible to switch the pins to output mode.

Alternatively, the device can be triggered by auxiliary codes in a ITU-R BT. 656 data stream via PD7 to PD0.

Only vertical frequencies of 50 and 60 Hz are allowed with the SAA7108E; SAA7109E. In slave mode, it is not possible to lock the encoders colour carrier to the line frequency with the PHRES bits.

In the (more common) master mode, the time base of the circuit is continuously free-running. The IC can output a frame sync at pin FSVGC, a vertical sync at pin VSVGC, a horizontal sync at pin HSVGC and a composite blanking signal at pin $\overline{\mathrm{CBO}}$. All of these signals are defined in the PIXCLK domain. The duration of HSVGC and VSVGC are fixed, they are 64 clocks for HSVGC and 1 line for VSVGC. The leading slopes are in phase and the polarities can be programmed.

The input line length can be programmed. The field length is always derived from the field length of the encoder and the pixel clock frequency that is being used.
$\overline{\mathrm{CBO}}$ acts as a data request signal. The circuit accepts input data at a programmable number of clocks after $\overline{\mathrm{CBO}}$ goes active. This signal is programmable and it is possible to adjust the following (see Figs 48 and 49):

- The horizontal offset
- The length of the active part of the line
- The distance from active start to first expected data
- The vertical offset separately for odd and even fields
- The number of lines per input field.

In most cases, the vertical offsets for odd and even fields are equal. If they are not, then the even field will start later. The SAA7108E; SAA7109E will also request the first input lines in the even field, the total number of requested lines will increase by the difference of the offsets.

As stated above, the circuit can be programmed to accept the look-up and cursor data in the first 2 lines of each field. The timing generator provides normal data request pulses for these lines; the duration is the same as for regular lines. The additional request pulses will be suppressed with LUTL set to logic 0; see Table 139. The other vertical timings do not change in this case, so the first active line can be number 2 , counted from 0 .

## $8.16 \quad I^{2} \mathrm{C}$-bus interface

The $\mathrm{I}^{2} \mathrm{C}$-bus interface is a standard slave transceiver, supporting 7 -bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and read, except two read only status bytes.
The register bit map consists of an RGB Look-Up Table (LUT), a cursor bit map and control registers. The LUT contains three banks of 256 bytes, where each RGB triplet is assigned to one address. Thus a write access needs the LUT address and three data bytes following subaddress FFH. For further write access auto-incrementing of the LUT address is performed. The cursor bit map access is similar to the LUT access but contains only a single byte per address.
The $\mathrm{I}^{2} \mathrm{C}$-bus slave address is defined as 88 H .

### 8.17 Programming the graphics acquisition scaler of the video encoder

In order to program the graphics acquisition scaler it is first necessary to determine the input and output field timings. The timings are controlled by decoding binary counters that index the position in the current line and field respectively. In both cases, 0 means the start of the sync pulse.

At 60 Hz , the first visible pixel has the index 256 , 710 pixels can be encoded; at 50 Hz , the index is 284 , 702 pixels can be visible. Some variables are defined below:

- InPix: the number of active pixels per input line
- InPpl: the length of the entire input line in pixel clocks
- InLin: the number of active lines per input field/frame
- TPclk: the pixel clock period
- OutPix: the number of active pixels per output line
- OutLin: the number of active lines per output field
- TXclk: the encoder clock period (37.037 ns).

The output lines should be centred on the screen. It should be noted that the encoder has 2 clocks per pixel; see Table 106.

ADWHS = $256+710-$ OutPix ( 60 Hz );
ADWHS = $284+702-$ OutPix ( 50 Hz );
ADWHE $=$ ADWHS + OutPix $\times 2$ (all frequencies)

For vertical, the procedure is the same. At 60 Hz , the first line with video information is number 19, 240 lines can be active. For 50 Hz , the numbers are 23 and 287;
see Table 112
FAL $=19+\frac{240-\text { OutLin }}{2}(60 \mathrm{~Hz})$;
FAL $=23+\frac{287-\text { OutLin }}{2}(50 \mathrm{~Hz})$;
LAL $=$ FAL + OutLin (all frequencies)
Most TV sets use overscan, and not all pixels respectively lines are visible. There is no standard for the factor, it is highly recommended to make the number of output pixels and lines adjustable. A reasonable underscan factor is $10 \%$, giving approximately 640 output pixels per line.

The total number of pixel clocks per line and the input horizontal offset need to be chosen next. The only constraint is that the horizontal blanking has at least 10 clock pulses.

The required pixel clock frequency can be determined in the following way: Due to the limited internal FIFO size, the input path has to provide all pixels in the same time frame as the encoders vertical active time. The scaler also has to process the first and last border lines for the anti-flicker function. Thus:
TPclk $=\frac{262.5 \times 1716 \times \text { TXclk }}{\operatorname{InPpl} \times \text { integer }\left(\frac{\operatorname{lnLin}+2}{\text { OutLin }} \times 262.5\right)}(60 \mathrm{~Hz})$
TPclk $=\frac{312.5 \times 1728 \times \text { TXclk }}{\operatorname{InPpl} \times \text { integer }\left(\frac{\operatorname{InLin}+2}{\text { OutLin }} \times 312.5\right)}(50 \mathrm{~Hz})$
and for the pixel clock generator PCL $=\frac{\mathrm{TXclk}}{\mathrm{TPclk}} \times 2^{21}$
(all frequencies); see Table 115.
The input vertical offset can be taken from the assumption that the scaler should just have finished writing the first line when the encoder starts reading it:
YOFS $=\frac{\text { FAL } \times 1716 \times \text { TXclk }}{\operatorname{InPpl} \times \text { TPclk }}-2(60 \mathrm{~Hz})$
YOFS $=\frac{\text { FAL } \times 1728 \times \text { TXclk }}{\operatorname{InPpl} \times \text { TPclk }}-2(50 \mathrm{~Hz})$
In most cases the vertical offsets will be the same for odd and even fields. The results should be rounded down.

Once the timings are known the scaler can be programmed.

XOFS can be chosen arbitrarily, the condition being that XOFS + XPIX $\leq$ HLEN is fulfilled. Values given by the VESA display timings are preferred.

HLEN $=\operatorname{InPpl}-1$ XPIX $=\frac{\operatorname{lnPix}}{2} \quad$ XINC $=\frac{\text { OutPix }}{\ln P i x} \times 4096$
XINC needs to be rounded up, it needs to be set to 0 for a scaling factor of 1 .

YPIX = InLin
YSKIP defines the anti-flicker function. 0 means maximum flicker reduction but minimum vertical bandwidth, 4095 gives no flicker reduction and maximum bandwidth.

YINC $=\frac{\text { OutLin }}{\operatorname{lnLin}+2} \times\left(1+\frac{\text { YSKIP }}{4095}\right) \times 4096$
YIWGTO $=\frac{\text { YINC }}{2}+2048$
YIWGTE $=\frac{\text { YINC }- \text { YSKIP }}{2}$
When YINC $=0$ it sets the scaler to scaling factor 1 . The initial weighting factors must not be set to 0 in this case. YIWGTE may go negative. In this event, YINC should be added and YOFSE incremented. This can be repeated as often as necessary to make YIWGTE positive.
Due to the limited amount of memory it is not possible to get valid vertical scaler settings only from the formulae above. In some cases it is necessary to adjust the vertical offsets or the scaler increment to get valid settings.
Tables 6 to 23 show verified settings. They are organised in the following way: The tables are separate for the standard to be encoded, the input resolution and three different anti-flicker filter settings. Each table contains 5 vertical sizes with 5 different offsets. They are intended to be selected according to the current TV set. The corresponding horizontal resolutions of 640 pixels give proper aspect ratios. They can be adjusted according to the formulae above. The next line gives a minimum size intended to fit on the screen under all circumstances. The corresponding horizontal resolution is 620 pixels. Overscan is only possible with an input resolution of $800 \times 600$ pixels. Where possible, the corresponding settings are given on the last lines of the tables.

## PC-CODEC

SAA7108E; SAA7109E

### 8.18 Input levels and formats

The SAA7108E; SAA7109E accepts digital $\mathrm{Y}, \mathrm{C}_{\mathrm{B}}, \mathrm{C}_{\mathrm{R}}$ or RGB data with levels (digital codes) in accordance with "ITU-R BT.601"; see Table 24.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated for by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively $C_{R}-Y-C_{B}$ path features an individual gain setting for luminance ( $G Y$ ) and colour difference signals (GCD). Reference levels are measured with a colour bar, $100 \%$ white, $100 \%$ amplitude and $100 \%$ saturation.

Table 6 Y scaler programming at NTSC, input frame size: $640 \times 400$, full anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

Regular size (horizontal TV size: $\mathbf{6 4 0}$ pixels, offset $\pm \mathbf{1 0}$ pixels)

| 212 | -4 | 29 | 241 | 1851099 | 2163 | 0 | 52 | 52 | 3128 | 1080 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 212 | -2 | 31 | 243 | 1851099 | 2163 | 0 | 56 | 56 | 3128 | 1080 |
| 212 | 0 | 33 | 245 | 1851099 | 2163 | 0 | 60 | 60 | 3128 | 1080 |
| 212 | 2 | 35 | 247 | 1851099 | 2163 | 0 | 63 | 63 | 3128 | 1080 |
| 212 | 4 | 37 | 249 | 1851099 | 2163 | 0 | 67 | 67 | 3128 | 1080 |
| 214 | -4 | 28 | 242 | 1836201 | 2181 | 0 | 50 | 50 | 3138 | 1090 |
| 214 | -2 | 30 | 244 | 1836201 | 2181 | 0 | 54 | 54 | 3138 | 1090 |
| 214 | 0 | 32 | 246 | 1836201 | 2181 | 0 | 57 | 57 | 3138 | 1090 |
| 214 | 2 | 34 | 248 | 1836201 | 2181 | 0 | 61 | 61 | 3138 | 1090 |
| 214 | 4 | 36 | 250 | 1836201 | 2181 | 0 | 65 | 65 | 3138 | 1090 |
| 216 | -4 | 27 | 243 | 1817578 | 2202 | 0 | 47 | 47 | 3148 | 1100 |
| 216 | -2 | 29 | 245 | 1817578 | 2202 | 0 | 51 | 51 | 3148 | 1100 |
| 216 | 0 | 31 | 247 | 1817578 | 2202 | 0 | 55 | 55 | 3148 | 1100 |
| 216 | 2 | 33 | 249 | 1817578 | 2202 | 0 | 58 | 58 | 3148 | 1100 |
| 216 | 4 | 35 | 251 | 1817578 | 2202 | 0 | 62 | 62 | 3148 | 1100 |
| 218 | -4 | 26 | 244 | 1802680 | 2222 | 0 | 45 | 45 | 3158 | 1110 |
| 218 | -2 | 28 | 246 | 1802680 | 2222 | 0 | 49 | 49 | 3158 | 1110 |
| 218 | 0 | 30 | 248 | 1802680 | 2222 | 0 | 53 | 53 | 3158 | 1110 |
| 218 | 2 | 32 | 250 | 1802680 | 2222 | 0 | 56 | 56 | 3158 | 1110 |
| 218 | 4 | 34 | 252 | 1802680 | 2222 | 0 | 60 | 60 | 3158 | 1110 |
| 220 | -4 | 25 | 245 | 1784057 | 2245 | 0 | 43 | 43 | 3168 | 1120 |
| 220 | -2 | 27 | 247 | 1784057 | 2245 | 0 | 46 | 46 | 3168 | 1120 |
| 220 | 0 | 29 | 249 | 1784057 | 2245 | 0 | 50 | 50 | 3168 | 1120 |
| 220 | 2 | 31 | 251 | 1784057 | 2245 | 0 | 54 | 54 | 3168 | 1120 |
| 220 | 4 | 33 | 253 | 1784057 | 2245 | 0 | 57 | 57 | 3168 | 1120 |
| $0 v a n$ | 4 | 2 | 2 |  |  |  |  |  |  |  |


| Overscan (horizontal size: 710 pixels) |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 241 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Small size (horizontal size: 620 pixels) |  |  |  |  |  |  |  |  |  |  |
| 204 | 0 | 37 | 241 | 1925590 | 2079 | 0 | 70 | 70 | 3087 | 1039 |

## PC-CODEC

SAA7108E; SAA7109E

Table 7 Y scaler programming at NTSC, input frame size: $640 \times 400$, half anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

Regular size (horizontal TV size: $\mathbf{6 4 0}$ pixels, offset $\pm 10$ pixels)

| 212 | -4 | 29 | 241 | 1851099 | 3123 | 1820 | 52 | 52 | 3668 | 596 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 212 | -2 | 31 | 243 | 1851099 | 3123 | 1820 | 56 | 56 | 3668 | 596 |
| 212 | 0 | 33 | 245 | 1851099 | 3123 | 1820 | 60 | 60 | 3668 | 596 |
| 212 | 2 | 35 | 247 | 1851099 | 3123 | 1820 | 64 | 64 | 3668 | 596 |
| 212 | 4 | 37 | 249 | 1851099 | 3123 | 1820 | 67 | 67 | 3668 | 596 |
| 214 | -4 | 28 | 242 | 1836201 | 3135 | 1790 | 50 | 50 | 3683 | 611 |
| 214 | -2 | 30 | 244 | 1836201 | 3135 | 1790 | 54 | 54 | 3683 | 611 |
| 214 | 0 | 32 | 246 | 1836201 | 3135 | 1790 | 58 | 58 | 3683 | 611 |
| 214 | 2 | 34 | 248 | 1836201 | 3135 | 1790 | 61 | 61 | 3683 | 611 |
| 214 | 4 | 36 | 250 | 1836201 | 3135 | 1790 | 65 | 65 | 3683 | 611 |
| 216 | -4 | 27 | 243 | 1817578 | 3145 | 1750 | 48 | 48 | 3698 | 626 |
| 216 | -2 | 29 | 245 | 1817578 | 3145 | 1750 | 51 | 51 | 3698 | 626 |
| 216 | 0 | 31 | 247 | 1817578 | 3145 | 1750 | 55 | 55 | 3698 | 626 |
| 216 | 2 | 33 | 249 | 1817578 | 3145 | 1750 | 59 | 59 | 3698 | 626 |
| 216 | 4 | 35 | 251 | 1817578 | 3145 | 1750 | 63 | 63 | 3698 | 626 |
| 218 | -4 | 26 | 244 | 1802680 | 3155 | 1720 | 45 | 45 | 3714 | 642 |
| 218 | -2 | 28 | 246 | 1802680 | 3155 | 1720 | 49 | 49 | 3714 | 642 |
| 218 | 0 | 30 | 248 | 1802680 | 3155 | 1720 | 53 | 53 | 3714 | 642 |
| 218 | 2 | 32 | 250 | 1802680 | 3155 | 1720 | 56 | 56 | 3714 | 642 |
| 218 | 4 | 34 | 252 | 1802680 | 3155 | 1720 | 60 | 60 | 3714 | 642 |
| 220 | -4 | 25 | 245 | 1784057 | 3165 | 1680 | 43 | 43 | 3729 | 657 |
| 220 | -2 | 27 | 247 | 1784057 | 3165 | 1680 | 47 | 47 | 3729 | 657 |
| 220 | 0 | 29 | 249 | 1784057 | 3165 | 1680 | 50 | 50 | 3729 | 657 |
| 220 | 2 | 31 | 251 | 1784057 | 3165 | 1680 | 54 | 54 | 3729 | 657 |
| 220 | 4 | 33 | 253 | 1784057 | 3165 | 1680 | 58 | 58 | 3729 | 657 |

## Full size (horizontal size: $\mathbf{7 1 0}$ pixels)

| 241 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 204 | 0 | 37 | 241 | 1925590 | 3087 | 1980 | 70 | 70 |
| 3589 | 551 |  |  |  |  |  |  |  |

## PC-CODEC

Table 8 Y scaler programming at NTSC, input frame size: $640 \times 400$, no anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 212 | -4 | 29 | 241 | 1851099 | 4094 | 3655 | 52 | 52 | 4092 | 216 |
| 212 | -2 | 31 | 243 | 1851099 | 4094 | 3655 | 56 | 56 | 4092 | 216 |
| 212 | 0 | 33 | 245 | 1851099 | 4094 | 3655 | 60 | 60 | 4092 | 216 |
| 212 | 2 | 35 | 247 | 1851099 | 4094 | 3655 | 64 | 64 | 4092 | 216 |
| 212 | 4 | 37 | 249 | 1851099 | 4094 | 3655 | 68 | 68 | 4092 | 216 |
| 214 | -4 | 28 | 242 | 1836201 | 4090 | 3580 | 50 | 50 | 4091 | 253 |
| 214 | -2 | 30 | 244 | 1836201 | 4090 | 3580 | 54 | 54 | 4091 | 253 |
| 214 | 0 | 32 | 246 | 1836201 | 4090 | 3580 | 58 | 58 | 4091 | 253 |
| 214 | 2 | 34 | 248 | 1836201 | 4088 | 3580 | 61 | 61 | 4091 | 253 |
| 214 | 4 | 36 | 250 | 1836201 | 4088 | 3580 | 65 | 65 | 4091 | 253 |
| 216 | -4 | 27 | 243 | 1817578 | 4093 | 3510 | 48 | 48 | 4091 | 288 |
| 216 | -2 | 29 | 245 | 1817578 | 4093 | 3510 | 52 | 52 | 4091 | 288 |
| 216 | 0 | 31 | 247 | 1817578 | 4093 | 3510 | 55 | 55 | 4091 | 288 |
| 216 | 2 | 33 | 249 | 1817578 | 4093 | 3510 | 59 | 59 | 4091 | 288 |
| 216 | 4 | 35 | 251 | 1817578 | 4093 | 3510 | 63 | 63 | 4091 | 288 |
| 218 | -4 | 26 | 244 | 1802680 | 4092 | 3445 | 46 | 46 | 4092 | 322 |
| 218 | -2 | 28 | 246 | 1802680 | 4092 | 3445 | 49 | 49 | 4092 | 322 |
| 218 | 0 | 30 | 248 | 1802680 | 4092 | 3445 | 53 | 53 | 4092 | 322 |
| 218 | 2 | 32 | 250 | 1802680 | 4092 | 3445 | 57 | 57 | 4092 | 322 |
| 218 | 4 | 34 | 252 | 1802680 | 4092 | 3445 | 60 | 60 | 4092 | 322 |
| 220 | -4 | 25 | 245 | 1784057 | 4090 | 3370 | 43 | 43 | 4091 | 358 |
| 220 | -2 | 27 | 247 | 1784057 | 4090 | 3370 | 47 | 47 | 4091 | 358 |
| 220 | 0 | 29 | 249 | 1784057 | 4090 | 3370 | 50 | 50 | 4091 | 358 |
| 220 | 2 | 31 | 251 | 1784057 | 4090 | 3370 | 54 | 54 | 4091 | 358 |
| 220 | 4 | 33 | 253 | 1784057 | 4090 | 3370 | 58 | 58 | 4091 | 358 |

## Full size (horizontal size: $\mathbf{7 1 0}$ pixels)

| 241 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 204 | 0 | 37 | 241 | 1925590 | 4087 | 3950 | 70 | 70 |
| 4089 | 66 |  |  |  |  |  |  |  |

## PC-CODEC

Table 9 Y scaler programming at NTSC, input frame size: $640 \times 480$, full anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 212 | -4 | 29 | 241 | 2219829 | 1804 | 0 | 63 | 63 | 2948 | 900 |
| 212 | -2 | 31 | 243 | 2219829 | 1804 | 0 | 67 | 67 | 2948 | 900 |
| 212 | 0 | 33 | 245 | 2219829 | 1804 | 0 | 72 | 72 | 2948 | 900 |
| 212 | 2 | 35 | 247 | 2219829 | 1804 | 0 | 77 | 77 | 2948 | 900 |
| 212 | 4 | 37 | 249 | 2219829 | 1804 | 0 | 81 | 81 | 2948 | 900 |
| 214 | -4 | 28 | 242 | 2201206 | 1819 | 0 | 60 | 60 | 2957 | 909 |
| 214 | -2 | 30 | 244 | 2201206 | 1819 | 0 | 65 | 65 | 2957 | 909 |
| 214 | 0 | 32 | 246 | 2201206 | 1819 | 0 | 69 | 69 | 2957 | 909 |
| 214 | 2 | 34 | 248 | 2201206 | 1819 | 0 | 73 | 73 | 2957 | 909 |
| 214 | 4 | 36 | 250 | 2201206 | 1819 | 0 | 78 | 78 | 2957 | 909 |
| 216 | -4 | 27 | 243 | 2178859 | 1836 | 0 | 57 | 57 | 2965 | 917 |
| 216 | -2 | 29 | 245 | 2178859 | 1836 | 0 | 61 | 61 | 2965 | 917 |
| 216 | 0 | 31 | 247 | 2178859 | 1836 | 0 | 66 | 66 | 2965 | 917 |
| 216 | 2 | 33 | 249 | 2178859 | 1836 | 0 | 70 | 70 | 2965 | 917 |
| 216 | 4 | 35 | 251 | 2178859 | 1836 | 0 | 75 | 75 | 2965 | 917 |
| 218 | -4 | 26 | 244 | 2160236 | 1853 | 0 | 54 | 54 | 2974 | 926 |
| 218 | -2 | 28 | 246 | 2160236 | 1853 | 0 | 59 | 59 | 2974 | 926 |
| 218 | 0 | 30 | 248 | 2160236 | 1853 | 0 | 63 | 63 | 2974 | 926 |
| 218 | 2 | 32 | 250 | 2160236 | 1853 | 0 | 68 | 68 | 2974 | 926 |
| 218 | 4 | 34 | 252 | 2160236 | 1853 | 0 | 72 | 72 | 2974 | 926 |
| 220 | -4 | 25 | 245 | 2141613 | 1870 | 0 | 52 | 52 | 2982 | 934 |
| 220 | -2 | 27 | 247 | 2141613 | 1870 | 0 | 56 | 56 | 2982 | 934 |
| 220 | 0 | 29 | 249 | 2141613 | 1870 | 0 | 61 | 61 | 2982 | 934 |
| 220 | 2 | 31 | 251 | 2141613 | 1870 | 0 | 65 | 65 | 2982 | 934 |
| 220 | 4 | 33 | 253 | 2141613 | 1870 | 0 | 69 | 69 | 2982 | 934 |

## Full size (horizontal size: $\mathbf{7 1 0}$ pixels)

| 241 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 204 | 0 | 37 | 241 | 2309218 | 1734 | 0 | 84 | 84 |
| 2941 | 866 |  |  |  |  |  |  |  |

## PC-CODEC

SAA7108E; SAA7109E

Table 10 Y scaler programming at NTSC, input frame size: $640 \times 480$, half anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm \mathbf{1 0}$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 212 | -4 | 29 | 241 | 2219829 | 2704 | 2048 | 63 | 63 | 3399 | 327 |
| 212 | -2 | 31 | 243 | 2219829 | 2704 | 2048 | 67 | 67 | 3399 | 327 |
| 212 | 0 | 33 | 245 | 2219829 | 2704 | 2048 | 72 | 72 | 3399 | 327 |
| 212 | 2 | 35 | 247 | 2219829 | 2704 | 2048 | 77 | 77 | 3399 | 327 |
| 212 | 4 | 37 | 249 | 2219829 | 2704 | 2048 | 81 | 81 | 3399 | 327 |
| 214 | -4 | 28 | 242 | 2201206 | 2730 | 2048 | 60 | 60 | 3412 | 340 |
| 214 | -2 | 30 | 244 | 2201206 | 2730 | 2048 | 65 | 65 | 3412 | 340 |
| 214 | 0 | 32 | 246 | 2201206 | 2730 | 2048 | 69 | 69 | 3412 | 340 |
| 214 | 2 | 34 | 248 | 2201206 | 2730 | 2048 | 74 | 74 | 3412 | 340 |
| 214 | 4 | 36 | 250 | 2201206 | 2730 | 2048 | 78 | 78 | 3412 | 340 |
| 216 | -4 | 27 | 243 | 2178859 | 2756 | 2048 | 57 | 57 | 3424 | 352 |
| 216 | -2 | 29 | 245 | 2178859 | 2756 | 2048 | 62 | 62 | 3424 | 352 |
| 216 | 0 | 31 | 247 | 2178859 | 2756 | 2048 | 66 | 66 | 3424 | 352 |
| 216 | 2 | 33 | 249 | 2178859 | 2756 | 2048 | 71 | 71 | 3424 | 352 |
| 216 | 4 | 35 | 251 | 2178859 | 2756 | 2048 | 75 | 75 | 3424 | 352 |
| 218 | -4 | 26 | 244 | 2160236 | 2781 | 2048 | 55 | 55 | 3437 | 365 |
| 218 | -2 | 28 | 246 | 2160236 | 2781 | 2048 | 59 | 59 | 3437 | 365 |
| 218 | 0 | 30 | 248 | 2160236 | 2781 | 2048 | 63 | 63 | 3437 | 365 |
| 218 | 2 | 32 | 250 | 2160236 | 2781 | 2048 | 68 | 68 | 3437 | 365 |
| 218 | 4 | 34 | 252 | 2160236 | 2781 | 2048 | 72 | 72 | 3437 | 365 |
| 220 | -4 | 25 | 245 | 2141613 | 2807 | 2048 | 52 | 52 | 3450 | 378 |
| 220 | -2 | 27 | 247 | 2141613 | 2807 | 2048 | 57 | 57 | 3450 | 378 |
| 220 | 0 | 29 | 249 | 2141613 | 2807 | 2048 | 61 | 61 | 3450 | 378 |
| 220 | 2 | 31 | 251 | 2141613 | 2807 | 2048 | 65 | 65 | 3450 | 378 |
| 220 | 4 | 33 | 253 | 2141613 | 2807 | 2048 | 70 | 70 | 3450 | 378 |
|  | 4 |  |  |  |  |  |  |  |  |  |

## Full size (horizontal size: $\mathbf{7 1 0}$ pixels)

| 241 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | | Small size (horizontal size: 620 pixels) |
| :---: |
| 204 |

## PC-CODEC

SAA7108E; SAA7109E

Table 11 Y scaler programming at NTSC, input frame size: $640 \times 480$, no anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 212 | -4 | 29 | 241 | 2219829 | 3607 | 4095 | 63 | 64 | 3849 | 3362 |
| 212 | -2 | 31 | 243 | 2219829 | 3607 | 4095 | 68 | 69 | 3849 | 3362 |
| 212 | 0 | 33 | 245 | 2219829 | 3607 | 4095 | 72 | 73 | 3849 | 3362 |
| 212 | 2 | 35 | 247 | 2219829 | 3607 | 4095 | 77 | 78 | 3849 | 3362 |
| 212 | 4 | 37 | 249 | 2219829 | 3607 | 4095 | 81 | 82 | 3849 | 3362 |
| 214 | -4 | 28 | 242 | 2201206 | 3639 | 4095 | 60 | 61 | 3866 | 3413 |
| 214 | -2 | 30 | 244 | 2201206 | 3639 | 4095 | 65 | 66 | 3866 | 3413 |
| 214 | 0 | 32 | 246 | 2201206 | 3639 | 4095 | 69 | 70 | 3866 | 3413 |
| 214 | 2 | 34 | 248 | 2201206 | 3639 | 4095 | 74 | 75 | 3866 | 3413 |
| 214 | 4 | 36 | 250 | 2201206 | 3639 | 4095 | 78 | 79 | 3866 | 3413 |
| 216 | -4 | 27 | 243 | 2178859 | 3675 | 4095 | 57 | 58 | 3883 | 3464 |
| 216 | -2 | 29 | 245 | 2178859 | 3675 | 4095 | 62 | 63 | 3883 | 3464 |
| 216 | 0 | 31 | 247 | 2178859 | 3675 | 4095 | 66 | 67 | 3883 | 3464 |
| 216 | 2 | 33 | 249 | 2178859 | 3675 | 4095 | 71 | 72 | 3883 | 3464 |
| 216 | 4 | 35 | 251 | 2178859 | 3675 | 4095 | 75 | 76 | 3883 | 3464 |
| 218 | -4 | 26 | 244 | 2160236 | 3709 | 4095 | 55 | 56 | 3900 | 3515 |
| 218 | -2 | 28 | 246 | 2160236 | 3709 | 4095 | 59 | 60 | 3900 | 3515 |
| 218 | 0 | 30 | 248 | 2160236 | 3709 | 4095 | 64 | 65 | 3900 | 3515 |
| 218 | 2 | 32 | 250 | 2160236 | 3709 | 4095 | 68 | 69 | 3900 | 3515 |
| 218 | 4 | 34 | 252 | 2160236 | 3709 | 4095 | 73 | 74 | 3900 | 3515 |
| 220 | -4 | 25 | 245 | 2141613 | 3741 | 4095 | 52 | 53 | 3917 | 3566 |
| 220 | -2 | 27 | 247 | 2141613 | 3741 | 4095 | 57 | 58 | 3917 | 3566 |
| 220 | 0 | 29 | 249 | 2141613 | 3741 | 4095 | 61 | 62 | 3917 | 3566 |
| 220 | 2 | 31 | 251 | 2141613 | 3741 | 4095 | 65 | 66 | 3917 | 3566 |
| 220 | 4 | 33 | 253 | 2141613 | 3741 | 4095 | 70 | 71 | 3917 | 3566 |

## Full size (horizontal size: $\mathbf{7 1 0}$ pixels)

| 241 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 204 | 0 | 37 | 241 | 2309218 | 3471 | 4095 | 85 | 86 | 3781 |

## PC-CODEC

Table 12 Y scaler programming at NTSC, input frame size: $800 \times 600$, full anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 212 | -4 | 29 | 241 | 3551726 | 1443 | 0 | 79 | 79 | 2769 | 721 |
| 212 | -2 | 31 | 243 | 3551726 | 1443 | 0 | 84 | 84 | 2769 | 721 |
| 212 | 0 | 33 | 245 | 3551726 | 1443 | 0 | 90 | 90 | 2769 | 721 |
| 212 | 2 | 35 | 247 | 3551726 | 1443 | 0 | 96 | 96 | 2769 | 721 |
| 212 | 4 | 37 | 249 | 3551726 | 1443 | 0 | 102 | 102 | 2769 | 721 |
| 214 | -4 | 28 | 242 | 3518354 | 1457 | 0 | 75 | 75 | 2776 | 728 |
| 214 | -2 | 30 | 244 | 3518354 | 1457 | 0 | 81 | 81 | 2776 | 728 |
| 214 | 0 | 32 | 246 | 3518354 | 1457 | 0 | 86 | 86 | 2776 | 728 |
| 214 | 2 | 34 | 248 | 3518354 | 1457 | 0 | 92 | 92 | 2776 | 728 |
| 214 | 4 | 36 | 250 | 3518354 | 1457 | 0 | 98 | 98 | 2776 | 728 |
| 216 | -4 | 27 | 243 | 3484982 | 1470 | 0 | 72 | 72 | 2782 | 734 |
| 216 | -2 | 29 | 245 | 3484982 | 1470 | 0 | 77 | 77 | 2782 | 734 |
| 216 | 0 | 31 | 247 | 3484982 | 1470 | 0 | 82 | 82 | 2782 | 734 |
| 216 | 2 | 33 | 249 | 3484982 | 1470 | 0 | 88 | 88 | 2782 | 734 |
| 216 | 4 | 35 | 251 | 3484982 | 1470 | 0 | 94 | 94 | 2782 | 734 |
| 218 | -4 | 26 | 244 | 3451610 | 1484 | 0 | 68 | 68 | 2789 | 741 |
| 218 | -2 | 28 | 246 | 3451610 | 1484 | 0 | 73 | 73 | 2789 | 741 |
| 218 | 0 | 30 | 248 | 3451610 | 1484 | 0 | 79 | 79 | 2789 | 741 |
| 218 | 2 | 32 | 250 | 3451610 | 1484 | 0 | 85 | 85 | 2789 | 741 |
| 218 | 4 | 34 | 252 | 3451610 | 1484 | 0 | 90 | 90 | 2789 | 741 |
| 220 | -4 | 25 | 245 | 3423006 | 1497 | 0 | 65 | 65 | 2796 | 748 |
| 220 | -2 | 27 | 247 | 3423006 | 1497 | 0 | 71 | 71 | 2796 | 748 |
| 220 | 0 | 29 | 249 | 3423006 | 1497 | 0 | 76 | 76 | 2796 | 748 |
| 220 | 2 | 31 | 251 | 3423006 | 1497 | 0 | 81 | 81 | 2796 | 748 |
| 220 | 4 | 33 | 253 | 3423006 | 1497 | 0 | 87 | 87 | 2796 | 748 |

## Full size (horizontal size: $\mathbf{7 1 0}$ pixels)

| 241 | 0 | 18 | 259 | 3122659 | 1642 | 0 | 42 | 42 | 2867 | 819 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Small size (horizontal size: 620 pixels) |  |  |  |  |  |  |  |  |  |  |
| 204 | 0 | 37 | 241 | 3689981 | 1389 | 0 | 106 | 106 | 2742 | 694 |

## PC-CODEC

SAA7108E; SAA7109E

Table 13 Y scaler programming at NTSC, input frame size: $800 \times 600$, half anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm \mathbf{1 0}$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 212 | -4 | 29 | 241 | 3551726 | 2165 | 2048 | 79 | 79 | 3129 | 57 |
| 212 | -2 | 31 | 243 | 3551726 | 2165 | 2048 | 85 | 85 | 3129 | 57 |
| 212 | 0 | 33 | 245 | 3551726 | 2165 | 2048 | 91 | 91 | 3129 | 57 |
| 212 | 2 | 35 | 247 | 3551726 | 2165 | 2048 | 96 | 96 | 3129 | 57 |
| 212 | 4 | 37 | 249 | 3551726 | 2165 | 2048 | 102 | 102 | 3129 | 57 |
| 214 | -4 | 28 | 242 | 3518354 | 2185 | 2048 | 75 | 75 | 3140 | 68 |
| 214 | -2 | 30 | 244 | 3518354 | 2185 | 2048 | 81 | 81 | 3140 | 68 |
| 214 | 0 | 32 | 246 | 3518354 | 2185 | 2048 | 87 | 87 | 3140 | 68 |
| 214 | 2 | 34 | 248 | 3518354 | 2185 | 2048 | 92 | 92 | 3140 | 68 |
| 214 | 4 | 36 | 250 | 3518354 | 2185 | 2048 | 98 | 98 | 3140 | 68 |
| 216 | -4 | 27 | 243 | 3484982 | 2205 | 2048 | 72 | 72 | 3150 | 78 |
| 216 | -2 | 29 | 245 | 3484982 | 2205 | 2048 | 77 | 77 | 3150 | 78 |
| 216 | 0 | 31 | 247 | 3484982 | 2205 | 2048 | 83 | 83 | 3150 | 78 |
| 216 | 2 | 33 | 249 | 3484982 | 2205 | 2048 | 89 | 89 | 3150 | 78 |
| 216 | 4 | 35 | 251 | 3484982 | 2205 | 2048 | 94 | 94 | 3150 | 78 |
| 218 | -4 | 26 | 244 | 3451610 | 2226 | 2048 | 68 | 68 | 3160 | 88 |
| 218 | -2 | 28 | 246 | 3451610 | 2226 | 2048 | 74 | 74 | 3160 | 88 |
| 218 | 0 | 30 | 248 | 3451610 | 2226 | 2048 | 80 | 80 | 3160 | 88 |
| 218 | 2 | 32 | 250 | 3451610 | 2226 | 2048 | 85 | 85 | 3160 | 88 |
| 218 | 4 | 34 | 252 | 3451610 | 2226 | 2048 | 90 | 90 | 3160 | 88 |
| 220 | -4 | 25 | 245 | 3423006 | 2246 | 2048 | 65 | 65 | 3170 | 98 |
| 220 | -2 | 27 | 247 | 3423006 | 2246 | 2048 | 71 | 71 | 3170 | 98 |
| 220 | 0 | 29 | 249 | 3423006 | 2246 | 2048 | 76 | 76 | 3170 | 98 |
| 220 | 2 | 31 | 251 | 3423006 | 2246 | 2048 | 81 | 81 | 3170 | 98 |
| 220 | 4 | 33 | 253 | 3423006 | 2246 | 2048 | 87 | 87 | 3170 | 98 |
|  | 4 |  |  |  |  |  |  |  |  |  |

## Full size (horizontal size: 710 pixels)

| 241 | 0 | 18 | 259 | 3122659 | 2461 | 2048 | 42 | 42 | 3277 | 205 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 204 | 0 | 37 | 241 | 3689981 | 2083 | 2048 | 106 | 106 | 3089 |

## PC-CODEC

SAA7108E; SAA7109E

Table 14 Y scaler programming at NTSC, input frame size: $800 \times 600$, no anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 212 | -4 | 29 | 241 | 3551726 | 2887 | 4095 | 79 | 80 | 3490 | 2282 |
| 212 | -2 | 31 | 243 | 3551726 | 2887 | 4095 | 85 | 86 | 3490 | 2282 |
| 212 | 0 | 33 | 245 | 3551726 | 2887 | 4095 | 91 | 92 | 3490 | 2282 |
| 212 | 2 | 35 | 247 | 3551726 | 2887 | 4095 | 96 | 97 | 3490 | 2282 |
| 212 | 4 | 37 | 249 | 3551726 | 2887 | 4095 | 102 | 103 | 3490 | 2282 |
| 214 | -4 | 28 | 242 | 3518354 | 2912 | 4095 | 76 | 77 | 3504 | 2323 |
| 214 | -2 | 30 | 244 | 3518354 | 2912 | 4095 | 81 | 82 | 3504 | 2323 |
| 214 | 0 | 32 | 246 | 3518354 | 2912 | 4095 | 87 | 88 | 3504 | 2323 |
| 214 | 2 | 34 | 248 | 3518354 | 2912 | 4095 | 92 | 93 | 3504 | 2323 |
| 214 | 4 | 36 | 250 | 3518354 | 2912 | 4095 | 98 | 99 | 3504 | 2323 |
| 216 | -4 | 27 | 243 | 3484982 | 2941 | 4095 | 72 | 73 | 3517 | 2364 |
| 216 | -2 | 29 | 245 | 3484982 | 2941 | 4095 | 78 | 79 | 3517 | 2364 |
| 216 | 0 | 31 | 247 | 3484982 | 2941 | 4095 | 83 | 84 | 3517 | 2364 |
| 216 | 2 | 33 | 249 | 3484982 | 2941 | 4095 | 89 | 90 | 3517 | 2364 |
| 216 | 4 | 35 | 251 | 3484982 | 2941 | 4095 | 94 | 95 | 3517 | 2364 |
| 218 | -4 | 26 | 244 | 3451610 | 2969 | 4095 | 69 | 70 | 3531 | 2405 |
| 218 | -2 | 28 | 246 | 3451610 | 2969 | 4095 | 74 | 75 | 3531 | 2405 |
| 218 | 0 | 30 | 248 | 3451610 | 2969 | 4095 | 80 | 81 | 3531 | 2405 |
| 218 | 2 | 32 | 250 | 3451610 | 2969 | 4095 | 85 | 86 | 3531 | 2405 |
| 218 | 4 | 34 | 252 | 3451610 | 2969 | 4095 | 90 | 91 | 3531 | 2405 |
| 220 | -4 | 25 | 245 | 3423006 | 2994 | 4095 | 65 | 66 | 3544 | 2446 |
| 220 | -2 | 27 | 247 | 3423006 | 2994 | 4095 | 71 | 72 | 3544 | 2446 |
| 220 | 0 | 29 | 249 | 3423006 | 2994 | 4095 | 76 | 77 | 3544 | 2446 |
| 220 | 2 | 31 | 251 | 3423006 | 2994 | 4095 | 82 | 83 | 3544 | 2446 |
| 220 | 4 | 33 | 253 | 3423006 | 2994 | 4095 | 87 | 88 | 3544 | 2446 |

## Full size (horizontal size: $\mathbf{7 1 0}$ pixels)

| 241 | 0 | 18 | 259 | 3122659 | 3282 | 4095 | 42 | 43 | 3687 | 2875 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 204 | 0 | 37 | 241 | 3689981 | 2778 | 4095 | 106 | 107 | 3436 |

## PC-CODEC

Table 15 Y scaler programming at PAL, input frame size: $640 \times 400$, full anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 1528590 | 2600 | 0 | 52 | 52 | 3347 | 1299 |
| 255 | -2 | 37 | 292 | 1528590 | 2602 | 0 | 55 | 55 | 3347 | 1299 |
| 255 | 0 | 39 | 294 | 1528590 | 2602 | 0 | 59 | 59 | 3347 | 1299 |
| 255 | 2 | 41 | 296 | 1528590 | 2602 | 0 | 62 | 62 | 3347 | 1299 |
| 255 | 4 | 43 | 298 | 1528590 | 2602 | 0 | 65 | 65 | 3347 | 1299 |
| 257 | -4 | 34 | 291 | 1516163 | 2621 | 0 | 50 | 50 | 3357 | 1309 |
| 257 | -2 | 36 | 293 | 1516163 | 2623 | 0 | 53 | 53 | 3357 | 1309 |
| 257 | 0 | 38 | 295 | 1516163 | 2623 | 0 | 57 | 57 | 3357 | 1309 |
| 257 | 2 | 40 | 297 | 1516163 | 2623 | 0 | 60 | 60 | 3357 | 1309 |
| 257 | 4 | 42 | 299 | 1516163 | 2623 | 0 | 63 | 63 | 3357 | 1309 |
| 259 | -4 | 33 | 292 | 1506842 | 2641 | 0 | 49 | 49 | 3367 | 1319 |
| 259 | -2 | 35 | 294 | 1506842 | 2641 | 0 | 52 | 52 | 3367 | 1319 |
| 259 | 0 | 37 | 296 | 1506842 | 2641 | 0 | 55 | 55 | 3367 | 1319 |
| 259 | 2 | 39 | 298 | 1506842 | 2641 | 0 | 58 | 58 | 3367 | 1319 |
| 259 | 4 | 41 | 300 | 1506842 | 2641 | 0 | 61 | 61 | 3367 | 1319 |
| 261 | -4 | 32 | 293 | 1494414 | 2661 | 0 | 47 | 47 | 3377 | 1329 |
| 261 | -2 | 34 | 295 | 1494414 | 2661 | 0 | 50 | 50 | 3377 | 1329 |
| 261 | 0 | 36 | 297 | 1494414 | 2661 | 0 | 53 | 53 | 3377 | 1329 |
| 261 | 2 | 38 | 299 | 1494414 | 2661 | 0 | 56 | 56 | 3377 | 1329 |
| 261 | 4 | 40 | 301 | 1494414 | 2661 | 0 | 59 | 59 | 3377 | 1329 |
| 263 | -4 | 31 | 294 | 1481987 | 2684 | 0 | 45 | 45 | 3387 | 1339 |
| 263 | -2 | 33 | 296 | 1481987 | 2684 | 0 | 48 | 48 | 3387 | 1339 |
| 263 | 0 | 35 | 298 | 1481987 | 2684 | 0 | 51 | 51 | 3387 | 1339 |
| 263 | 2 | 37 | 300 | 1481987 | 2684 | 0 | 54 | 54 | 3387 | 1339 |
| 263 | 4 | 39 | 302 | 1481987 | 2684 | 0 | 57 | 57 | 3387 | 1339 |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | | Small size (horizontal size: 620 pixels) |
| :---: |
| 250 |

## PC-CODEC

SAA7108E; SAA7109E

Table 16 Y scaler programming at PAL, input frame size: $640 \times 400$, half anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 1528590 | 3346 | 1170 | 53 | 53 | 3996 | 924 |
| 255 | -2 | 37 | 292 | 1528590 | 3346 | 1170 | 56 | 56 | 3996 | 924 |
| 255 | 0 | 39 | 294 | 1528590 | 3346 | 1170 | 59 | 59 | 3996 | 924 |
| 255 | 2 | 41 | 296 | 1528590 | 3346 | 1170 | 62 | 62 | 3996 | 924 |
| 255 | 4 | 43 | 298 | 1528590 | 3346 | 1170 | 65 | 65 | 3996 | 924 |
| 257 | -4 | 34 | 291 | 1516163 | 3360 | 1150 | 51 | 51 | 4012 | 940 |
| 257 | -2 | 36 | 293 | 1516163 | 3360 | 1150 | 54 | 54 | 4012 | 940 |
| 257 | 0 | 38 | 295 | 1516163 | 3360 | 1150 | 57 | 57 | 4012 | 940 |
| 257 | 2 | 40 | 297 | 1516163 | 3360 | 1150 | 60 | 60 | 4012 | 940 |
| 257 | 4 | 42 | 299 | 1516163 | 3360 | 1150 | 63 | 63 | 4012 | 940 |
| 259 | -4 | 33 | 292 | 1506842 | 3362 | 1120 | 49 | 49 | 4070 | 998 |
| 259 | -2 | 35 | 294 | 1506842 | 3362 | 1120 | 52 | 52 | 4070 | 998 |
| 259 | 0 | 37 | 296 | 1506842 | 3362 | 1120 | 55 | 55 | 4070 | 998 |
| 259 | 2 | 39 | 298 | 1506842 | 3362 | 1120 | 58 | 58 | 4070 | 998 |
| 259 | 4 | 41 | 300 | 1506842 | 3362 | 1120 | 61 | 61 | 4070 | 998 |
| 261 | -4 | 32 | 293 | 1494414 | 3378 | 1100 | 47 | 47 | 4042 | 970 |
| 261 | -2 | 34 | 295 | 1494414 | 3378 | 1100 | 50 | 50 | 4042 | 970 |
| 261 | 0 | 36 | 297 | 1494414 | 3378 | 1100 | 53 | 53 | 4042 | 970 |
| 261 | 2 | 38 | 299 | 1494414 | 3378 | 1100 | 56 | 56 | 4042 | 970 |
| 261 | 4 | 40 | 301 | 1494414 | 3378 | 1100 | 59 | 59 | 4042 | 970 |
| 263 | -4 | 31 | 294 | 1481987 | 3384 | 1070 | 45 | 45 | 4057 | 985 |
| 263 | -2 | 33 | 296 | 1481987 | 3384 | 1070 | 48 | 48 | 4057 | 985 |
| 263 | 0 | 35 | 298 | 1481987 | 3384 | 1070 | 51 | 51 | 4057 | 985 |
| 263 | 2 | 37 | 300 | 1481987 | 3384 | 1070 | 54 | 54 | 4057 | 985 |
| 263 | 4 | 39 | 302 | 1481987 | 3384 | 1070 | 57 | 57 | 4057 | 985 |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 250 | 0 | 41 | 291 | 1559659 | 3322 | 1240 | 63 | 63 | 3707 |

## PC-CODEC

Table 17 Y scaler programming at PAL, input frame size: $640 \times 400$, no anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 1528590 | 4095 | 2350 | 53 | 53 | 4092 | 869 |
| 255 | -2 | 37 | 292 | 1528590 | 4095 | 2350 | 56 | 56 | 4092 | 869 |
| 255 | 0 | 39 | 294 | 1528590 | 4095 | 2350 | 59 | 59 | 4092 | 869 |
| 255 | 2 | 41 | 296 | 1528590 | 4095 | 2350 | 62 | 62 | 4092 | 869 |
| 255 | 4 | 43 | 298 | 1528590 | 4095 | 2350 | 65 | 65 | 4092 | 869 |
| 257 | -4 | 34 | 291 | 1516163 | 4095 | 2300 | 51 | 51 | 4092 | 894 |
| 257 | -2 | 36 | 293 | 1516163 | 4095 | 2300 | 54 | 54 | 4092 | 894 |
| 257 | 0 | 38 | 295 | 1516163 | 4095 | 2300 | 57 | 57 | 4092 | 894 |
| 257 | 2 | 40 | 297 | 1516163 | 4095 | 2300 | 60 | 60 | 4092 | 894 |
| 257 | 4 | 42 | 299 | 1516163 | 4095 | 2300 | 63 | 63 | 4092 | 894 |
| 259 | -4 | 33 | 292 | 1506842 | 4093 | 2250 | 49 | 49 | 4092 | 919 |
| 259 | -2 | 35 | 294 | 1506842 | 4093 | 2250 | 52 | 52 | 4092 | 919 |
| 259 | 0 | 37 | 296 | 1506842 | 4093 | 2250 | 55 | 55 | 4092 | 919 |
| 259 | 2 | 39 | 298 | 1506842 | 4091 | 2250 | 58 | 58 | 4092 | 919 |
| 259 | 4 | 42 | 301 | 1506842 | 4091 | 2250 | 63 | 63 | 4092 | 919 |
| 261 | -4 | 32 | 293 | 1494414 | 4094 | 2200 | 47 | 47 | 4092 | 944 |
| 261 | -2 | 34 | 295 | 1494414 | 4094 | 2200 | 50 | 50 | 4092 | 944 |
| 261 | 0 | 36 | 297 | 1494414 | 4094 | 2200 | 53 | 53 | 4092 | 944 |
| 261 | 2 | 38 | 299 | 1494414 | 4093 | 2200 | 56 | 56 | 4092 | 944 |
| 261 | 4 | 40 | 301 | 1494414 | 4093 | 2200 | 59 | 59 | 4092 | 944 |
| 263 | -4 | 31 | 294 | 1481987 | 4092 | 2150 | 45 | 45 | 4091 | 968 |
| 263 | -2 | 33 | 296 | 1481987 | 4092 | 2150 | 48 | 48 | 4091 | 968 |
| 263 | 0 | 35 | 298 | 1481987 | 4092 | 2150 | 51 | 51 | 4091 | 968 |
| 263 | 2 | 37 | 300 | 1481987 | 4092 | 2150 | 54 | 54 | 4091 | 968 |
| 263 | 4 | 39 | 302 | 1481987 | 4092 | 2150 | 57 | 57 | 4091 | 968 |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 250 | 0 | 41 | 291 | 1559659 | 4087 | 2470 | 63 | 63 | 4089 |

## PC-CODEC

Table 18 Y scaler programming at PAL, input frame size: $640 \times 480$, full anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 1833066 | 2168 | 0 | 63 | 63 | 3131 | 1083 |
| 255 | -2 | 37 | 292 | 1833066 | 2168 | 0 | 67 | 67 | 3131 | 1083 |
| 255 | 0 | 39 | 294 | 1833066 | 2168 | 0 | 71 | 71 | 3131 | 1083 |
| 255 | 2 | 41 | 296 | 1833066 | 2168 | 0 | 74 | 74 | 3131 | 1083 |
| 255 | 4 | 43 | 298 | 1833066 | 2168 | 0 | 78 | 78 | 3131 | 1083 |
| 257 | -4 | 34 | 291 | 1820638 | 2185 | 0 | 61 | 61 | 3139 | 1091 |
| 257 | -2 | 36 | 293 | 1820638 | 2185 | 0 | 65 | 65 | 3139 | 1091 |
| 257 | 0 | 38 | 295 | 1820638 | 2185 | 0 | 69 | 69 | 3139 | 1091 |
| 257 | 2 | 40 | 297 | 1820638 | 2185 | 0 | 72 | 72 | 3139 | 1091 |
| 257 | 4 | 42 | 299 | 1820638 | 2185 | 0 | 76 | 76 | 3139 | 1091 |
| 259 | -4 | 33 | 292 | 1805104 | 2202 | 0 | 58 | 58 | 3148 | 1100 |
| 259 | -2 | 35 | 294 | 1805104 | 2202 | 0 | 62 | 62 | 3148 | 1100 |
| 259 | 0 | 37 | 296 | 1805104 | 2202 | 0 | 66 | 66 | 3148 | 1100 |
| 259 | 2 | 39 | 298 | 1805104 | 2204 | 0 | 70 | 70 | 3148 | 1100 |
| 259 | 4 | 41 | 300 | 1805104 | 2202 | 0 | 73 | 73 | 3148 | 1100 |
| 261 | -4 | 32 | 293 | 1792676 | 2219 | 0 | 56 | 56 | 3156 | 1108 |
| 261 | -2 | 34 | 295 | 1792676 | 2219 | 0 | 60 | 60 | 3156 | 1108 |
| 261 | 0 | 36 | 297 | 1792676 | 2219 | 0 | 64 | 64 | 3156 | 1108 |
| 261 | 2 | 38 | 299 | 1792676 | 2219 | 0 | 67 | 67 | 3156 | 1108 |
| 261 | 4 | 40 | 301 | 1792676 | 2219 | 0 | 71 | 71 | 3156 | 1108 |
| 263 | -4 | 31 | 294 | 1777142 | 2238 | 0 | 54 | 54 | 3165 | 1117 |
| 263 | -2 | 33 | 296 | 1777142 | 2238 | 0 | 58 | 58 | 3165 | 1117 |
| 263 | 0 | 35 | 298 | 1777142 | 2238 | 0 | 61 | 61 | 3165 | 1117 |
| 263 | 2 | 37 | 300 | 1777142 | 2238 | 0 | 65 | 65 | 3165 | 1117 |
| 263 | 4 | 39 | 302 | 1777142 | 2238 | 0 | 69 | 69 | 3165 | 1117 |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | | Small size (horizontal size: 620 pixels) |
| :---: |
| 250 |

## PC-CODEC

Table 19 Y scaler programming at PAL, input frame size: $640 \times 480$, half anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm 10$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 1833066 | 3254 | 2048 | 63 | 63 | 3673 | 601 |
| 255 | -2 | 37 | 292 | 1833066 | 3254 | 2048 | 67 | 67 | 3673 | 601 |
| 255 | 0 | 39 | 294 | 1833066 | 3254 | 2048 | 71 | 71 | 3673 | 601 |
| 255 | 2 | 41 | 296 | 1833066 | 3254 | 2048 | 75 | 75 | 3673 | 601 |
| 255 | 4 | 43 | 298 | 1833066 | 3254 | 2048 | 79 | 79 | 3673 | 601 |
| 257 | -4 | 34 | 291 | 1820638 | 3277 | 2048 | 61 | 61 | 3686 | 614 |
| 257 | -2 | 36 | 293 | 1820638 | 3277 | 2048 | 65 | 65 | 3686 | 614 |
| 257 | 0 | 38 | 295 | 1820638 | 3277 | 2048 | 69 | 69 | 3686 | 614 |
| 257 | 2 | 40 | 297 | 1820638 | 3277 | 2048 | 72 | 72 | 3686 | 614 |
| 257 | 4 | 42 | 299 | 1820638 | 3277 | 2048 | 76 | 76 | 3686 | 614 |
| 259 | -4 | 33 | 292 | 1805104 | 3305 | 2048 | 59 | 59 | 3698 | 626 |
| 259 | -2 | 35 | 294 | 1805104 | 3305 | 2048 | 63 | 63 | 3698 | 626 |
| 259 | 0 | 37 | 296 | 1805104 | 3305 | 2048 | 66 | 66 | 3698 | 626 |
| 259 | 2 | 39 | 298 | 1805104 | 3305 | 2048 | 70 | 70 | 3698 | 626 |
| 259 | 4 | 41 | 300 | 1805104 | 3305 | 2048 | 74 | 74 | 3698 | 626 |
| 261 | -4 | 32 | 293 | 1792676 | 3328 | 2048 | 57 | 57 | 3711 | 639 |
| 261 | -2 | 34 | 295 | 1792676 | 3328 | 2048 | 60 | 60 | 3711 | 639 |
| 261 | 0 | 36 | 297 | 1792676 | 3328 | 2048 | 64 | 64 | 3711 | 639 |
| 261 | 2 | 38 | 299 | 1792676 | 3328 | 2048 | 68 | 68 | 3711 | 639 |
| 261 | 4 | 40 | 301 | 1792676 | 3328 | 2048 | 71 | 71 | 3711 | 639 |
| 263 | -4 | 31 | 294 | 1777142 | 3354 | 2048 | 54 | 54 | 3724 | 652 |
| 263 | -2 | 33 | 296 | 1777142 | 3354 | 2048 | 58 | 58 | 3724 | 652 |
| 263 | 0 | 35 | 298 | 1777142 | 3354 | 2048 | 61 | 61 | 3724 | 652 |
| 263 | 2 | 37 | 300 | 1777142 | 3354 | 2048 | 65 | 65 | 3724 | 652 |
| 263 | 4 | 39 | 302 | 1777142 | 3354 | 2048 | 69 | 69 | 3724 | 652 |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 250 | 0 | 41 | 291 | 1870348 | 3108 | 1890 | 76 | 76 | 3600 |
| 607 |  |  |  |  |  |  |  |  |  |

## PC-CODEC

Table 20 Y scaler programming at PAL, input frame size: $640 \times 480$, no anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

Regular size (horizontal TV size: $\mathbf{6 4 0}$ pixels, offset $\pm \mathbf{1 0}$ pixels)

| 255 | -4 | 35 | 290 | 1833066 | 4093 | 3630 | 64 | 64 | 4091 | 228 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 255 | -2 | 37 | 292 | 1833066 | 4093 | 3630 | 67 | 67 | 4091 | 228 |
| 255 | 0 | 39 | 294 | 1833066 | 4093 | 3630 | 71 | 71 | 4091 | 228 |
| 255 | 2 | 41 | 296 | 1833066 | 4093 | 3630 | 75 | 75 | 4091 | 228 |
| 255 | 4 | 43 | 298 | 1833066 | 4093 | 3630 | 79 | 79 | 4091 | 228 |
| 257 | -4 | 34 | 291 | 1820638 | 4090 | 3570 | 61 | 61 | 4091 | 258 |
| 257 | -2 | 36 | 293 | 1820638 | 4090 | 3570 | 65 | 65 | 4091 | 258 |
| 257 | 0 | 38 | 295 | 1820638 | 4090 | 3570 | 69 | 69 | 4091 | 258 |
| 257 | 2 | 40 | 297 | 1820638 | 4090 | 3570 | 73 | 73 | 4091 | 258 |
| 257 | 4 | 42 | 299 | 1820638 | 4090 | 3570 | 76 | 76 | 4091 | 258 |
| 259 | -4 | 33 | 292 | 1805104 | 4092 | 3510 | 59 | 59 | 4091 | 288 |
| 259 | -2 | 35 | 294 | 1805104 | 4092 | 3510 | 63 | 63 | 4091 | 288 |
| 259 | 0 | 37 | 296 | 1805104 | 4092 | 3510 | 66 | 66 | 4091 | 288 |
| 259 | 2 | 39 | 298 | 1805104 | 4092 | 3510 | 70 | 70 | 4091 | 288 |
| 259 | 4 | 41 | 300 | 1805104 | 4092 | 3510 | 74 | 74 | 4091 | 288 |
| 261 | -4 | 32 | 293 | 1792676 | 4088 | 3450 | 57 | 57 | 4091 | 318 |
| 261 | -2 | 34 | 295 | 1792676 | 4088 | 3450 | 60 | 60 | 4091 | 318 |
| 261 | 0 | 36 | 297 | 1792676 | 4088 | 3450 | 64 | 64 | 4091 | 318 |
| 261 | 2 | 38 | 299 | 1792676 | 4088 | 3450 | 68 | 68 | 4091 | 318 |
| 261 | 4 | 40 | 301 | 1792676 | 4088 | 3450 | 71 | 71 | 4091 | 318 |
| 263 | -4 | 31 | 294 | 1777142 | 4095 | 3400 | 54 | 54 | 4095 | 345 |
| 263 | -2 | 33 | 296 | 1777142 | 4095 | 3400 | 58 | 58 | 4095 | 345 |
| 263 | 0 | 35 | 298 | 1777142 | 4095 | 3400 | 62 | 62 | 4095 | 345 |
| 263 | 2 | 37 | 300 | 1777142 | 4095 | 3400 | 65 | 65 | 4095 | 345 |
| 263 | 4 | 39 | 302 | 1777142 | 4095 | 3400 | 69 | 69 | 4095 | 345 |
|  | 2 |  |  |  |  |  |  |  |  |  |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 250 | 0 | 41 | 291 | 1870348 | 4088 | 3780 | 76 | 76 | 4090 |

## PC-CODEC

Table 21 Y scaler programming at PAL, input frame size: $800 \times 600$, full anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm$ 10 pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 2930917 | 1736 | 0 | 79 | 79 | 2915 | 867 |
| 255 | -2 | 37 | 292 | 2930917 | 1736 | 0 | 84 | 84 | 2915 | 867 |
| 255 | 0 | 39 | 294 | 2930917 | 1736 | 0 | 89 | 89 | 2915 | 867 |
| 255 | 2 | 41 | 296 | 2930917 | 1736 | 0 | 93 | 93 | 2915 | 867 |
| 255 | 4 | 43 | 298 | 2930917 | 1736 | 0 | 98 | 98 | 2915 | 867 |
| 257 | -4 | 34 | 291 | 2911033 | 1749 | 0 | 77 | 77 | 2922 | 874 |
| 257 | -2 | 36 | 293 | 2911033 | 1749 | 0 | 81 | 81 | 2922 | 874 |
| 257 | 0 | 38 | 295 | 2911033 | 1749 | 0 | 86 | 86 | 2922 | 874 |
| 257 | 2 | 40 | 297 | 2911033 | 1749 | 0 | 91 | 91 | 2922 | 874 |
| 257 | 4 | 42 | 299 | 2911033 | 1749 | 0 | 95 | 95 | 2922 | 874 |
| 259 | -4 | 33 | 292 | 2887172 | 1763 | 0 | 73 | 73 | 2929 | 881 |
| 259 | -2 | 35 | 294 | 2887172 | 1763 | 0 | 78 | 78 | 2929 | 881 |
| 259 | 0 | 37 | 296 | 2887172 | 1763 | 0 | 83 | 83 | 2929 | 881 |
| 259 | 2 | 39 | 298 | 2887172 | 1763 | 0 | 87 | 87 | 2929 | 881 |
| 259 | 4 | 41 | 300 | 2887172 | 1763 | 0 | 92 | 92 | 2929 | 881 |
| 261 | -4 | 32 | 293 | 2863311 | 1778 | 0 | 71 | 71 | 2935 | 887 |
| 261 | -2 | 34 | 295 | 2863311 | 1778 | 0 | 75 | 75 | 2935 | 887 |
| 261 | 0 | 36 | 297 | 2863311 | 1778 | 0 | 80 | 80 | 2935 | 887 |
| 261 | 2 | 38 | 299 | 2863311 | 1778 | 0 | 85 | 85 | 2935 | 887 |
| 261 | 4 | 40 | 301 | 2863311 | 1778 | 0 | 89 | 89 | 2935 | 887 |
| 263 | -4 | 31 | 294 | 2843427 | 1790 | 0 | 68 | 68 | 2942 | 894 |
| 263 | -2 | 33 | 296 | 2843427 | 1790 | 0 | 72 | 72 | 2942 | 894 |
| 263 | 0 | 35 | 298 | 2843427 | 1790 | 0 | 77 | 77 | 2942 | 894 |
| 263 | 2 | 37 | 300 | 2843427 | 1790 | 0 | 82 | 82 | 2942 | 894 |
| 263 | 4 | 39 | 302 | 2843427 | 1790 | 0 | 86 | 86 | 2942 | 894 |
|  |  |  |  |  |  |  |  |  |  |  |

## Full size (horizontal size: 702 pixels)

| 288 | 0 | 22 | 310 | 2596864 | 1960 | 0 | 43 | 43 | 3027 | 979 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 250 | 0 | 41 | 291 | 2990569 | 1701 | 0 | 95 | 95 | 2898 |

## PC-CODEC

Table 22 Y scaler programming at PAL, input frame size: $800 \times 600$, half anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: 640 pixels, offset $\pm \mathbf{1 0}$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 2930917 | 2604 | 2048 | 80 | 80 | 3349 | 277 |
| 255 | -2 | 37 | 292 | 2930917 | 2604 | 2048 | 84 | 84 | 3349 | 277 |
| 255 | 0 | 39 | 294 | 2930917 | 2604 | 2048 | 89 | 89 | 3349 | 277 |
| 255 | 2 | 41 | 296 | 2930917 | 2604 | 2048 | 94 | 94 | 3349 | 277 |
| 255 | 4 | 43 | 298 | 2930917 | 2604 | 2048 | 98 | 98 | 3349 | 277 |
| 257 | -4 | 34 | 291 | 2911033 | 2625 | 2048 | 77 | 77 | 3359 | 287 |
| 257 | -2 | 36 | 293 | 2911033 | 2625 | 2048 | 82 | 82 | 3359 | 287 |
| 257 | 0 | 38 | 295 | 2911033 | 2625 | 2048 | 86 | 86 | 3359 | 287 |
| 257 | 2 | 40 | 297 | 2911033 | 2625 | 2048 | 91 | 91 | 3359 | 287 |
| 257 | 4 | 42 | 299 | 2911033 | 2625 | 2048 | 96 | 96 | 3359 | 287 |
| 259 | -4 | 33 | 292 | 2887172 | 2645 | 2048 | 74 | 74 | 3369 | 297 |
| 259 | -2 | 35 | 294 | 2887172 | 2645 | 2048 | 79 | 79 | 3369 | 297 |
| 259 | 0 | 37 | 296 | 2887172 | 2645 | 2048 | 83 | 83 | 3369 | 297 |
| 259 | 2 | 39 | 298 | 2887172 | 2645 | 2048 | 88 | 88 | 3369 | 297 |
| 259 | 4 | 41 | 300 | 2887172 | 2645 | 2048 | 92 | 92 | 3369 | 297 |
| 261 | -4 | 32 | 293 | 2863311 | 2666 | 2048 | 71 | 71 | 3379 | 307 |
| 261 | -2 | 34 | 295 | 2863311 | 2666 | 2048 | 75 | 75 | 3379 | 307 |
| 261 | 0 | 36 | 297 | 2863311 | 2666 | 2048 | 80 | 80 | 3379 | 307 |
| 261 | 2 | 38 | 299 | 2863311 | 2666 | 2048 | 85 | 85 | 3379 | 307 |
| 261 | 4 | 40 | 301 | 2863311 | 2666 | 2048 | 89 | 89 | 3379 | 307 |
| 263 | -4 | 31 | 294 | 2843427 | 2686 | 2048 | 68 | 68 | 3390 | 318 |
| 263 | -2 | 33 | 296 | 2843427 | 2686 | 2048 | 73 | 73 | 3390 | 318 |
| 263 | 0 | 35 | 298 | 2843427 | 2686 | 2048 | 77 | 77 | 3390 | 318 |
| 263 | 2 | 37 | 300 | 2843427 | 2686 | 2048 | 82 | 82 | 3390 | 318 |
| 263 | 4 | 39 | 302 | 2843427 | 2686 | 2048 | 86 | 86 | 3390 | 318 |
|  | 4 |  |  |  |  |  |  |  |  |  |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 22 | 310 | 2596864 | 2940 | 2048 | 43 | 43 | 3517 | 445 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 250 | 0 | 41 | 291 | 2990569 | 2553 | 2048 | 96 | 96 |

## PC-CODEC

Table 23 Y scaler programming at PAL, input frame size: $800 \times 600$, no anti-flicker filter

| TV LINE | OFFSET | FAL | LAL | PCL | YINC | YSKIP | YOFSO | YOFSE | YIWGTO | YIWGTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regular size (horizontal TV size: $\mathbf{6 4 0}$ pixels, offset $\pm \mathbf{1 0}$ pixels) |  |  |  |  |  |  |  |  |  |  |
| 255 | -4 | 35 | 290 | 2930917 | 3473 | 4095 | 80 | 81 | 3783 | 3161 |
| 255 | -2 | 37 | 292 | 2930917 | 3473 | 4095 | 84 | 85 | 3783 | 3161 |
| 255 | 0 | 39 | 294 | 2930917 | 3473 | 4095 | 89 | 90 | 3783 | 3161 |
| 255 | 2 | 41 | 296 | 2930917 | 3473 | 4095 | 94 | 95 | 3783 | 3161 |
| 255 | 4 | 43 | 298 | 2930917 | 3473 | 4095 | 99 | 100 | 3783 | 3161 |
| 257 | -4 | 34 | 291 | 2911033 | 3500 | 4095 | 77 | 78 | 3796 | 3202 |
| 257 | -2 | 36 | 293 | 2911033 | 3500 | 4095 | 82 | 83 | 3796 | 3202 |
| 257 | 0 | 38 | 295 | 2911033 | 3500 | 4095 | 87 | 88 | 3796 | 3202 |
| 257 | 2 | 40 | 297 | 2911033 | 3500 | 4095 | 91 | 92 | 3796 | 3202 |
| 257 | 4 | 42 | 299 | 2911033 | 3500 | 4095 | 96 | 97 | 3796 | 3202 |
| 259 | -4 | 33 | 292 | 2887172 | 3527 | 4095 | 74 | 75 | 3810 | 3242 |
| 259 | -2 | 35 | 294 | 2887172 | 3527 | 4095 | 79 | 80 | 3810 | 3242 |
| 259 | 0 | 37 | 296 | 2887172 | 3527 | 4095 | 83 | 84 | 3810 | 3242 |
| 259 | 2 | 39 | 298 | 2887172 | 3527 | 4095 | 88 | 89 | 3810 | 3242 |
| 259 | 4 | 41 | 300 | 2887172 | 3527 | 4095 | 93 | 94 | 3810 | 3242 |
| 261 | -4 | 32 | 293 | 2863311 | 3555 | 4095 | 71 | 72 | 3823 | 3284 |
| 261 | -2 | 34 | 295 | 2863311 | 3555 | 4095 | 76 | 77 | 3823 | 3284 |
| 261 | 0 | 36 | 297 | 2863311 | 3555 | 4095 | 80 | 81 | 3823 | 3284 |
| 261 | 2 | 38 | 299 | 2863311 | 3555 | 4095 | 85 | 86 | 3823 | 3284 |
| 261 | 4 | 40 | 301 | 2863311 | 3555 | 4095 | 89 | 90 | 3823 | 3284 |
| 263 | -4 | 31 | 294 | 2843427 | 3582 | 4095 | 68 | 69 | 3837 | 3324 |
| 263 | -2 | 33 | 296 | 2843427 | 3582 | 4095 | 73 | 74 | 3837 | 3324 |
| 263 | 0 | 35 | 298 | 2843427 | 3582 | 4095 | 78 | 79 | 3837 | 3324 |
| 263 | 2 | 37 | 300 | 2843427 | 3582 | 4095 | 82 | 83 | 3837 | 3324 |
| 263 | 4 | 39 | 302 | 2843427 | 3582 | 4095 | 87 | 88 | 3837 | 3324 |
|  | 4 |  |  |  |  |  |  |  |  |  |

## Full size (horizontal size: $\mathbf{7 0 2}$ pixels)

| 288 | 0 | 22 | 310 | 2596864 | 3923 | 4095 | 44 | 45 | 4007 | 3836 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | Small size (horizontal size: 620 pixels) $\quad$|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 250 | 0 | 41 | 291 | 2990569 | 3405 | 4095 | 96 | 97 | 3748 |

## PC-CODEC

Table 24 "ITU-R BT.601" signal component levels

| COLOUR | SIGNALS $^{(1)}$ |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathbf{Y}$ | $\mathbf{C}_{\mathbf{B}}$ | $\mathbf{C}_{\mathbf{R}}$ | $\mathbf{R}$ | $\mathbf{G}$ | $\mathbf{B}$ |
| White | 235 | 128 | 128 | 235 | 235 | 235 |
| Yellow | 210 | 16 | 146 | 235 | 235 | 16 |
| Cyan | 170 | 166 | 16 | 16 | 235 | 235 |
| Green | 145 | 54 | 34 | 16 | 235 | 16 |
| Magenta | 106 | 202 | 222 | 235 | 16 | 235 |
| Red | 81 | 90 | 240 | 235 | 16 | 16 |
| Blue | 41 | 240 | 110 | 16 | 16 | 235 |
| Black | 16 | 128 | 128 | 16 | 16 | 16 |

## Note

1. Transformation:
a) $R=Y+1.3707 \times\left(C_{R}-128\right)$
b) $G=Y-0.3365 \times\left(C_{B}-128\right)-0.6982 \times\left(C_{R}-128\right)$
c) $B=Y+1.7324 \times\left(C_{B}-128\right)$.

Table 25 Pin assignment for input format 0

| $\begin{gathered} 8+8+8 \text {-BIT } 4: 4: 4 \text { NON-INTERLACED } \\ \text { RGB/C } C_{B}-Y-C_{R} \end{gathered}$ |  |  |
| :---: | :---: | :---: |
| PIN | FALLING CLOCK EDGE | RISING CLOCK EDGE |
| PD11 | G3/Y3 | $\mathrm{R} 7 / \mathrm{C}_{\mathrm{R}} 7$ |
| PD10 | G2/Y2 | $\mathrm{R} 6 / \mathrm{C}_{\mathrm{R}} 6$ |
| PD9 | G1/Y1 | $\mathrm{R} 5 / \mathrm{C}_{\mathrm{R}} 5$ |
| PD8 | G0/Y0 | R4/CR 4 |
| PD7 | $\mathrm{B} 7 / \mathrm{C}_{\mathrm{B}} 7$ | $\mathrm{R} 3 / \mathrm{C}_{\mathrm{R}} 3$ |
| PD6 | $\mathrm{B} 6 / \mathrm{C}_{\mathrm{B}} 6$ | $\mathrm{R} 2 / \mathrm{C}_{\mathrm{R}} 2$ |
| PD5 | $\mathrm{B} 5 / \mathrm{C}_{\mathrm{B}} 5$ | $\mathrm{R} 1 / \mathrm{C}_{\mathrm{R}} 1$ |
| PD4 | B4/C ${ }_{\text {B }} 4$ | $\mathrm{R} 0 / \mathrm{C}_{\mathrm{R}} 0$ |
| PD3 | B3/C ${ }_{\text {B }} 3$ | G7/Y7 |
| PD2 | $\mathrm{B} 2 / \mathrm{C}_{\mathrm{B}} 2$ | G6/Y6 |
| PD1 | $\mathrm{B} 1 / \mathrm{C}_{\mathrm{B}} 1$ | G5/Y5 |
| PD0 | $\mathrm{B} 0 / \mathrm{C}_{\mathrm{B}} 0$ | G4/Y4 |

Table 26 Pin assignment for input format 1

| $\mathbf{5 + 5}+\mathbf{5 - B I T} \mathbf{4}: \mathbf{4}: \mathbf{4}$ NON-INTERLACED RGB |  |  |
| :--- | :---: | :---: |
| PIN |  | FALLING <br> CLOCK EDGE |
| PLOCK EDGE |  |  |
| CLI | G2 | X |
| PD6 | G1 | R4 |
| PD5 | G0 | R3 |
| PD4 | B4 | R2 |
| PD3 | B3 | R1 |
| PD2 | B2 | R0 |
| PD1 | B1 | G4 |
| PD0 | B0 | G3 |

Table 27 Pin assignment for input format 2

| $5+\mathbf{6}+5$-BIT $\mathbf{4}: \mathbf{4}: \mathbf{4}$ NON-INTERLACED RGB |  |  |
| :--- | :---: | :---: |
| PIN |  | FALLING <br> CLOCK EDGE |
| PD7 | RISING <br> CLOCK EDGE |  |
| PD6 | G2 | R4 |
| PD5 | G1 | R3 |
| PD4 | G0 | R2 |
| PD3 | B4 | R1 |
| PD2 | B3 | R0 |
| PD1 | B2 | G5 |
| PD0 | B1 | G4 |

Table 28 Pin assignment for input format 3

| 8+8+8-BIT 4:2:2 NON-INTERLACED $\mathrm{C}_{\mathrm{B}}$ - $\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| PIN | FALLING CLOCK EDGE n | RISING CLOCK EDGE n | FALLING CLOCK EDGE n + 1 | RISING CLOCK EDGE n + 1 |
| PD7 | $\mathrm{C}_{\mathrm{B}} 7$ (0) | Y7(0) | $\mathrm{C}_{\mathrm{R}} 7(0)$ | Y7(1) |
| PD6 | $\mathrm{C}_{\mathrm{B}} 6$ (0) | Y6(0) | $\mathrm{C}_{\mathrm{R}} 6$ (0) | Y6(1) |
| PD5 | $\mathrm{C}_{\mathrm{B}} 5(0)$ | Y5(0) | $\mathrm{C}_{\mathrm{R}} 5(0)$ | Y5(1) |
| PD4 | $\mathrm{C}_{\mathrm{B}} 4$ (0) | Y4(0) | $\mathrm{C}_{\mathrm{R}} 4$ (0) | Y4(1) |
| PD3 | $\mathrm{C}_{\mathrm{B}} 3$ (0) | Y3(0) | $\mathrm{C}_{\mathrm{R}} 3$ (0) | Y3(1) |
| PD2 | $\mathrm{C}_{\mathrm{B}} 2$ (0) | Y2(0) | $\mathrm{C}_{\mathrm{R}} 2(0)$ | Y2(1) |
| PD1 | $\mathrm{C}_{\mathrm{B}} 1$ (0) | Y1(0) | $\mathrm{C}_{\mathrm{R}} 1$ (0) | Y1(1) |
| PD0 | $\mathrm{C}_{\mathrm{B}} \mathrm{O}(0)$ | YO(0) | $\mathrm{C}_{\mathrm{R}} \mathrm{O}(0)$ | Y0(1) |

Table 29 Pin assignment for input format 4

| 8 + 8 + 8-BIT 4 : 2 : 2 INTERLACED $C_{B}-Y-C_{R}$ <br> (ITU-R BT.656, 27 MHz CLOCK) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| PIN | RISING CLOCK EDGE n | RISING CLOCK EDGE n + 1 | RISING <br> CLOCK <br> EDGE $\mathrm{n}+2$ | RISING CLOCK EDGE n + 3 |
| PD7 | $\mathrm{C}_{\mathrm{B}} 7(0)$ | Y7(0) | $\mathrm{C}_{\mathrm{R}} 7(0)$ | Y7(1) |
| PD6 | $\mathrm{C}_{\mathrm{B}} 6$ (0) | Y6(0) | $\mathrm{C}_{\mathrm{R}} 6(0)$ | Y6(1) |
| PD5 | $\mathrm{C}_{\mathrm{B}} 5(0)$ | Y5(0) | $\mathrm{C}_{\mathrm{R}} 5(0)$ | Y5(1) |
| PD4 | $\mathrm{C}_{\mathrm{B}} 4(0)$ | Y4(0) | $\mathrm{C}_{\mathrm{R}} 4(0)$ | Y4(1) |
| PD3 | $\mathrm{C}_{\mathrm{B}} 3(0)$ | Y3(0) | $\mathrm{C}_{\mathrm{R}} 3(0)$ | Y3(1) |
| PD2 | $\mathrm{C}_{\mathrm{B}} 2(0)$ | Y2(0) | $\mathrm{C}_{\mathrm{R}} 2(0)$ | Y2(1) |
| PD1 | $\mathrm{C}_{\mathrm{B}} 1(0)$ | Y1(0) | $\mathrm{C}_{\mathrm{R}} 1(0)$ | Y1(1) |
| PD0 | $\mathrm{C}_{\mathrm{B}} 0(0)$ | Y0(0) | $\mathrm{C}_{\mathrm{R}} 0(0)$ | Y0(1) |

Table 30 Pin assignment for input format 5; note 1

| 8-BIT NON-INTERLACED INDEX COLOUR |  |  |
| :--- | :---: | :---: |
| PIN |  | FALLING <br> CLOCK EDGE |
| PD11 | RISING <br> CLOCK EDGE |  |
| PD10 | $X$ | $X$ |
| PD9 | $X$ | $X$ |
| PD8 | $X$ | $X$ |
| PD7 | INDEX7 | $X$ |
| PD6 | INDEX6 | $X$ |
| PD5 | INDEX5 | $X$ |
| PD4 | INDEX4 | $X$ |
| PD3 | INDEX3 | $X$ |
| PD2 | INDEX2 | $X$ |
| PD1 | INDEX1 | $X$ |
| PD0 | INDEX0 | $X$ |

## Note

1. $X=$ don't care.

Table 31 Pin assignment for input format 6

| $\begin{gathered} 8+8+8 \text {-BIT } 4: 4: 4 \text { NON-INTERLACED } \\ \text { RGB/C } C_{B}-Y-C_{R} \end{gathered}$ |  |  |
| :---: | :---: | :---: |
| PIN | $\begin{aligned} & \text { FALLING } \\ & \text { CLOCK EDGE } \end{aligned}$ | RISING CLOCK EDGE |
| PD11 | G4/Y4 | $\mathrm{R} 7 / \mathrm{C}_{\mathrm{R}} 7$ |
| PD10 | G3/Y3 | $\mathrm{R} 6 / \mathrm{C}_{\mathrm{R}} 6$ |
| PD9 | G2/Y2 | $\mathrm{R} 5 / \mathrm{C}_{\mathrm{R}} 5$ |
| PD8 | B7/C ${ }^{\text {7 }}$ | $\mathrm{R} 4 / \mathrm{C}_{\mathrm{R}} 4$ |
| PD7 | $\mathrm{B} 6 / \mathrm{C}_{\mathrm{B}} 6$ | $\mathrm{R} 3 / \mathrm{C}_{\mathrm{R}} 3$ |
| PD6 | B5/C C 5 | G7/Y7 |
| PD5 | B4/CB4 | G6/Y6 |
| PD4 | B3/CB3 | G5/Y5 |
| PD3 | G0/Y0 | $\mathrm{R} 2 / \mathrm{C}_{\mathrm{R}} 2$ |
| PD2 | $\mathrm{B} 2 / \mathrm{C}_{\mathrm{B}} 2$ | $\mathrm{R} 1 / \mathrm{C}_{\mathrm{R}} 1$ |
| PD1 | $\mathrm{B} 1 / \mathrm{C}_{\mathrm{B}} 1$ | $\mathrm{R} 0 / \mathrm{C}_{\mathrm{R}} 0$ |
| PD0 | $\mathrm{B} 0 / \mathrm{C}_{\mathrm{B}} 0$ | G1/Y1 |

## PC-CODEC

## 9 FUNCTIONAL DESCRIPTION OF DIGITAL VIDEO DECODER PART

### 9.1 Decoder

### 9.1.1 ANALOG INPUT PROCESSING

The SAA7108E; SAA7109E offers six analog signal inputs, two analog main channels with source switch, clamp circuit, analog amplifier, anti-alias filter and video 9-bit CMOS ADC; see Fig.14.

### 9.1.2 ANALOG CONTROL CIRCUITS

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. The characteristics are illustrated in Fig.11. During the vertical blanking period, gain and clamping control is frozen.


Fig. 11 Anti-alias filter.

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### 9.1.2.1 Clamping

The clamping control circuit controls the correct clamping of the analog input signals. A coupling capacitor is used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal.

### 9.1.2.2 Gain control

The gain control circuit receives (via the $\mathrm{I}^{2} \mathrm{C}$-bus) the static gain levels for the two analog amplifiers, or controls one of these amplifiers automatically via a built-in Automatic Gain Control (AGC) as part of the Analog Input Control (AICO).

The AGC (automatic gain control for luminance) is used to amplify a CVBS or $Y$ signal to the required signal amplitude, which is matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal.
Signal (white) peak control limits the gain at signal overshoots. The influence of supply voltage variation within the specified range is automatically eliminated by clamping and automatic gain control. The flow charts show more details of the AGC; see Figs 15 and 16.


Fig. 13 Automatic gain range.


Fig. 14 Analog input processing using the SAA7108E; SAA7109E as differential front-end with 9-bit ADC.



WIPE $=$ white peak level (254).
SBOT = sync bottom level (1).
CLL = clamp level [60 Y (128 C)].
HSY = horizontal sync pulse.
HCL = horizontal clamp pulse.
Fig. 16 Clamp and gain flow.

### 9.1.3 CHROMINANCE AND LUMINANCE PROCESSING



Fig. 17 Chrominance and luminance processing

### 9.1.3.1 Chrominance path

The 9-bit CVBS or chrominance input signal is fed to the input of a quadrature demodulator, where it is multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 1 ( 0 and $90^{\circ}$ phase relationship to the demodulator axis). The frequency is dependent on the chosen colour standard.

The time-multiplexed output signals of the multipliers are low-pass filtered (low-pass 1). Eight characteristics are programmable via LCBW3 to LCBW0 to achieve the desired bandwidth for the colour difference signals (PAL, NTSC) or the $0^{\circ}$ and $90^{\circ} \mathrm{FM}$ signals (SECAM).

The chrominance low-pass 1 characteristic also influences the grade of cross-luminance reduction during horizontal colour transients (large chrominance bandwidth means strong suppression of cross-luminance). If the Y comb filter is disabled when YCOMB $=0$ the filter directly influences the width of the chrominance notch within the luminance path (large chrominance bandwidth means wide chrominance notch resulting to lower luminance bandwidth).

The low-pass filtered signals are fed to the adaptive comb filter block. The chrominance components are separated from the luminance via a two-line vertical stage (four lines for PAL standards) and a decision logic circuit between the filtered and the non-filtered output signals: this block is bypassed for SECAM signals. The comb filter logic can be enabled independently for the succeeding luminance and chrominance processing by YCOMB (subaddress 09H, bit 6) and/or CCOMB (subaddress 0 EH , bit 0 ). It is always bypassed during VBI or raw data lines, programmable by the LCRn registers (subaddresses 41 H to 57 H ); see Section 9.2.

The separated $C_{B}-C_{R}$ components are further processed by a second filter stage (low-pass 2 ) to modify the chrominance bandwidth without influencing the luminance path. It's characteristic is controlled by CHBW (subaddress 10 H , bit 3). For the complete transfer characteristic of low-pass filters 1 and 2 see Figs 18 and 19.

The SECAM processing (bypassed for QAM standards) contains the following blocks:

- Baseband 'bell' filters to reconstruct the amplitude and phase equalized $0^{\circ}$ and $90^{\circ} \mathrm{FM}$ signals
- Phase demodulator and differentiator (FM demodulation)
- De-emphasis filter to compensate the pre-emphasized input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM switch signal).

The succeeding chrominance gain control block amplifies or attenuates the $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ signal according to the required ITU 601/656 levels. It is controlled by the output signal from the amplitude detection circuit within the burst processing block.

The burst processing block provides the feedback loop of the chrominance PLL and contains the following:

- Burst gate accumulator
- Colour identification and killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)
- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, $\mathrm{H} / 2$-switch generation.
The increment generation circuit produces the Discrete Time Oscillator (DTO) increment for both subcarrier generation blocks. It contains a division by the increment of the line-locked clock generator to create a stable phase-locked sine signal under all conditions (e.g. for non-standard signals).

The PAL delay line block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC colour standards, the delay line can be used as an additional vertical filter. If desired, it can be switched off by DCVF = 1 . It is always disabled during VBI or raw data lines programmable by the LCRn registers (subaddresses 41 H to 57 H ), see
Section 9.2. The embedded line delay is also used for SECAM recombination (cross-over switches).
(1) $\operatorname{LCBW}[2: 0]=000$.
(2) $\operatorname{LCBW}[2: 0]=010$.
(3) LCBW[2:0] $=100$.
(4) $\operatorname{LCBW}[2: 0]=110$.
(5) $\operatorname{LCBW}[2: 0]=001$.
(6) $\operatorname{LCBW}[2: 0]=011$.
(7) LCBW[2:0] $=101$.
(8) $\operatorname{LCBW}[2: 0]=111$.



Fig. 18 Transfer characteristics of the chrominance low-pass at $\mathrm{CHBW}=0$.
(1) $\operatorname{LCBW}[2: 0]=000$.
(2) LCBW[2:0] $=010$.
(3) LCBW[2:0] $=100$.
(4) $\operatorname{LCBW}[2: 0]=110$.
(5) $\operatorname{LCBW}[2: 0]=001$.
(6) $\operatorname{LCBW}[2: 0]=011$.
(7) LCBW[2:0] $=101$.
(8) $\operatorname{LCBW}[2: 0]=111$.



Fig. 19 Transfer characteristics of the chrominance low-pass at $\mathrm{CHBW}=1$.

### 9.1.3.2 Luminance path

The rejection of the chrominance components within the 9-bit CVBS or Y input signal is done by subtracting the re-modulated chrominance signal from the CVBS input.

The comb filtered $C_{B}-C_{R}$ components are interpolated (upsampled) by the low-pass 3 block. It's characteristic is controlled by LUBW (subaddress 09H, bit 4) to modify the width of the chrominance 'notch' without influencing the chrominance path. The programmable frequency characteristics available, in conjunction with the LCBW2 to LCBW0 settings, can be seen in Figs 20 to 23. It should be noted that these frequency curves are only valid for Y comb disabled filter mode (YCOMB $=0$ ). In comb filter mode the frequency response is flat. The centre frequency of the notch is automatically adapted to the chosen colour standard.

The interpolated $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ samples are multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 2. This second DTO is locked to the first subcarrier generator by an increment delay circuit matched to the processing delay, which is different for PAL and NTSC standards according to the chosen comb filter algorithm. The two modulated signals are finally added to create the re-modulated chrominance signal.

The frequency characteristic of the separated luminance signal can be further modified by the succeeding luminance filter block. It can be configured as peaking (resolution enhancement) or low-pass block by LUFI3 to LUFI0 (subaddress 09H, bits 3 to 0). The 16 resulting frequency characteristics can be seen in Fig.24. The LUFI3 to LUFIO settings can be used as a user programmable sharpness control.

The luminance filter block also contains the adjustable Y delay part; programmable by YDEL2 to YDEL0 (subaddress 11 H , bits 2 to 0 ).
(1) LCBW[2:0] $=000$.
(2) LCBW[2:0] $=010$.
(3) LCBW[2:0] $=100$.
(4) $\operatorname{LCBW}[2: 0]=110$.



Fig. 20 Transfer characteristics of the luminance notch filter in 3.58 MHz mode ( Y -comb filter disabled) at LUBW $=0$.
(1) $\operatorname{LCBW}[2: 0]=000$
(2) $\operatorname{LCBW}[2: 0]=010$
(3) LCBW[2:0] $=100$
(4) $\operatorname{LCBW}[2: 0]=110$


V
(dB)


Fig. 21 Transfer characteristics of the luminance notch filter in 3.58 MHz mode ( Y -comb filter disabled) at LUBW =1.
(1) LCBW[2:0] $=000$.
(2) LCBW[2:0] $=010$.
(3) $\operatorname{LCBW}[2: 0]=100$.
(4) LCBW[2:0] $=110$.


V
(dB)


Fig. 22 Transfer characteristics of the luminance notch filter in 4.43 MHz mode ( Y -comb filter disabled) at LUBW $=0$.

(1) $\operatorname{LUFI[3:0]}=0001$
(2) LUFI[3:0] $=0010$.
(3) LUFI[3:0] $=0011$
(4) $\operatorname{LUFI[3:0]}=0100$
(5) LUFI[3:0] $=0101$.
(6) LUFI[3:0] $=0110$
(7) LUFI[3:0] $=0111$
(8) LUFI[3:0] $=0000$
(9) LUFI[3:0] $=1000$
(10) LUFI[3:0] = 1001
(11) LUFI[3:0] $=1010$
(12) LUFI[3:0] $=1011$
(13) $\operatorname{LUFI}[3: 0]=1100$
(14) LUFI[3:0] = 1101
(15) LUFI[3:0] $=1110$.
(16) LUFI[3:0] = 1111.



Fig. 24 Transfer characteristics of the luminance peaking/low-pass filter (sharpness).

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### 9.1.3.3 Brightness Contrast Saturation (BCS) control and decoder output levels

The resulting $Y(C V B S)$ and $C_{B}-C_{R}$ signals are fed to the BCS block, which contains the following functions:

- Chrominance saturation control by DSAT7 to DSAT0
- Luminance contrast and brightness control by DCON7 to DCON0 and DBRI7 to DBRIO
- Raw data (CVBS) gain and offset adjustment by RAWG7 to RAWG0 and RAWO7 to RAWO0
- Limiting $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ or CVBS to the values 1 (minimum) and 254 (maximum) to fulfil "ITU Recommendation 601/656".

[^0]
a. Sources containing 7.5 IRE black level offset (e.g. NTSC M).
b. Sources not containing black level offset.

CVBS levels with default settings RAWG[7:0] = 64 and RAWO[7:0] $=128$.
Equation for modification of the raw data levels via bytes RAWG and RAWO:
CVBS $_{\text {OUT }}=\operatorname{Int}\left[\frac{\text { RAWG }}{64} \times\left(\right.\right.$ CVBS $\left.\left._{\text {nom }}-128\right)\right]+$ RAWO
It should be noted that the resulting levels are limited to 1 to 254 in accordance with "ITU Recommendation 601/656".
Fig. 26 CVBS (raw data) range for scaler input, data slicer and $X$ port output.

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### 9.1.4 SYNCHRONIZATION

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is further reduced to 1 MHz by a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e.g. HCL and HSY) are generated in accordance with analog front-end requirements. The loop filter signal drives an oscillator to generate the line frequency control signal (LFCO); see Fig. 27.

The detection of 'pseudo syncs' as part of the macrovision copy protection standard is also done within the synchronization circuit.

The result is reported as flag COPRO within the decoder status byte at subaddress 1 FH .

### 9.1.5 CLOCK GENERATION CIRCUIT

The internal CGC generates all clock signals required for the video input processor.

The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is a multiple of the line frequency:

$$
\begin{aligned}
& 6.75 \mathrm{MHz}=429 \times \mathrm{f}_{\mathrm{H}}(50 \mathrm{~Hz}) \text {, or } \\
& 6.75 \mathrm{MHz}=432 \times \mathrm{f}_{\mathrm{H}}(60 \mathrm{~Hz}) .
\end{aligned}
$$

The LFCO signal is multiplied Internally by a factor of 2 and 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the output clock signals. The rectangular output clocks have a $50 \%$ duty cycle.

Table 32 Decoder clock frequencies

| CLOCK | FREQUENCY (MHz) |
| :--- | :---: |
| XTAL | 24.576 or 32.110 |
| LLC | 27 |
| LLC2 | 13.5 |
| LLC4 (internal) | 6.75 |
| LLC8 (virtual) | 3.375 |



Fig. 27 Block diagram of the clock generation circuit.

### 9.1.6 Power-on reset and CE input

A missing clock, insufficient digital or analog $\mathrm{V}_{\text {DDAd }}$ supply voltages (below 2.7 V ) will start the reset sequence; all outputs are forced to 3 -state (see Fig.28). The indicator output $\overline{\text { RES }}$ is LOW for approximately 128 LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

It is possible to force a reset by pulling the Chip Enable (CE) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2 and SDAd return from 3-state to active, while the other signals have to be activated via programming.



POC = Power-on Control.
$\mathrm{CE}=$ chip enable input.
XTALO = crystal oscillator output.
LLCINT = internal system clock.
RESINT = internal reset.
LLC = line-locked clock output.
$\overline{R E S}=$ reset output.
Fig. 28 Power-on control circuit.

### 9.2 Decoder output formatter

The output interface block of the decoder part contains the ITU 656 formatter for the expansion port data output XPD7 to XPD0 (see Section 10.4.1) and the control circuit for the signals needed for the internal paths to the scaler and data slicer part. It also controls the selection of the reference signals for the RT port (RTCO, RTS0 and RTS1) and the expansion port (XRH, XRV and XDQ).

The generation of the decoder data type control signals SET_RAW and SET VBI is also done within this block. These signals are decoded from the requested data type for the scaler input and/or the data slicer, selectable by the control registers LCR2 to LCR24 (see Section 18.2.4.2).

For each LCR value, from 2 to 23, the data type can be programmed individually. LCR2 to LCR23 refer to line numbers. The selection in LCR24 values is valid for the rest of the corresponding field. The upper nibble contains the value for field 1 (odd), the lower nibble for field 2 (even). The relationship between LCR values and line numbers can be adjusted via VOFF8 to VOFF0, located in subaddresses 5BH (bit 4) and 5AH (bits 7 to 0 ) and FOFF subaddress 5BH (bit 7). The recommended values are VOFF[8:0] = 03 H for 50 Hz sources (with FOFF = 0) and VOFF[8:0] $=06 \mathrm{H}$ for 60 Hz sources (with FOFF = 1), to accommodate line number conventions as used for PAL, SECAM and NTSC standards; see Tables 34 to 37.

Table 33 Data formats at decoder output

| DATA TYPE NUMBER | DATA TYPE | DECODER OUTPUT DATA FORMAT |
| :---: | :---: | :---: |
| 0 | teletext EuroWST, CCST | raw |
| 1 | European Closed Caption | raw |
| 2 | Video Programming Service (VPS) | raw |
| 3 | Wide screen signalling bits | raw |
| 4 | US teletext (WST) | raw |
| 5 | US Closed Caption (line 21) | raw |
| 6 | video component signal, VBI region | Y-C $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2 |
| 7 | CVBS data | raw |
| 8 | teletext | raw |
| 9 | VITC/EBU time codes (Europe) | raw |
| 10 | VITC/SMPTE time codes (USA) | raw |
| 11 | reserved | raw |
| 12 | US NABTS | raw |
| 13 | MOJI (Japanese) | raw |
| 14 | Japanese format switch (L20/22) | raw |
| 15 | video component signal, active video region | $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$ |

Table 34 Relationship of LCR to line numbers in 525 lines/ 60 Hz systems (part 1)
Vertical line offset, VOFF[8:0] = 06 H (subaddresses $5 \mathrm{BH}[4]$ and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and

| Line number (1st field) | 521 | 522 | 523 | 524 | 525 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | active video |  |  |  |  | equalization pulses |  |  | serration pulses |  |  | equalization pulses |  |  |
| Line number (2nd field) | 259 | 260 | 261 | 262 | 263 | 264 | 265 | 266 | 267 | 268 | 269 | 270 | 271 | 272 |
|  | active video |  |  |  | equalization pulses |  |  |  | serration pulses |  |  | ualiz | puls |  |
| LCR | 24 |  |  |  |  |  | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

Table 35 Relationship of LCR to line numbers in 525 lines/ 60 Hz systems (part 2)
Vertical line offset, VOFF[8:0] = 06H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and

| Line number (1st field) | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | nominal VBI-lines F1 |  |  |  |  |  |  |  |  |  |  |  | active video |  |  |  |
| Line number (2nd field) | 273 | 274 | 275 | 276 | 277 | 278 | 279 | 280 | 281 | 282 | 283 | 284 | 285 | 286 | 287 | 288 |
|  | nominal VBI-lines F2 |  |  |  |  |  |  |  |  |  |  |  | active video |  |  |  |
| LCR | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |  |  |

Vertical line offset, VOFF[8:0] $=03 \mathrm{H}$ (subaddresses $5 \mathrm{BH}[4]$ and $5 \mathrm{AH}[7: 0]$ ); horizont 59H[7:0]); FOFF = 0 (subaddress 5BH[7])


Table 37 Relationship of LCR to line numbers in 625 lines $/ 50 \mathrm{~Hz}$ systems (part 2)
Vertical line offset, VOFF[8:0] = 03H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 0 (subaddress 5BH[7])

| Line number (1st field) | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | nominal VBI-lines F1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | active video |  |
| Line number (2nd field) | 319 | 320 | 321 | 322 | 323 | 324 | 325 | 326 | 327 | 328 | 329 | 330 | 331 | 332 | 333 | 334 | 335 | 336 | 337 | 338 |
|  | nominal VBI-lines F2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | active video |  |  |
| LCR | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |  |  |


(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.
The control signals listed above are available on pins RTSO, RTS1, XRH and XRV according to the following table:

| NAME | RTS0 (PIN K13) | RTS1 (PIN L10) | XRH (PIN N2) | XRV (PIN L5) |
| :--- | :---: | :---: | :---: | :---: |
| HREF | X | X | X | - |
| F_ITU656 | - | - | - | X |
| V123 | X | X | - | X |
| VGATE | X | X | - | - |
| FID | X | X | - | - |

For further information see programming section, Tables 167, 168 and 169.
Fig. 29 Vertical timing diagram for $50 \mathrm{~Hz} / 625$ line systems.

(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.
The control signals listed above are available on pins RTSO, RTS1, XRH and XRV according to the following table:

| NAME | RTS0 (PIN K13 | RTS1 (PIN L10) | XRH (PIN N2) | XRV (PIN L5) |
| :--- | :---: | :---: | :---: | :---: |
| HREF | X | X | X | - |
| F_ITU656 | - | - | - | X |
| V123 | X | X | - | X |
| VGATE | X | X | - | - |
| FID | X | X | - | - |

For further information see programming section, Tables 167, 168 and 169.
Fig. 30 Vertical timing diagram for $60 \mathrm{~Hz} / 525$ line systems.


The signals HREF, HS, CREF2 and CREF are available on pins RTS0 and/or RTS1 (see Section 18.2.2.19 Tables 167 and 168); their polarity can be inverted via RTP0 and/or RTP1.
The signals HREF and HS are available on pin XRH (see Section 18.2.2.20 Table 169).
Fig. 31 Horizontal timing diagram $(50 / 60 \mathrm{~Hz})$.

### 9.3 Scaler

The High Performance video Scaler (HPS) is based on the system as implemented in the SAA7140, but enhanced in some aspects. Vertical upsampling is supported and the processing pipeline buffer capacity is enhanced, to allow more flexible video stream timing at the image port, discontinuous transfers and handshake. The internal data flow from block to block is discontinuous dynamically, due to the scaling process.

The flow is controlled by internal data valid and data request flags (internal handshake signalling) between the sub-blocks. Therefore the entire scaler acts as a pipeline buffer. Depending on the actually programmed scaling parameters the effective buffer can exceed to an entire line. The access/bandwidth requirements to the VGA frame buffer are reduced significantly.

The high performance video scaler in the SAA7108E; SAA7109E has the following major blocks.

- Acquisition control (horizontal and vertical timer) and task handling (the region/field/frame based processing)
- Prescaler, for horizontal downscaling by an integer factor, combined with appropriate band limiting filters, especially anti-aliasing for CIF format
- Brightness, saturation and contrast control for scaled output data
- Line buffer, with asynchronous read and write, to support vertical upscaling (e.g. for videophone application, converting 240 into 288 lines, $Y-C_{B}-C_{R}$ 4:2:2)
- Vertical scaling, with phase accurate Linear Phase Interpolation (LPI) for zoom and downscaling, or phase accurate Accumulation Mode (ACM) for large downscaling ratios and better anti-alias suppression
- Variable Phase Delay (VPD), operates as horizontal phase accurate interpolation for arbitrary non-integer scaling ratios, supporting conversion between square and rectangular pixel sampling
- Output formatter for scaled $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$, $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : 1:1 and Y only (format also for raw data)
- FIFO, 32-bit wide, with 64 pixel capacity in $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ formats
- Output interface, 8 or 16-bit (only if extended by H port) data pins wide, synchronous or asynchronous operation, with stream events on discrete pins, or coded in the data stream.

The overall H and V zooming ( HV _zoom) is restricted by the input/output data rate relationships. With a safety margin of $2 \%$ for running in and running out, the maximum HV_zoom is equal to:
$0.98 \times \frac{\text { T_input_field }- \text { T_v_blanking }}{\text { in_pixel } \times \text { in_lines } \times \text { out_cycle_per_pix } \times \text { T_out_clk }}$
For example:

1. Input from decoder: $50 \mathrm{~Hz}, 720$ pixel, 288 lines, 16-bit data at 13.5 MHz data rate, 1 cycle per pixel; output: 8 -bit data at $27 \mathrm{MHz}, 2$ cycles per pixel; the maximum HV_zoom is equal to:
$0.98 \times \frac{20 \mathrm{~ms}-24 \times 64 \mu \mathrm{~s}}{720 \times 288 \times 2 \times 37 \mathrm{~ns}}=1.18$
2. Input from $X$ port: $60 \mathrm{~Hz}, 720$ pixel, 240 lines, 8 -bit data at 27 MHz data rate (ITU 656), 2 cycles per pixel; output via I + H port: 16-bit data at 27 MHz clock, 1 cycle per pixel; the maximum HV_zoom is equal to:
$0.98 \times \frac{16.666 \mathrm{~ms}-22 \times 64 \mu \mathrm{~s}}{720 \times 240 \times 1 \times 37 \mathrm{~ns}}=2.34$
The video scaler receives its input signal from the video decoder or from the expansion port ( X port). It gets 16-bit $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2 input data at a continuous rate of 13.5 MHz from the decoder. A discontinuous data stream can be accepted from the expansion port, normally 8 -bit wide ITU 656 like $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ data, accompanied by a pixel qualifier on XDQ.
The input data stream is sorted into two data paths, one for luminance (or raw samples), and one for time multiplexed chrominance $C_{B}$ and $C_{R}$ samples. $A Y-C_{B}-C_{R} 4: 1: 1$ input format is converted to $4: 2: 2$ for the horizontal prescaling and vertical filter scaling operation.
The scaler operation is defined by two programming pages $A$ and $B$, representing two different tasks that can be applied field alternating or to define two regions in a field (e.g. with different scaling range, factors, and signal source during odd and even fields).

Each programming page contains control for:

- Signal source selection and formats
- Task handling and trigger conditions
- Input and output acquisition window definition
- H prescaler, V scaler and H phase scaling.

Raw VBI data will be handled as specific input format and need its own programming page (equals own task).

In VBI pass through operation the processing of prescaler and vertical scaling has to be disabled, however the horizontal fine scaling VPD can be activated. Upscaling (oversampling, zooming), free of frequency folding, up to factor 3.5 can be achieved, as required by some software data slicing algorithms.

These raw samples are transported through the image port as valid data and can be output as $Y$ only format. The lines are framed by SAV and EAV codes.

### 9.3.1 ACQUISITION CONTROL AND TASK HANDLING (SUbaddresses $80 \mathrm{H}, 90 \mathrm{H}, 91 \mathrm{H}, 94 \mathrm{H}$ to 9FH and C4H To CFH)

The acquisition control receives horizontal and vertical synchronization signals from the decoder section or from the $X$ port. The acquisition window is generated via pixel and line counters at the appropriate places in the data path. Only qualified pixels and lines (lines with qualified pixel) are counted from the $X$ port.
The acquisition window parameters are as follows:

- Signal source selection: input video stream and formats from the decoder, or from the $X$ port (programming bits SCSRC[1:0] 91H[5:4] and FSC[2:0] 91H[2:0])
Remark: The input of raw VBI data from the internal decoder should be controlled via the decoder output formatter and the LCR registers (see Section 9.2)
- Vertical offset: defined in lines of the video source, parameter $\mathrm{YO}[11: 0]$ 99H[3:0] 98H[7:0]
- Vertical length: defined in lines of the video source, parameter YS[11:0] 9BH[3:0] 9AH[7:0]
- Vertical length: defined in number of target lines, as a result of vertical scaling, parameter YD[11:0] 9FH[3:0] 9EH[7:0]
- Horizontal offset: defined in number of pixels of the video source, parameter XO[11:0] 95H[3:0] 94H[7:0]
- Horizontal length: defined in number of pixels of the video source, parameter XS[11:0] 97H[3:0] 96H[7:0]
- Horizontal destination size: defined in target pixels after fine scaling, parameter XD[11:0] 9DH[3:0] 9CH[7:0].
The source start offset $\mathrm{XO}(11: 0)$ and $\mathrm{YO}(11: 0)$ opens the acquisition window, and the target size (XD11 to XD0, YD11 to YD0) closes the window, however the window is cut vertically if there are less output lines than required. The trigger events for the pixel and line counts are the horizontal and vertical reference edges as defined in subaddress 92 H .

The task handling is controlled by subaddress 90 H ; see Section 9.3.1.2.

### 9.3.1.1 Input field processing

The trigger event for the field sequence detection from external signals (X port) are defined in subaddress 92 H . The state of the scalers horizontal reference signal at the time of the vertical reference edge is taken from the $X$ port as field sequence identifier (FID). For example, if the falling edge of the XRV input signal is the reference and the state of XRH input is logic 0 at that time, the detected field ID is logic 0 .
The bits XFDV[92H[7]] and XFDH[92H[6]] define the detection event and state of the flag from the $X$ port. For the default setting of XFDV and XFDH at ' 00 ' is taken from the state of the horizontal input at the falling edge of the vertical input.
The scaler gets corresponding field ID information directly from the SAA7108E; SAA7109E decoder path.

The FID flag is used to determine whether the first or second field of a frame is going to be processed within the scaler, and it is also used as trigger conditions for the task handling (see bits STRC[1:0] 90H[1:0]).

According to ITU 656, FID at logic 0 means first field of a frame. To ease the application, the polarities of the detection results on the X port signals and the internal decoder ID can be changed via XFDH.

As the V sync from the decoder path has a half line timing (due to the interlaced video signal), but the scaler processing only recognises full lines, during 1st fields from the decoder the line count of the scaler can possibly shift by one line, compared to the 2nd field. This can be compensated for by switching the vertical trigger event, as defined by XDV0, to the opposite V sync edge or by using the vertical scalers phase offsets. The vertical timing of the decoder can be seen in Figs 29 and 30.

As the horizontal and vertical reference events inside the ITU 656 data stream (from X port) and the real-time reference signals from the decoder path are processed differently, the trigger events for the input acquisition also have to be programmed differently.

Table 38 Processing trigger and start

| $\begin{aligned} & \text { XDV1 } \\ & 92 H[5] \end{aligned}$ | $\begin{gathered} \text { XDVO } \\ 92 H[4] \end{gathered}$ | $\begin{gathered} \text { XDH } \\ 92 \mathrm{H}[2] \end{gathered}$ | DESCRIPTION |
| :---: | :---: | :---: | :---: |
|  |  |  | Internal decoder: The processing triggers at the falling edge of the V123 pulse (see Figs $29(50 \mathrm{~Hz})$ and $30(60 \mathrm{~Hz})$ ), and starts earliest with the rising edge of the decoder HREF at line number: |
| 0 | 1 | 0 | $4 / 7$ ( $50 / 60 \mathrm{~Hz}$, 1st field), respectively $3 / 6$ ( $50 / 60 \mathrm{~Hz}$, 2nd field) (decoder count) |
| 0 | 0 | 0 | $2 / 5$ ( $50 / 60 \mathrm{~Hz}$, 1st field), respectively $2 / 5$ ( $50 / 60 \mathrm{~Hz}$, 2nd field) (decoder count) |
| 0 | 0 | 0 | External ITU 656 stream: The processing starts earliest with SAV at line number 23 ( 50 Hz system), respectively line 20 ( 60 Hz system) (according ITU 656 count) |

### 9.3.1.2 Task handling

The task handler controls the switching between the two programming register sets. It is controlled by subaddresses 90 H and COH . A task is enabled via the global control bits TEA[80H[4]] and TEB[80H[5]]. The handler is then triggered by events which can be defined for each register set.

In the event of a programming error the task handling and the complete scaler can be reset to the initial states by the software reset bit SWRST[88H[5]] being set to logic 0 . A software reset must be done after programming especially if the programming registers, related acquisition window and scaler are reprogrammed while a task is active.

The difference in the disabling/enabling of a task, which is evaluated at the end of a running task (when SWRST is set to logic 0 ) is that it sets the internal state machines directly to their idle states.

The start condition for the handler is defined by bits STRC[1:0] 90H[1:0] and means: start immediately, wait for next $V$ sync, next FID at logic 0 or next FID at logic 1. The FID is evaluated if the vertical and horizontal offsets are reached.

With RPTSK[90H[2]] at logic 1 the actual running task is repeated (under the defined trigger conditions) before handing control over to the alternate task.

To support field rate reduction, the handler is also enabled to skip fields (bits FSKP[2:0] 90H[5:3]) before executing the task. A TOGGLE flag is generated (used for the correct output field processing), which changes state at the beginning of a task every time a task is activated; examples are given in Section 9.3.1.3.

## Remarks:

- To activate a task, the start condition must be fulfilled and the acquisition window offsets must be reached. For example, in case of 'start immediately', and two regions are defined for one field, the offset of the lower region must be greater than (offset + length) the upper region, if not, the actual counted H and V position at the end of the upper task is beyond the programmed offsets and the processing will 'wait for next V'.
- Basically, the trigger conditions are checked when a task is activated. It is important to know that they are not checked while a task is inactive. So it is not possible to trigger to the next logic 0 or logic 1 with overlapping offset and active video ranges between the tasks (e.g. task A STRC[2:0] = 2, YO[11:0] = 310 and task B STRC[2:0] = 3, YO[11:0] = 310 results in an output field rate of $50 / 3 \mathrm{~Hz}$ ).
- After power-on or software reset (via SWRST[88H[5]]) task B gets priority over task A.


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### 9.3.1.3 Output field processing

As a reference for the output field processing, two signals are available for the back-end hardware.

These signals are the input field ID from the scaler source and a TOGGLE flag, which shows that an active task is used an odd ( $1,3,5 \ldots$ ) or even ( $2,4,6 \ldots$...) number of times. Using a single or both tasks and reducing the field or frame rate with the task handling functionality, the TOGGLE information can be used to reconstruct an interlaced scaled picture at a reduced frame rate. The TOGGLE flag is not synchronized to the input field detection, as it is only dependent on the interpretation of this information by the external hardware i.e. whether the output of the scaler is processed correctly; see Section 9.3.3.

When OFIDC $=0$, the scalers input field ID is available as output field ID on bit D6 of SAV and EAV, and respectively on pin IGP0 (IGP1), if the FID output is selected.

When OFIDC[90H[6]] = 1 , the TOGGLE information is available as output field ID on bit D6 of SAV and EAV, and respectively on pin IGP0 (IGP1) if the FID output is selected.

Additionally bit D7 of SAV and EAV can be defined via CONLH[90H[7]]. When CONLH[90H[7]] = 0 (default) it sets bit $D 7$ to logic 1; a logic 1 inverts the SAV/EAV bit D7. So it is possible to mark the output of both tasks by different SAV/EAV codes. This bit can also be seen as 'task flag' on the pins IGP0 (IGP1), if the TASK output is selected.
Table 39 Example for field processing

| SUBJECT | FIELD SEQUENCE FRAME/FIELD |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | EXAMPLE 1 ${ }^{(1)}$ |  |  | EXAMPLE $\mathbf{2}^{(2)(3)}$ |  |  |  | EXAMPLE $3^{(2)(4)(5)}$ |  |  |  |  |  | EXAMPLE $\mathbf{4}^{(2)(4)(6)}$ |  |  |  |  |  |
|  | 1/1 | 1/2 | 2/1 | 1/1 | 1/2 | 2/1 | 2/2 | 1/1 | 1/2 | 2/1 | 2/2 | 3/1 | 3/2 | 1/1 | 1/2 | 2/1 | 2/2 | 3/1 | 3/2 |
| Processed by task | A | A | A | B | A | B | A | B | B | A | B | B | A | B | B | A | B | B | A |
| State of detected ITU 656 FID | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| TOGGLE flag | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | $0{ }^{(7)}$ | 1 | 1 | $1^{(7)}$ | 0 | 0 |
| Bit D6 of SAV/EAV byte | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | $0{ }^{(7)}$ | 1 | 1 | $1{ }^{(7)}$ | 0 | 0 |
| Required sequence conversion at the vertical scaler ${ }^{(8)}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \mathrm{LO} \\ \downarrow \\ \mathrm{LO} \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \mathrm{LO} \\ \downarrow \\ \mathrm{LO} \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \mathrm{LO} \\ \downarrow \\ \mathrm{LO} \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { LO } \end{gathered}$ | $\begin{gathered} \mathrm{LO} \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { LO } \end{gathered}$ | $\begin{gathered} \text { LO } \\ \downarrow \\ \text { LO } \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \mathrm{LO} \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \text { LO } \\ \downarrow \\ \text { LO } \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { LO } \end{gathered}$ | $\begin{gathered} \text { LO } \\ \downarrow \\ \text { LO } \end{gathered}$ | $\begin{gathered} \text { UP } \\ \downarrow \\ \text { UP } \end{gathered}$ | $\begin{gathered} \text { LO } \\ \downarrow \\ \text { UP } \end{gathered}$ |
| Output ${ }^{(9)}$ | 0 | 0 | O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | O | 0 | NO | 0 | 0 | NO | 0 | 0 |

## Notes

1. Single task every field; OFIDC $=0$; subaddress 90 H at 40 H ; TEB[80H[5]] $=0$.
2. Tasks are used to scale to different output windows, priority on task $B$ after SWRST.
3. Both tasks at $1 / 2$ frame rate; OFIDC $=0$; subaddresses 90 H at 43 H and COH at 42 H .
4. In examples 3 and 4 the association between input FID and tasks can be flipped, dependent on which time the SWRST is de-asserted. 5. Task $B$ at $2 / 3$ frame rate constructed from neighbouring motion phases; task $A$ at $1 / 3$ frame rate of equidistant motion phases; OFIDC $=1$; subaddresses 90 H at 41 H and COH at 45 H .
5. Task $A$ and $B$ at $1 / 3$ frame rate of equidistant motion phases; OFIDC $=1$; subaddresses 90 H at 41 H and COH at 49 H . 7. State of prior field.
6. It is assumed that input/output FID $=0$ (upper lines); UP = upper lines; LO = lower lines. 9. $\mathrm{O}=$ data output; $\mathrm{NO}=$ no output.

### 9.3.2 HORIZONTAL SCALING

The overall horizontal scaling factor has to be split into a binary and a rational value according to the following
equation: H scale ratio $=\frac{\text { output pixel }}{\text { input pixel }}$
$H$ scale ratio $=\frac{1}{X P S C[5: 0]} \times \frac{1024}{\operatorname{XSCY}[12: 0]}$
where, the parameter of the prescaler XPSC[5:0] $=1$ to 63 and the parameter of VPD phase interpolation XSCY[12:0] = 300 to 8191 ( 0 to 299 are only theoretical values). For example, $1 / 3.5$ is split into $1 / 4 \times 1.14286$. The binary factor is processed by the prescaler, the arbitrary non-integer ratio is achieved via the variable phase delay VPD circuitry, called horizontal fine scaling. The latter calculates horizontally interpolated new samples with a 6 -bit phase accuracy, which relates to less than 1 ns jitter for regular sampling schemes. Together the prescaler and fine scaler form the horizontal scaler of the SAA7108E; SAA7109E.

Using the accumulation length function of the prescaler (XACL[5:0] A1H[5:0]), application and destination dependent (e.g. scale for display or for a compression machine), a compromise between visible bandwidth and alias suppression can be found.

### 9.3.2.1 Horizontal prescaler (subaddresses AOH to A7H and DOH to D7H)

The prescaling function consists of an FIR anti-alias filter stage and an integer prescaler, which together form an adaptive prescale dependent low-pass filter to balance the sharpness and aliasing effects.

The FIR pre-filter stage implements different low-pass characteristics to reduce the anti-alias for downscales in the range of 1 to $1 / 2$. A CIF optimized filter is built-in, which reduces artefacts for CIF output formats (to be used in combination with the prescaler set to $1 / 2$ scale); see Table 40.

The function of the prescaler is defined by:

- An integer prescaling ratio XPSC[5:0] AOH[5:0] (equals 1 to 63), which covers the integer downscale range 1 to $1 / 63$
- An averaging sequence length $\operatorname{XACL[5:0]~} \mathrm{A} 1 \mathrm{H}[5: 0]$ (equals 0 to 63); range 1 to 64
- A DC gain renormalization XDCG[2:0] A2H[2:0]; 1 down to $1 / 128$ )
- The bit XC2_1[A2H[3]], which defines the weighting of the incoming pixels during the averaging process
- XC2_1 = $0 \Rightarrow 1+1 \ldots+1+1$
- XC2_1 = $1 \Rightarrow 1+2 \ldots+2+1$

The prescaler creates a prescale dependent FIR low-pass, with up to $64+7$ filter taps. The parameter XACL[5:0] can be used to vary the low-pass characteristic for a given integer prescale of $1 / \mathrm{XPSC}[5: 0]$. The user can therewith decide between signal bandwidth (sharpness impression) and alias.

The equation for the XPSC[5:0] calculation is:
XPSC[5:0] $=$ lower integer of $\frac{\text { Npix_in }}{\text { Npix_out }}$
where,
the range is 1 to 63 (value $\mathbf{0}$ is not allowed);
Npix_in = number of input pixel, and
Npix_out = number of desired output pixel over the complete horizontal scaler.
The use of the prescaler results in a XACL[5:0] and XC2_1 dependent gain amplification. The amplification can be calculated according to the equation:

DC gain $=\left[\left(X A C L[5: 0]-X C 2 \_1\right)+1\right] \times\left(X C 2 \_1+1\right)$
It is recommended to use sequence lengths and weights, which results in a $2^{\mathrm{N}} \mathrm{DC}$ gain amplification, as these amplitudes can be renormalized by the XDCG[2:0] controlled $\frac{1}{2^{N}}$ shifter of the prescaler.

The renormalization range of XDCG[2:0] is $1,1 / 2 \ldots$ down to $1 / 128$.
Other amplifications have to be normalized by using the following BCS control circuitry. In these cases the prescaler has to be set to an overall gain $\leq 1$, e.g. for an accumulation sequence of ' $1+1+1$ ' (XACL[5:0] $=2$ and XC2_1 = 0), XDCG[2:0] must be set to '010', which equals $1 / 4$ and the BCS has to amplify the signal to $4 / 3$ (SATN[7:0] and CONT[7:0] value $=$ lower integer of $4 / 3 \times 64)$.

## The use of XACL[5:0] is XPSC[5:0] dependent. XACL[5:0] must be $<2 \times$ XPSC[5:0].

XACL[5:0] can be used to find a compromise between bandwidth (sharpness) and alias effects.

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Remark: Due to bandwidth considerations XPSC[5:0] and XACL[5:0] can be chosen differently to the previously mentioned equations or Table 41, as the horizontal phase scaling is able to scale in the range from zooming up by factor 3 to downscaling by a factor of 1024/8191.
Figs 34 and 35 show some frequency characteristics of the prescaler.

Table 41 shows the recommended prescaler programming. Other programming, than given in Table 41, may result in better alias suppression, but the resulting DC gain amplification needs to be compensated by the BCS control, according to the equation:
CONT[7:0] $=$ SATN[7:0] $=$ lower integer of $\frac{2^{\mathrm{XDCG}[2: 0]}}{\text { DC gain } \times 64}$
Where:

$$
\begin{aligned}
& 2^{X D C G[2: 0]} \geq \text { DC gain } \\
& \text { DC gain }=\left(X C 2 \_1+1\right) \times \text { XACL[5:0] }+\left(1-X C 2 \_1\right) .
\end{aligned}
$$

For example, if $\mathrm{XACL}[5: 0]=5, \mathrm{XC2} 21=1$, then DC gain $=10$ and the required $\operatorname{XDCG}[2: 0]=4$.

The horizontal source acquisition timing and the prescaling ratio is identical for both the luminance and chrominance path, but the FIR filter settings can be defined differently in the two channels.

Fade-in and fade-out of the filters is achieved by copying an original source sample each as first and last pixel after prescaling.
Figs 32 and 33 show the frequency characteristics of the selectable FIR filters.

Table 40 FIR prefilter functions

| PFUV[1:0] A2H[7:6] <br> PFY[1:0] A2H[5:4] | LUMINANCE FILTER <br> COEFFICIENTS | CHROMINANCE COEFFICIENTS |
| :---: | :---: | :---: |
| 00 | bypassed | bypassed |
| 01 | 121 | 121 |
| 10 | $-111.754 .51 .751-1$ | 381083 |
| 11 | 12221 | 12221 |

(1) $\operatorname{PFY}[1: 0]=01$.
(2) $\operatorname{PFY}[1: 0]=10$.
(3) $\operatorname{PFY}[1: 0]=11$.


Fig. 32 Luminance prefilter characteristic.
(1) PFUV[1:0] $=01$.
(2) $\operatorname{PFUV}[1: 0]=10$.
(3) $\operatorname{PFUV}[1: 0]=11$.


Fig. 33 Chrominance prefilter characteristic.


Fig. 34 Examples for prescaler filter characteristics: effect of increasing XACL[5:0].
(1) XC2_1 $=0$ and $X A C L[5: 0]=1$.
(2) $X C 2 \_1=1$ and $X A C L[5: 0]=2$.
(3) XC2_1 = 0 and $X A C L[5: 0]=3$.
(4) XC2_1 = 1 and XACL[5:0] $=4$.
(5) XC2_1 = 0 and XACL[5:0] $=7$.
(6) XC2_1 = 1 and XACL[5:0] = 8 .


Fig. 35 Examples for prescaler filter characteristics: setting XC2_1 =1.

Table 41 Example of XACL[5:0] usage

| PRESCALE RATIO | $\begin{gathered} \text { XPSC } \\ \text { [5:0] } \end{gathered}$ | RECOMMENDED VALUES |  |  |  |  |  | FIR PREFILTER PFY[1:0]/ PFUV[1:0] |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | FOR LOWER BANDWIDTH REQUIREMENTS |  |  | FOR HIGHER BANDWIDTH REQUIREMENTS |  |  |  |
|  |  | XACL[5:0] | XC2_1 | XDCG[2:0] | XACL[5:0] | XC2_1 | XDCG[2:0] |  |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 to 2 |
| 1/2 | 2 | 2 | 1 | 2 | 1 | 0 | 1 | 0 to 2 |
|  |  | $(121) \times 1 / 4^{(1)}$ |  |  | $(11) \times 1 / 2^{(1)}$ |  |  |  |
| 1/3 | 3 | 4 | 1 | 3 | 3 | 0 | 2 | 2 |
|  |  | $(12221) \times 1 / 8^{(1)}$ |  |  | $(1111) \times 1 / 4^{(1)}$ |  |  |  |
| 1/4 | 4 | 7 | 0 | 3 | 4 | 1 | 3 | 2 |
|  |  | $(11111111) \times 1 / 8^{(1)}$ |  |  | $(12221) \times 1 / 8^{(1)}$ |  |  |  |
| 1/5 | 5 | 8 | 1 | 4 | 7 | 0 | 3 | 2 |
|  |  | (1222222 1) $\times 1 / 16^{(1)}$ |  |  | $(11111111) \times 1 / 8^{(1)}$ |  |  |  |
| 1/6 | 6 | 8 | 1 | 4 | 7 | 0 | 3 | 3 |
|  |  | (1222222 1) $\times 1 / 16^{(1)}$ |  |  | $(11111111) \times 1 / 8^{(1)}$ |  |  |  |
| $1 / 7$ | 7 | 8 | 1 | 4 | 7 | 0 | 3 | 3 |
|  |  | $(12222221) \times 1 / 16^{(1)}$ |  |  | $(11111111) \times 1 / 8^{(1)}$ |  |  |  |
| 1/8 | 8 | 15 | 0 | 4 | 8 | 1 | 4 | 3 |
|  |  | $(1111111111111111) \times 1 / 16^{(1)}$ |  |  | (12222222 1) $\times 1 / 16^{(1)}$ |  |  |  |
| 1/9 | 9 | 15 | 0 | 4 | 8 | 1 | 4 | 3 |
|  |  | $(1111111111111111) \times \frac{1 / 16^{(1)}}{}$ |  |  | (1222222 1) $\times 1 / 16^{(1)}$ |  |  |  |
| $1 / 10$ | 10 | 16 | 1 | 5 | 8 | 1 | 4 | 3 |
|  |  | (12222222222222221) $\times 1 / 32^{(1)}$ |  |  | (1222222 1) $\times 1 / 16^{(1)}$ |  |  |  |
| 1/13 | 13 | 16 | 1 | 5 | 16 | 1 | 5 | 3 |
| 1/15 | 15 | 31 | 0 | 5 | 16 | 1 | 5 | 3 |
| 1/16 | 16 | 31 | 0 | 5 | 16 | 1 | 5 | 3 |
| $1 / 19$ | 19 | 32 | 1 | 6 | 32 | 1 | 6 | 3 |
| 1/31 | 31 | 32 | 1 | 6 | 32 | 1 | 6 | 3 |
| $1 / 32$ | 32 | 63 | 1 | 7 | 32 | 1 | 6 | 3 |
| 1/35 | 35 | 63 | 1 | 7 | 63 | 1 | 7 | 3 |

## Note

1. Resulting FIR function.

### 9.3.2.2 Horizontal fine scaling (variable phase delay filter; subaddresses A8H to AFH and D8H to DFH)

The horizontal fine scaling (VPD) should operate at scaling ratios between $1 / 2$ and 2 ( 0.8 and 1.6), but can also be used for direct scaling in the range from $1 / 7.999$ to (theoretical) zoom 3.5 (restriction due to the internal data path architecture), without prescaler.

In combination with the prescaler a compromise between sharpness impression and alias can be found, which is signal source and application dependent.

For the luminance channel a filter structure with 10 taps is implemented, for the chrominance a filter with 4 taps.

Luminance and chrominance scale increments
(XSCY[12:0] A9H[4:0] A8H[7:0] and XSCC[12:0] ADH[4:0] ACH[7:0]) are defined independently, but must be set in a $2: 1$ relationship in the actual data path implementation. The phase offsets XPHY[7:0] AAH[7:0] and XPHC[7:0]
AEH[7:0] can be used to shift the sample phases slightly. XPHY[7:0] and XPHC[7:0] covers the phase offset range 7.999 T to $1 / 32 \mathrm{~T}$. The phase offsets should also be programmed in a 2 : 1 ratio.

The underlying phase controlling DTO has a 13-bit resolution

According to the equations
XSCY[12:0] $=1024 \times \frac{\text { Npix_in }}{\text { XPSC[5:0] }} \times \frac{1}{\text { Npix_out }}$ and
$\operatorname{XSCC}[12: 0]=\frac{\mathrm{XSCY}[12: 0]}{2}$
The VPD covers the scale range from 0.125 to zoom 3.5. The VPD acts equivalent to a polyphase filter with 64 possible phases. In combination with the prescaler, it is possible to get high accurate samples from a highly anti-aliased integer downscaled input picture.

### 9.3.3 Vertical scaling

The vertical scaler of the SAA7108E; SAA7109E decoder part consists of a line FIFO buffer for line repetition and the vertical scaler block, which implements the vertical scaling on the input data stream in 2 different operational modes from theoretical zoom by 64 down to icon size $1 / 64$. The vertical scaler is located between the BCS and horizontal fine scaler, so that the BCS can be used to compensate for the DC gain amplification of the ACM mode (see
Section 9.3.3.2) as the internal RAMs are only 8 -bit wide.

### 9.3.3.1 Line FIFO buffer (subaddresses 91H, B4H and C1H, E4H)

The line FIFO buffer is a dual ported RAM structure for 768 pixels, with asynchronous write and read access. The line buffer can be used for various functions, but not all functions may be available simultaneously.

The line buffer can buffer a complete unscaled active video line or more than one shorter lines (only for non-mirror mode), for selective repetition for vertical zoom-up.

For zooming up from 240 lines to 288 lines e.g., every fourth line is requested (read) twice from the vertical scaling circuitry for calculation.

For conversion of a $4: 2: 0$ or $4: 1: 0$ input sampling scheme (MPEG, video phone, Indeo YUV-9) to ITU like sampling scheme $4: 2: 2$, the chrominance line buffer is read twice or four times, before being refilled again by the source. By means of the input acquisition window definition it has to be preserved, that the processing starts with a line containing luminance and chrominance information for $4: 2: 0$ and $4: 1: 0$ input. The bits FSC[2:1] 91H[2:1] define the distance between the Y/C lines. In case of $4: 2: 2$ and $4: 1: 1$ FSC2 and FSC1 have to be set to ' 00 '.

The line buffer can also be used for mirroring, i.e. for flipping the image left to right, for the vanity picture in video phone application (bit YMIR[B4H[4]]). In mirror mode only one active prescaled line can be held in the FIFO at a time.
The line buffer can be utilized as excessive pipeline buffer for discontinuous and variable rate transfer conditions at the expansion port or image port.

### 9.3.3.2 Vertical scaler (subaddresses BOH to BFH and $E O H$ to $E F H$ )

Vertical scaling of any ratio from 64 (theoretical zoom) to $1 / 63$ (icon) can be applied.

The vertical scaling block consists of another line delay, and the vertical filter structure, that can operate in two different modes. These are the Linear Phase Interpolation (LPI) and Accumulation (ACM) modes, controlled by YMODE[B4H[0]].

- LPI mode: In the linear phase interpolation mode (YMODE $=0$ ) two neighbouring lines of the source video stream are added together, but weighted by factors corresponding to the vertical position (phase) of the target output line relative to the source lines. This linear interpolation has a 6-bit phase resolution, which equals 64 intra line phases. It interpolates between two consecutive input lines only. The LPI mode should be applied for scaling ratios around 1 (down to $1 / 2$ ), it must be applied for vertical zooming.
- ACM mode: The vertical Accumulation (ACM) mode (YMODE =1) represents a vertical averaging window over multiple lines, sliding over the field. This mode also generates phase correct output lines. The averaging window length corresponds to the scaling ratio, resulting in an adaptive vertical low-pass effect, to greatly reduce aliasing artefacts. ACM can be applied for downscales only from ratio 1 down to $1 / 64$. ACM results in a scale dependent DC gain amplification, which has to be precorrected by the BCS control of the scaler part.

The phase and scale controlling DTO calculates in 16-bit resolution, controlled by parameters YSCY[15:0] B1H[7:0] $\mathrm{BOH}[7: 0]$ and YSCC[15:0] B3H[7:0] B2H[7:0], continuously over the entire filed. A start offset can be applied to the phase processing by means of the parameters YPY3[7:0] to YPY0[7:0] in BFH[7:0] to BCH[7:0] and YPC3[7:0] to YPC0[7:0] in BBH[7:0] to B8H[7:0]. The start phase covers the range of $255 / 32$ to $1 / 32$ lines offset.
By programming appropriate, opposite, vertical start phase values (subaddresses B8H to BFH and E8H to EFH) depending on odd/even field ID of the source video stream and $A / B$ page cycle, frame ID conversion and field rate conversion are supported (i.e. de-interlacing, re-interlacing).

Figs 36 and 37 and Tables 42 and 43 describe the use of the offsets.

## Remark: The vertical start phase, as well as the scaling ratio are defined independently for luminance and chrominance channels, but must be set to the same values in the actual implementation for accurate 4:2:2 output processing.

The vertical processing communicates on its input side with the line FIFO buffer. The scale related equations are:

- Scaling increment calculation for ACM and LPI mode, downscale and zoom: YSCY[15:0] and YSCC[15:0]
$=$ lower integer of $\left(1024 \times \frac{\text { Nline_in }}{\text { Nline_out }}\right)$
- BCS value to compensate DC gain in ACM mode (contrast and saturation have to be set): CONT[7:0] A5H[7:0] respectively SATN[7:0] A6H[7:0]
$=$ lower integer of $\left(\frac{\text { Nline_out }}{\text { Nline_in }} \times 64\right)$, or
$=$ lower integer of $\left(\frac{1024}{\mathrm{YSCY}[15: 0]} \times 64\right)$


### 9.3.3.3 Use of the vertical phase offsets

As shown in Section 9.3.1.3, the scaler processing may run randomly over the interlaced input sequence. Additionally the interpretation and timing between ITU 656 field ID and real-time detection by means of the state of $H$ sync at the falling edge of $V$ sync may result in different field ID interpretation.
A vertically scaled interlaced output also gets a larger vertical sampling phase error, if the interlaced input fields are processed, without regard to the actual scale at the starting point of operation (see Fig.36).
The four events to be considered are illustrated in Fig.37.
In Tables 42 and 43 PHO is a usable common phase offset.
It should be noted that the equations in Fig. 37 also produce an interpolated output for the unscaled case, as the geometrical reference position for all conversions is the position of the first line of the lower field (see Table 42).
If there is no need for UP-LO and LO-UP conversion and the input field ID is the reference for the back-end operation, then it is UP-LO = UP-UP and LO-UP $=$ LO-LO and the $1 / 2$ line phase shift $(\mathrm{PHO}+16)$ that can be skipped; this case is given in Table 43.
The SAA7108E; SAA7109E supports 4 phase offset registers per task and component (luminance and chrominance). The value of 20 H represents a phase shift of one line.
The registers are assigned to the following events; e.g. subaddresses B8H to BBH:

- B8H: 00 = input field ID 0 , task status bit 0 (toggle status, see Section 9.3.1.3)
- B9H: 01 = input field ID 0 , task status bit 1
- BAH: 10 = input field ID 1, task status bit 0
- BBH: 11 = input field ID 1, task status bit 1.


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Depending on the input signal (interlaced or non-interlaced) and the task processing ( 50 Hz or field reduced processing with one or two tasks, see examples in Section 9.3.1.3), other combinations may also be possible, but the basic equations are the same.



Table 42 Examples for vertical phase offset usage: global equations

| INPUT FIELD UNDER <br> PROCESSING | OUTPUT FIELD <br> INTERPRETED AS | USED ABBREVIATION | EQUATION FOR PHASE OFFSET <br> CALCULATION (DECIMAL VALUES) |
| :--- | :--- | :--- | :--- |
| Upper input lines | upper output lines | UP-UP | PHO +16 |
| Upper input lines | lower output lines | UP-LO | PHO $+\frac{\text { YSCY[15:0] }}{64}+16$ |
| Lower input lines | upper output lines | LO-UP | PHO |
| Lower input lines | lower output lines | LO-LO | PHO $+\frac{\mathrm{YSCY[15:0]}}{64}$ |

Table 43 Vertical phase offset usage; assignment of the phase offsets

| DETECTED INPUT FIELD ID | TASK STATUS BIT | VERTICAL PHASE OFFSET | CASE | EQUATION TO BE USED |
| :---: | :---: | :---: | :---: | :---: |
| 0 = upper lines | 0 | $\begin{aligned} & \text { YPY0[7:0] and } \\ & \text { YPC0[7:0] } \end{aligned}$ | case $1^{(1)}$ | UP-UP (PHO) |
|  |  |  | case $2^{(2)}$ | UP-UP |
|  |  |  | case $3^{(3)}$ | UP-LO |
| 0 = upper lines | 1 | $\begin{aligned} & \text { YPY1[7:0] and } \\ & \text { YPC1[7:0] } \end{aligned}$ | case 1 | UP-UP (PHO) |
|  |  |  | case 2 | UP-LO |
|  |  |  | case 3 | UP-UP |
| 1 = lower lines | 0 | $\begin{aligned} & \text { YPY2[7:0] and } \\ & \text { YPC2[7:0] } \end{aligned}$ | case 1 | LO-LO (PHO + YSCY[15:0] $64-16)$ |
|  |  |  | case 2 | LO-UP |
|  |  |  | case 3 | LO-LO |
| 1 = lower lines | 1 | YPY3[7:0] and YPC3[7:0] | case 1 | LO-LO (PHO + YSCY[15:0] $64-16)$ |
|  |  |  | case 2 | LO-LO |
|  |  |  | case 3 | LO-UP |

## Notes

1. Case 1: OFIDC[90H[6]] $=0$; scaler input field ID as output ID; back-end interprets output field ID at logic 0 as upper output lines.
2. Case 2: OFIDC[90H[6]] = 1; task status bit as output ID; back-end interprets output field ID at logic 0 as upper output lines.
3. Case 3: OFIDC[90H[6]] = 1; task status bit as output ID; back-end interprets output field ID at logic 1 as upper output lines.

### 9.4 VBI-data decoder and capture (subaddresses 40H to 7FH)

The SAA7108E; SAA7109E contains a versatile VBI data decoder.

The implementation and programming model accords to the VBI data slicer the built-in multimedia video data acquisition circuit of the SAA5284.

The circuitry recovers the actual clock phase during the clock run-in period, slices the data bits with the selected data rate, and groups them into bytes. The result is buffered into a dedicated VBI data FIFO with a capacity of $2 \times 56$ bytes ( $2 \times 14$ Dwords). The clock frequency, signal source, field frequency and accepted error count must be defined in subaddress 40 H .

The VBI data standards that are supported are given in Table 44.

For lines 2 to 24 of a field, per VBI line, 1 of 16 standards can be selected (LCRxxx[41:57[7:0]]: $23 \times 2 \times 4$-bit programming bits). The definition for line 24 is valid for the rest of the corresponding field, normally no text data (video data) should be selected there (LCR24 = FFH) to stop the activity of the VBI data slicer during active video.

To adjust the slicers processing to the input signal source, there are offsets in the horizontal and vertical direction available (parameters HOFF[5B,59[2:0,7:0]], VOFF[5B,5A[4,7:0]] and FOFF[5B[7]]).
In difference to the scalers counting, the slicers offsets define the position of the horizontal and vertical trigger events related to the processed video field. The trigger events are the falling edge of HREF and the falling edge of V123 from the decoder processing part.

The relationship of these programming values to the input signal and the recommended values can be seen in Tables 34 to 37.

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Table 44 Data types supported by the data slicer block

| DATA TYPE <br> NUMBER | STANDARD TYPE | DATA RATE <br> (Mbits/s) | FRAMING CODE | FC <br> WINDOW | HAM <br> CHECK |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0000 | teletext EuroWST, CCST | 6.9375 | 27 H | WST625 | always |
| 0001 | European Closed Caption | 0.500 | 001 | CC625 |  |
| 0010 | VPS | 5 | 9951 H | VPS |  |
| 0011 | wide screen signalling bits | 5 | 1E3C1FH | WSS |  |
| 0100 | US teletext (WST) | 5.7272 | 27 H | WST525 | always |
| 0101 | US Closed Caption (line 21) | 0.503 | 001 | CC525 |  |
| 0110 | (video data selected) | 5 | none | disable |  |
| 0111 | (raw data selected) | 5 | none | disable |  |
| 1000 | teletext | 6.9375 | programmable | general text | optional |
| 1001 | VITC/EBU time codes (Europe) | 1.8125 | programmable | VITC625 |  |
| 1010 | VITC/SMPTE time codes (USA) | 1.7898 | programmable | VITC525 |  |
| 1011 |  | 5 | programmable | open |  |
| 1100 | US NABTS | 5.7272 | programmable | NABTS | optional |
| 1101 | MOJI (Japanese) | 5.7272 | programmable (A7H) | Japtext |  |
| 1110 | Japanese format switch (L20/22) | 5 | programmable | open |  |
| 1111 | no sliced data transmitted <br> (video data selected) | 5 | none | disable |  |

### 9.5 Image port output formatter (subaddresses 84 H to 87 H )

The output interface consists of a FIFO for video and for sliced text data, an arbitration circuit, which controls the mixed transfer of video and sliced text data over the I port, and a decoding and multiplexing unit, which generates the 8 or 16-bit wide output data stream together with the accompanying reference and help information.

The clock for the output interface can be derived from an internal clock, decoder, expansion port or an externally provided clock which is appropriate, for example, for the VGA and frame buffer. The clock can be up to 33 MHz . The scaler provides the following video related timing reference events (signals), which are available on pins as defined by subaddresses 84 H and 85 H :

- Output field ID
- Start and end of vertical active video range
- Start and end of active video line
- Data qualifier or gated clock
- Actually activated programming page (if CONLH is used)
- Threshold controlled FIFO filling flags (empty, full, filled)
- Sliced data marker.

The disconnected data stream at the scaler output is accompanied by a data valid flag (or data qualifier), or is transported via a gated clock. Clock cycles with invalid data on the I port data bus (including the HPD pins in 16-bit output mode) are marked with code 00 H .

The output interface also arbitrates the transfer between scaled video data and sliced text data over the I port output.

The bits VITX1 and VITX0 (subaddress 86 H ) are used to control the arbitration.

The serialization of the internal 32-bit Dwords to 8-bit or 16-bit output (optional), as well as the insertion of the extended ITU 656 codes (SAV/EAV for video data, ANC or SAV/EAV codes for sliced text data) are also done here.

For handshaking with the VGA controller, or other memory or bus interface circuitry, programmable FIFO flags are provided; see Section 9.5.2.

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### 9.5.1 SCALER OUTPUT FORMATTER

(SUBADDRESSES 93H and C3H)
The output formatter organizes the packing into the output FIFO. The following formats are available:
Y-C $C_{B}-C_{R} 4: 2: 2, Y-C_{B}-C_{R} 4: 1: 1, Y-C_{B}-C_{R} 4: 2: 0$, $Y-C_{B}-C_{R} 4: 1: 0, Y$ only (e.g. for raw samples). The formatting is controlled by FSI[2:0] 93H[2:0], FOI[1:0] 93H[4:3] and FYSK[93H[5]].

The data formats are defined on Dwords, or multiples thereof, and are similar to the video formats as recommended for PCI multimedia applications (see SAA7146A). Planar formats are not supported.

FSI[2:0] defines the horizontal packing of the data, FOI[1:0] defines how many $Y$ only lines are expected before a Y/C line will be formatted. If FYSK is set to logic 0 preceding Y only lines will be skipped, and the output will always start with a Y/C line.

Additionally the output formatter limits the amplitude range of the video data (controlled by ILLV[85H[5]]); see Table 47.

Table 45 Byte stream for different output formats

| OUTPUT FORMAT | BYTE SEQUENCE FOR 8-BIT OUTPUT MODES |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Y- $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : $2: 2$ | $\mathrm{C}_{\mathrm{B}} 0$ | Y0 | $\mathrm{C}_{\mathrm{R}} 0$ | Y1 | $\mathrm{C}_{\mathrm{B}} 2$ | Y2 | $\mathrm{C}_{\mathrm{R}} 2$ | Y3 | $\mathrm{C}_{\mathrm{B}} 4$ | Y4 | $\mathrm{C}_{\mathrm{R}} 4$ | Y5 | $\mathrm{C}_{\mathrm{B}} 6$ | Y6 |
| Y- $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 1: 1$ | $\mathrm{C}_{\mathrm{B}} 0$ | Y0 | $\mathrm{C}_{\mathrm{R}} 0$ | Y1 | $\mathrm{C}_{\mathrm{B}} 4$ | Y2 | $\mathrm{C}_{\mathrm{R}} 4$ | Y3 | Y4 | Y5 | Y6 | Y7 | $\mathrm{C}_{\mathrm{B}} 8$ | Y8 |
| Yonly | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 | Y9 | Y10 | Y11 | Y12 | Y13 |

Table 46 Explanation to Table 45

| NAME | EXPLANATION |
| :--- | :--- |
| $\mathrm{C}_{\mathrm{B}} \mathrm{n}$ | $\mathrm{C}_{\mathrm{B}}(\mathrm{B}-\mathrm{Y})$ colour difference component, pixel number $\mathrm{n}=0,2,4$ to 718 |
| Yn | Y (luminance) component, pixel number $\mathrm{n}=0,1,2,3$ to 719 |
| $\mathrm{C}_{\mathrm{R}} \mathrm{n}$ | $\mathrm{C}_{\mathrm{R}}(\mathrm{R}-\mathrm{Y})$ colour difference component, pixel number $\mathrm{n}=0,2,4$ to 718 |

Table 47 Limiting range on I port

| LIMIT STEP <br> ILLV[85H[5]] | VALID RANGE |  | SUPPRESSED CODES (HEXADECIMAL VALUE) |  |
| :---: | :---: | :---: | :---: | :---: |
|  | DECIMAL VALUE | HEXADECIMAL VALUE | LOWER RANGE | UPPER RANGE |
| 0 | 1 to 254 | 01 to FE | 00 | FF |
| 1 | 8 to 247 | 08 to F7 | 00 to 07 | F8 to FF |

### 9.5.2 VIDEO FIFO (SUBADDRESS 86H)

The video FIFO at the scaler output contains 32 Dwords. That corresponds to 64 pixels in 16-bit $Y-C_{B}-C_{R} 4: 2$ : 2 format. But as the entire scaler can act as a pipeline buffer, the actually available buffer capacity for the image port is much higher, and can exceed beyond a video line.

The image port and the video FIFO, can operate with the video source clock (synchronous mode) or with an externally provided clock (asynchronous, and burst mode), as appropriate for the VGA controller or attached frame buffer.

The video FIFO provides 4 internal flags, which report to what extent the FIFO is actually filled. These are:

- The FIFO Almost Empty (FAE) flag
- The FIFO combined flag (FCF) or FIFO filled, which is set at almost full level and reset, with hysteresis, only after the level crosses below the almost empty mark
- The FIFO Almost Full (FAF) flag
- The FIFO Overflow (FOVL) flag.

The trigger levels for FAE and FAF are programmable by FFL[1:0] 86H[3:2] (16, 24, 28, full) and FEL[1:0] 86H[1:0] (16, 8, 4, empty).

The state of this flag can be seen on pins IGP0 or IGP1. The pin mapping is defined by subaddresses 84 H and 85 H ; see Section 10.5.

### 9.5.3 TEXT FIFO

The data of the terminal VBI data slicer is collected in the text FIFO before transmission over the I port is requested (normally before the video window starts) and partitioned into two FIFO sections. A complete line is fed into the FIFO before a data transfer is requested. So normally, one line of text data is ready for transfer while the next text line is collected. Thus sliced text data is delivered as a block of qualified data, without any qualification gaps in the byte stream of the I port.

The decoded VBI data is collected in the dedicated VBI data FIFO. Once the capture of a line is completed, the FIFO can be streamed through the image port, preceded by a header, giving the line number and standard.

The VBI data period can be signalled via the sliced data flag on pin IGP0 or IGP1. The decoded VBI data is lead by the ITU ancillary data header (DID[5:0] 5DH[5:0] at value $<3 E H$ ) or by SAV/EAV codes selected by DID[5:0] at value 3EH or 3FH. IGP0 or IGP1 is set if the first byte of the ANC header is valid on the I port bus; it is reset if an SAV occurs. Therefore it may frame multiple lines of text data output, in case the video processing starts with a distance of several video lines to the region of text data. Valid sliced data from the text FIFO is available on the I port as long as the IGP0 or IGP1 flag is set and the data qualifier is active on pin IDQ.

The decoded VBI data is presented in two different data formats, controlled by bit RECODE.

RECODE $=1$ : values 00 H and FFH will be recoded to even parity values 03 H and FCH
RECODE $=0$ : values 00 H and FFH may occur in the data stream as detected.

### 9.5.4 VIDEO AND TEXT ARBITRATION (SUBADDRESS 86H)

Sliced text data and scaled video data are transferred over the same bus, the I port. The mixed transfer is controlled by an arbitration circuit. If the video data is transferred without any interrupt and the video FIFO does not need to buffer any output pixel, the text data is inserted after the end of a scaled video line, normally during the video blanking interval.

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### 9.5.5 DATA STREAM CODING AND REFERENCE SIGNAL GENERATION (SUBADDRESSES 84H, 85H AND 93H)

As horizontal and vertical reference signals are logic 1, active gate signals are generated, which frame the transfer of the valid output data. Alternatively, the horizontal and vertical trigger pulses can be generated on the rising edges of the gates.

Due to the dynamic FIFO behaviour of the complete scaler path, the output signal timing has no fixed timing relationship to the real-time input video stream. Thus fixed propagation delays, in terms of clock cycles, related to the analog input can not be defined.

The data stream is accompanied by a data qualifier.
Additionally invalid data cycles are marked with code 00H.

If ITU 656 like codes are not required, they can be suppressed in the output stream.

As a further option, it is possible to provide the scaler with an external gating signal on pin ITRDY. It is therefore possible to hold the data output for a certain time and to get valid output data in bursts of a guaranteed length.

The sketched reference signals and events can be mapped to the I port output pins IDQ, IGPH, IGPV, IGP0 and IGP1. The polarities of all the outputs can be modified to enable flexible use. The default polarity for the qualifier and reference signals is logic 1 (active).

Table 48 shows the relevant and supported SAV and EAV coding.

Table 48 SAV/EAV codes on the I port

| EVENT DESCRIPTION | SAV/EAV CODES ON I PORT ${ }^{(1)}$ (HEX) |  |  |  | COMMENT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MSB ${ }^{(2)}$ OF SAV/EAV BYTE $=0$ |  | MSB ${ }^{(2)}$ OF SAV/EAV BYTE $=1$ |  |  |
|  | FIELD ID = 0 | FIELD ID = 1 | FIELD ID = 0 | FIELD ID = 1 |  |
| Next pixel is FIRST pixel of any active line | 0E | 49 | 80 | C7 | HREF = active; <br> VREF = active |
| Previous pixel was LAST pixel of any active line, but not the last | 13 | 54 | 9D | DA | HREF = inactive; <br> VREF = active |
| Next pixel is FIRST pixel of any V-blanking line | 25 | 62 | AB | EC | $\begin{aligned} & \text { HREF = active; } \\ & \text { VREF = inactive } \end{aligned}$ |
| Previous pixel was LAST pixel of the last active line or of any V-blanking line | 38 | 7F | B6 | F1 | HREF = inactive; <br> VREF = inactive |
| No valid data, do not capture and do not increment pointer | 00 |  |  |  | IDQ pin inactive |

## Notes

1. The leading byte sequence is: $\mathrm{FFH}-00 \mathrm{H}-00 \mathrm{H}$.
2. The MSB of the SAV/EAV code byte is controlled by:
a) Scaler output data: task $A \Rightarrow M S B=\overline{\mathrm{CONLH}}[90 \mathrm{H}[7]]$; task $\mathrm{B} \Rightarrow \mathrm{MSB}=\overline{\mathrm{CONLH}}[\mathrm{COH}[7]]$.
b) VBI-data slicer output data: $\operatorname{DID}[5: 0] 5 D H[5: 0]=3 E H \Rightarrow M S B=1$; $\operatorname{DID}[5: 0] 5 D H[5: 0]=3 F H \Rightarrow M S B=0$.

Table 49 Explanation to Fig. 38

| NAME | EXPLANATION |
| :---: | :---: |
| SAV | start of active data; see Table 50 |
| SDID | sliced data identification: NEP(1), EP ${ }^{(2)}$, SDID5 to SDID0, freely programmable via ${ }^{2} \mathrm{C}$-bus subaddress 5 EH , D5 to D0, e. g. to be used as source identifier |
| DC | Dword count: NEP( ${ }^{(1)}$, EP ${ }^{(2)}$, DC5 to DC0. DC describes the number of succeeding 32-bit words: <br> - For SAV/EAV mode DC is fixed to 11 Dwords (byte value 4BH) <br> - For ANC mode it is: $D C=1 / 4(C+n)$, where $C=2$ (the two data identification bytes IDI1 and IDI2) and $n=$ number of decoded bytes according to the chosen text standard. <br> Note that the number of valid bytes inside the stream can be seen in the BC byte. |
| IDI1 | internal data identification 1: $\mathrm{OP}^{(3)}$, FID (field $1=0$, field $2=1$ ), LineNumber8 to LineNumber3 = Dword 1 byte 1; see Table 50 |
| IDI2 | internal data identification 2: $\mathrm{OP}^{(3)}$, LineNumber2 to LineNumber0, DataType3 to DataType0 = Dword 1 byte 2; see Table 50 |
| $\mathrm{D}_{\mathrm{n} \_} \mathrm{m}$ | Dword number $\mathbf{n}$, byte number $\mathbf{m}$ |
| $\mathrm{D}_{\text {DC_4 }}$ | last Dword byte 4, note: for SAV/EAV framing DC is fixed to 0BH, missing data bytes are filled up; the fill value is A0H |
| CS | the check sum byte, the check sum is accumulated from the SAV (respectively DID) byte to the $\mathrm{D}_{\text {DC_4 }}$ byte |
| BC | number of valid sliced bytes counted from the IDI1 byte |
| EAV | end of active data; see Table 50 |

Notes

1. Inverted EP (bit 7); for EP see note 2.
2. Even parity (bit 6 ) of bits 5 to 0 .
3. Odd parity (bit 7 ) of bits 6 to 0 .

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Table 50 Bytes stream of the data slicer

| NICK NAME | COMMENT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \text { DID, } \\ & \text { SAV, } \\ & \text { EAV } \end{aligned}$ | subaddress $5 \mathrm{DH}=00 \mathrm{H}$ | NEP ${ }^{(1)}$ | $E P^{(2)}$ | 0 | 1 | 0 | FID ${ }^{(3)}$ | $11^{(4)}$ | $10^{(4)}$ |
|  | subaddress 5DH; D5 = 1 | NEP | EP | 0 | D4[5DH] | D3[5DH] | D2[5DH] | D1[5DH] | D0[5DH] |
|  | subaddress 5DH D5 = 3EH; note 5 | 1 | FID ${ }^{(3)}$ | $\mathrm{V}^{(6)}$ | $\mathrm{H}^{(7)}$ | P3 | P2 | P1 | P0 |
|  | subaddress 5DH D5 $=3 \mathrm{FH}$; note 5 | 0 | FID ${ }^{(3)}$ | $V^{(6)}$ | $\mathrm{H}^{(7)}$ | P3 | P2 | P1 | P0 |
| SDID | programmable via subaddress 5EH | NEP | EP | D5[5EH] | D4[5EH] | D3[5EH] | D2[5EH] | D1[5EH] | D0[5EH] |
| DC ${ }^{(8)}$ |  | NEP | $E P^{(2)}$ | DC5 | DC4 | DC3 | DC2 | DC1 | DC0 |
| IDI1 |  | $\mathrm{OP}^{(9)}$ | FID ${ }^{(3)}$ | LN8 ${ }^{(10)}$ | LN7 ${ }^{(10)}$ | LN6 ${ }^{(10)}$ | LN5 ${ }^{(10)}$ | LN4 ${ }^{(10)}$ | LN3 ${ }^{(10)}$ |
| IDI2 |  | OP | LN2 ${ }^{(10)}$ | LN1 ${ }^{(10)}$ | LN0 ${ }^{(10)}$ | DT3 ${ }^{(11)}$ | DT2 ${ }^{(11)}$ | DT1 ${ }^{(11)}$ | DT0 ${ }^{(11)}$ |
| CS | check sum byte | $\overline{\mathrm{CS6}}$ | CS6 | CS5 | CS4 | CS3 | CS2 | CS1 | CS0 |
| BC | valid byte count | OP | 0 | CNT5 | CNT4 | CNT3 | CNT2 | CNT1 | CNT0 |

## Notes

1. NEP = inverted EP (see note 2).
2. $E P=$ Even Parity of bits 5 to 0 .
3. FID $=0$ : field 1 ; FID $=1$ : field 2 .
4. $I 1=0$ and $I 0=0$ : before line $1 ; I 1=0$ and $I 0=1$ : lines 1 to $23 ; I 1=1$ and $I 0=0$ : after line $23 ; I 1=1$ and $I 0=1$ : line 24 to end of field.
5. Subaddress 5DH at 3EH and 3FH are used for ITU 656 like SAV/EAV header generation; recommended value.
6. $\mathrm{V}=0$ : active video; $\mathrm{V}=1$ : blanking.
7. $H=0$ : start of line; $H=1$ : end of line.
8. $D C=$ Data Count in Dwords according to the data type.
9. $\mathrm{OP}=$ Odd Parity of bits 6 to 0 .
10. $\mathrm{LN}=$ Line Number.
11. $D T=$ Data Type according to table.

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### 9.6 Audio clock generation

 (subaddresses 30H to 3FH)The SAA7108E; SAA7109E incorporates the generation of a field-locked audio clock, as an auxiliary function for video capture. An audio sample clock, that is locked to the field frequency, ensures that there is always the same predefined number of audio samples associated with a field, or a set of fields. This ensures synchronous playback of audio and video after digital recording (e.g. capture to hard disk), MPEG or other compression or non-linear editing.

### 9.6.1 MASTER AUDIO CLOCK

The audio clock is synthesized from the same crystal frequency as the line-locked video clock is generated. The master audio clock is defined by the parameters:

- Audio master Clocks Per Field, ACPF[17:0] 32H[1:0] $31 \mathrm{H}[7: 0] 30 \mathrm{H}[7: 0]$ according to the equation:
$\operatorname{ACPF}[17: 0]=$ round $\left(\frac{\text { audio frequency }}{\text { field frequency }}\right)$
- Audio master Clocks Nominal Increment, ACNI[21:0] $36 \mathrm{H}[5: 0] 35 \mathrm{H}[7: 0] 34 \mathrm{H}[7: 0]$ according to the equation:
$\mathrm{ACNI}[21: 0]=$ round $\left(\frac{\text { audio frequency }}{\text { crystal frequency }} \times 2^{23}\right)$
See Table 51 for examples.
Remark: For standard applications the synthesized audio clock AMCLK can be used directly as master clock and as input clock for port AMXCLK (short cut) to generate ASCLK and ALRCLK. For high-end applications it is recommended to use an external analog PLL circuit to enhance the performance of the generated audio clock.

Table 51 Programming examples for audio master clock generation

| CRYSTAL FREQUENCY (MHz) | $\begin{aligned} & \text { FIELD } \\ & \text { (Hz) } \end{aligned}$ | ACPF |  | ACNI |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | DECIMAL | HEX | DECIMAL | HEX |
| AMCLK $=256 \times 48 \mathrm{kHz}$ (12.288 MHz) |  |  |  |  |  |
| 32.11 | 50 | 245760 | 3C000 | 3210190 | 30FBCE |
|  | 59.94 | 205005 | 320CD | 3210190 | 30FBCE |
| 24.576 | 50 | - | - | - | - |
|  | 59.94 | - | - | - | - |
| AMCLK $=256 \times \mathbf{4 4 . 1 ~ k H z ~ ( 1 1 . 2 8 9 6 ~ M H z ) ~}$ |  |  |  |  |  |
| 32.11 | 50 | 225792 | 37200 | 2949362 | 2D00F2 |
|  | 59.94 | 188348 | 2DFBC | 2949362 | 2D00F2 |
| 24.576 | 50 | 225792 | 37200 | 3853517 | 3ACCCD |
|  | 59.94 | 188348 | 2DFBC | 3853517 | 3ACCCD |
| AMCLK $=256 \times \mathbf{3 2 ~ k H z ~ ( 8 . 1 9 2 ~ M H z ) ~}$ |  |  |  |  |  |
| 32.11 | 50 | 163840 | 28000 | 2140127 | 20A7DF |
|  | 59.94 | 136670 | 215DE | 2140127 | 20A7DF |
| 24.576 | 50 | 163840 | 28000 | 2796203 | 2AAAAB |
|  | 59.94 | 136670 | 215DE | 2796203 | 2AAAAB |

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### 9.6.2 Signals ASCLK and ALRCLK

Two binary divided signals ASCLK and ALRCLK are provided for slower serial digital audio signal transmission and for channel-select. The frequencies of these signals are defined by the parameters:

- $\operatorname{SDIV[5:0]~38H[5:0]~according~to~the~equation:~} \mathrm{f}_{\text {ASCLK }}=\frac{\mathrm{f}_{\text {AMXCLK }}}{(\mathrm{SDIV}+1) \times 2} \Rightarrow$ SDIV[5:0] $=\frac{\mathrm{f}_{\text {AMXCLK }}}{2 f_{\text {ASCLK }}}-1$
- LRDIV[5:0] 39H[5:0] according to the equation: $\mathrm{f}_{\text {ALRCLK }}=\frac{\mathrm{f}_{\text {ASCLK }}}{\text { LRDIV } \times 2} \Rightarrow$ LRDIV[5:0] $=\frac{\mathrm{f}_{\text {ASCLK }}}{2 \mathrm{f}_{\text {ALRCLK }}}$

See Table 52 for examples.
Table 52 Programming examples for ASCLK/ALRCLK clock generation

| AMXCLK (MHz) | $\begin{aligned} & \text { ASCLK } \\ & \text { (kHz) } \end{aligned}$ | SDIV |  | $\begin{aligned} & \text { ALRCLK } \\ & \text { (kHz) } \end{aligned}$ | LRDIV |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | DECIMAL | HEX |  | DECIMAL | HEX |
| 12.288 | 1536 | 3 | 03 | 48 | 16 | 10 |
|  | 768 | 7 | 07 |  | 8 | 08 |
| 11.2896 | 1411.2 | 3 | 03 | 44.1 | 16 | 10 |
|  | 2822.4 | 1 | 01 |  | 32 | 10 |
| 8.192 | 1024 | 3 | 03 | 32 | 16 | 10 |
|  | 2048 | 1 | 01 |  | 32 | 10 |

### 9.6.3 OTHER CONTROL SIGNALS

Further control signals are available to define reference clock edges and vertical references; see Table 53
Table 53 Control signals

| CONTROL SIGNAL | DESCRIPTION |
| :---: | :---: |
| APLL[3AH[3]] | Audio PLL mode: |
|  | 0: PLL closed |
|  | 1: PLL open |
| AMVR[3AH[2]] | Audio Master clock Vertical Reference: |
|  | 0: internal vertical reference |
|  | 1: external vertical reference |
| LRPH[3AH[1]] | ALRCLK Phase: |
|  | 0: invert ASCLK, ALRCLK edges triggered by falling edge of ASCLK |
|  | 1: do not invert ASCLK, ALRCLK edges triggered by rising edge of ASCLK |
| SCPH[3AH[0]] | ASCLK Phase: |
|  | 0: invert AMXCLK, ASCLK edges triggered by falling edge of AMXCLK |
|  | 1: do not invert AMXCLK, ASCLK edges triggered by rising edge of AMXCLK |

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## 10 INPUT/OUTPUT INTERFACES AND PORTS OF DIGITAL VIDEO DECODER PART

The SAA7108E; SAA7109E has 5 different I/O interfaces. These are:

- Analog video input interface, for analog CVBS and/or Y and C input signals
- Audio clock port
- Digital real-time signal port (RT port)
- Digital video expansion port (X port), for unscaled digital video input and output
- Digital image port (I port) for scaled video data output and programming
- Digital host port (H port) for extension of the image port or expansion port from 8 to 16-bit.


### 10.1 Analog terminals

The SAA7108E; SAA7109E has 6 analog inputs Al21 to Al24, Al11 and Al12 (see Table 54) for composite video CVBS or S-video Y/C signal pairs. Additionally, there are two differential reference inputs, which must be connected to ground via a capacitor equivalent to the decoupling capacitors at the 6 inputs. There are no peripheral components required other than the decoupling capacitors and $18 \Omega / 56 \Omega$ termination resistors, one set per connected input signal (see also application example in Fig.52). Two anti-alias filters are integrated, and self adjusting via the clock frequency.

Clamp and gain control for the two ADCs are also integrated. An analog video output pin (AOUT) is provided for testing purposes.

Table 54 Analog pin description

| SYMBOL | PIN | I/O | DESCRIPTION | BIT |
| :--- | :--- | :--- | :--- | :--- |
| Al24 to AI21 | P6, P7, P9 <br> and P10 | I | analog video signal inputs, e.g. 2 CVBS signals and <br> two Y/C pairs can be connected simultaneously | MODE3 to MODE0 |
| Al12 and Al11 | P11 and P13 |  |  |  |
| AOUT | M10 | O | analog video output, for test purposes | AOSL1 and AOSL0 |
| Al1D and Al2D | P12 and P8 | I | analog reference pins for differential ADC operation | - |

### 10.2 Audio clock signals

The SAA7108E; SAA7109E also synchronizes the audio clock and sampling rate to the video frame rate, via a very slow PLL. This ensures that the multimedia capture and compression processes always gather the same predefined number of samples per video frame.
An audio master clock AMCLK and two divided clocks, ASCLK and ALRCLK, are generated; see Table 55.

- ASCLK: can be used as audio serial clock
- ALRCLK: audio left/right channel clock.

The ratios are programmable, see Section 9.6.
Table 55 Audio clock pin description

| SYMBOL | PIN | I/O | DESCRIPTION | BIT |
| :--- | :--- | :--- | :--- | :--- |
| AMCLK | K12 | O | audio master clock output | ACPF[17:0] 32H[1:0] 31H[7:0] 30H[7:0] <br> and ACNI[21:0] 36H[5:0] 35H[7:0] <br> $34 \mathrm{H}[7: 0]$ |
| AMXCLK | J12 | I | external audio master clock input for the clock <br> division circuit, can be directly connected to <br> output AMCLK for standard applications | - |
| ASCLK | K14 | O | serial audio clock output, can be synchronized to <br> rising or falling edge of AMXCLK | SDIV[5:0] 38H[5:0] and SCPH[3AH[0]] |
| ALRCLK | J13 | O | audio channel (left/right) clock output, can be <br> synchronized to rising or falling edge of ASCLK | LRDIV[5:0] 39H[5:0] and LRPH[3AH[1]] |

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### 10.3 Clock and real-time synchronization signals

A crystal accurate frequency reference is required for the generation of the line-locked video (pixel) clock LLC, and the frame-locked audio serial bit clock. An oscillator is built-in, for fundamental or 3rd-harmonic crystals. The supported crystal frequencies are 32.11 or 24.576 MHz (defined during reset by strapping pin ALRCLK).

Alternatively pins XTALId and XTALle can be driven from an external single-ended oscillator.

The crystal oscillation can be propagated as clock to other ICs in the system via pin XTOUTd.

The Line-Locked Clock (LLC) is the double pixel clock at a nominal 27 MHz . It is locked to the selected video input, generating baseband video pixels according to "ITU recommendation 601". In order to support interfacing circuits, a direct pixel clock LLC2 is also provided.

The pins for line and field timing reference signals are RTCO, RTS1 and RTS0. Various real-time status information can be selected for the RTS pins. The signals are always available (output) and reflect the synchronization operation of the decoder part in the SAA7108E; SAA7109E. The function of the RTS1 and RTS0 pins can be defined by bits RTSE1[3:0] 12H[7:4] and RTSE0[3:0] 12H[3:0]; see Table 56.

Table 56 Clock and real-time synchronization signals

| SYMBOL | PIN | I/O | DESCRIPTION | BIT |  |
| :--- | :---: | :---: | :--- | :--- | :--- |
| Crystal oscillator |  |  |  |  |  |
| XTALId | P2 | I | input for crystal oscillator, or reference clock | - |  |
| XTALOd | P3 | O | output of crystal oscillator | - |  |
| XTOUTd | P4 | O | reference (crystal) clock output drive (optional) | XTOUTE[14H[3]] |  |
| Real-time signals (RT port) | - |  |  |  |  |
| LLC | M14 | O | line-locked clock; nominal 27 MHz, double pixel clock locked to the <br> selected video input signal | - |  |
| LLC2 | L14 | O | line-locked pixel clock; nominal 13.5 MHz | - |  |
| RTCO | L13 | O | real-time control output; transfers real-time status information <br> supporting RTC level 3.1 (see external document "RTC Functional <br> Description", available on request) | - |  |
| RTS0 | K13 | O | real-time status information line 0; can be programmed to carry <br> various real-time informations; see Table 167 | RTSE0[3:0] 12H[3:0] |  |
| RTS1 | L10 | O | real-time status information line 1; can be programmed to carry <br> various real-time informations; see Table 168 | RTSE1[3:0] 12H[7:4] |  |

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### 10.4 Video expansion port (X port)

The expansion port is intended for transporting video streams of image data from other digital video circuits such as MPEG encoder/decoder and video phone codec, to the image port (I port); see Table 57.

The expansion port consists of two groups of signals/pins:

- 8-bit data, I/O, regular video components $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ $4: 2$ : 2, i.e. $C_{B}-Y-C_{R}-Y$, byte serial, exceptionally raw video samples (e.g. ADC test). In input mode the data bus can be extended to 16-bit by pins HPD7 to HPD0.
- Clock, synchronization and auxiliary signals, accompanying the data stream, I/O.

As output, these are direct copies of the decoder signals.
The data transfers through the expansion port represent a single D1 port, with half duplex mode. The SAV and EAV codes may be inserted optionally for data input (controlled by bit XCODE[92H[3]]). The input/output direction is switched for complete fields only.

Table 57 Signals dedicated to the expansion port

| SYMBOL | PIN | 1/0 | DESCRIPTION | BIT |
| :---: | :---: | :---: | :---: | :---: |
| XPD7 to XPDO | K2, K3, L1 to L3, M1, M2 and N1 | 1/O | X port data: in output mode controlled by decoder section, for data format see Table 58; in input mode $Y-C_{B}-C_{R} 4: 2: 2$ serial input data or luminance part of a 16 -bit $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$ input | OFTS[2:0] 13H[2:0], 91H[7:0] and C1H[7:0] |
| XCLK | M3 | 1/0 | clock at expansion port: if output, then copy of LLC; as input normally a double pixel clock of up to 32 MHz or a gated clock (clock gated with a qualifier) | XCKS[92H[0]] |
| XDQ | M4 | 1/O | data valid flag of the expansion port input (qualifier): if output, then decoder (HREF and VGATE) gate (see Fig.31) | - |
| XRDY | N3 | 0 | data request flag = ready to receive, to work with optional buffer in external device, to prevent internal buffer overflow; second function: input related task flag A/B | XRQT[83H[2]] |
| XRH | N2 | I/O | horizontal reference signal for the $X$ port: as output: HREF or HS from the decoder (see Fig.31); as input: a reference edge for horizontal input timing and a polarity for input field ID detection can be defined | XRHS[13H[6]], XFDH[92H[6]] and $\mathrm{XDH}[92 \mathrm{H}[2]]$ |
| XRV | L5 | I/O | vertical reference signal for the X port: as output: V123 or field ID from the decoder, see Figs 29 and 30 ; as input: a reference edge for vertical input timing and for input field ID detection can be defined | XRVS[1:0] 13H[5:4], <br> XFDV[92H[7]] and XDV[1:0] <br> 92H[5:4] |
| XTRI | K1 | 1 | port control: switches X port input to 3 -state | XPE[1:0] 83H[1:0] |

### 10.4.1 X PORT CONFIGURED AS OUTPUT

If the data output is enabled at the expansion port, then the data stream from the decoder is present. The data format of the 8-bit data bus is dependent on the chosen data type which is selectable by the line control registers LCR2 to LCR24; see Table 33. In contrast to the image port, the sliced data format is not available on the expansion port. Instead, raw CVBS samples are always transferred if any sliced data type is selected.

Details of some of the data types on the expansion port are as follows:

- Active video: (data type 15) contains components $Y-C_{B}-C_{R} 4: 2: 2$ signal, 720 active pixels per line. The amplitude and offsets are programmable via DBRI7 to DBRI0, DCON7 to DCON0, DSAT7 to DSAT0, OFFU1, OFFU0, OFFV1 and OFFV0. For nominal levels see Fig. 25.
- Test line: (data type 6) is similar to the active video format, with some constraints within the data processing:
- adaptive chrominance comb filter, vertical filter (chrominance comb filter for NTSC standards, PAL phase error correction) within the chrominance processing are disabled
- adaptive luminance comb filter, peaking and chrominance trap are bypassed within the luminance processing.
This data type is defined for future enhancements. It can be activated for lines containing standard test signals within the vertical blanking period. Currently most sources do not contain test lines. For nominal levels see Fig. 25.
- Raw samples (data types 0 to 5 and 7 to 14): $C_{B}-C_{R}$ samples are similar to data type 6 , but CVBS samples are transferred instead of processed luminance samples within the $Y$ time slots.
The amplitude and offset of the CVBS signal is programmable via RAWG7 to RAWG0 and RAWO7 to RAWO0, see Chapter 18,
Tables 174 and 175. For nominal levels see Fig.26.
The relationship of LCR programming to line numbers is described in Section 9.2; see Tables 34 to 37.

The data type selections by LCR are overruled by setting OFTS2 = 1 (subaddress 13H bit 2). This setting is mainly intended for device production testing. The VPO-bus carries the upper or lower 8 bits of the two ADCs depending on the OFTS[1:0] 13H[1:0] settings; see Table 169. The output configuration is done via MODE[3:0] 02H[3:0] settings; see Table 151. If a Y/C mode is selected, the expansion port carries the multiplexed output signals of both ADCs, in CVBS mode the output of only one ADC. No timing reference codes are generated in this mode.
Remark: The LSBs (bit 0) of the ADCs are also available on pin RTS0; see Table 167.

The SAV/EAV timing reference codes define the start and end of valid data regions. The ITU-blanking code sequence '- 80-10-80-10-...' is transmitted during the horizontal blanking period, between EAV and SAV.

The position of the F bit is constant according to ITU 656; see Tables 60 and 61.
The $V$ bit can be generated in two different ways (see Tables 60 and 61) controlled via OFTS1 and OFTS0; see Table 169.

F and V bits change synchronously with the EAV code.

Table 58 Data format on the expansion port

|  | $\begin{aligned} & \text { ANK } \\ & \hline \text { ERI } \end{aligned}$ |  | TIMING REFERENCE CODE (HEX) ${ }^{(1)}$ |  |  |  | 720 PIXELS $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ 4:2:2 DATA $^{(2)}$ |  |  |  |  |  |  |  |  | TIMING REFERENCE CODE (HEX) ${ }^{(1)}$ |  |  |  | BLANKINGPERIOD |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\ldots$ | 80 | 10 | FF | 00 | 00 | SAV | $\mathrm{C}_{\mathrm{B}} \mathrm{O}$ | YO | $\mathrm{C}_{\mathrm{R}} 0$ | Y1 | $\mathrm{C}_{\mathrm{B}} 2$ | Y2 | ... | $\mathrm{C}_{\mathrm{R}} 718$ | Y719 | FF | 00 | 00 | EAV | 80 | 10 |  |

## Notes

1. The generation of the timing reference codes can be suppressed by setting OFTS[2:0] to '010'; see Table 169. In this event the code sequence is replaced by the standard '- 80-10-' blanking values.
2. If raw samples or sliced data are selected by the line control registers (LCR2 to LCR24), the $Y$ samples are replaced by CVBS samples.

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Table 59 SAV/EAV format on expansion port XPD7 to XPD0

| BIT 7 | BIT 6 <br> (F) | BIT 5 <br> (V) | BIT 4 <br> (H) | BIT 3 <br> (P3) | BIT 2 <br> (P2) | BIT 1 <br> (P1) | BIT 0 <br> (P0) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | field bit | vertical blanking bit | format |  |  |  |  |
|  | 1st field: $\mathrm{F}=0$ |  |  |  |  |  |  |
| 2nd field: $\mathrm{F}=1$ |  |  |  |  |  |  |  |

Table 60525 lines $/ 60 \mathrm{~Hz}$ vertical timing

| LINE NUMBER | F (ITU 656) | V |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | OFTS[2:0] = 000 (ITU 656) | OFTS[2:0] = 001 |  |
| 1 to 3 | 1 | 1 | according to selected VGATE position type via <br> VSTA and VSTO (subaddresses 15H to 17H); <br> see Tables 171 to 173 |  |
| 4 to 19 | 0 | 1 |  |  |
| 20 | 0 | 0 |  |  |
| 21 | 0 | 0 |  |  |
| 22 to 261 | 0 | 0 |  |  |
| 262 | 0 | 0 |  |  |
| 263 | 0 | 0 |  |  |
| 264 and 265 | 0 | 1 |  |  |
| 266 to 282 | 1 | 1 |  |  |
| 283 | 1 | 0 |  |  |
| 284 | 1 | 0 |  |  |
| 285 to 524 | 1 | 0 |  |  |
| 525 | 1 | 0 |  |  |

Table 61625 lines/50 Hz vertical timing

| LINE NUMBER | F (ITU 656) | V |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | OFTS[2:0] = 000 (ITU 656) | OFTS[1:0] = 10 |  |
| 1 to 22 | 0 | 1 | according to selected VGATE position type via <br> VSTA and VSTO (subaddresses 15H to 17H); <br> see Tables 171 to 173 |  |
| 23 | 0 | 0 |  |  |
| 24 to 309 | 0 | 0 |  |  |
| 310 | 0 | 0 |  |  |
| 311 and 312 | 0 | 1 |  |  |
| 313 to 335 | 1 | 1 |  |  |
| 336 | 1 | 0 |  |  |
| 337 to 622 | 1 | 0 |  |  |
| 623 | 1 | 0 |  |  |
| 624 and 625 | 1 | 1 |  |  |

### 10.4.2 X PORT CONFIGURED AS INPUT

If data input mode is selected at the expansion port, then the scaler can choose its input data stream from the on-chip video decoder, or from the expansion port (controlled by bit SCSRC[1:0] 91H[5:4]). Byte serial $Y-C_{B}-C_{R} 4: 2: 2$, or subsets for other sampling schemes, or raw samples from an external ADC may be input (see also bits FSC[2:0] 91H[2:0]). The input data stream must be accompanied by an external clock XCLK, qualifier XDQ and reference signals XRH and XRV. Instead of the reference signal, embedded SAV and EAV codes, according to ITU 656, can also be accepted. The protection bits are not evaluated.

XRH and XRV carry the horizontal and vertical synchronization signals for the digital video stream through the expansion port. The field ID of the input video stream is carried in the phase (edge) of XRV and state of XRH, or directly as FS (frame sync, odd/even signal) on the XRV pin (controlled by XFDV[92H[7]], XFDH[92H[6]] and XDV1[92H[5]]).

The trigger events on XRH (rising/falling edge) and XRV (rising/falling both edges) for the scalers acquisition window are defined by XDV[1:0] 92H[5:4] and XDH[92H[2]]. The signal polarity of the qualifier can also be defined by bit XDQ[92H[1]]. As an alternative to the qualifier, the input clock can be applied to a gated clock (clock gated with a data qualifier, controlled by bit XCKS[92H[0]]). In this event, all input data will be qualified.

### 10.5 Image port (I port)

The image port transfers data from the scaler as well as from the VBI data slicer, if selected (maximum 33 MHz ). The reference clock is available at the ICLK pin as an output or as an input (maximum 33 MHz ). As an output, the ICLK is derived from the line-locked decoder or expansion port input clock. The data stream from the scaler output is normally discontinuous. Therefore valid data during a clock cycle is accompanied by a data qualifying (data valid) flag on pin IDQ. For pin constrained applications the IDQ pin can be programmed to function as a gated clock output (bit ICKS2[80H[2]]).

The data formats at the image port are defined in Dwords of 32 bits ( 4 bytes), such as the related FIFO structures. However, the physical data stream at the image port is only 16 -bit or 8 -bit wide; in 16-bit mode data pins HPD7 to HPD0 are used for chrominance data. The four bytes of the Dwords are serialized in words or bytes.

The available formats are as follows:

- $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : $2: 2$
- $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 1: 1$
- Raw samples
- Decoded VBI data.

For handshaking with the receiving VGA controller, or other memory or bus interface circuitry, F, H and V reference signals and programmable FIFO flags are provided. The information is provided on pins IGPO, IGP1, IGPH and IGPV. The function on these pins is controlled via subaddresses 84 H and 85 H .

VBI data is collected over an entire line in its own FIFO and transferred as an uninterrupted block of bytes. Decoded VBI data can be signed by the VBI flag on pins IGPO and IGP1.

Because scaled video data and decoded VBI data may come from different and asynchronous sources, an arbitration scheme is needed. Normally the VBI data slicer has priority.

The image port consists of the pins and/or signals, as given in Table 62.
For pin constrained applications, or interfaces, the relevant timing and data reference signals can also be encoded into the data stream. Therefore the corresponding pins do not need to be connected. The minimum image port configuration requires 9 pins only, i.e. 8 pins for data including codes, and 1 pin for clock or gated clock. The inserted codes are defined in close relationship to the ITU-R BT. 656 (D1) recommendation, where possible.

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The following deviations from "ITU 656 recommendation" are implemented at the SAA7108E; SAA7109Es image port interface:

- SAV and EAV codes are only present in those lines, where data is to be transferred, i.e. active video lines, or VBI raw samples, no codes for empty lines
- There may be more or less than 720 pixels between SAV and EAV
- The data content and number of clock cycles during horizontal and vertical blanking is undefined, and may be not constant
- The data stream may be interleaved with not-valid data codes, 00 H , but SAV and EAV 4-byte codes are not interleaved with not-valid data codes
- There may be an irregular pattern of not-valid data, or IDQ, and as a result, ' $C_{B}-Y-C_{R}-Y$-' is not in a fixed phase to a regular clock divider
- VBI raw sample streams are enveloped with SAV and EAV, like normal video
- Decoded VBI data is transported as Ancillary (ANC) data, two modes:
- direct decoded VBI data bytes (8-bit) are directly placed in the ANC data field, 00 H and FFH codes may appear in the data block (violation to ITU-R BT.656)
- recoded VBI data bytes (8-bit) directly placed in ANC data field, 00 H and FFH codes will be recoded to even parity codes 03H and FCH to suppress invalid ITU-R BT. 656 codes.

There are no empty cycles in the ancillary code or its data field. The data codes 00 H and FFH are suppressed (changed to 01 H or FEH respectively) in the active video stream, as well as in the VBI raw sample stream (VBI pass-through). As an option the number range can be limited further.

Table 62 Signals dedicated to the image port

| SYMBOL | PIN | I/O | DESCRIPTION | BIT |
| :--- | :---: | :---: | :--- | :--- |
| IPD7 to <br> IPD0 | E14, D14, <br> C14, B14, <br> E13, D13, <br> C13 and B13 | I/O | I port data | ICODE[93H[7]], ISWP[1:0] 85H[7:6] <br> and IPE[1:0] 87H[1:0] |
| ICLK | H12 | I/O | continuous reference clock at image port, <br> can be input or output, as output decoder <br> LLC or XCLK from X port | ICKS[1:0] 80H[1:0] and IPE[1:0] <br> $87 H[1: 0]$ |
| IDQ | H14 | O | data valid flag at image port, qualifier, with <br> programmable polarity; <br> secondary function: gated clock | ICKS2[80H[2]], IDQP[85H[0]] and <br> IPE[1:0] 87H[1:0] |
| IGPH | G12 | O | horizontal reference output signal, copy of <br> the horizontal gate signal of the scaler, with <br> programmable polarity; <br> alternative function: HRESET pulse | IDH[1:0] 84H[1:0], IRHP[85H[1]] and <br> IPE[1:0] 87H[1:0] |
| IGPV | F13 | O | vertical reference output signal, copy of the <br> vertical gate signal of the scaler, with <br> programmable polarity; <br> alternative function: VRESET pulse | IDV[1:0] 84H[3:2], IRVP[85H[2]] and <br> IPE[1:0] 87H[1:0] |
| IGP1 | G13 | O | general purpose output signal for I port | IDG12[86H[4]], IDG1[1:0] 84H[5:4], <br> IG1P[85H[3]] and IPE[1:0] 87H[1:0] |
| IGP0 | F14 | O | general purpose output signal for I port | IDG02[86H[5]], IDGO[1:0] 84H[7:6], <br> IG0P[85H[4]] and IPE[1:0] 87H[1:0] |
| ITRDY | J14 | I | target ready input signals | - |
| ITRI | G14 | I | port control, switches I port into 3-state | IPE[1:0] 87H[1:0] |

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### 10.6 Host port for 16-bit extension of video data I/O (H port)

The H port, pins HPD, can be used to extend the data I/O paths to 16-bit.
The I port has functional priority. If 18 _16[93H[6]] is set to logic 1 the output drivers of the H port are enabled and are dependent on the I port enable control. When I8_16=0, the HPD output is disabled.

Table 63 Signals dedicated to the host port

| SYMBOL | PIN | I/O | DESCRIPTION | BIT |
| :--- | :---: | :---: | :--- | :--- |
| HPD7 to <br> HPD0 | A13, D12, C12, B12, <br> A12, C11, B11 and A11 | I/O | 16-bit extension for digital I/O <br> (chrominance component) | IPE[1:0] 87H[1:0], ITRI[8FH[6]] and <br> I8_16[93H[6]] |

### 10.7 Basic input and output timing diagrams for the $I$ and $X$ ports

### 10.7.1 I PORT OUTPUT TIMING

The following diagrams (Figs 39 to 45 ) illustrate the output timing via the I port. IGPH and IGPV are indicated as logic 1 active gate signals. If reference pulses are programmed, these pulses are generated on the rising edge of the logic 1 active gates. Valid data is accompanied by the output data qualifier on pin IDQ. In addition, invalid cycles are marked with output code 00 H .

The IDQ output pin may be defined to be a gated clock output signal (ICLK AND internal IDQ).

### 10.7.2 X PORT INPUT TIMING

The input timing requirements at the X port are the same as those for the I port output. However, the following differences should be noted:

- It is not necessary to mark invalid cycles with a 00 H code
- No constraints on the input qualifier (can be a random pattern)
- XCLK may by a gated clock (XCLK AND external XDQ).

Remark: All timings illustrated are given for an uninterrupted output stream (no handshake with the external hardware).


Fig. 39 Output timing at the I port for serial 8-bit data at start of a line $(I C O D E=1)$.


Fig. 40 Output timing at the I port for serial 8-bit data at start of a line $(I C O D E=0)$.


Fig. 41 Output timing at the I port for serial 8-bit data at end of a line $(I C O D E=1)$.


Fig. 42 Output timing at the I port for serial 8-bit data at end of a line $(I C O D E=0)$.


Fig. 43 Output timing for 16 -bit data output via the I and H port with codes $(I C O D E=1)$, timing is like 8 -bit output, but packages of 2 bytes per valid cycle.


Fig. 44 Horizontal and vertical gate output timing.


Fig. 45 Output timing for sliced VBI data in 8-bit serial output mode (dotted graphs for SAV/EAV mode).

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## 11 BOUNDARY SCAN TEST

The SAA7108E; SAA7109E has built-in logic and 2 times 5 dedicated pins to support boundary scan testing, separately for the encoder and decoder part, which allows board testing without special hardware (nails). The SAA7108E; SAA7109E follows the "IEEE Std. 1149.1Standard Test Access Port and Boundary-Scan Architecture" set by the Joint Test Action Group (JTAG) chaired by Philips.

The 10 special pins are Test Mode Select (TMSe and TMSd), Test Clock (TCLKe and TCLKd), Test Reset (TRSTe and TRSTd), Test Data Input (TDIe and TDId) and Test Data Output (TDOe and TDOd), where extension ' $e$ ' refers to the encoder part and extension ' $d$ ' refers to the decoder part.

The Boundary Scan Test (BST) functions BYPASS, EXTEST, INTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 64. Details about the JTAG BST-TEST can be found in the specification "IEEE Std. 1149.1". Two files containing the detailed Boundary Scan Description Language (BSDL) of the SAA7108E; SAA7109E are available on request.

Table 64 BST instructions supported by the SAA7108E; SAA7109E

| INSTRUCTION | DESCRIPTION |
| :---: | :--- |
| BYPASS | This mandatory instruction provides a minimum length serial path (1 bit) between TDle (or TDId) <br> and TDOe (or TDOd) when no test operation of the component is required. |
| EXTEST | This mandatory instruction allows testing of off-chip circuitry and board level interconnections. |
| SAMPLE | This mandatory instruction can be used to take a sample of the inputs during normal operation of <br> the component. It can also be used to preload data values into the latched outputs of the boundary <br> scan register. |
| CLAMP | This optional instruction is useful for testing when not all ICs have BST. This instruction addresses <br> the bypass register while the boundary scan register is in external test mode. |
| IDCODE | This optional instruction will provide information on the components manufacturer, part number and <br> version number. |
| INTEST | This optional instruction allows testing of the internal logic (no support for customers available). |
| USER1 | This private instruction allows testing by the manufacturer (no support for customers available). |

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### 11.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRSTe or TRSTd pin LOW.

### 11.2 Device identification codes

A device identification register is specified in "IEEE Std. 1149.1b-1994". It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and to determine the version number of the ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDle (or TDId) and TDOe (or TDOd) of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller, this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0 , where bit 31 is the most significant bit (nearest to TDIe or TDId) and bit 0 is the least significant bit (nearest to TDOe or TDOd); see Fig. 46.


Fig. 4632 bits of identification code.

## 12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all ground pins connected together and all supply pins connected together.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{V}_{\text {DDD }}$ | digital supply voltage |  | -0.5 | +4.6 | V |
| $\mathrm{~V}_{\text {DDA }}$ | analog supply voltage |  | -0.5 | +4.6 | V |
| $\mathrm{~V}_{\mathrm{i}(\mathrm{A})}$ | input voltage at analog inputs |  | -0.5 | $\mathrm{~V}_{\mathrm{DDA}}+0.5^{(1)}$ | V |
| $\mathrm{V}_{\mathrm{o}(\mathrm{A})}$ | output voltage at analog outputs | -0.5 | $\mathrm{~V}_{\mathrm{DDA}}+0.5$ | V |  |
| $\mathrm{~V}_{\mathrm{i}(\mathrm{D})}$ | input voltage at digital inputs and outputs | outputs in 3-state; <br> note 2 | -0.5 | +5.5 | V |
| $\mathrm{~V}_{\mathrm{o}(\mathrm{D})}$ | output voltage at digital outputs | outputs active | -0.5 | $\mathrm{~V}_{\mathrm{DDD}}+0.5$ | V |
| $\Delta \mathrm{~V}_{\text {SS }}$ | voltage difference between $\mathrm{V}_{\text {SSA(n) }}$ and $\mathrm{V}_{\mathrm{SSD}(\mathrm{n})}$ |  | - | 100 | mV |
| $\mathrm{T}_{\text {stg }}$ | storage temperature |  | -65 | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {amb }}$ | ambient temperature |  | 0 | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {esd }}$ | electrostatic discharge voltage all pins | note 3 | -2000 | +2000 | V |

## Notes

1. Maximum: 4.6 V .
2. Except pins XTALId and XTALIe.
3. Human body model: equivalent to discharging a 100 pF capacitor through a $1.5 \mathrm{k} \Omega$ resistor.

## 13 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
| :--- | :--- | :--- | :---: | :---: |
| $\mathrm{R}_{\mathrm{th}(\mathrm{j}-\mathrm{a})}$ | thermal resistance from junction to ambient | in free air | $<35$ | K/W |

## 14 CHARACTERISTICS OF THE DIGITAL VIDEO ENCODER PART

$\mathrm{V}_{\mathrm{DDD}}=3.0$ to 3.6 V ; $\mathrm{T}_{\mathrm{amb}}=0$ to $70^{\circ} \mathrm{C}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supplies |  |  |  |  |  |  |
| $V_{\text {DDA }}$ | analog supply voltage |  | 3.15 | 3.3 | 3.45 | V |
| $\mathrm{V}_{\text {DDD }}$ | digital supply voltage |  | 3.0 | 3.3 | 3.6 | V |
| IDDA | analog supply current | note 1 | 1 | 107 | 120 | mA |
| $\mathrm{I}_{\text {DDD }}$ | digital supply current | $\mathrm{V}_{\text {DDD }}=3.3 \mathrm{~V}$; note 2 | 1 | 57 | 75 | mA |
| Inputs |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IL }}$ | LOW-level input voltage at all digital input pins except pins SDAe and SCLe |  | -0.5 | - | +0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH-level input voltage at all digital input pins except pins SDAe and SCLe |  | 2.0 | - | $V_{\text {DDD }}+0.3$ | V |
| $\mathrm{ILI}^{\prime}$ | input leakage current |  | - | - | 10 | $\mu \mathrm{A}$ |
| $\mathrm{Ci}_{i}$ | input capacitance | clocks | - | - | 10 | pF |
|  |  | data | - | - | 8 | pF |
|  |  | I/Os at high-impedance | - | - | 8 | pF |
| Outputs; all digital output pins except pin SDAe |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW-level output voltage | $\mathrm{IOL}=2 \mathrm{~mA}$ | - | - | 0.4 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH-level output voltage | $\mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}$ | 2.4 | - | - | V |
| $1^{2} \mathrm{C}$-bus; pins SDAe and SCLe |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IL }}$ | LOW-level input voltage |  | -0.5 | - | $0.3 \mathrm{~V}_{\text {DDD }}$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH-level input voltage |  | $0.7 \mathrm{~V}_{\text {DDD }}$ | - | $\mathrm{V}_{\mathrm{DDD}}+0.3$ | V |
| $\mathrm{I}_{\mathrm{i}}$ | input current | $\mathrm{V}_{\mathrm{i}}=$ LOW or HIGH | -10 | - | +10 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW-level output voltage (pin SDAe) | $\mathrm{l}_{\mathrm{OL}}=3 \mathrm{~mA}$ | - | - | 0.4 | V |
| $\mathrm{I}_{0}$ | output current | during acknowledge | 3 | - | - | mA |
| Clock timing; pins PIXCLKI and PIXCLKO |  |  |  |  |  |  |
| TPIXCLK | cycle time | note 3 | 22.5 | - | 100 | ns |
| $\mathrm{t}_{\mathrm{d} \text { (CLKD) }}$ | delay from PIXCLKO to PIXCLKK | note 4 | - | - | - | ns |
| $\delta$ | duty factor $\mathrm{t}_{\text {HIGH }} / \mathrm{T}_{\text {PIXCLK }}$ | note 3 | 40 | 50 | 60 | \% |
|  | duty factor $\mathrm{t}_{\text {HIGH }} / \mathrm{T}_{\text {CLKO2 }}$ | output | 40 | 50 | 60 | \% |
| $\mathrm{t}_{\mathrm{r}}$ | rise time | note 3 | - | - | 3 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | fall time | note 3 | - | - | 3 | ns |
| Input timing |  |  |  |  |  |  |
| $\mathrm{t}_{\text {SU; DAT }}$ | input data set-up time |  | 5 | - | - | ns |
| $\mathrm{t}_{\text {HD } ; \text { DAT }}$ | input data hold time |  | 0 | - | - | ns |


| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Crystal oscillator |  |  |  |  |  |  |
| $\mathrm{f}_{\text {nom }}$ | nominal frequency |  | - | 27 | - | MHz |
| $\Delta \mathrm{f} / \mathrm{f}_{\text {nom }}$ | permissible deviation of nominal frequency | note 5 | -50 | - | +50 | $10^{-6}$ |
| CRYStal specification |  |  |  |  |  |  |
| $\mathrm{T}_{\text {amb }}$ | ambient temperature |  | 0 | - | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{C}_{\mathrm{L}}$ | load capacitance |  | 8 | - | - | pF |
| $\mathrm{R}_{\mathrm{S}}$ | series resistance |  | - | - | 80 | $\Omega$ |
| $\mathrm{C}_{1}$ | motional capacitance (typical) |  | 1.2 | 1.5 | 1.8 | fF |
| $\mathrm{C}_{0}$ | parallel capacitance (typical) |  | 2.8 | 3.5 | 4.2 | pF |
| Data and reference signal output timing |  |  |  |  |  |  |
| $\mathrm{C}_{0}($ L $)$ | output load capacitance |  | 8 | - | 40 | pF |
| $\mathrm{t}_{\text {(h) }}$ | output hold time |  | 2 | - | - | ns |
| $\mathrm{t}_{\text {(d) }}$ | output delay time |  | - | - | 16 | ns |
| CVBS and RGB outputs |  |  |  |  |  |  |
| $\mathrm{V}_{\text {O(CVBS)(p-p) }}$ | output voltage CVBS (peak-to-peak value) | see Table 65 | - | 1.23 | - | V |
| $\mathrm{V}_{\text {o(VBS ( }(p-p)}$ | output voltage VBS (S-video) (peak-to-peak value) | see Table 65 | - | 1.0 | - | V |
| $\mathrm{V}_{\mathrm{o}}(\mathrm{C})(\mathrm{p}-\mathrm{p})$ | output voltage C (S-video) (peak-to-peak value) | see Table 65 | - | 0.89 | - | V |
| $\mathrm{V}_{\mathrm{o} \text { (RGB)(p-p) }}$ | output voltage R, G, B (peak-to-peak value) | see Table 65 | - | 0.7 | - | V |
| $\Delta V_{0}$ | inequality of output signal voltages |  | - | 2 | - | \% |
| $\mathrm{R}_{0 \text { (L) }}$ | output load resistance |  | - | 37.5 | - | $\Omega$ |
| $\mathrm{B}_{\text {DAC }}$ | output signal bandwidth of DACs | $-3 \mathrm{~dB}$ | 15 | - | - | MHz |
| ILE ${ }_{\text {If( } \mathrm{DAC}}$ | low frequency integral linearity error of DACs |  | - | - | $\pm 3$ | LSB |
| DLE $\mathrm{lf}_{\text {(DAC) }}$ | low frequency differential linearity error of DACs |  | - | - | $\pm 1$ | LSB |

## Notes

1. Minimum value for $\mathrm{I}^{2} \mathrm{C}$-bus bit $\mathrm{DOWNA}=1$.
2. Minimum value for $I^{2} \mathrm{C}$-bus bit $\mathrm{DOWND}=1$.
3. The data is for both input and output direction.
4. This parameter is arbitrary, if PIXCLKI is looped through the VGC.
5. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.

## 15 CHARACTERISTICS OF THE DIGITAL VIDEO DECODER PART

$\mathrm{V}_{\mathrm{DDD}}=3.0$ to 3.6 V ; $\mathrm{V}_{\mathrm{DDA}}=3.1$ to $3.5 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$; timings and levels refer to drawings and conditions illustrated in Fig. 51; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supplies |  |  |  |  |  |  |
| $\mathrm{V}_{\text {DDD }}$ | digital supply voltage |  | 3.0 | 3.3 | 3.6 | V |
| I ${ }^{\text {IDD }}$ | digital supply current | X port 3-state; 8-bit I port | - | 90 | - | mA |
| $\mathrm{P}_{\mathrm{D}}$ | power dissipation digital part |  | - | 300 | - | mW |
| V ${ }_{\text {DDA }}$ | analog supply voltage |  | 3.15 | 3.3 | 3.45 | V |
| IDDA | analog supply current | $\begin{aligned} & \text { AOSL1 and AOSLO = } 0 \\ & \text { CVBS mode } \\ & \text { Y/C mode } \end{aligned}$ | $\mid-$ | $\begin{aligned} & 47 \\ & 72 \end{aligned}$ | $\mid-$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\mathrm{P}_{\mathrm{A}}$ | power dissipation analog part | CVBS mode | - | 150 | - | mW |
|  |  | Y/C mode | - | 240 | - | mW |
| $\mathrm{P}_{\text {tot(A+D) }}$ | total power dissipation analog and digital part | CVBS mode | - | 450 | - | mW |
|  |  | Y/C mode | - | 540 | - | mW |
| $\mathrm{P}_{\text {tot(A+D)(pd) }}$ | total power dissipation analog and digital part in power-down mode | CE pulled down to ground | - | 5 | - | mW |
| $P_{\text {tot(A+D)(ps) }}$ | total power dissipation analog and digital part in power-save mode | ${ }^{2}$ ²-bus controlled via address $88 \mathrm{H}=0 \mathrm{FH}$ | - | 75 | - | mW |
| Analog part |  |  |  |  |  |  |
| $\mathrm{I}_{\text {clamp }}$ | clamping current | $\mathrm{V}_{1}=0.9 \mathrm{~V}$ DC | - | $\pm 8$ | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{i}(\mathrm{p}-\mathrm{p})}$ | input voltage (peak-to-peak value) | for normal video levels $1 \mathrm{~V}(\mathrm{p}-\mathrm{p}),-3 \mathrm{~dB}$ termination $27 / 47 \Omega$ and AC coupling required; coupling capacitor $=22 \mathrm{nF}$ | - | 0.7 | - | V |
| $\left\|\mathrm{Z}_{\mathrm{i}}\right\|$ | input impedance | clamping current off | 200 | - | - | k $\Omega$ |
| $\mathrm{C}_{i}$ | input capacitance |  | - | - | 10 | pF |
| $\alpha_{\text {cs }}$ | channel crosstalk | $\mathrm{f}_{\mathrm{i}}<5 \mathrm{MHz}$ | - | - | -50 | dB |
| 9-bit analog-to-digital converters |  |  |  |  |  |  |
| B | analog bandwidth | at -3 dB | - | 7 | - | MHz |
| $\phi_{\text {diff }}$ | differential phase (amplifier plus anti-alias filter bypassed) |  | - | 2 | - | deg |
| $\mathrm{G}_{\text {diff }}$ | differential gain (amplifier plus anti-alias filter bypassed) |  | - | 2 | - | \% |
| $\mathrm{f}_{\mathrm{clk}(\mathrm{ADC})}$ | ADC clock frequency |  | 12.8 | - | 14.3 | MHz |
| DLE $_{\text {dc }}(\mathrm{d})$ | DC differential linearity error |  | - | 0.7 | - | LSB |


| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ILE ${ }_{\text {dc }(i)}$ | DC integral linearity error |  | - | 1 | - | LSB |
| Digital inputs |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IL(SDAd, SCLd) }}$ | LOW-level input voltage pins SDAd and SCLd |  | -0.5 | - | $+0.3 \mathrm{~V}_{\text {DDD }}$ | V |
| $\mathrm{V}_{\mathrm{IH}(\text { SDAd,SCLd })}$ | HIGH-level input voltage pins SDAd and SCLd |  | $0.7 \mathrm{~V}_{\text {DDD }}$ | - | $\mathrm{V}_{\mathrm{DDD}}+0.5$ | V |
| $\mathrm{V}_{\text {IL (XTALId) }}$ | LOW-level CMOS input voltage pin XTALId |  | -0.3 | - | +0.8 | V |
| $\mathrm{V}_{\text {IH(XTALId) }}$ | HIGH-level CMOS input voltage pin XTALId |  | 2.0 | - | $\mathrm{V}_{\text {DDD }}+0.3$ | V |
| $\mathrm{V}_{\mathrm{IL}(\mathrm{n})}$ | LOW-level input voltage all other inputs |  | -0.3 | - | +0.8 | V |
| $\mathrm{V}_{\mathrm{IH}(\mathrm{n})}$ | HIGH-level input voltage all other inputs |  | 2.0 | - | 5.5 | V |
| $\mathrm{I}_{\text {LI }}$ | input leakage current |  | - | - | 1 | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\mathrm{L} / \mathrm{O}}$ | I/O leakage current |  | - | - | 10 | $\mu \mathrm{A}$ |
| $\mathrm{C}_{i}$ | input capacitance | I/O at high-impedance | - | - | 8 | pF |

Digital outputs; note 1

| $V_{\text {OL(SDAd) }}$ | LOW-level output voltage <br> pin SDAd | SDAd at 3 mA sink current | - | - | 0.4 | V |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~V}_{\mathrm{OL}(\mathrm{clk})}$ | LOW-level output voltage <br> for clocks |  | -0.5 | - | +0.6 | V |
| $\mathrm{~V}_{\mathrm{OH}(\mathrm{clk})}$ | HIGH-level output voltage <br> for clocks |  | 2.4 | - | $\mathrm{V}_{\mathrm{DDD}}+0.5$ | V |
| $\mathrm{~V}_{\mathrm{OL}}$ | LOW-level output voltage <br> all other digital outputs |  | 0 | - | 0.4 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | HIGH-level output voltage <br> all other digital outputs |  | 2.4 | - | $\mathrm{V}_{\mathrm{DDD}}+0.5$ | V |

Clock output timing (LLC and LLC2); note 2

| $\mathrm{C}_{\mathrm{L}(\mathrm{LLC})}$ | output load capacitance |  | 15 | - | 50 | pF |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{T}_{\mathrm{cy}}$ | cycle time | pin LLC | 35 | - | 39 | ns |
|  |  | pin LLC2 | 70 | - | 78 | ns |
| $\delta$ | duty factors for $\mathrm{t}_{\mathrm{LLCH}} / \mathrm{tLLC}$ <br> and $\mathrm{tLLC2H} / \mathrm{tLLC}^{2}$ | $\mathrm{C}_{\mathrm{L}}=40 \mathrm{pF}$ | 40 | - | 60 | $\%$ |
| $\mathrm{t}_{\mathrm{r}}$ | rise time LLC and LLC2 | 0.2 V to $\mathrm{V}_{\mathrm{DDD}}-0.2 \mathrm{~V}$ | - | - | 5 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | fall time LLC and LLC2 | $\mathrm{V}_{\mathrm{DDD}}-0.2 \mathrm{~V}$ to 0.2 V | - | - | 5 | ns |
| $\mathrm{t}_{\mathrm{d}(\text { LLC-LLC2 })}$ | delay time between LLC <br> and LLC2 output | measured at $1.5 \mathrm{~V} ;$ <br> $\mathrm{C}_{\mathrm{L}}=25 \mathrm{pF}$ | -4 | - | +8 | ns |

## Horizontal PLL

| $\mathrm{f}_{\mathrm{H}(\text { nom })}$ | nominal line frequency | 50 Hz field | - | 15625 | - | Hz |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  | 60 Hz field | - | 15734 | - | Hz |
| $\Delta \mathrm{f}_{\mathrm{H}} / \mathrm{f}_{\mathrm{H}(\mathrm{n})}$ | permissible static deviation |  | - | - | 5.7 | $\%$ |


| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Subcarrier PLL |  |  |  |  |  |  |
| $\mathrm{f}_{\mathrm{sc}(\mathrm{nom})}$ | nominal subcarrier frequency | PAL BGHI | - | 4433619 | - | Hz |
|  |  | NTSC M | - | 3579545 | - | Hz |
|  |  | PAL M | - | 3575612 | - | Hz |
|  |  | PAL N | - | 3582056 | - | Hz |
| $\Delta \mathrm{f}_{\text {sc }}$ | lock-in range |  | $\pm 400$ | - | - | Hz |

Crystal oscillator for $\mathbf{3 2 . 1 1} \mathbf{~ M H z}$; note 3

| $\mathrm{f}_{\text {xtal(nom) }}$ | nominal frequency | 3rd-harmonic | - | 32.11 | - | MHz |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\Delta \mathrm{f}_{\text {xtal(nom) }}$ | permissible nominal <br> frequency deviation |  | - | - | $\pm 70 \times 10^{-6}$ |  |
| $\Delta \mathrm{f}_{\text {xtal(nom)(T) }}$ | permissible nominal <br> frequency deviation with <br> temperature |  | - | - | $\pm 30 \times 10^{-6}$ |  |
| CRYSTAL SPECIFICATION (X1) | ambient temperature |  |  |  |  |  |
| $\mathrm{T}_{\text {amb(X1) }}$ | load capacitance |  | 0 | - | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{C}_{\mathrm{L}}$ | series resonance resistor |  | 8 | - | - | pF |
| $\mathrm{R}_{\mathrm{S}}$ | motional capacitance |  | - | 40 | 80 | $\Omega$ |
| $\mathrm{C}_{1}$ | parallel capacitance |  | - | $1.5 \pm 20 \%$ | - | fF |
| $\mathrm{C}_{0}$ |  | - | $4.3 \pm 20 \%$ | - | pF |  |

Crystal oscillator for $\mathbf{2 4 . 5 7 6 ~ M H z ; ~ n o t e ~} 3$

| $\mathrm{f}_{\text {xtal(nom) }}$ | nominal frequency | 3rd-harmonic | - | 24.576 | - | MHz |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\Delta \mathrm{f}_{\text {xtal(nom) }}$ | permissible nominal <br> frequency deviation |  | - | - | $\pm 50 \times 10^{-6}$ |  |
| $\Delta \mathrm{f}_{\text {xtal(nom)( } \mathrm{T})}$ | permissible nominal <br> frequency deviation with <br> temperature |  | - | - | $\pm 20 \times 10^{-6}$ |  |
| CRYSTAL SPECIFICATION (X1) | ambient temperature |  |  |  |  |  |
| $\mathrm{T}_{\text {amb(X1) }}$ | load capacitance | series resonance resistor |  | 0 | - | 70 |
| $\mathrm{C}_{\mathrm{L}}$ | motional capacitance |  | 8 | - | - | pF |
| $\mathrm{R}_{\mathrm{S}}$ | parallel capacitance |  | - | 40 | 80 | $\Omega$ |
| $\mathrm{C}_{1}$ |  | - | $1.5 \pm 20 \%$ | - | fF |  |
| $\mathrm{C}_{0}$ |  | - | $3.5 \pm 20 \%$ | - | pF |  |

## Clock input timing (XCLK)

| $\mathrm{T}_{\mathrm{cy}}$ | cycle time |  | 31 | - | 45 | ns |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\delta$ | duty factors for $\mathrm{tLLCH}^{\prime} / \mathrm{tLCC}$ |  | 40 | 50 | 60 | $\%$ |
| $\mathrm{t}_{\mathrm{r}}$ | rise time |  | - | - | 5 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | fall time |  | - | - | 5 | ns |

Data and control signal input timing X port, related to XCLK input

| t $_{\text {SU; DAT }}$ | input data set-up time |  | - | 10 | - | ns |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{t}_{\text {HD } ; \text { DAT }}$ | input data hold time |  | - | 3 | - | ns |


| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Clock output timing |  |  |  |  |  |  |
| $\mathrm{C}_{\mathrm{L}}$ | output load capacitance |  | 15 | - | 50 | pF |
| $\mathrm{T}_{\text {cy }}$ | cycle time |  | 35 | - | 39 | ns |
| $\delta$ | duty factors for tXCLKH/t ${ }_{\text {XCLKL }}$ |  | 35 | - | 65 | \% |
| $\mathrm{t}_{\mathrm{r}}$ | rise time | 0.6 to 2.6 V | - | - | 5 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | fall time | 2.6 to 0.6 V | - | - | 5 | ns |
| Data and control signal output timing X port, related to XCLK output (for XPCK[1:0] 83H[5:4] = 00 is default); note 2 |  |  |  |  |  |  |
| $\mathrm{C}_{\mathrm{L}}$ | output load capacitance |  | 15 | - | 50 | pF |
| tohd; ${ }^{\text {dat }}$ | output hold time | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | - | 14 | - | ns |
| tPD | propagation delay from positive edge of XCLK output | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | - | 24 | - | ns |
| Control signal output timing RT port, related to LLC output |  |  |  |  |  |  |
| $\mathrm{C}_{\mathrm{L}}$ | output load capacitance |  | 15 | - | 50 | pF |
| tohd; ${ }^{\text {dat }}$ | output hold time | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | - | 14 | - | ns |
| tPD | propagation delay from positive edge of LLC output | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | - | 24 | - | ns |
| ICLK output timing |  |  |  |  |  |  |
| $\mathrm{C}_{\mathrm{L}}$ | output load capacitance |  | 15 | - | 50 | pF |
| $\mathrm{T}_{\mathrm{cy}}$ | cycle time |  | 31 | - | 45 | ns |
| $\delta$ | duty factors for $\mathrm{t}_{\text {ICLKH }} / \mathrm{t}_{\text {ICLKL }}$ |  | 35 | - | 65 | \% |
| $\mathrm{t}_{\mathrm{r}}$ | rise time | 0.6 to 2.6 V | - | - | 5 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | fall time | 2.6 to 0.6 V | - |  | 5 | ns |
| Data and control signal output timing I port, related to ICLK output (for IPCK[1:0] 87H[5:4] = 00 is default) |  |  |  |  |  |  |
| $\mathrm{C}_{\mathrm{L}}$ | output load capacitance at all outputs |  | 15 | - | 50 | pF |
| tohd; DAT | output data hold time | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | - | 12 | - | ns |
| $\mathrm{t}_{\text {(d) }}$ | output delay time | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | - | 22 | - | ns |
| ICLK input timing |  |  |  |  |  |  |
| $\mathrm{T}_{\text {cy }}$ | cycle time |  | 31 | - | 100 | ns |

## Notes

1. The levels must be measured with load circuits; $1.2 \mathrm{k} \Omega$ at 3 V (TTL load); $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$.
2. The effects of rise and fall times are included in the calculation of $t_{O H D} ; \mathrm{DAT}$ and $t_{\text {PD }}$. Timings and levels refer to drawings and conditions illustrated in Fig.51.
3. The crystal oscillator drive level is 0.28 mW (typ.).

## 16 TIMING

### 16.1 Digital video encoder part



Fig. 47 Input/output timing specification.


Fig. 48 Horizontal input timing.


Fig. 49 Vertical input timing.

## PC-CODEC

### 16.1.1 TELETEXT TIMING

Time $t_{F D}$ is the time needed to interpolate input data TTX and insert it into the CVBS and VBS output signal, such that it appears at $\mathrm{t}_{\mathrm{TT}}=9.78 \mu \mathrm{~s}(\mathrm{PAL})$ or $\mathrm{t}_{\mathrm{TT}}=10.5 \mu \mathrm{~s}$ (NTSC) after the leading edge of the horizontal synchronization pulse.

Time $t_{P D}$ is the pipeline delay time introduced by the source that is gated by TTXRQ_XCLKO2 in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ_XCLKO2, a new teletext bit must be provided by the source.

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of the outgoing horizontal synchronization pulse.

Time $t_{i(T T X W)}$ is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of $6.9375 \mathrm{Mbits} / \mathrm{s}$ (PAL), 296 teletext bits at a text data rate of 5.7272 Mbits/s (world standard TTX) or 288 teletext bits at a text data rate of 5.7272 Mbits/s (NABTS). The insertion window is not opened if the control bit TTXEN is zero.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

It is essential to note that the two pins used for teletext insertion must be configured for this purpose by the correct $\mathrm{I}^{2} \mathrm{C}$-bus register settings.


Fig. 50 Teletext timing.

### 16.2 Digital video decoder part



Fig. 51 Data input/output timing diagram (X port, RT port and I port).

## 17 APPLICATION INFORMATION



Fig. 52 Application circuit (decoder part).

|  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |


Fig. 53 Application circuit (encoder part).

(1a) With 3rd-harmonic quartz.
Crystal load $=8 \mathrm{pF}$.

(2a) With 3rd-harmonic quartz.
Crystal load $=8 \mathrm{pF}$.

(3a) With direct clock.

(1b) With fundamental quartz.
Crystal load $=20 \mathrm{pF}$.

(2b) With fundamental quartz.
Crystal load $=20 \mathrm{pF}$.

(3b) With fundamental quartz and restricted drive level. When $\mathrm{P}_{\text {drive }}$ of the internal oscillator is too high, a resistance $R_{s}$ can be placed in series with the oscillator output XTALOd.

Note: The decreased crystal amplitude results in a lower drive level but on the other hand the jitter performance will decrease.

Fig. 54 Oscillator application for decoder part.

(1a) With 3rd-harmonic quartz.
Crystal load $=8 \mathrm{pF}$.


(1b) With fundamental quartz.
Crystal load $=20 \mathrm{pF}$.

(2a) With direct clock
(2b) With fundamental quartz and restricted drive level. When $\mathrm{P}_{\text {drive }}$ of the internal oscillator is too high, a resistance $R_{s}$ can be placed in series with the oscillator output XTALOe.
Note: The decreased crystal amplitude results in a lower drive level but on the other hand the jitter performance will decrease.

Fig. 55 Oscillator application for encoder part.

## PC-CODEC

### 17.1 Analog output voltages

The analog output voltages are dependent on the total load (typical value $37.5 \Omega$ ), the digital gain parameters and the $I^{2} \mathrm{C}$-bus settings of the DAC reference currents (analog settings).
The digital output signals in front of the DACs under nominal (nominal here stands for the settings given in Tables 88 to 95 for example a standard PAL or NTSC signal) conditions occupy different conversion ranges, as indicated in Table 65 for a 100/100 colour bar signal.

By setting the reference currents of the DACs as shown in Table 65, standard compliant amplitudes can be achieved for all signal combinations; it is assumed that in subaddress 16 H , parameter $\mathrm{DACF}=0000 \mathrm{~b}$, that means the fine adjustment for all DACs in common is set to 0\%.
If $S$-video output is desired, the adjustment for the $C$ (chrominance subcarrier) output should be identical to the one for VBS (luminance plus sync) output.

Table 65 Digital output signals conversion range

| SET/OUT | CVBS, SYNC TIP-TO-WHITE | VBS, SYNC TIP-TO-WHITE | RGB, BLACK-TO-WHITE |
| :--- | :---: | :---: | :---: |
| Digital settings | see Tables 88 to 95 | see Tables 88 to 95 | see Table 83 |
| Digital output | 1014 | 881 | 876 |
| Analog settings | e.g. B DAC $=1$ FH | e.g. G DAC $=1$ BH | e.g. R DAC $=$ G DAC $=$ B DAC $=0 \mathrm{BH}$ |
| Analog output | $1.23 \mathrm{~V}(\mathrm{p}-\mathrm{p})$ | $1.00 \mathrm{~V}(\mathrm{p}-\mathrm{p})$ | $0.70 \mathrm{~V}(\mathrm{p}-\mathrm{p})$ |

### 17.2 Suggestions for a board layout

Use separate ground planes for analog and digital ground. Connect these planes only at one point directly under the device, by using a $0 \Omega$ resistor directly at the supply stage. Use separate supply lines for the analog and digital supply. Place the supply decoupling capacitors close to the supply pins.
Use $L_{\text {bead }}$ (ferrite coil) in each digital supply line close to the decoupling capacitors to minimize radiation energy (EMC).

Place the analog coupling (clamp) capacitors close to the analog input pins. Place the analog termination resistors close to the coupling capacitors.

Be careful of hidden layout capacitors around the crystal application.

Use serial resistors in clock, sync and data lines, to avoid clock or data reflection effects and to soften data energy.
$18 I^{2} \mathrm{C}$-BUS DESCRIPTION
18.1 Digital video encoder part

| REGISTER FUNCTION | SUB <br> (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Status byte (read only) | 00 | VER2 | VER1 | VERO | CCRDO | CCRDE | (1) | FSEQ | O_E |
| Null | 01 to 15 | (1) | (1) | (1) | ${ }^{(1)}$ | ${ }^{(1)}$ | ${ }^{(1)}$ | ${ }^{(1)}$ | (1) |
| Common DAC adjust fine | 16 | ${ }^{(1)}$ | ${ }^{(1)}$ | ${ }^{(1)}$ | (1) | DACF3 | DACF2 | DACF1 | DACFO |
| R DAC adjust coarse | 17 | (1) | ${ }^{(1)}$ | (1) | RDACC4 | RDACC3 | RDACC2 | RDACC1 | RDACC0 |
| G DAC adjust coarse | 18 | (1) | (1) | ${ }^{(1)}$ | GDACC4 | GDACC3 | GDACC2 | GDACC1 | GDACC0 |
| B DAC adjust coarse | 19 | (1) | (1) | (1) | BDACC4 | BDACC3 | BDACC2 | BDACC1 | BDACC0 |
| MSM threshold | 1A | MSMT7 | MSMT6 | MSMT5 | MSMT4 | MSMT3 | MSMT2 | MSMT1 | MSMT0 |
| Monitor sense mode | 1B | MSM | (1) | (1) | (1) | (1) | RCOMP | GCOMP | BCOMP |
| Chip ID (02B or 03B, read only) | 1 C | CID7 | CID6 | CID5 | CID4 | CID3 | CID2 | CID1 | CID0 |
| Wide screen signal | 26 | WSS7 | WSS6 | WSS5 | WSS4 | WSS3 | WSS2 | WSS1 | WSSO |
| Wide screen signal | 27 | WSSON | ${ }^{(1)}$ | WSS13 | WSS12 | WSS11 | WSS10 | WSS9 | WSS8 |
| Real-time control, burst start | 28 | (1) | (1) | BS5 | BS4 | BS3 | BS2 | BS1 | BSO |
| Sync reset enable, burst end | 29 | SRES | ${ }^{(1)}$ | BE5 | BE4 | BE3 | BE2 | BE1 | BE0 |
| Copy generation 0 | 2A | CG07 | CG06 | CG05 | CG04 | CG03 | CG02 | CG01 | CG00 |
| Copy generation 1 | 2B | CG15 | CG14 | CG13 | CG12 | CG11 | CG10 | CG09 | CG08 |
| CG enable, copy generation 2 | 2 C | CGEN | (1) | (1) | (1) | CG19 | CG18 | CG17 | CG16 |
| Output port control | 2D | VBSEN | CVBSEN1 | CVBSENO | CEN | ENCOFF | CLK2EN | (1) | (1) |
| Null | 2E to 37 | ${ }^{(1)}$ | ${ }^{(1)}$ | ${ }^{(1)}$ | (1) | (1) | (1) | (1) | (1) |
| Gain luminance for RGB | 38 | (1) | (1) | (1) | GY4 | GY3 | GY2 | GY1 | GY0 |
| Gain colour difference for RGB | 39 | (1) | (1) | (1) | GCD4 | GCD3 | GCD2 | GCD1 | GCD0 |
| Input port control 1 | 3A | CBENB | (1) | ${ }^{(1)}$ | SYMP | DEMOFF | CSYNC | Y2C | UV2C |
| VPS enable, input control 2 | 54 | VPSEN | ${ }^{(1)}$ | (1) | ${ }^{(1)}$ | ${ }^{(1)}$ | ${ }^{(1)}$ | EDGE2 | EDGE1 |
| VPS byte 5 | 55 | VPS57 | VPS56 | VPS55 | VPS54 | VPS53 | VPS52 | VPS51 | VPS50 |
| VPS byte 11 | 56 | VPS117 | VPS116 | VPS115 | VPS114 | VPS113 | VPS112 | VPS111 | VPS110 |
| VPS byte 12 | 57 | VPS127 | VPS126 | VPS125 | VPS124 | VPS123 | VPS122 | VPS121 | VPS120 |
| VPS byte 13 | 58 | VPS137 | VPS136 | VPS135 | VPS134 | VPS133 | VPS132 | VPS131 | VPS130 |
| VPS byte 14 | 59 | VPS147 | VPS146 | VPS145 | VPS144 | VPS143 | VPS142 | VPS141 | VPS140 |
| Chrominance phase | 5A | CHPS7 | CHPS6 | CHPS5 | CHPS4 | CHPS3 | CHPS2 | CHPS1 | CHPS0 |


| REGISTER FUNCTION |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Gain U | 5B | GAINU7 | GAINU6 | GAINU5 | GAINU4 | GAINU3 | GAINU2 | GAINU1 | GAINU0 |
| Gain V | 5C | GAINV7 | GAINV6 | GAINV5 | GAINV4 | GAINV3 | GAINV2 | GAINV1 | GAINV0 |
| Gain U MSB, black level | 5D | GAINU8 | (1) | BLCKL5 | BLCKL4 | BLCKL3 | BLCKL2 | BLCKL1 | BLCKL0 |
| Gain V MSB, blanking level | 5E | GAINV8 | (1) | BLNNL5 | BLNNL4 | BLNNL3 | BLNNL2 | BLNNL1 | BLNNL0 |
| CCR, blanking level VBI | 5F | CCRS1 | CCRS0 | BLNVB5 | BLNVB4 | BLNVB3 | BLNVB2 | BLNVB1 | BLNVB0 |
| Null | 60 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Standard control | 61 | DOWND | DOWNA | (1) | YGS | (1) | SCBW | PAL | FISE |
| Burst amplitude | 62 | (1) | BSTA6 | BSTA5 | BSTA4 | BSTA3 | BSTA2 | BSTA1 | BSTA0 |
| Subcarrier 0 | 63 | FSC07 | FSC06 | FSC05 | FSC04 | FSC03 | FSC02 | FSC01 | FSC00 |
| Subcarrier 1 | 64 | FSC15 | FSC14 | FSC13 | FSC12 | FSC11 | FSC10 | FSC09 | FSC08 |
| Subcarrier 2 | 65 | FSC23 | FSC22 | FSC21 | FSC20 | FSC19 | FSC18 | FSC17 | FSC16 |
| Subcarrier 3 | 66 | FSC31 | FSC30 | FSC29 | FSC28 | FSC27 | FSC26 | FSC25 | FSC24 |
| Line 21 odd 0 | 67 | L21007 | L21006 | L21005 | L21004 | L21003 | L21002 | L21001 | L21000 |
| Line 21 odd 1 | 68 | L21017 | L21016 | L21015 | L21014 | L21013 | L21012 | L21011 | L21010 |
| Line 21 even 0 | 69 | L21E07 | L21E06 | L21E05 | L21E04 | L21E03 | L21E02 | L21E01 | L21E00 |
| Line 21 even 1 | 6A | L21E17 | L21E16 | L21E15 | L21E14 | L21E13 | L21E12 | L21E11 | L21E10 |
| Null | 6B | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Trigger control | 6C | HTRIG7 | HTRIG6 | HTRIG5 | HTRIG4 | HTRIG3 | HTRIG2 | HTRIG1 | HTRIG0 |
| Trigger control | 6D | HTRIG10 | HTRIG9 | HTRIG8 | VTRIG4 | VTRIG3 | VTRIG2 | VTRIG1 | VTRIG0 |
| Multi control | 6E | (1) | BLCKON | PHRES1 | PHRES0 | LDEL1 | LDEL0 | FLC1 | FLC0 |
| Closed Caption, teletext enable | 6F | CCEN1 | CCEN0 | TTXEN | SCCLN4 | SCCLN3 | SCCLN2 | SCCLN1 | SCCLN0 |
| Active display window horizontal start | 70 | ADWHS7 | ADWHS6 | ADWHS5 | ADWHS4 | ADWHS3 | ADWHS2 | ADWHS1 | ADWHS0 |
| Active display window horizontal end | 71 | ADWHE7 | ADWHE6 | ADWHE5 | ADWHE4 | ADWHE3 | ADWHE2 | ADWHE1 | ADWHEO |
| MSBs ADWH | 72 | (1) | ADWHE10 | ADWHE9 | ADWHE8 | (1) | ADWHS10 | ADWHS9 | ADWHS8 |
| TTX request horizontal start | 73 | TTXHS7 | TTXHS6 | TTXHS5 | TTXHS4 | TTXHS3 | TTXHS2 | TTXHS1 | TTXHS0 |
| TTX request horizontal delay | 74 | (1) | (1) | (1) | (1) | TTXHD3 | TTXHD2 | TTXHD1 | TTXHD0 |
| CSYNC advance | 75 | CSYNCA4 | CSYNCA3 | CSYNCA2 | CSYNCA1 | CSYNCA0 | (1) | (1) | ${ }^{(1)}$ |
| TTX odd request vertical start | 76 | TTXOVS7 | TTXOVS6 | TTXOVS5 | TTXOVS4 | TTXOVS3 | TTXOVS2 | TTXOVS1 | TTXOVS0 |
| TTX odd request vertical end | 77 | TTXOVE7 | TTXOVE6 | TTXOVE5 | TTXOVE4 | TTXOVE3 | TTXOVE2 | TTXOVE1 | TTXOVE0 |
| TTX even request vertical start | 78 | TTXEVS7 | TTXEVS6 | TTXEVS5 | TTXEVS4 | TTXEVS3 | TTXEVS2 | TTXEVS1 | TTXEVS0 |


| REGISTER FUNCTION | SUB ADDR. <br> (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TTX even request vertical end | 79 | TTXEVE7 | TTXEVE6 | TTXEVE5 | TTXEVE4 | TTXEVE3 | TTXEVE2 | TTXEVE1 | TTXEVE0 |
| First active line | 7A | FAL7 | FAL6 | FAL5 | FAL4 | FAL3 | FAL2 | FAL1 | FALO |
| Last active line | 7B | LAL7 | LAL6 | LAL5 | LAL4 | LAL3 | LAL2 | LAL1 | LAL0 |
| TTX mode, MSB vertical | 7C | TTX60 | LAL8 | (1) | FAL8 | TTXEVE8 | TTXOVE8 | TTXEVS8 | TTXOVS8 |
| Null | 7D | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Disable TTX line | 7E | LINE12 | LINE11 | LINE10 | LINE9 | LINE8 | LINE7 | LINE6 | LINE5 |
| Disable TTX line | 7F | LINE20 | LINE19 | LINE18 | LINE17 | LINE16 | LINE15 | LINE14 | LINE13 |
| FIFO status (read only) | 80 | (1) | (1) | (1) | (1) | (1) | (1) | OVFL | UDFL |
| Pixel clock 0 | 81 | PCL07 | PCL06 | PCL05 | PCL04 | PCL03 | PCL02 | PCL01 | PCLO0 |
| Pixel clock 1 | 82 | PCL15 | PCL14 | PCL13 | PCL12 | PCL11 | PCL10 | PCL09 | PCL08 |
| Pixel clock 2 | 83 | PCL23 | PCL22 | PCL21 | PCL20 | PCL19 | PCL18 | PCL17 | PCL16 |
| Null | 84 to 8F | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Horizontal offset | 90 | XOFS7 | XOFS6 | XOFS5 | XOFS4 | XOFS3 | XOFS2 | XOFS1 | XOFS0 |
| Pixel number | 91 | XPIX7 | XPIX6 | XPIX5 | XPIX4 | XPIX3 | XPIX2 | XPIX1 | XPIX0 |
| Vertical offset odd | 92 | YOFSO7 | YOFSO6 | YOFSO5 | YOFSO4 | YOFSO3 | YOFSO2 | YOFSO1 | YOFSO0 |
| Vertical offset even | 93 | YOFSE7 | YOFSE6 | YOFSE5 | YOFSE4 | YOFSE3 | YOFSE2 | YOFSE1 | YOFSE0 |
| MSBs | 94 | YOFSE9 | YOFSE8 | YOFSO9 | YOFSO8 | XPIX9 | XPIX8 | XOFS9 | XOFS8 |
| Line number | 95 | YPIX7 | YPIX6 | YPIX5 | YPIX4 | YPIX3 | YPIX2 | YPIX1 | YPIX0 |
| Scaler CTRL, MCB YPIX | 96 | EFS | PCBN | SLAVE | ILC | YFIL | HSL | YPIX9 | YPIX8 |
| Sync control | 97 | HFS | VFS | OFS | PFS | OVS | PVS | OHS | PHS |
| Line length | 98 | HLEN7 | HLEN6 | HLEN5 | HLEN4 | HLEN3 | HLEN2 | HLEN1 | HLEN0 |
| Input delay, MSB line length | 99 | IDEL3 | IDEL2 | IDEL1 | IDEL0 | (1) | HLEN10 | HLEN9 | HLEN8 |
| Horizontal increment | 9A | XINC7 | XINC6 | XINC5 | XINC4 | XINC3 | XINC2 | XINC1 | XINC0 |
| Vertical increment | 9 B | YINC7 | YINC6 | YINC5 | YINC4 | YINC3 | YINC2 | YINC1 | YINC0 |
| MSBs vertical and horizontal increment | 9 C | YINC11 | YINC10 | YINC9 | YINC8 | XINC11 | XINC10 | XINC9 | XINC8 |
| Weighting factor odd | 9D | YIWGTO7 | YIWGTO6 | YIWGTO5 | YIWGTO4 | YIWGTO3 | YIWGTO2 | YIWGTO1 | YIWGTO0 |
| Weighting factor even | 9E | YIWGTE7 | YIWGTE6 | YIWGTE5 | YIWGTE4 | YIWGTE3 | YIWGTE2 | YIWGTE1 | YIWGTE0 |
| Weighting factor MSB | 9 F | YIWGTE11 | YIWGTE10 | YIWGTE9 | YIWGTE8 | YIWGTO11 | YIWGTO10 | YIWGTO9 | YIWGTO8 |
| Vertical line skip | A0 | YSKIP7 | YSKIP6 | YSKIP5 | YSKIP4 | YSKIP3 | YSKIP2 | YSKIP1 | YSKIP0 |
| Blank enable for NI-bypass, vertical line skip MSB | A1 | BLEN | (1) | (1) | (1) | YSKIP11 | YSKIP10 | YSKIP9 | YSKIP8 |


| REGISTER FUNCTION |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Border colour Y | A2 | BCY7 | BCY6 | BCY5 | BCY4 | BCY3 | BCY2 | BCY1 | BCYO |
| Border colour U | A3 | BCU7 | BCU6 | BCU5 | BCU4 | BCU3 | BCU2 | BCU1 | BCU0 |
| Border colour V | A4 | BCV7 | BCV6 | BCV5 | BCV4 | BCV3 | BCV2 | BCV1 | BCV0 |
| Cursor colour 1 R | F0 | CC1R7 | CC1R6 | CC1R5 | CC1R4 | CC1R3 | CC1R2 | CC1R1 | CC1R0 |
| Cursor colour 1 G | F1 | CC1G7 | CC1G6 | CC1G5 | CC1G4 | CC1G3 | CC1G2 | CC1G1 | CC1G0 |
| Cursor colour 1 B | F2 | CC1B7 | CC1B6 | CC1B5 | CC1B4 | CC1B3 | CC1B2 | CC1B1 | CC1B0 |
| Cursor colour 2 R | F3 | CC2R7 | CC2R6 | CC2R5 | CC2R4 | CC2R3 | CC2R2 | CC2R1 | CC2R0 |
| Cursor colour 2 G | F4 | CC2G7 | CC2G6 | CC2G5 | CC2G4 | CC2G3 | CC2G2 | CC2G1 | CC2G0 |
| Cursor colour 2 B | F5 | CC2B7 | CC2B6 | CC2B5 | CC2B4 | CC2B3 | CC2B2 | CC2B1 | CC2B0 |
| Auxiliary cursor colour R | F6 | AUXR7 | AUXR6 | AUXR5 | AUXR4 | AUXR3 | AUXR2 | AUXR1 | AUXR0 |
| Auxiliary cursor colour G | F7 | AUXG7 | AUXG6 | AUXG5 | AUXG4 | AUXG3 | AUXG2 | AUXG1 | AUXG0 |
| Auxiliary cursor colour B | F8 | AUXB7 | AUXB6 | AUXB5 | AUXB4 | AUXB3 | AUXB2 | AUXB1 | AUXB0 |
| Horizontal cursor position | F9 | XCP7 | XCP6 | XCP5 | XCP4 | XCP3 | XCP2 | XCP1 | XCP0 |
| Horizontal hot spot, MSB XCP | FA | XHS4 | XHS3 | XHS2 | XHS1 | XHSO | XCP10 | XCP9 | XCP8 |
| Vertical cursor position | FB | YCP7 | YCP6 | YCP5 | YCP4 | YCP3 | YCP2 | YCP1 | YCP0 |
| Vertical hot spot, MSB YCP | FC | YHS4 | YHS3 | YHS2 | YHS1 | YHSO | (1) | YCP9 | YCP8 |
| Input path control | FD | LUTOFF | CMODE | LUTL | IF2 | IF1 | IF0 | MATOFF | DFOFF |
| Cursor bit map | FE | RAM address (see Table 140) |  |  |  |  |  |  |  |
| Colour look-up table | FF | RAM address (see Table 141) |  |  |  |  |  |  |  |

1. All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

## PC-CODEC

### 18.1.1 $\quad{ }^{2} \mathrm{C}$-bus format

Table $67{ }^{2}$ ² C-bus write access to control registers; see Table 72

| S | 10001000 | A | SUBADDRESS | A | DATA 0 | A | ------- | DATA n | A |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Table $68{ }^{1}{ }^{2} \mathrm{C}$-bus write access to cursor bit map (subaddress FEH); see Table 72

| S | 10001000 | A | FEH | A | RAM ADDRESS | A | DATA 0 | A | ------ | DATA $n$ | A |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Table $69{ }^{1}{ }^{2} \mathrm{C}$-bus write access to colour look-up table (subaddress FFH); see Table 72

| S | 10001000 | A | FFH | A | RAM ADDRESS | A | DATA 0R | A | DATA 0G | A | DATA 0B | A | ------- |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Table $70{ }^{2}$ ²-bus read access to control registers; see Table 72

| S | 10001000 | A | SUBADDRESS | A | Sr | 10001001 | A | DATA 0 | Am | ------- | DATA $n$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Table $71 \mathrm{I}^{2} \mathrm{C}$-bus read access to cursor bit map or colour LUT; see Table 72


Table 72 Explanations of Tables 67 to 71

| CODE |  |
| :--- | :--- |
| S | START condition |
| Sr | repeated START condition |
| 1000100 X; note 1 | slave address |
| A | acknowledge generated by the slave |
| Am | acknowledge generated by the master |
| SUBADDRESS; note 2 | subaddress byte |
| DATA | data byte |
| ------- | continued data bytes and acknowledges |
| P | STOP condition |
| RAM ADDRESS | start address for RAM access |

## Notes

1. $X$ is the read/write control bit; $X=$ logic 0 is order to write; $X=$ logic 1 is order to read.
2. If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

### 18.1.2 SLAVE RECEIVER

Table 73 Subaddress 16H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| DACF | output level adjustment fine in $1 \%$ steps for all DACs; default after reset is 00 H ; see Table 74 |

Table 74 Fine adjustment of DAC output voltage

| BINARY | GAIN (\%) |
| :---: | :---: |
| 0111 | 7 |
| 0110 | 6 |
| 0101 | 5 |
| 0100 | 4 |
| 0011 | 3 |
| 0010 | 2 |
| 0001 | 1 |
| 0000 | 0 |
| 1000 | 0 |
| 1001 | -1 |
| 1010 | -2 |
| 1011 | -3 |
| 1100 | -4 |
| 1101 | -5 |
| 1110 | -6 |
| 1111 | -7 |

Table 75 Subaddresses 17H to 19H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| RDACC | output level coarse adjustment for RED DAC; default after reset is 1 BH for output of C signal <br> $00000 \mathrm{~b} \equiv 0.585 \mathrm{~V}$ to $11111 \mathrm{~b} \equiv 1.240 \mathrm{~V}$ at $37.5 \Omega$ nominal for full-scale conversion |
| GDACC | output level coarse adjustment for GREEN DAC; default after reset is 1 BH for output of VBS signal <br> $00000 \mathrm{~b} \equiv 0.585 \mathrm{~V}$ to $11111 \mathrm{~b} \equiv 1.240 \mathrm{~V}$ at $37.5 \Omega$ nominal for full-scale conversion |
| BDACC | output level coarse adjustment for BLUE DAC; default after reset is 1 FH for output of CVBS signal <br> $00000 \mathrm{~b} \equiv 0.585 \mathrm{~V}$ to $11111 \mathrm{~b} \equiv 1.240 \mathrm{~V}$ at $37.5 \Omega$ nominal for full-scale conversion |

Table 76 Subaddress 1AH

| DATA BYTE |  |
| :--- | :--- |
| MSMT | monitor sense mode threshold for DAC output voltage, should be set to 70 |

## PC-CODEC

Table 77 Subaddress 1BH

| DATA BYTE | LOGIC <br> LEVEL |  |
| :--- | :---: | :--- |
|  | 0 | monitor sense mode off; RCOMP, GCOMP and BCOMP bits are not valid; default after reset |
|  | 1 | monitor sense mode on |
| RCOMP <br> (read only) | 0 | check comparator at DAC on pin C8 is active, output is loaded |
| GCOMP <br> (read only) | 1 | check comparator at DAC on pin C8 is inactive, output is not loaded |
| BCOMP <br> (read only) | 0 | check comparator at DAC on pin C7 is active, output is loaded |
|  | 1 | check comparator at DAC on pin C7 is inactive, output is not loaded |
|  | 0 | check comparator at DAC on pin C6 is active, output is loaded |

Table 78 Subaddresses 26H and 27H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :---: | :---: | :---: |
| WSS | - | wide screen signalling bits <br> 3 to $0=$ aspect ratio <br> 7 to $4=$ enhanced services <br> 10 to $8=$ subtitles <br> 13 to 11 = reserved |
| WSSON | 0 | wide screen signalling output is disabled; default after reset |
|  | 1 | wide screen signalling output is enabled |

Table 79 Subaddress 28H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION | REMARKS |
| :--- | :---: | :--- | :--- |
| BS | - | starting point of burst in clock cycles | PAL: BS $=33(21 \mathrm{H}) ;$ default after reset if <br> strapping pin G 1 tied HIGH |
|  |  | NTSC: $\mathrm{BS}=25(19 \mathrm{H}) ;$ default after reset if <br> strapping pin G 1 tied LOW |  |

Table 80 Subaddress 29H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION | REMARKS |
| :--- | :---: | :--- | :--- |
| SRES | 0 | pin C3 accepts a teletext bit stream (TTX) | default after reset |
|  | 1 | pin C3 accepts a sync reset input (SRES) | a HIGH impulse resets synchronization of the <br> encoder (first field, first line) |
| BE | - | ending point of burst in clock cycles | PAL: BE $=29(1 \mathrm{DH}) ;$ default after reset if <br> strapping pin G1 tied HIGH |
|  |  | NTSC: BE $=29$ (1DH); default after reset if <br> strapping pin G1 tied LOW |  |

Table 81 Subaddresses 2AH to 2CH

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :--- | :---: | :--- |
| CG | - | LSB of the respective bytes are encoded immediately after run-in, the MSBs of the <br> respective bytes have to carry the CRCC bits, in accordance with the definition of copy <br> generation management system encoding format. |
| CGEN | 0 | copy generation data output is disabled; default after reset |
|  | 1 | copy generation data output is enabled |

Table 82 Subaddress 2DH

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :---: | :---: | :---: |
| VBSEN | 0 | pin C7 provides a component GREEN signal (CVBSEN1 = 0) or CVBS signal (CVBSEN1 = 1) |
|  | 1 | pin C7 provides a luminance (VBS) signal; default after reset |
| CVBSEN1 | 0 | pin C 7 provides a component GREEN (G) or luminance (VBS) signal; default after reset |
|  | 1 | pin C7 provides a CVBS signal |
| CVBSEN0 | 0 | pin C 6 provides a component BLUE (B) or colour difference BLUE $\left(\mathrm{C}_{\mathrm{B}}\right)$ signal |
|  | 1 | pin C6 provides a CVBS signal; default after reset |
| CEN | 0 | pin C8 provides a component RED (R) or colour difference RED ( $\mathrm{C}_{R}$ ) signal |
|  | 1 | pin C8 provides a chrominance signal (C) as modulated subcarrier for S-video; default after reset |
| ENCOFF | 0 | encoder is active; default after reset |
|  | 1 | encoder bypass, DACs are provided with RGB signal after cursor insertion block |
| CLK2EN | 0 | pin C4 provides a teletext request signal (TTXRQ) |
|  | 1 | pin C4 provides the buffered crystal clock divided by two ( 13.5 MHz ); default after reset |

Table 83 Subaddresses 38H and 39H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| GY4 to GY0 | Gain luminance of $R G B\left(C_{R}, Y\right.$ and $\left.C_{B}\right)$ output, ranging from $(1-16 / 32)$ to $(1+15 / 32)$. <br> Suggested nominal value $=0$, depending on external application. |
| GCD4 to GCD0 | Gain colour difference of $R G B\left(C_{R}, Y\right.$ Yand $\left.C_{B}\right)$ output, ranging from $(1-16 / 32)$ to $(1+15 / 32)$. <br> Suggested nominal value $=0$, depending on external application. |

## PC-CODEC

Table 84 Subaddress 3AH

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :---: | :---: | :---: |
| CBENB | 0 | data from input ports is encoded |
|  | 1 | colour bar with fixed colours is encoded |
| SYMP | 0 | horizontal and vertical trigger is taken from FSVGC or both VSVGC and HSVGC; default after reset |
|  | 1 | horizontal and vertical trigger is decoded out of "ITU-R BT.656" compatible data at PD port |
| DEMOFF | 0 | Y- $\mathrm{C}_{B}-\mathrm{C}_{R}$ to RGB dematrix is active; default after reset |
|  | 1 | $\mathrm{Y}-\mathrm{C}_{B}-\mathrm{C}_{\mathrm{R}}$ to RGB dematrix is bypassed |
| CSYNC | 0 | pin D8 provides a horizontal sync for non-interlaced VGA components output (at PIXCLK) |
|  | 1 | pin D8 provides a composite sync for interlaced components output (at XTAL clock) |
| Y2C | 0 | input luminance data is twos complement from PD input port |
|  | 1 | input luminance data is straight binary from PD input port; default after reset |
| UV2C | 0 | input colour difference data is twos complement from PD input port |
|  | 1 | input colour difference data is straight binary from PD input port; default after reset |

Table 85 Subaddress 54H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :--- | :---: | :--- |
| VPSEN | 0 | video programming system data insertion is disabled; default after reset |
|  | 1 | video programming system data insertion in line 16 is enabled |
| EDGE2 | 0 | internal PPD2 data is sampled on the rising clock edge |
|  | 1 | internal PPD2 data is sampled on the falling clock edge; see Tables 25 to 30; default after <br> reset |
| EDGE1 | 0 | internal PPD1 data is sampled on the rising clock edge; see Tables 25 to 30; default after <br> reset |
|  | 1 | internal PPD1 data is sampled on the falling clock edge |

Table 86 Subaddresses 55H to 59H

| DATA BYTE | DESCRIPTION | REMARKS |  |
| :--- | :--- | :--- | :---: |
| VPS5 | fifth byte of video programming system data | in line 16; LSB first; all other bytes are not |  |
| relevant for VPS |  |  |  |
| VPS11 | eleventh byte of video programming system data |  |  |
| VPS12 | twelfth byte of video programming system data |  |  |
| VPS13 | thirteenth byte of video programming system data |  |  |
| VPS14 | fourteenth byte of video programming system data |  |  |

## PC-CODEC

Table 87 Subaddress 5AH; note 1

| DATA BYTE | DESCRIPTION | VALUE |  |
| :--- | :--- | :---: | :--- |
| CHPS | phase of encoded colour subcarrier | 6 BH | PAL B/G and data from input ports in master mode |
|  | (including burst) relative to horizontal |  |  |
|  | sync; can be adjusted in steps of | 16 H | PAL B/G and data from look-up table |
|  | $360 / 256$ degrees | 25 H | NTSC M and data from input ports in master mode |
|  |  | 46 H | NTSC M and data from look-up table |

## Note

1. The default after reset is 00 H .

Table 88 Subaddresses 5BH and 5DH

| DATA BYTE | DESCRIPTION | CONDITIONS | REMARKS |
| :--- | :--- | :--- | :--- |
| GAINU | variable gain for <br> $\mathrm{C}_{\mathrm{B}}$ signal; input <br> representation in <br> accordance with <br> "ITU-R BT.601" | white-to-black $=92.5$ IRE | GAINU $=-2.17 \times$ nominal to $+2.16 \times$ nominal |
|  | GAINU $=0$ | GAINU $=118(76 \mathrm{H})$ | output subcarrier of $U$ contribution $=$ nominal |
|  |  | white-to-black $=100$ IRE | GAINU $=-2.05 \times$ nominal to $+2.04 \times$ nominal |
|  |  | GAINU $=0$ | output subcarrier of $U$ contribution $=0$ |
|  | GAINU $=125(7 \mathrm{DH})$ | output subcarrier of $U$ contribution $=$ nominal |  |

Table 89 Subaddresses 5CH and 5EH

| DATA BYTE | DESCRIPTION | CONDITIONS | REMARKS |
| :---: | :---: | :---: | :---: |
| GAINV | variable gain for $\mathrm{C}_{\mathrm{R}}$ signal; input representation in accordance with "ITU-R BT.601" | white-to-black = 92.5 IRE | GAINV $=-1.55 \times$ nominal to $+1.55 \times$ nominal |
|  |  | GAINV = 0 | output subcarrier of V contribution $=0$ |
|  |  | GAINV = 165 (A5H) | output subcarrier of V contribution $=$ nominal |
|  |  | white-to-black $=100$ IRE | GAINV $=-1.46 \times$ nominal to $+1.46 \times$ nominal |
|  |  | GAINV = 0 | output subcarrier of V contribution $=0$ |
|  |  | GAINV = 175 (AFH) | output subcarrier of V contribution $=$ nominal |

Table 90 Subaddress 5DH

| DATA BYTE | DESCRIPTION | CONDITIONS | REMARKS |
| :---: | :---: | :---: | :---: |
| BLCKL | variable black level; input representation in accordance with "ITU-R BT.601" | white-to-sync = 140 IRE; note 1 | recommended value: BLCKL = 58 (3AH) |
|  |  | BLCKL = 0; note 1 | output black level = 29 IRE |
|  |  | BLCKL = 63 (3FH); note 1 | output black level = 49 IRE |
|  |  | white-to-sync = 143 IRE; note 2 | recommended value: BLCKL = 51 (33H) |
|  |  | BLCKL = 0; note 2 | output black level = 27 IRE |
|  |  | BLCKL = 63 (3FH); note 2 | output black level = 47 IRE |

## Notes

1. Output black level/IRE $=B L C K L \times 2 / 6.29+28.9$.
2. Output black level/IRE $=$ BLCKL $\times 2 / 6.18+26.5$.

Table 91 Subaddress 5EH

| DATA BYTE | DESCRIPTION | CONDITIONS | REMARKS |
| :---: | :---: | :---: | :---: |
| BLNNL | variable blanking level | white-to-sync = 140 IRE; note 1 | recommended value: BLNNL = 46 (2EH) |
|  |  | BLNNL = 0; note 1 | output blanking level $=25$ IRE |
|  |  | BLNNL = 63 (3FH); note 1 | output blanking level = 45 IRE |
|  |  | white-to-sync = 143 IRE; note 2 | recommended value: BLNNL = 53 (35H) |
|  |  | BLNNL = 0; note 2 | output blanking level = 26 IRE |
|  |  | BLNNL = 63 (3FH); note 2 | output blanking level $=46$ IRE |

## Notes

1. Output black level/IRE $=B L N N L \times 2 / 6.29+25.4$.
2. Output black level/IRE $=B L N N L \times 2 / 6.18+25.9$; default after reset: 35 H .

Table 92 Subaddress 5FH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| CCRS | select cross-colour reduction filter in luminance; see Table 93 |
| BLNVB | variable blanking level during vertical blanking interval is typically identical to value of BLNNL |

Table 93 Logic levels and function of CCRS

| CCRS1 | CCRS0 | DESCRIPTION |
| :---: | :---: | :--- |
| 0 | 0 | no cross-colour reduction; for overall transfer characteristic of luminance see Fig.7 |
| 0 | 1 | cross-colour reduction \#1 active; for overall transfer characteristic see Fig.7 |
| 1 | 0 | cross-colour reduction \#2 active; for overall transfer characteristic see Fig.7 |
| 1 | 1 | cross-colour reduction \#3 active; for overall transfer characteristic see Fig.7 |

Table 94 Subaddress 61H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :--- | :---: | :--- |
|  | 0 | digital core in normal operational mode; default after reset |
|  | 1 | digital core in sleep mode and is reactivated with an ${ }^{2}$ C-bus address |
| DOWNA | 0 | DACs in normal operational mode; default after reset |
|  | 1 | DACs in Power-down mode |
|  | 0 | luminance gain for white - black 100 IRE |
|  | 1 | luminance gain for white - black 92.5 IRE including 7.5 IRE set-up of black |
| PAL | 0 | enlarged bandwidth for chrominance encoding (for overall transfer characteristic of <br> chrominance in baseband representation see Figs 5 and 6) |
|  | 1 | standard bandwidth for chrominance encoding (for overall transfer characteristic of <br> chrominance in baseband representation see Figs 5 and 6); default after reset |
| FISE | 0 | NTSC encoding (non-alternating V component) |
|  | 1 | PAL encoding (alternating V component) |
|  | 0 | 864 total pixel clocks per line |
|  | 1 | 858 total pixel clocks per line |

## PC-CODEC

Table 95 Subaddress 62H

| DATA BYTE | DESCRIPTION | CONDITIONS | REMARKS |
| :---: | :---: | :---: | :---: |
| BSTA | amplitude of colour burst; input representation in accordance with "ITU-R BT.601" | ```white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 2.02 }\times\mathrm{ nominal``` | recommended value: $\text { BSTA = } 63(3 \mathrm{FH})$ |
|  |  | white-to-black $=92.5$ IRE; burst = 40 IRE; PAL encoding BSTA $=0$ to $2.82 \times$ nominal | recommended value: $\text { BSTA = } 45 \text { (2DH) }$ |
|  |  | $\begin{array}{\|l} \hline \text { white-to-black }=100 \text { IRE; } \\ \text { burst }=43 \text { IRE; NTSC encoding } \\ \text { BSTA }=0 \text { to } 1.90 \times \text { nominal } \end{array}$ | recommended value: $\text { BSTA = } 67(43 \mathrm{H})$ |
|  |  | white-to-black $=100$ IRE; burst = 43 IRE; PAL encoding BSTA $=0$ to $3.02 \times$ nominal | recommended value: BSTA = 47 (2FH); default after reset |

Table 96 Subaddresses 63H to 66H (four bytes to program subcarrier frequency)

| DATA BYTE | DESCRIPTION | CONDITIONS | REMARKS |
| :--- | :--- | :---: | :---: |
| FSC0 to <br> FSC3 | $\mathrm{f}_{\text {fsc }}=$ subcarrier frequency <br> (in multiples of line <br> frequency); $f_{\\| l c}=$ clock <br> frequency (in multiples of <br> line frequency) | FSC $=$ round $\left(\frac{f_{\text {fsc }}}{f_{\text {IIc }}} \times 2^{32}\right) ;$ note 1 | FSC3 $=$ most significant byte; <br> FSC0 $=$ least significant byte |

## Note

1. Examples:
a) NTSC M: $\mathrm{f}_{\mathrm{fsc}}=227.5, \mathrm{f}_{\mathrm{llc}}=1716 \rightarrow \mathrm{FSC}=569408543$ (21F07C1FH).
b) PAL B/G: $\mathrm{f}_{\mathrm{fsc}}=283.7516, \mathrm{f}_{\| \mathrm{Cc}}=1728 \rightarrow \mathrm{FSC}=705268427(2 \mathrm{~A} 098 \mathrm{ACBH})$.

Table 97 Subaddresses 67H to 6AH

| DATA BYTE | DESCRIPTION | REMARKS |
| :---: | :---: | :---: |
| L2100 | first byte of captioning data, odd field | LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format. |
| L2101 | second byte of captioning data, odd field |  |
| L21E0 | first byte of extended data, even field |  |
| L21E1 | second byte of extended data, even field |  |

Table 98 Subaddresses 6CH and 6DH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| HTRIG | sets the horizontal trigger phase related to chip-internal horizontal input <br> values above 1715 (FISE $=1$ ) or 1727 (FISE $=0$ ) are not allowed; increasing HTRIG decreases <br> delays of all internally generated timing signals; the default value is 0 |

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Table 99 Subaddress 6DH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| VTRIG | sets the vertical trigger phase related to chip-internal vertical input <br> increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; <br> variation range of VTRIG $=0$ to $31(1 \mathrm{FH})$; the default value is 0 |

Table 100Subaddress 6EH

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :--- | :---: | :--- |
|  | 0 | encoder in normal operation mode; default after reset |
|  | 1 | output signal is forced to blanking level |
| PHRES | - | selects the phase reset mode of the colour subcarrier generator; see Table 101 |
| LDEL | - | selects the delay on luminance path with reference to chrominance path; see Table 102 |
| FLC | - | field length control; see Table 103 |

Table 101 Logic levels and function of PHRES

| DATA BYTE |  |  |
| :---: | :---: | :--- | :--- |
| PHRES1 | PHRESO |  |
| 0 | 0 | no subcarrier reset |
| 0 | 1 | subcarrier reset every two lines |
| 1 | 0 | subcarrier reset every eight fields |
| 1 | 1 | subcarrier reset every four fields |

Table 102 Logic levels and function of LDEL

| DATA BYTE |  |  |
| :---: | :---: | :--- |
| LDEL1 | LDELO |  |
| 0 | 0 | no luminance delay; default after reset |
| 0 | 1 | 1 LLC luminance delay |
| 1 | 0 | 2 LLC luminance delay |
| 1 | 1 | 3 LLC luminance delay |

Table 103 Logic levels and function of FLC

| DATA BYTE |  |  |
| :---: | :---: | :--- |
| FLC1 | FLCO |  |
| 0 | 0 | interlaced 312.5 lines/field at $50 \mathrm{~Hz}, 262.5$ lines/field at 60 Hz ; default after reset |
| 0 | 1 | non-interlaced 312 lines/field at $50 \mathrm{~Hz}, 262$ lines/field at 60 Hz |
| 1 | 0 | non-interlaced 313 lines/field at $50 \mathrm{~Hz}, 263$ lines/field at 60 Hz |
| 1 | 1 | non-interlaced 313 lines/field at $50 \mathrm{~Hz}, 263$ lines/field at 60 Hz |

## PC-CODEC

Table 104 Subaddress 6FH

| DATA <br> BYTE | LOGIC <br> LEVEL |  |
| :--- | :---: | :--- |
| CCEN | - | enables individual line 21 encoding; see Table 105 |
| TTXEN | 0 | disables teletext insertion; default after reset |
|  | 1 | enables teletext insertion |
| SCCLN | - | selects the actual line, where Closed Caption or extended data are encoded; <br> line $=($ SCCLN +4$)$ for M-systems; line $=($ SCCLN +1$)$ for other systems |

Table 105 Logic levels and function of CCEN

| DATA BYTE |  |  |
| :---: | :---: | :--- |
| CCEN1 | CCENO |  |
| 0 | 0 | line 21 encoding off; default after reset |
| 0 | 1 | enables encoding in field 1 (odd) |
| 1 | 0 | enables encoding in field 2 (even) |
| 1 | 1 | enables encoding in both fields |

Table 106 Subaddresses 70 H to 72 H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| ADWHS | active display window horizontal start; defines the start of the active TV display portion after <br> the border colour <br> values above 1715 (FISE $=1)$ or $1727($ FISE $=0)$ are not allowed |
| ADWHE | active display window horizontal end; defines the end of the active TV display portion before <br> the border colour <br> values above 1715 (FISE $=1)$ or $1727($ FISE $=0)$ are not allowed |

Table 107 Subaddress 73H

| DATA BYTE | DESCRIPTION | REMARKS |
| :--- | :--- | :--- |
| TTXHS | start of signal TTXRQ on pin TTXRQ_XCLKO2 <br> (CLK2EN = 0); see Fig.50 | TTXHS $=42 \mathrm{H}$; is default after <br> reset if strapped to PAL |
|  |  | TTXHS $=54 \mathrm{H}$; is default after <br> reset if strapped to NTSC |

Table 108 Subaddress 74H

| DATA BYTE | DESCRIPTION | REMARKS |
| :--- | :--- | :--- |
| TTXHD | indicates the delay in clock cycles between rising edge <br> of TTXRQ output signal on pin TTXRQ_XCLKO2 <br> (CLK2EN = 0) and valid data at pin TTX_SRES | minimum value: TTXHD = 2; is <br> default after reset |

Table 109 Subaddress 75H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| CSYNCA | advanced composite sync against RGB output from 0 XTAL clocks to 31 XTAL clocks |

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Table 110 Subaddresses 76H, 77H and 7CH

| DATA BYTE | DESCRIPTION | REMARKS |
| :---: | :---: | :---: |
| TTXOVS | first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN $=0$ ) in odd field <br> line $=($ TTXOVS +4$)$ for M-systems <br> line $=($ TTXOVS +1$)$ for other systems | TTXOVS $=05 \mathrm{H}$; is default after reset if strapped to PAL TTXOVS $=06 \mathrm{H}$; is default after reset if strapped to NTSC |
| TTXOVE | last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN $=0$ ) in odd field $\begin{aligned} & \text { line }=(\text { TTXOVE }+3) \text { for M-systems } \\ & \text { line }=\text { TTXOVE for other systems } \end{aligned}$ | TTXOVE $=16 \mathrm{H}$; is default after reset if strapped to PAL TTXOVE $=10 \mathrm{H}$; is default after reset if strapped to NTSC |

Table 111 Subaddresses 78H, 79H and 7CH

| DATA BYTE | DESCRIPTION | REMARKS |
| :--- | :--- | :--- |
| TTXEVS | first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 <br> $($ CLK2EN $=0)$ in even field <br> line $=($ TTXEVS +4$)$ for M-systems <br> line $=($ TTXEVS +1$)$ for other systems | TTXEVS $=04 \mathrm{H} ;$ is default after <br> reset if strapped to PAL <br> TTXEVS $=05 \mathrm{H} ;$ is default after <br> reset if strapped to NTSC |
| TTXEVE | last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 <br> (CLK2EN $=0)$ in even field <br> line $=($ TTXEVE +3$)$ for M-systems <br> line $=$ TTXEVE for other systems | TTXEVE $=16 \mathrm{H} ;$ is default after <br> reset if strapped to PAL <br> TTXEVE $=10 \mathrm{H} ;$ is default after <br> reset if strapped to NTSC |

Table 112 Subaddresses 7AH to 7CH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| FAL | first active line $=\mathrm{FAL}+4$ for M -systems and FAL +1 for other systems, measured in lines <br> FAL $=0$ coincides with the first field synchronization pulse |
| LAL | last active line $=\mathrm{LAL}+3$ for M -systems and LAL for other system, measured in lines <br> LAL $=0$ coincides with the first field synchronization pulse |

Table 113 Subaddress 7CH

| DATA BYTE | LOGIC <br> LEVEL |  |
| :--- | :---: | :--- |
| TTX60 | 0 | enables NABTS (FISE $=1$ ) or European TTX (FISE $=0)$; default after reset |
|  | 1 | enables world standard teletext $60 \mathrm{~Hz}($ FISE $=1)$ |

Table 114 Subaddresses 7EH and 7FH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| LINE | individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective <br> bits, disabled line = LINExx (50 Hz field rate) <br> this bit mask is effective only if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE |

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Table 115 Subaddresses 81H to 83H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| PCL | defines the frequency of the synthesized pixel clock PIXCLKO; <br> $f_{\text {PIXCLK }}=\left(\frac{P C L}{2^{24}} \times f_{X T A L}\right) \times 8 ; f_{X T A L}=27 \mathrm{MHz}$ nominal, e.g. $640 \times 480$ to NTSC M: PCL $=20 \mathrm{~F} 63 \mathrm{BH} ;$ <br>  <br>  <br> $640 \times 480$ to PAL $\mathrm{B} / \mathrm{G}: ~ P C L=1 B 5 A 73 H$ (as by strapping pins) |

Table 116 Subaddresses 90 H and 94 H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| XOFS | horizontal offset; defines the number of PIXCLKs from horizontal sync (HSVGC) output to composite <br> blanking $(\overline{\mathrm{CBO}})$ output |

Table 117 Subaddresses 91H and 94H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| XPIX | pixel in $X$ direction; defines half the number of active pixels per input line (identical to the length of <br> CBO pulses) |

Table 118 Subaddresses 92H and 94H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| YOFSO | vertical offset in odd field; defines (in the odd field) the number of lines from VSVGC to first line with <br> active $\overline{\mathrm{CBO}}$; if no LUT data is requested, the first active $\overline{\mathrm{CBO}}$ will be output at YOFSO + 2; usually, <br> YOFSO = YOFSE with the exception of extreme vertical downscaling and interlacing |

Table 119 Subaddresses 93H and 94H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| YOFSE | vertical offset in even field; defines (in the even field) the number of lines from VSVGC to first line with <br> active $\overline{\text { CBO }}$; if no LUT data is requested, the first active $\overline{\text { CBO }}$ will be output at YOFSE $+2 ;$ usually, <br> YOFSE $=$ YOFSO with the exception of extreme vertical downscaling and interlacing |

Table 120 Subaddresses 95 H and 96 H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| YPIX | defines the number of requested input lines from the feeding device; <br> number of requested lines $=$ YPIX + YOFSE - YOFSO |

Table 121 Subaddress 96H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :--- | :---: | :--- |
|  | 0 | frame sync signal at pin FSVGC ignored in slave mode |
|  | 1 | frame sync signal at pin FSVGC accepted in slave mode |
| PCBN | 0 | normal polarity of $\overline{\text { CBO }}$ signal (HIGH during active video) |
|  | 1 | inverted polarity of $\overline{\text { CBO }}$ signal (LOW during active video) |
| SLAVE | 0 | the SAA7108E; SAA7109E is timing master to the graphics controller |
|  | 1 | the SAA7108E; SAA7109E is timing slave to the graphics controller |


| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :--- | :---: | :--- |
|  | 0 | if hardware cursor insertion is active, set LOW for non-interlaced input signals |
|  | 1 | if hardware cursor insertion is active, set HIGH for interlaced input signals |
| YFIL | 0 | luminance sharpness booster disabled |
|  | 1 | luminance sharpness booster enabled |
|  | 0 | normal trigger event handling of the horizontal state machine, if the SAA7108E; <br> SAA7109E is slave to HSVGC input |
|  | 1 | trigger event for horizontal state machine is shifted 128 PIXCLKs in advance, adapted <br> to a late HSVGC in slave mode |

Table 122 Subaddress 97H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :---: | :---: | :---: |
| HFS | 0 | horizontal sync is directly derived from input signal (slave mode) at pin HSVGC |
|  | 1 | horizontal sync is derived from a frame sync signal (slave mode) at pin FSVGC (only if EFS is set HIGH) |
| VFS | 0 | vertical sync (field sync) is directly derived from input signal (slave mode) at pin VSVGC |
|  | 1 | vertical sync (field sync) is derived from a frame sync signal (slave mode) at pin FSVGC (only if EFS is set HIGH) |
| OFS | 0 | pin FSVGC is switched to input |
|  | 1 | pin FSVGC is switched to active output |
| PFS | 0 | polarity of signal at pin FSVGC in output mode (master mode) is active HIGH; rising edge of the input signal is used in slave mode |
|  | 1 | polarity of signal at pin FSVGC in output mode (master mode) is active LOW; falling edge of the input signal is used in slave mode |
| OVS | 0 | pin VSVGC is switched to input |
|  | 1 | pin VSVGC is switched to active output |
| PVS | 0 | polarity of signal at pin VSVGC in output mode (master mode) is active HIGH; rising edge of the input signal is used in slave mode |
|  | 1 | polarity of signal at pin VSVGC in output mode (master mode) is active LOW; falling edge of the input signal is used in slave mode |
| OHS | 0 | pin HSVGC is switched to input |
|  | 1 | pin HSVGC is switched to active output |
| PHS | 0 | polarity of signal at pin HSVGC in output mode (master mode) is active HIGH; rising edge of the input signal is used in slave mode |
|  | 1 | polarity of signal at pin HSVGC in output mode (master mode) is active LOW; falling edge of the input signal is used in slave mode |

Table 123 Subaddresses 98H and 99H

| DATA BYTE |  |
| :--- | :--- |
| HLEN | horizontal length; HLEN $=\frac{\text { number of PIXCLKs }}{\text { line }}-1$ |

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Table 124 Subaddress 99H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| IDEL | input delay; defines the distance in PIXCLKs between the active edge of $\overline{\text { CBO }}$ and the first received <br> valid pixel |

Table 125 Subaddresses 9AH and 9CH

| DATA BYTE | DESCRIPTION |
| :--- | :---: |
| XINC | incremental fraction of the horizontal scaling engine; XINC $=\frac{\frac{\text { number of output pixels }}{\text { line }}}{\frac{\text { number of input pixels }}{\text { line }}} \times 4096$ |

Table 126 Subaddresses 9BH and 9CH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| YINC | incremental fraction of the vertical scaling engine; YINC $=\frac{\text { number of active output lines }}{\text { number of active input lines }} \times 4096$ |

Table 127 Subaddresses 9DH and 9FH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| YIWGTO | weighting factor for the first line of the odd field; YIWGTO $=\frac{\text { YINC }}{2}+2048$ |

Table 128 Subaddresses 9EH and 9FH

| DATA BYTE | DESCRIPTION |
| :--- | :---: |
| YIWGTE | weighting factor for the first line of the even field; YIWGTE $=\frac{\text { YINC }- \text { YSKIP }}{2}$ |

Table 129 Subaddresses A0H and A1H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| YSKIP | vertical line skip; defines the effectiveness of the anti-flicker filter; YSKIP $=0$ : most effective; <br> YSKIP $=4095:$ anti-flicker filter switched off |

Table 130 Subaddress A1H

| DATA BYTE | LOGIC <br> LEVEL |  |
| :--- | :---: | :--- |
| BLEN | 0 | no internal blanking for non-interlaced graphics in bypass mode; default after reset |
|  | 1 | forced internal blanking for non-interlaced graphics in bypass mode |

Table 131 Subaddresses A2H to A4H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| BCY, BCU <br> and BCV | luminance and colour difference portion of border colour in underscan area |

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Table 132 Subaddresses FOH to F2H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| CC1R, CC1G <br> and CC1B | RED, GREEN and BLUE portion of first cursor colour |

Table 133 Subaddresses F3H to F5H

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| CC2R, CC2G <br> and CC2B | RED, GREEN and BLUE portion of second cursor colour |

Table 134 Subaddresses F6H to F8H

| DATA BYTE | DESCRIPTION |
| :---: | :---: |
| AUXR, AUXG <br> and AUXB | RED, GREEN and BLUE portion of auxiliary cursor colour |

Table 135 Subaddresses F9H and FAH

| DATA BYTE |  | DESCRIPTION |
| :--- | :--- | :--- |
| XCP | horizontal cursor position |  |

Table 136 Subaddress FAH

| DATA BYTE |  | DESCRIPTION |
| :--- | :--- | :--- |
| XHS | horizontal hot spot of cursor |  |

Table 137 Subaddresses FBH and FCH

| DATA BYTE |  |
| :--- | :--- |
| YCP | vertical cursor position |

Table 138 Subaddress FCH

| DATA BYTE |  |
| :--- | :--- |
| YHS | vertical hot spot of cursor |

Table 139 Subaddress FDH

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :---: | :---: | :---: |
| LUTOFF | 0 | colour look-up table is active |
|  | 1 | colour look-up table is bypassed |
| CMODE | 0 | cursor mode; input colour will be inverted |
|  | 1 | auxiliary cursor colour will be inserted |
| LUTL | 0 | LUT loading via input data stream is inactive |
|  | 1 | colour and cursor LUTs are loaded via input data stream |
| IF | 0 | input format is $8+8+8$ bit $4: 4: 4$ non-interlaced RGB or $\mathrm{C}_{B}-Y$ - $\mathrm{C}_{R}$ |
|  | 1 | input format is $5+5+5$ bit $4: 4: 4$ non-interlaced RGB |
|  | 2 | input format is $5+6+5$ bit $4: 4: 4$ non-interlaced RGB |
|  | 3 | input format is $8+8+8$ bit $4: 2: 2$ non-interlaced $C_{B}-Y-C_{R}$ |
|  | 4 | input format is $8+8+8$ bit $4: 2: 2$ interlaced $\mathrm{C}_{\mathrm{B}}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ (ITU-R BT.656, 27 MHz clock) (in subaddresses 91 H and 94 H set XPIX = number of active pixels/line) |
|  | 5 | input format is 8-bit non-interlaced index colour |
|  | 6 | input format is $8+8+8$ bit $4: 4: 4$ non-interlaced $R G B$ or $\mathrm{C}_{B}-\mathrm{Y}-\mathrm{C}_{\mathrm{R}}$ (special bit ordering) |
| MATOFF | 0 | RGB to $C_{R}-Y-C_{B}$ matrix is active |
|  | 1 | RGB to $\mathrm{C}_{\mathrm{R}}-\mathrm{Y}-\mathrm{C}_{\mathrm{B}}$ matrix is bypassed |
| DFOFF | 0 | down formatter (4:4:4 to $4: 2: 2)$ in input path is active |
|  | 1 | down formatter is bypassed |

Table 140 Subaddress FEH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| CURSA | RAM start address for cursor bit map; the byte following subaddress FEH points to the first cell to be <br> loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop <br> condition |

Table 141 Subaddress FFH

| DATA BYTE | DESCRIPTION |
| :--- | :--- |
| COLSA | RAM start address for colour LUT; the byte following subaddress FFH points to the first cell to be <br> loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop <br> condition |

In subaddresses 5BH, 5CH, 5DH, 5EH and 62H all IRE values are rounded up.

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### 18.1.3 SLAVE TRANSMITTER

Table 142 Slave transmitter (slave address 89H)

| REGISTER FUNCTION | SUBADDRESS | DATA BYTE |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Status byte | 00H | VER2 | VER1 | VER0 | CCRDO | CCRDE | 0 | FSEQ | O_E |
| Chip ID | 1 CH | CID7 | CID6 | CID5 | CID4 | CID3 | CID2 | CID1 | CID0 |
| FIFO status | 80H | 0 | 0 | 0 | 0 | 0 | 0 | OVFL | UDFL |

Table 143 Subaddress 00H

| DATA BYTE | LOGIC LEVEL | DESCRIPTION |
| :---: | :---: | :---: |
| VER | - | version identification of the device: it will be changed with all versions of the IC that have different programming models; current version is 010 binary |
| CCRDO | 1 | Closed Caption bytes of the odd field have been encoded |
|  | 0 | the bit is reset after information has been written to the subaddresses 67 H and 68 H ; it is set immediately after the data has been encoded |
| CCRDE | 1 | Closed Caption bytes of the even field have been encoded |
|  | 0 | the bit is reset after information has been written to the subaddresses 69H and 6AH; it is set immediately after the data has been encoded |
| FSEQ | 1 | during first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields) |
|  | 0 | not first field of a sequence |
| O_E | 1 | during even field |
|  | 0 | during odd field |

Table 144 Subaddress 1CH

| DATA BYTE |  |
| :--- | :--- |
| DESCRIPTION |  |

Table 145 Subaddress 80H

| DATA BYTE | LOGIC <br> LEVEL | DESCRIPTION |
| :--- | :---: | :--- |
| OVFL | 0 | no FIFO overflow |
|  | 1 | FIFO overflow has occurred; this bit is reset after this subaddress has been read |
| UDFL | 0 | no FIFO underflow |
|  | 1 | FIFO underflow has occurred; this bit is reset after this subaddress has been read |

## PC-CODEC

### 18.2 Digital video decoder part

### 18.2.1 $\quad{ }^{2} \mathrm{C}$-BUS FORMAT


a. Write procedure.

b. Read procedure (combined).

Fig. $56 \mathrm{I}^{2} \mathrm{C}$-bus format.

Table 146 Description of $\mathrm{I}^{2} \mathrm{C}$-bus format; note 1

| CODE | DESCRIPTION |
| :--- | :--- |
| S | START condition |
| Sr | repeated START condition |
| SLAVE ADDRESS W | '0100 0010' (42H, default) or ‘0100 0000 ' (40H; note 2) |
| SLAVE ADDRESS R | '0100 0011' (43H, default) or ‘0100 0001’ (41H; note 2) |
| ACK-s | acknowledge generated by the slave |
| ACK-m | acknowledge generated by the master |
| SUBADDRESS | subaddress byte; see Tables 147 and 148 |
| DATA | data byte; see Table 148 ; if more than one byte DATA is transmitted the subaddress pointer is <br> automatically incremented |
| P | STOP condition |
| X | read/write control bit (LSB slave address); $\mathrm{X}=0$, order to write (the circuit is slave receiver); <br> $\mathrm{X}=1$, order to read (the circuit is slave transmitter) |

## Notes

1. The SAA7108E; SAA7109E supports the 'fast mode' $I^{2} \mathrm{C}$-bus specification extension (data rate up to $400 \mathrm{kbits} / \mathrm{s}$ ).
2. If pin RTCO strapped to $\mathrm{V}_{\text {DDD }}$ via a $3.3 \mathrm{k} \Omega$ resistor.

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Table 147 Subaddress description and access

| SUBADDRESS | DESCRIPTION | ACCESS (READ/WRITE) |
| :---: | :---: | :---: |
| 00H | chip version | read only |
| FOH to FFH | reserved | - |
| Video decoder: 01H to 2FH |  |  |
| 01H to 05H | front-end part | read and write |
| 06 H to 19H | decoder part | read and write |
| 1 AH to 1EH | reserved | - |
| 1FH | video decoder status byte | read only |
| 20H to 2FH | reserved | - |
| Audio clock generation: 30H to 3FH |  |  |
| 30H to 3AH | audio clock generator | read and write |
| 3BH to 3FH | reserved | - |
| General purpose VBI-data slicer: 40H to 7FH |  |  |
| 40H to 5EH | VBI data slicer | read and write |
| 5FH | reserved | - |
| 60 H to 62H | VBI data slicer status | read only |
| 63 H to 7FH | reserved | - |
| X port, I port and the scaler: 80 H to EFH |  |  |
| 80 H to 8FH | task independent global settings | read and write |
| 90H to BFH | task A definition | read and write |
| COH to EFH | task B definition | read and write |

Table $148 \mathrm{I}^{2} \mathrm{C}$-bus receiver/transmitter overview

| REGISTER FUNCTION |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Chip version: register 00H |  |  |  |  |  |  |  |  |  |
| Chip version (read only) | 00 | ID7 | ID6 | ID5 | ID4 | - | - | - | - |
| Video decoder: registers 01H to 2FH |  |  |  |  |  |  |  |  |  |
| FRONT-END PART: REGISTERS 01H TO 05H |  |  |  |  |  |  |  |  |  |
| Increment delay | 01 | (1) | (1) | (1) | (1) | IDEL3 | IDEL2 | IDEL1 | IDEL0 |
| Analog input control 1 | 02 | FUSE1 | FUSE0 | GUDL1 | GUDL0 | MODE3 | MODE2 | MODE1 | MODE0 |
| Analog input control 2 | 03 | (1) | HLNRS | VBSL | WPOFF | HOLDG | GAFIX | GAI28 | GAI18 |
| Analog input control 3 | 04 | GAl17 | GAI16 | GAI15 | GAI14 | GAI13 | GAl12 | GAl11 | GAI10 |
| Analog input control 4 | 05 | GAI27 | GAI26 | GAI25 | GAI24 | GAI23 | GAI22 | GAI21 | GAI20 |
| Decoder part: REGISters 06H To 2FH |  |  |  |  |  |  |  |  |  |
| Horizontal sync start | 06 | HSB7 | HSB6 | HSB5 | HSB4 | HSB3 | HSB2 | HSB1 | HSB0 |
| Horizontal sync stop | 07 | HSS7 | HSS6 | HSS5 | HSS4 | HSS3 | HSS2 | HSS1 | HSS0 |
| Sync control | 08 | AUFD | FSEL | FOET | HTC1 | HTC0 | HPLL | VNOI1 | VNOIO |
| Luminance control | 09 | BYPS | YCOMB | LDEL | LUBW | LUFI3 | LUFI2 | LUFI1 | LUFIO |
| Luminance brightness control | OA | DBRI7 | DBRI6 | DBRI5 | DBRI4 | DBRI3 | DBRI2 | DBRI1 | DBRI0 |
| Luminance contrast control | OB | DCON7 | DCON6 | DCON5 | DCON4 | DCON3 | DCON2 | DCON1 | DCON0 |
| Chrominance saturation control | OC | DSAT7 | DSAT6 | DSAT5 | DSAT4 | DSAT3 | DSAT2 | DSAT1 | DSAT0 |
| Chrominance hue control | OD | HUEC7 | HUEC6 | HUEC5 | HUEC4 | HUEC3 | HUEC2 | HUEC1 | HUEC0 |
| Chrominance control 1 | OE | CDTO | CSTD2 | CSTD1 | CSTD0 | DCVF | FCTC | (1) | CCOMB |
| Chrominance gain control | OF | ACGC | CGAIN6 | CGAIN5 | CGAIN4 | CGAIN3 | CGAIN2 | CGAIN1 | CGAIN0 |
| Chrominance control 2 | 10 | OFFU1 | OFFU0 | OFFV1 | OFFV0 | CHBW | LCBW2 | LCBW1 | LCBW0 |
| Mode/delay control | 11 | COLO | RTP1 | HDEL1 | HDEL0 | RTP0 | YDEL2 | YDEL1 | YDEL0 |
| RT signal control | 12 | RTSE13 | RTSE12 | RTSE11 | RTSE10 | RTSE03 | RTSE02 | RTSE01 | RTSE00 |
| RT/X port output control | 13 | RTCE | XRHS | XRVS1 | XRVS0 | HLSEL | OFTS2 | OFTS1 | OFTS0 |
| Analog/ADC/compatibility control | 14 | CM99 | UPTCV | AOSL1 | AOSLO | XTOUTE | OLDSB | APCK1 | APCK0 |
| VGATE start, FID change | 15 | VSTA7 | VSTA6 | VSTA5 | VSTA4 | VSTA3 | VSTA2 | VSTA1 | VSTA0 |
| VGATE stop | 16 | VSTO7 | VSTO6 | VSTO5 | VSTO4 | VSTO3 | VSTO2 | VSTO1 | VSTO0 |


| REGISTER FUNCTION |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Miscellaneous, VGATE configuration and MSBs | 17 | LLCE | LLC2E | (1) | (1) | (1) | VGPS | VSTO8 | VSTA8 |
| Raw data gain control | 18 | RAWG7 | RAWG6 | RAWG5 | RAWG4 | RAWG3 | RAWG2 | RAWG1 | RAWG0 |
| Raw data offset control | 19 | RAWO7 | RAWO6 | RAWO5 | RAWO4 | RAWO3 | RAWO2 | RAWO1 | RAWO0 |
| Reserved | 1A to 1E | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Status byte video decoder (read only, OLDSB = 0) | 1F | INTL | HLVLN | FIDT | GLIMT | GLIMB | WIPA | COPRO | RDCAP |
| Status byte video decoder (read only, OLDSB = 1) | 1F | INTL | HLCK | FIDT | GLIMT | GLIMB | WIPA | SLTCA | CODE |
| Reserved | 20 to 2F | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Audio clock generator part: registers 30H to 3FH |  |  |  |  |  |  |  |  |  |
| Audio master clock cycles per field | 30 | ACPF7 | ACPF6 | ACPF5 | ACPF4 | ACPF3 | ACPF2 | ACPF1 | ACPF0 |
|  | 31 | ACPF15 | ACPF14 | ACPF13 | ACPF12 | ACPF11 | ACPF10 | ACPF9 | ACPF8 |
|  | 32 | (1) | (1) | (1) | (1) | (1) | (1) | ACPF17 | ACPF16 |
| Reserved | 33 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Audio master clock nominal increment | 34 | ACNI7 | ACNI6 | ACNI5 | ACNI4 | ACNI3 | ACNI2 | ACNI1 | ACNIO |
|  | 35 | ACNI15 | ACNI14 | ACNI13 | ACNI12 | ACNI11 | ACNI10 | ACNI9 | ACNI8 |
|  | 36 | (1) | (1) | ACNI21 | ACNI20 | ACNI19 | ACN118 | ACNI17 | ACNI16 |
| Reserved | 37 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | ${ }^{(1)}$ |
| Clock ratio AMXCLK to ASCLK | 38 | (1) | (1) | SDIV5 | SDIV4 | SDIV3 | SDIV2 | SDIV1 | SDIV0 |
| Clock ratio ASCLK to ALRCLK | 39 | (1) | (1) | LRDIV5 | LRDIV4 | LRDIV3 | LRDIV2 | LRDIV1 | LRDIV0 |
| Audio clock generator basic setup | 3A | (1) | (1) | (1) | (1) | APLL | AMVR | LRPH | SCPH |
| Reserved | 3B to 3F | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| General purpose VBI-data slicer part: registers 40H to 7FH |  |  |  |  |  |  |  |  |  |
| Slicer control 1 | 40 | (1) | HAM_N | FCE | HUNT_N | (1) | (1) | (1) | (1) |
| LCR2 to LCR24 ( $\mathrm{n}=2$ to 24) | 41 to 57 | LCRn_7 | LCRn_6 | LCRn_5 | LCRn_4 | LCRn_3 | LCRn_2 | LCRn_1 | LCRn_0 |
| Programmable framing code | 58 | FC7 | FC6 | FC5 | FC4 | FC3 | FC2 | FC1 | FC0 |


| REGISTER FUNCTION | SUB ADDR. (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Horizontal offset for slicer | 59 | HOFF7 | HOFF6 | HOFF5 | HOFF4 | HOFF3 | HOFF2 | HOFF1 | HOFF0 |
| Vertical offset for slicer | 5A | VOFF7 | VOFF6 | VOFF5 | VOFF4 | VOFF3 | VOFF2 | VOFF1 | VOFF0 |
| Field offset and MSBs for horizontal and vertical offset | 5B | FOFF | RECODE | (1) | VOFF8 | (1) | HOFF10 | HOFF9 | HOFF8 |
| Reserved (for testing) | 5C | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Header and data identification (DID) code control | 5D | FVREF | (1) | DID5 | DID4 | DID3 | DID2 | DID1 | DID0 |
| Sliced data identification (SDID) code | 5E | (1) | (1) | SDID5 | SDID4 | SDID3 | SDID2 | SDID1 | SDID0 |
| Reserved | 5F | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Slicer status byte 0 (read only) | 60 | - | FC8V | FC7V | VPSV | PPV | CCV | - | - |
| Slicer status byte 1 (read only) | 61 | - | - | F21_N | LN8 | LN7 | LN6 | LN5 | LN4 |
| Slicer status byte 2 (read only) | 62 | LN3 | LN2 | LN1 | LN0 | DT3 | DT2 | DT1 | DT0 |
| Reserved | 63 to 7F | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| X port, I port and the scaler part: registers 80H to EFH |  |  |  |  |  |  |  |  |  |
| TASK INDEPENDENT GLOBAL SETTINGS: 80H To 8FH |  |  |  |  |  |  |  |  |  |
| Global control 1 | 80 | (1) | SMOD | TEB | TEA | ICKS3 | ICKS2 | ICKS1 | ICKS0 |
| Reserved | $\begin{gathered} 81 \text { and } \\ 82 \end{gathered}$ | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| X port I/O enable and output clock phase control | 83 | (1) | (1) | XPCK1 | XPCK0 | (1) | XRQT | XPE1 | XPE0 |
| I port signal definitions | 84 | IDG01 | IDG00 | IDG11 | IDG10 | IDV1 | IDV0 | IDH1 | IDH0 |
| I port signal polarities | 85 | ISWP1 | ISWP0 | ILLV | IGOP | IG1P | IRVP | IRHP | IDQP |
| I port FIFO flag control and arbitration | 86 | VITX1 | VITX0 | IDG02 | IDG12 | FFL1 | FFLO | FEL1 | FELO |
| I port I/O enable, output clock and gated clock phase control | 87 | IPCK3 | IPCK2 | IPCK1 | IPCK0 | (1) | (1) | IPE1 | IPE0 |
| Power save control | 88 | CH4EN | CH2EN | SWRST | DPROG | SLM3 | (1) | SLM1 | SLM0 |
| Reserved | 89 to 8E | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Status information scaler part | 8F | XTRI | ITRI | FFIL | FFOV | PRDON | ERROF | FIDSCI | FIDSCO |


| REGISTER FUNCTION |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TASk A definition: REGISters 90H To BFH |  |  |  |  |  |  |  |  |  |
| Basic settings and acquisition window definition |  |  |  |  |  |  |  |  |  |
| Task handling control | 90 | CONLH | OFIDC | FSKP2 | FSKP1 | FSKP0 | RPTSK | STRC1 | STRC0 |
| X port formats and configuration | 91 | CONLV | HLDFV | SCSRC1 | SCSRC0 | SCRQE | FSC2 | FSC1 | FSC0 |
| $X$ port input reference signal definitions | 92 | XFDV | XFDH | XDV1 | XDV0 | XCODE | XDH | XDQ | XCKS |
| I port output formats and configuration | 93 | ICODE | 18_16 | FYSK | FOI1 | FOIO | FSI2 | FSI1 | FSIO |
| Horizontal input window start | 94 | XO7 | XO6 | XO5 | XO4 | XO3 | XO2 | XO1 | XO0 |
|  | 95 | (1) | (1) | (1) | (1) | XO11 | XO10 | XO9 | XO8 |
| Horizontal input window length | 96 | XS7 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 |
|  | 97 | (1) | (1) | (1) | (1) | XS11 | XS10 | XS9 | XS8 |
| Vertical input window start | 98 | YO7 | YO6 | YO5 | YO4 | YO3 | YO2 | YO1 | YOO |
|  | 99 | (1) | (1) | (1) | (1) | YO11 | YO10 | YO9 | YO8 |
| Vertical input window length | 9A | YS7 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 |
|  | 9B | (1) | (1) | (1) | (1) | YS11 | YS10 | YS9 | YS8 |
| Horizontal output window length | 9C | XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |
|  | 9D | (1) | (1) | (1) | (1) | XD11 | XD10 | XD9 | XD8 |
| Vertical output window length | 9E | YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 |
|  | 9 F | (1) | (1) | (1) | (1) | YD11 | YD10 | YD9 | YD8 |
| FIR filtering and prescaling |  |  |  |  |  |  |  |  |  |
| Horizontal prescaling | A0 | (1) | (1) | XPSC5 | XPSC4 | XPSC3 | XPSC2 | XPSC1 | XPSC0 |
| Accumulation length | A1 | (1) | (1) | XACL5 | XACL4 | XACL3 | XACL2 | XACL1 | XACLO |
| Prescaler DC gain and FIR prefilter control | A2 | PFUV1 | PFUV0 | PFY1 | PFYO | XC2_1 | XDCG2 | XDCG1 | XDCG0 |
| Reserved | A3 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Luminance brightness control | A4 | BRIG7 | BRIG6 | BRIG5 | BRIG4 | BRIG3 | BRIG2 | BRIG1 | BRIG0 |
| Luminance contrast control | A5 | CONT7 | CONT6 | CONT5 | CONT4 | CONT3 | CONT2 | CONT1 | CONT0 |
| Chrominance saturation control | A6 | SATN7 | SATN6 | SATN5 | SATN4 | SATN3 | SATN2 | SATN1 | SATN0 |
| Reserved | A7 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |


| REGISTER FUNCTION | SUB ADDR. (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Horizontal phase scaling |  |  |  |  |  |  |  |  |  |
| Horizontal luminance scaling increment | A8 | XSCY7 | XSCY6 | XSCY5 | XSCY4 | XSCY3 | XSCY2 | XSCY1 | XSCY0 |
|  | A9 | (1) | ${ }^{(1)}$ | (1) | XSCY12 | XSCY11 | XSCY10 | XSCY9 | XSCY8 |
| Horizontal luminance phase offset | AA | XPHY7 | XPHY6 | XPHY5 | XPHY4 | XPHY3 | XPHY2 | XPHY1 | XPHYO |
| Reserved | AB | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Horizontal chrominance scaling increment | AC | XSCC7 | XSCC6 | XSCC5 | XSCC4 | XSCC3 | XSCC2 | XSCC1 | XSCC0 |
|  | AD | (1) | ${ }^{(1)}$ | (1) | XSCC12 | XSCC11 | XSCC10 | XSCC9 | XSCC8 |
| Horizontal chrominance phase offset | AE | XPHC7 | XPHC6 | XPHC5 | XPHC4 | XPHC3 | XPHC2 | XPHC1 | XPHCO |
| Reserved | AF | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Vertical scaling |  |  |  |  |  |  |  |  |  |
| Vertical luminance scaling increment | B0 | YSCY7 | YSCY6 | YSCY5 | YSCY4 | YSCY3 | YSCY2 | YSCY1 | YSCY0 |
|  | B1 | YSCY15 | YSCY14 | YSCY13 | YSCY12 | YSCY11 | YSCY10 | YSCY9 | YSCY8 |
| Vertical chrominance scaling increment | B2 | YSCC7 | YSCC6 | YSCC5 | YSCC4 | YSCC3 | YSCC2 | YSCC1 | YSCC0 |
|  | B3 | YSCC15 | YSCC14 | YSCC13 | YSCC12 | YSCC11 | YSCC10 | YSCC9 | YSCC8 |
| Vertical scaling mode control | B4 | (1) | (1) | (1) | YMIR | (1) | (1) | (1) | YMODE |
| Reserved | B5 to B7 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Vertical chrominance phase offset '00' | B8 | YPC07 | YPC06 | YPC05 | YPC04 | YPC03 | YPC02 | YPC01 | YPC00 |
| Vertical chrominance phase offset '01' | B9 | YPC17 | YPC16 | YPC15 | YPC14 | YPC13 | YPC12 | YPC11 | YPC10 |
| Vertical chrominance phase offset '10' | BA | YPC27 | YPC26 | YPC25 | YPC24 | YPC23 | YPC22 | YPC21 | YPC20 |
| Vertical chrominance phase offset '11' | BB | YPC37 | YPC36 | YPC35 | YPC34 | YPC33 | YPC32 | YPC31 | YPC30 |
| Vertical luminance phase offset '00' | BC | YPY07 | YPY06 | YPY05 | YPY04 | YPY03 | YPY02 | YPY01 | YPY00 |
| Vertical luminance phase offset '01' | BD | YPY17 | YPY16 | YPY15 | YPY14 | YPY13 | YPY12 | YPY11 | YPY10 |
| Vertical luminance phase offset '10' | BE | YPY27 | YPY26 | YPY25 | YPY24 | YPY23 | YPY22 | YPY21 | YPY20 |


| REGISTER FUNCTION |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Vertical luminance phase offset '11' | BF | YPY37 | YPY36 | YPY35 | YPY34 | YPY33 | YPY32 | YPY31 | YPY30 |
| TASk B definition registers COH to EFH |  |  |  |  |  |  |  |  |  |
| Basic settings and acquisition window definition |  |  |  |  |  |  |  |  |  |
| Task handling control | C0 | CONLH | OFIDC | FSKP2 | FSKP1 | FSKP0 | RPTSK | STRC1 | STRC0 |
| X port formats and configuration | C1 | CONLV | HLDFV | SCSRC1 | SCSRC0 | SCRQE | FSC2 | FSC1 | FSC0 |
| Input reference signal definition | C2 | XFDV | XFDH | XDV1 | XDV0 | XCODE | XDH | XDQ | XCKS |
| I port formats and configuration | C3 | ICODE | I8_16 | FYSK | FOI1 | FOIO | FSI2 | FSI1 | FSIO |
| Horizontal input window start | C4 | XO7 | XO6 | XO5 | XO4 | XO3 | XO2 | XO1 | XO0 |
|  | C5 | (1) | (1) | (1) | (1) | XO11 | XO10 | XO9 | XO8 |
| Horizontal input window length | C6 | XS7 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 |
|  | C7 | (1) | (1) | (1) | (1) | XS11 | XS10 | XS9 | XS8 |
| Vertical input window start | C8 | YO7 | YO6 | YO5 | YO4 | YO3 | YO2 | YO1 | YO0 |
|  | C9 | (1) | (1) | (1) | (1) | YO11 | YO10 | YO9 | YO8 |
| Vertical input window length | CA | YS7 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 |
|  | CB | (1) | (1) | (1) | (1) | YS11 | YS10 | YS9 | YS8 |
| Horizontal output window length | CC | XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |
|  | CD | (1) | (1) | (1) | (1) | XD11 | XD10 | XD9 | XD8 |
| Vertical output window length | CE | YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 |
|  | CF | (1) | (1) | (1) | (1) | YD11 | YD10 | YD9 | YD8 |
| FIR filtering and prescaling |  |  |  |  |  |  |  |  |  |
| Horizontal prescaling | D0 | (1) | (1) | XPSC5 | XPSC4 | XPSC3 | XPSC2 | XPSC1 | XPSC0 |
| Accumulation length | D1 | (1) | (1) | XACL5 | XACL4 | XACL3 | XACL2 | XACL1 | XACLO |
| Prescaler DC gain and FIR prefilter control | D2 | PFUV1 | PFUV0 | PFY1 | PFYO | XC2_1 | XDCG2 | XDCG1 | XDCG0 |
| Reserved | D3 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Luminance brightness control | D4 | BRIG7 | BRIG6 | BRIG5 | BRIG4 | BRIG3 | BRIG2 | BRIG1 | BRIG0 |
| Luminance contrast control | D5 | CONT7 | CONT6 | CONT5 | CONT4 | CONT3 | CONT2 | CONT1 | CONT0 |
| Chrominance saturation control | D6 | SATN7 | SATN6 | SATN5 | SATN4 | SATN3 | SATN2 | SATN1 | SATN0 |
| Reserved | D7 | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |


| REGISTER FUNCTION | SUB ADDR. (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Horizontal phase scaling |  |  |  |  |  |  |  |  |  |
| Horizontal luminance scaling increment | D8 | XSCY7 | XSCY6 | XSCY5 | XSCY4 | XSCY3 | XSCY2 | XSCY1 | XSCY0 |
|  | D9 | (1) | (1) | (1) | XSCY12 | XSCY11 | XSCY10 | XSCY9 | XSCY8 |
| Horizontal luminance phase offset | DA | XPHY7 | XPHY6 | XPHY5 | XPHY4 | XPHY3 | XPHY2 | XPHY1 | XPHYO |
| Reserved | DB | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Horizontal chrominance scaling increment | DC | XSCC7 | XSCC6 | XSCC5 | XSCC4 | XSCC3 | XSCC2 | XSCC1 | XSCC0 |
|  | DD | (1) | (1) | (1) | XSCC12 | XSCC11 | XSCC10 | XSCC9 | XSCC8 |
| Horizontal chrominance phase offset | DE | XPHC7 | XPHC6 | XPHC5 | XPHC4 | XPHC3 | XPHC2 | XPHC1 | XPHC0 |
| Reserved | DF | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) |
| Vertical scaling |  |  |  |  |  |  |  |  |  |
| Vertical luminance scaling increment | E0 | YSCY7 | YSCY6 | YSCY5 | YSCY4 | YSCY3 | YSCY2 | YSCY1 | YSCY0 |
|  | E1 | YSCY15 | YSCY14 | YSCY13 | YSCY12 | YSCY11 | YSCY10 | YSCY9 | YSCY8 |
| Vertical chrominance scaling increment | E2 | YSCC7 | YSCC6 | YSCC5 | YSCC4 | YSCC3 | YSCC2 | YSCC1 | YSCC0 |
|  | E3 | YSCC15 | YSCC14 | YSCC13 | YSCC12 | YSCC11 | YSCC10 | YSCC9 | YSCC8 |
| Vertical scaling mode control | E4 | (1) | (1) | (1) | YMIR | (1) | (1) | (1) | YMODE |
| Reserved | E5 to E7 | (1) | (1) | (1) | ${ }^{(1)}$ | (1) | (1) | (1) | (1) |
| Vertical chrominance phase offset '00' | E8 | YPC07 | YPC06 | YPC05 | YPC04 | YPC03 | YPC02 | YPC01 | YPC00 |
| Vertical chrominance phase offset '01' | E9 | YPC17 | YPC16 | YPC15 | YPC14 | YPC13 | YPC12 | YPC11 | YPC10 |
| Vertical chrominance phase offset '10' | EA | YPC27 | YPC26 | YPC25 | YPC24 | YPC23 | YPC22 | YPC21 | YPC20 |
| Vertical chrominance phase offset '11' | EB | YPC37 | YPC36 | YPC35 | YPC34 | YPC33 | YPC32 | YPC31 | YPC30 |


| REGISTER FUNCTION | SUB <br> ADDR. <br> (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Vertical luminance phase <br> offset '00' | EC | YPY07 | YPY06 | YPY05 | YPY04 | YPY03 | YPY02 | YPY01 | YPY00 |
| Vertical luminance phase <br> offset '01' | ED | YPY17 | YPY16 | YPY15 | YPY14 | YPY13 | YPY12 | YPY11 | YPY10 |
| Vertical luminance phase <br> offset '10' | EE | YPY27 | YPY26 | YPY25 | YPY24 | YPY23 | YPY22 | YPY21 | YPY20 |
| Vertical luminance phase <br> offset '11' | EF | YPY37 | YPY36 | YPY35 | YPY34 | YPY33 | YPY32 | YPY31 | YPY30 |

1. All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

| FUNCTION | LOGIC LEVELS |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | ID7 | ID6 | ID5 | ID4 |
| Chip Version (CV) | CV3 | CV2 | CV1 | CV0 |

[^1]Table 149 Chip version (CV) identification; 00H[7:4]; read only register

### 18.2.2.3 Subaddress 02 H

Table 151 Analog input control 1 (AICO1); 02H[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D[7:6] | analog function select (see Fig.14) | FUSE[1:0] | 00 | amplifier plus anti-alias filter bypassed |
|  |  |  | 01 |  |
|  |  |  | 10 | amplifier active |
|  |  |  | 11 | amplifier plus anti-alias filter active |
| D[5:4] | update hysteresis for 9-bit gain (see Fig.15) | GUDL[1:0] | 00 | off |
|  |  |  | 01 | $\pm 1$ LSB |
|  |  |  | 10 | $\pm 2$ LSB |
|  |  |  | 11 | $\pm 3$ LSB |
| D[3:0] | mode selection | MODE[3:0] | 0000 | Mode 0: CVBS (automatic gain) from Al11 (pin P13); see Fig. 57 |
|  |  |  | 0001 | Mode 1: CVBS (automatic gain) from Al12 (pin P11); see Fig. 58 |
|  |  |  | 0010 | Mode 2: CVBS (automatic gain) from Al21 (pin P10); see Fig. 59 |
|  |  |  | 0011 | Mode 3: CVBS (automatic gain) from Al22 (pin P9); see Fig. 60 |
|  |  |  | 0100 | Mode 4: CVBS (automatic gain) from Al23 (pin P7); see Fig. 61 |
|  |  |  | 0101 | Mode 5: CVBS (automatic gain) from Al24 (pin P6); see Fig. 62 |
|  |  |  | 0110 | Mode 6: Y (automatic gain) from Al11 (pin P13) + C (gain adjustable via GAI28 to GAI20) from Al21 (pin P10); note 1; see Fig. 63 |
|  |  |  | 0111 | Mode 7: Y (automatic gain) from Al12 (pin P11) + C (gain adjustable via GAl28 to GAl20) from Al22 (pin P9); note 1; see Fig. 64 |
|  |  |  | 1000 | Mode 8: Y (automatic gain) from Al11 (pin P13) + C (gain adapted to Y gain) from Al21 (pin P10); note 1; see Fig. 65 |
|  |  |  | 1001 | Mode 9: Y (automatic gain) from Al12 (pin P11) + C (gain adapted to Y gain) from Al22 (pin P9); note 1; see Fig. 66 |
|  |  |  | 1111 | Modes 10 to 15: reserved |

## Note

1. To take full advantage of the $\mathrm{Y} / \mathrm{C}$-modes 6 to 9 the $\mathrm{I}^{2} \mathrm{C}$-bus bit BYPS (subaddress 09 H , bit 7 ) should be set to logic 1 (full luminance bandwidth).


Fig. 61 Mode 4; CVBS (automatic gain).

${ }^{2}$ ²-bus bit BYPS (subaddress 09 H , bit 7 ) should be set to logic 1 (full luminance bandwidth).

Fig. 63 Mode 6; Y + C (gain channel 2 adjusted via GAI2).

$I^{2} \mathrm{C}$-bus bit BYPS (subaddress 09H, bit 7) should be set to logic 1 (full luminance bandwidth).

Fig. 65 Mode 8; $\mathrm{Y}+\mathrm{C}$ (gain channel 2 adapted to Y gain).

${ }^{2}$ ² C-bus bit BYPS (subaddress 09H, bit 7) should be set to logic 1 (full luminance bandwidth).

Fig. 64 Mode 7; Y + C (gain channel 2 adjusted via GAI2).

$I^{2} \mathrm{C}$-bus bit BYPS (subaddress 09H, bit 7) should be set to logic 1 (full luminance bandwidth).

Fig. 66 Mode 9; $\mathrm{Y}+\mathrm{C}$ (gain channel 2 adapted to Y gain).

## PC-CODEC

### 18.2.2.4 Subaddress 03 H

Table 152 Analog input control 2 (AICO2); 03H[6:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D6 | HL not reference select | HLNRS | 0 | normal clamping if decoder is in unlocked state |
|  |  |  | $1^{(1)}$ | reference select if decoder is in unlocked state |
| D5 | AGC hold during vertical blanking period | VBSL | 0 | short vertical blanking (AGC disabled during equalization and serration pulses) |
|  |  |  | 1 | long vertical blanking (AGC disabled from start of pre-equalization pulses until start of active video (line 22 for 60 Hz , line 24 for 50 Hz ) |
| D4 | white peak control off | WPOFF | $0^{(1)}$ | white peak control active |
|  |  |  | 1 | white peak control off |
| D3 | automatic gain control integration | HOLDG | 0 | AGC active |
|  |  |  | 1 | AGC integration hold (freeze) |
| D2 | gain control fix | GAFIX | 0 | automatic gain controlled by MODE3 to MODE0 |
|  |  |  | 1 | gain is user programmable via GAI[17:10] and GAI[27:20] |
| D1 | static gain control channel 2 sign bit | GAI28 |  | see Table 154 |
| D0 | static gain control channel 1 sign bit | GAI18 |  | see Table 153 |

## Note

1. $\mathrm{HLNRS}=1$ should not be used in combination with $\mathrm{WPOFF}=0$.

### 18.2.2.5 Subaddress 04H

Table 153 Analog input control 3 (AICO3); static gain control channel 1; 03H[0] and 04H[7:0]

| DECIMAL VALUE | GAIN <br> (dB) | SIGN BIT 03H[0] | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | GAI18 | GAl17 | GAI16 | GAl15 | GAI14 | GAl13 | GAI12 | GAl11 | GAI10 |
| 0... | -3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ... 144 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 145... | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| ... 511 | +6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 18.2.2.6 Subaddress $05 H$

Table 154 Analog input control 4 (AICO4); static gain control channel 2; 03H[1] and 05H[7:0]

| DECIMAL VALUE | GAIN <br> (dB) | SIGN BIT 03H[1] | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | GAI28 | GAI27 | GAI26 | GAI25 | GAI24 | GAI23 | GAI22 | GAI21 | GAI20 |
| 0... | -3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ... 144 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 145... | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| ... 511 | +6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 18.2.2.7 Subaddress 06 H

Table 155 Horizontal sync start; 06H[7:0]

| DELAY TIME | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (STEP SIZE = 8/LLC) | HSB7 | HSB6 | HSB5 | HSB4 | HSB3 | HSB2 | HSB1 | HSB0 |
| -128...-109 (50 Hz) | forbidden (outside available central counter range) |  |  |  |  |  |  |  |
| -128...-108 (60 Hz) |  |  |  |  |  |  |  |  |
| -108 (50 Hz)... | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| -107 (60 Hz)... | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| ... $108(50 \mathrm{~Hz})$ | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| ... 107 (60 Hz) | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 109... 127 (50 Hz) | forbidden (outside available central counter range) |  |  |  |  |  |  |  |
| 108... 127 (60 Hz) |  |  |  |  |  |  |  |  |

### 18.2.2.8 Subaddress 07H

Table 156 Horizontal sync stop; 07H[7:0]

| DELAY TIME | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (STEP SIZE = 8/LLC) | HSS7 | HSS6 | HSS5 | HSS4 | HSS3 | HSS2 | HSS1 | HSSO |
| -128...-109 (50 Hz) | forbidden (outside available central counter range) |  |  |  |  |  |  |  |
| -128...-108 (60 Hz) |  |  |  |  |  |  |  |  |
| -108 (50 Hz)... | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| -107 (60 Hz)... | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| ... $108(50 \mathrm{~Hz})$ | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| ... 107 (60 Hz) | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 109... 127 ( 50 Hz ) | forbidden (outside available central counter range) |  |  |  |  |  |  |  |
| 108... 127 (60 Hz) |  |  |  |  |  |  |  |  |

### 18.2.2.9 Subaddress 08 H

Table 157 Sync control; 08H[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D7 | automatic field detection | AUFD | 0 | field state directly controlled via FSEL |
|  |  |  | 1 | automatic field detection; recommended setting |
| D6 | field selection | FSEL | 0 | $50 \mathrm{~Hz}, 625$ lines |
|  |  |  | 1 | $60 \mathrm{~Hz}, 525$ lines |
| D5 | forced ODD/EVEN toggle | FOET | 0 | ODD/EVEN signal toggles only with interlaced source |
|  |  |  | 1 | ODD/EVEN signal toggles fieldwise even if source is non-interlaced |
| D[4:3] | horizontal time constant selection | HTC[1:0] | 00 | TV mode, recommended for poor quality TV signals only; do not use for new applications |
|  |  |  | 01 | VTR mode, recommended if a deflection control circuit is directly connected to the SAA7108E; SAA7109E |
|  |  |  | 10 | reserved |
|  |  |  | 11 | fast locking mode; recommended setting |
| D2 | horizontal PLL | HPLL | 0 | PLL closed |
|  |  |  | 1 | PLL open; horizontal frequency fixed |
| D[1:0] | vertical noise reduction | VNOI[1:0] | 00 | normal mode; recommended setting |
|  |  |  | 01 | fast mode, applicable for stable sources only; automatic field detection (AUFD) must be disabled |
|  |  |  | 10 | free running mode |
|  |  |  | 11 | vertical noise reduction bypassed |

### 18.2.2.10 Subaddress $09 H$

Table 158 Luminance control; 09H[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D7 | chrominance trap/comb filter bypass | BYPS | 0 | chrominance trap or luminance comb filter active; default for CVBS mode |
|  |  |  | 1 | chrominance trap or luminance comb filter bypassed; default for S-video mode |
| D6 | adaptive luminance comb filter | YCOMB | 0 | disabled (= chrominance trap enabled, if BYPS $=0$ ) |
|  |  |  | 1 | active, if BYPS = 0 |
| D5 | processing delay in non comb filter mode | LDEL | 0 | processing delay is equal to internal pipelining delay |
|  |  |  | 1 | one (NTSC standards) or two (PAL standards) video lines additional processing delay |
| D4 | remodulation bandwidth for luminance; see Figs 20 to 23 | LUBW | 0 | small remodulation bandwidth (narrow chrominance notch $\Rightarrow$ higher luminance bandwidth) |
|  |  |  | 1 | large remodulation bandwidth (wider chrominance notch $\Rightarrow$ smaller luminance bandwidth) |
| D[3:0] | sharpness control, luminance filter characteristic; see Fig. 24 | LUFI[3:0] | 0001 | resolution enhancement filter; 8.0 dB at 4.1 MHz |
|  |  |  | 0010 | resolution enhancement filter; 6.8 dB at 4.1 MHz |
|  |  |  | 0011 | resolution enhancement filter; 5.1 dB at 4.1 MHz |
|  |  |  | 0100 | resolution enhancement filter; 4.1 dB at 4.1 MHz |
|  |  |  | 0101 | resolution enhancement filter; 3.0 dB at 4.1 MHz |
|  |  |  | 0110 | resolution enhancement filter; 2.3 dB at 4.1 MHz |
|  |  |  | 0111 | resolution enhancement filter; 1.6 dB at 4.1 MHz |
|  |  |  | 0000 | plain |
|  |  |  | 1000 | low-pass filter; 2 dB at 4.1 MHz |
|  |  |  | 1001 | low-pass filter; 3 dB at 4.1 MHz |
|  |  |  | 1010 | low-pass filter; 3 dB at $3.3 \mathrm{MHz} ; 4 \mathrm{~dB}$ at 4.1 MHz |
|  |  |  | 1011 | low-pass filter; 3 dB at 2.6 MHz ; 8 dB at 4.1 MHz |
|  |  |  | 1100 | low-pass filter; 3 dB at $2.4 \mathrm{MHz} ; 14 \mathrm{~dB}$ at 4.1 MHz |
|  |  |  | 1101 | low-pass filter; 3 dB at 2.2 MHz ; notch at 3.4 MHz |
|  |  |  | 1110 | low-pass filter; 3 dB at 1.9 MHz ; notch at 3.0 MHz |
|  |  |  | 1111 | low-pass filter; 3 dB at 1.7 MHz; notch at 2.5 MHz |

### 18.2.2.11 Subaddress OAH

Table 159 Luminance brightness control: decoder part; 0AH[7:0]

| OFFSET | CONTROL BITS D7 TO DO |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | DBRI7 | DBRI6 | DBRI5 | DBRI4 | DBRI3 | DBRI2 | DBRI1 | DBRI0 |
| 255 (bright) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 128 (ITU level) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 (dark) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 18.2.2.12 Subaddress $O B H$

Table 160 Luminance contrast control: decoder part; 0BH[7:0]

| GAIN | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | DCON7 | DCON6 | DCON5 | DCON4 | DCON3 | DCON2 | DCON1 | DCON0 |  |
| 1.984 (maximum) | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| 1.063 (ITU level) | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |  |
| 1.0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| 0 (luminance off) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| -1 (inverse luminance) | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| -2 (inverse luminance) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

### 18.2.2.13 Subaddress $O C H$

Table 161 Chrominance saturation control: decoder part; 0CH[7:0]

| GAIN | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | DSAT7 | DSAT6 | DSAT5 | DSAT4 | DSAT3 | DSAT2 | DSAT1 | DSAT0 |
| 1.984 (maximum) | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1.0 (ITU level) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 (colour off) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -1 (inverse chrominance) | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| -2 (inverse chrominance) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 18.2.2.14 Subaddress ODH

Table 162 Chrominance hue control: 0DH[7:0]

| HUE PHASE (DEG) | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | HUEC7 | HUEC6 | HUEC5 | HUEC4 | HUEC3 | HUEC2 | HUEC1 | HUEC0 |  |
| $+178.6 \ldots$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| $\ldots 0 \ldots$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| $\ldots-180$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

### 18.2.2.15 Subaddress OEH

Table 163 Chrominance control 1; 0EH[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $50 \mathrm{~Hz} / 625$ LINES | $60 \mathrm{~Hz} / 525$ LINES |
| D7 | clear DTO | CDTO | 0 | disabled |  |
|  |  |  | 1 | Every time CDTO is set, the internal subcarrier DTO phase is reset to $0^{\circ}$ and the RTCO output generates a logic 0 at time slot 68 (see document "RTC Functional Description", available on request). So an identical subcarrier phase can be generated by an external device (e.g. an encoder). |  |
| D[6:4] | colour standard selection | CSTD[2:0] | 000 | PAL BGDHI (4.43 MHz) | NTSC M (3.58 MHz) |
|  |  |  | 001 | NTSC 4.43 ( 50 Hz ) | PAL 4.43 (60 Hz) |
|  |  |  | 010 | $\begin{aligned} & \text { Combination-PAL N } \\ & \text { (3.58 MHz) } \end{aligned}$ | NTSC 4.43 (60 Hz) |
|  |  |  | 011 | NTSC N (3.58 MHz) | PAL M (3.58 MHz) |
|  |  |  | 100 | reserved | NTSC-Japan (3.58 MHz) |
|  |  |  | 101 | SECAM | reserved |
|  |  |  | 110 | reserved; do not use |  |
|  |  |  | 111 | reserved; do not use |  |
| D3 | disable chrominance vertical filter and PAL phase error correction | DCVF | 0 | chrominance vertical filter and PAL phase error correction on (during active video lines) |  |
|  |  |  | 1 | chrominance vertical filter and PAL phase error correction permanently off |  |
| D2 | fast colour time constant | FCTC | 0 | nominal time constant |  |
|  |  |  | 1 | fast time constant for special applications |  |
| D0 | adaptive chrominance comb filter | CCOMB | 0 | disabled |  |
|  |  |  | 1 | active |  |

18.2.2.16 Subaddress OFH

Table 164 Chrominance gain control; 0FH[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D7 | automatic chrominance gain control | ACGC | 0 | on |
|  |  |  | 1 | programmable gain via CGAIN6 to CGAIN0; need to be set for SECAM standard |
| D[6:0] | chrominance gain value (if ACGC is set to logic 1) | CGAIN[6:0] | 0000000 | minimum gain (0.5) |
|  |  |  | 0100100 | nominal gain (1.125) |
|  |  |  | 1111111 | maximum gain (7.5) |

### 18.2.2.17 Subaddress 10 H

Table 165 Chrominance control 2; 10H[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D[7:6] | fine offset adjustment B - Y component | OFFU[1:0] | 00 | 0 LSB |
|  |  |  | 01 | 1/4 LSB |
|  |  |  | 10 | 1/2 LSB |
|  |  |  | 11 | 3/4 LSB |
| D[5:4] | fine offset adjustment R - Y component | OFFV[1:0] | 00 | 0 LSB |
|  |  |  | 01 | 1/4LSB |
|  |  |  | 10 | 1/2LSB |
|  |  |  | 11 | 3/4LSB |
| D3 | chrominance bandwidth; see Figs 18 and 19 | CHBW | 0 | small |
|  |  |  | 1 | wide |
| D[2:0] | combined luminance/chrominance bandwidth adjustment; see Figs 18 to 24 | LCBW[2:0] | 000 | smallest chrominance bandwidth/largest luminance bandwidth |
|  |  |  | ... | ... to ... |
|  |  |  | 111 | largest chrominance bandwidth/smallest luminance bandwidth |

### 18.2.2.18 Subaddress 11 H

Table 166 Mode/delay control; 11H[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D7 | colour on | COLO | 0 | automatic colour killer enabled |
|  |  |  | 1 | colour forced on |
| D6 | polarity of RTS1 output signal | RTP1 | 0 | non inverted |
|  |  |  | 1 | inverted |
| D[5:4] | fine position of HS (steps in 2/LLC) | HDEL[1:0] | 00 | 0 |
|  |  |  | 01 | 1 |
|  |  |  | 10 | 2 |
|  |  |  | 11 | 3 |
| D3 | polarity of RTS0 output signal | RTP0 | 0 | non inverted |
|  |  |  | 1 | inverted |
| D[2:0] | luminance delay compensation (steps in 2/LLC) | YDEL[2:0] | 100 | -4... |
|  |  |  | 000 | ...0... |
|  |  |  | 011 | ... 3 |

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### 18.2.2.19 Subaddress 12 H

Table 167 RT signal control: RTS0 output; 12H[3:0]
The polarity of any signal on RTS0 can be inverted via RTPO[11H[3]].

| RTSO OUTPUT | RTSE03 | RTSE02 | RTSE01 | RTSE00 |
| :---: | :---: | :---: | :---: | :---: |
| 3-state | 0 | 0 | 0 | 0 |
| Constant LOW | 0 | 0 | 0 | 1 |
| CREF (13.5 MHz toggling pulse; see Fig.31) | 0 | 0 | 1 | 0 |
| CREF2 (6.75 MHz toggling pulse; see Fig.31) | 0 | 0 | 1 | 1 |
| HL; horizontal lock indicator (note 1): <br> HL = 0: unlocked <br> HL = 1: locked | 0 | 1 | 0 | 0 |
| VL; vertical and horizontal lock: $\begin{aligned} & \mathrm{VL}=0: \text { unlocked } \\ & \mathrm{VL}=1: \text { locked } \end{aligned}$ | 0 | 1 | 0 | 1 |
| DL; vertical and horizontal lock and colour detected: $\begin{aligned} & \mathrm{DL}=0: \text { unlocked } \\ & \mathrm{DL}=1: \text { locked } \end{aligned}$ | 0 | 1 | 1 | 0 |
| Reserved | 0 | 1 | 1 | 1 |
| HREF, horizontal reference signal; indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval (see Fig.31). | 1 | 0 | 0 | 0 |
| HS: <br> programmable width in LLC8 steps via HSB[7:0] 06H[7:0] and HSS[7:0] 07H[7:0] <br> fine position adjustment in LLC2 steps via HDEL[1:0] 11H[5:4]; see Fig. 31 | 1 | 0 | 0 | 1 |
| HQ; HREF gated with VGATE | 1 | 0 | 1 | 0 |
| Reserved | 1 | 0 | 1 | 1 |
| V123; vertical sync (see vertical timing diagrams Figs 29 and 30) | 1 | 1 | 0 | 0 |
| VGATE; programmable via VSTA[8:0] 17H[0] 15H[7:0], VSTO[8:0] 17H[1] 16H[7:0] and VGPS[17H[2]] | 1 | 1 | 0 | 1 |
| LSBs of the 9-bit ADC's | 1 | 1 | 1 | 0 |
| FID; position programmable via VSTA[8:0] 17H[0] 15H[7:0]; see vertical timing diagrams Figs 29 and 30 | 1 | 1 | 1 | 1 |

## Note

1. Function of HL is selectable via $\mathrm{HLSEL}[13 \mathrm{H}[3]]$ :
a) $\mathrm{HLSEL}=0$ : HL is standard horizontal lock indicator.
b) $\mathrm{HLSEL}=1$ : HL is fast horizontal lock indicator (use is not recommended for sources with unstable timebase e.g. VCRs).

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Table 168 RT signal control: RTS1 output; 12H[7:4]
The polarity of any signal on RTS1 can be inverted via RTP1[11H[6]].

| RTS1 OUTPUT CONTROL | RTSE13 | RTSE12 | RTSE11 | RTSE10 |
| :---: | :---: | :---: | :---: | :---: |
| 3-state | 0 | 0 | 0 | 0 |
| Constant LOW | 0 | 0 | 0 | 1 |
| CREF (13.5 MHz toggling pulse; see Fig.31) | 0 | 0 | 1 | 0 |
| CREF2 (6.75 MHz toggling pulse; see Fig.31) | 0 | 0 | 1 | 1 |
| HL; horizontal lock indicator (note 1): <br> HL = 0: unlocked <br> HL = 1: locked | 0 | 1 | 0 | 0 |
| VL; vertical and horizontal lock: <br> VL = 0: unlocked <br> VL = 1: locked | 0 | 1 | 0 | 1 |
| DL; vertical and horizontal lock and colour detected: $\begin{aligned} & \mathrm{DL}=0: \text { unlocked } \\ & \mathrm{DL}=1: \text { locked } \end{aligned}$ | 0 | 1 | 1 | 0 |
| Reserved | 0 | 1 | 1 | 1 |
| HREF, horizontal reference signal: indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval (see Fig.31). | 1 | 0 | 0 | 0 |
| HS: programmable width in LLC8 steps via HSB[7:0] 06H[7:0] and HSS[7:0] 07H[7:0] fine position adjustment in LLC2 steps via $\operatorname{HDEL[1:0]~11H[5:4];~see~Fig.~} 31$ | 1 | 0 | 0 | 1 |
| HQ; HREF gated with VGATE | 1 | 0 | 1 | 0 |
| Reserved | 1 | 0 | 1 | 1 |
| V123; vertical sync (see vertical timing diagrams Figs 29 and 30) | 1 | 1 | 0 | 0 |
| VGATE; programmable via VSTA[8:0] 17H[0] 15H[7:0], VSTO[8:0] 17H[1] 16H[7:0] and VGPS[17H[2]] | 1 | 1 | 0 | 1 |
| Reserved | 1 | 1 | 1 | 0 |
| FID; position programmable via VSTA[8:0] 17H[0] 15H[7:0]; see vertical timing diagrams Figs 29 and 30 | 1 | 1 | 1 | 1 |

## Note

1. Function of HL is selectable via $\mathrm{HLSEL}[13 \mathrm{H}[3]]$ :
a) $\mathrm{HLSEL}=0$ : HL is standard horizontal lock indicator.
b) HLSEL = 1: HL is fast horizontal lock indicator (use is not recommended for sources with unstable timebase e.g. VCRs).

### 18.2.2.20 Subaddress $13 H$

Table 169 RT/X port output control; 13H[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D7 | RTCO output enable | RTCE | 0 | 3-state |
|  |  |  | 1 | enabled |
| D6 | X port XRH output selection | XRHS | 0 | HREF (see Fig.31) |
|  |  |  | 1 | HS: <br> programmable width in LLC8 steps via HSB[7:0] 06H[7:0] and HSS[7:0] 07H[7:0] <br> fine position adjustment in LLC2 steps via HDEL[1:0] 11H[5:4] (see Fig.31) |
| D[5:4] | X port XRV output selection | XRVS[1:0] | 00 | V123; see Figs 29 and 30 |
|  |  |  | 01 | ITU 656 related field ID; see Figs 29 and 30 |
|  |  |  | 10 | inverted V123 |
|  |  |  | 11 | inverted ITU 656 related field ID |
| D3 | horizontal lock indicator selection | HLSEL | 0 | copy of inverted HLCK status bit (default) |
|  |  |  | 1 | fast horizontal lock indicator (for special applications only) |
| D[2:0] | XPD7 to XPD0 (port output format selection); see Section 10.4 | OFTS[2:0] | 000 | ITU 656 |
|  |  |  | 001 | ITU 656 like format with modified field blanking according to VGATE position (programmable via VSTA[8:0] 17H[0] 15H[7:0], VSTO[8:0] 17H[1] 16H[7:0] and VGPS[17H[2]]) |
|  |  |  | 010 | $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4$ : 2 : 2 8-bit format (no SAV/EAV codes inserted) |
|  |  |  | 011 | reserved |
|  |  |  | 100 | multiplexed AD2/AD1 bypass (bits 8 to 1) dependent on mode settings; if both ADCs are selected AD2 is output at CREF $=1$ and AD1 is output at CREF $=0$ |
|  |  |  | 101 | multiplexed AD2/AD1 bypass (bits 7 to 0 ) dependent on mode settings; if both ADCs are selected AD2 is output at CREF $=1$ and AD1 is output at CREF $=0$ |
|  |  |  | 110 | reserved |
|  |  |  | 111 | multiplexed ADC MSB/LSB bypass dependent on mode settings; only one ADC should be selected at a time; $A D x 8$ to $A D x 1$ are outputs at $C R E F=1$ and $A D \times 7$ to $A D \times 0$ are outputs at CREF $=0$ |

### 18.2.2.21 Subaddress 14 H

Table 170 Analog/ADC/compatibility control; 14H[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D7 | compatibility bit for SAA7199 | CM99 | 0 | off (default) |
|  |  |  | 1 | on (to be set only if SAA7199 is used for re-encoding in conjunction with RTCO active) |
| D6 | update time interval for AGC value | UPTCV | 0 | horizontal update (once per line) |
|  |  |  | 1 | vertical update (once per field) |
| D[5:4] | analog test select | AOSL[1:0] | 00 | AOUT connected to internal test point 1 |
|  |  |  | 01 | AOUT connected to input AD1 |
|  |  |  | 10 | AOUT connected to input AD2 |
|  |  |  | 11 | AOUT connected to internal test point 2 |
| D3 | XTOUTd output enable | XTOUTE | 0 | pin P4 (XTOUTd) 3-stated |
|  |  |  | 1 | pin P4 (XTOUTd) enabled |
| D2 | decoder status byte selection; see Table 176 | OLDSB | 0 | standard |
|  |  |  | 1 | backward compatibility to SAA7112 |
| D[1:0] | ADC sample clock phase delay | APCK[1:0] | 00 | application dependent |
|  |  |  | 01 |  |
|  |  |  | 10 |  |
|  |  |  | 11 |  |

18.2.2.22 Subaddress 15H

| FIELD |  | FRAME LINE COUNTING | DECIMAL VALUE | $\begin{gathered} \text { MSB } \\ \text { 17H[0] } \end{gathered}$ | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | VSTA8 |  | VSTA7 | VSTA6 | VSTA5 | VSTA4 | VSTA3 | VSTA2 | VSTA1 | VSTAO |
| 50 Hz | 1st |  | 1 | 312 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
|  | 2nd | 314 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 2 | 0... | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
|  | 2nd | 315 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 312 | ... 310 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  |
|  | 2nd | 625 |  |  |  |  |  |  |  |  |  |  |  |
| 60 Hz | 1st | 4 | 262 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |  |
|  | 2nd | 267 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 5 | 0... | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
|  | 2nd | 268 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 265 | ... 260 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |  |
|  | 2nd | 3 |  |  |  |  |  |  |  |  |  |  |  |

18.2.2.23 Subaddress 16H
Table 172 VGATE stop; 17H[1] and 16H[7:0]
Stop of VGATE pulse (HIGH-to-LOW transition), VGPS = 0; see Figs 29 and 30.

| FIELD |  | FRAME LINE COUNTING | DECIMAL VALUE | $\begin{gathered} \text { MSB } \\ \text { 17H[1] } \end{gathered}$ | CONTROL BITS D7 TO DO |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | vST08 |  | vSTO7 | VSTO6 | vSTO5 | vSTO4 | vsto3 | VSTO2 | vSTO1 | vstoo |
| 50 Hz | 1st |  | 1 | 312 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
|  | 2nd | 314 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 2 | 0... | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
|  | 2nd | 315 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 312 | ... 310 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  |
|  | 2nd | 625 |  |  |  |  |  |  |  |  |  |  |  |
| 60 Hz | 1st | 4 | 262 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |  |
|  | 2nd | 267 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 5 | 0... | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
|  | 2nd | 268 |  |  |  |  |  |  |  |  |  |  |  |
|  | 1st | 265 | ... 260 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |  |
|  | 2nd | 3 |  |  |  |  |  |  |  |  |  |  |  |

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### 18.2.2.24 Subaddress 17 H

Table 173 Miscellaneous/VGATE MSBs; 17H[7:6] and 17H[2:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |  |  |  |  |  |
| :---: | :--- | :---: | :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| D7 | LLC output enable | LLCE | 0 | enable |  |  |  |  |  |
|  |  |  | 1 | 3-state |  |  |  |  |  |
| D6 | LLC2 output enable | LLC2E | 0 | enable |  |  |  |  |  |
|  |  | 1 | 3-state |  |  |  |  |  |  |
| D2 | alternative VGATE <br> position | VGPS | 0 | VGATE position according to Tables 171 and 172 |  |  |  |  |  |
|  |  |  | VGATE occurs one line earlier during field 2 |  |  |  |  |  |  |
| D1 | MSB VGATE stop | VSTO8 | see Table 172 <br> D0 MSB VGATE start |  |  | VSTA8 | see Table 171 |  |  |

### 18.2.2.25 Subaddress 18 H

Table 174 Raw data gain control; RAWG[7:0] 18H[7:0]; see Fig. 26

| GAIN | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | RAWG7 | RAWG6 | RAWG5 | RAWG4 | RAWG3 | RAWG2 | RAWG1 | RAWG0 |
| 255 (double amplitude) | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 128 (nominal level) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 (off) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

18.2.2.26 Subaddress 19H

Table 175 Raw data offset control; RAWO[7:0] 19H[7:0]; see Fig. 26

| OFFSET | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | RAWO7 | RAWO6 | RAWO5 | RAWO4 | RAWO3 | RAWO2 | RAWO1 | RAWO0 |
| -128 LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| +128 LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## PC-CODEC

### 18.2.2.27 Subaddress 1FH

Table 176 Status byte video decoder; 1FH[7:0]; read only register

| BIT | DESCRIPTION | $\begin{gathered} \mathrm{I}^{2} \mathrm{C}-\mathrm{BUS} \\ \text { CONTROL } \\ \text { BIT } \end{gathered}$ | $\begin{aligned} & \text { OLDSB } \\ & \text { 14H[2] } \end{aligned}$ | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| D7 | status bit for interlace detection | INTL | - | 0 | non-interlaced |
|  |  |  |  | 1 | interlaced |
| D6 | status bit for horizontal and vertical loop | HLVLN | 0 | 0 | both loops locked |
|  |  |  |  | 1 | unlocked |
|  | status bit for locked horizontal frequency | HLCK | 1 | 0 | locked |
|  |  |  |  | 1 | unlocked |
| D5 | identification bit for detected field frequency | FIDT | - | 0 | 50 Hz |
|  |  |  |  | 1 | 60 Hz |
| D4 | gain value for active luminance channel is limited; maximum (top) | GLIMT | - | 0 | not active |
|  |  |  |  | 1 | active |
| D3 | gain value for active luminance channel is limited; minimum (bottom) | GLIMB | - | 0 | not active |
|  |  |  |  | 1 | active |
| D2 | white peak loop is activated | WIPA | - | 0 | not active |
|  |  |  |  | 1 | active |
| D1 | copy protected source detected according to macrovision version up to 7.01 | COPRO | 0 | 0 | not active |
|  |  |  |  | 1 | active |
|  | slow time constant active in WIPA mode | SLTCA | 1 | 0 | not active |
|  |  |  |  | 1 | active |
| D0 | ready for capture (all internal loops locked) | RDCAP | 0 | 0 | not active |
|  |  |  |  | 1 | active |
|  | colour signal in accordance with selected standard has been detected | CODE | 1 | 0 | not active |
|  |  |  |  | 1 | active |

### 18.2.3 Programming register audio clock generation

See equations in Section 9.6 and examples in Tables 51 and 52.

### 18.2.3.1 Subaddresses 30 H to 32 H

Table 177 Audio master clock (AMCLK) cycles per field

| SUBADDRESS | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 30 H | ACPF7 | ACPF6 | ACPF5 | ACPF4 | ACPF3 | ACPF2 | ACPF1 | ACPF0 |  |
| 31 H | ACPF15 | ACPF14 | ACPF13 | ACPF12 | ACPF11 | ACPF10 | ACPF9 | ACPF8 |  |
| 32 H | - | - | - | - | - | - | ACPF17 | ACPF16 |  |

## PC-CODEC

### 18.2.3.2 Subaddresses 34H to 36 H

Table 178 Audio master clock (AMCLK) nominal increment

| SUBADDRESS | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 34 H | ACNI7 | ACNI | ACNI5 | ACNI4 | ACNI3 | ACNI2 | ACNI1 | ACNI0 |
| 35 H | ACNI15 | ACNI14 | ACNI13 | ACNI12 | ACNI11 | ACNI10 | ACNI9 | ACNI8 |
| 36 H | - | - | ACNI21 | ACNI20 | ACNI19 | ACNI18 | ACNI17 | ACNI16 |

### 18.2.3.3 Subaddress 38 H

Table 179 Clock ratio audio master clock (AMXCLK) to serial bit clock (ASCLK)

| SUBADDRESS | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 38 H | - | - | SDIV5 | SDIV4 | SDIV3 | SDIV2 | SDIV1 | SDIV0 |  |

### 18.2.3.4 Subaddress 39H

Table 180 Clock ratio serial bit clock (ASCLK) to channel select clock (ALRCLK)

| SUBADDRESS | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 39 H | - | - | LRDIV5 | LRDIV4 | LRDIV3 | LRDIV2 | LRDIV1 | LRDIV0 |

### 18.2.3.5 Subaddress $3 A H$

Table 181 Audio clock control; 3AH[3:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D3 | audio PLL modes | APLL | 0 | PLL active, AMCLK is field-locked |
|  |  |  | 1 | PLL open, AMCLK is free-running |
| D2 | audio master clock vertical reference | AMVR | 0 | vertical reference pulse is taken from internal decoder |
|  |  |  | 1 | vertical reference is taken from XRV input (expansion port) |
| D1 | ALRCLK phase | LRPH | 0 | ALRCLK edges triggered by falling edges of ASCLK |
|  |  |  | 1 | ALRCLK edges triggered by rising edges of ASCLK |
| D0 | ASCLK phase | SCPH | 0 | ASCLK edges triggered by falling edges of AMCLK |
|  |  |  | 1 | ASCLK edges triggered by rising edges of AMCLK |

18.2.4 Programming register VBI-Data slicer

### 18.2.4.1 Subaddress 40 H

Table 182 Slicer control 1; 40H[6:4]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :--- | :---: | :---: | :--- |
| D6 | Hamming check | HAM_N | 0 | Hamming check for 2 bytes after framing code, <br> dependent on data type (default) |
|  |  |  | 1 | no Hamming check |
| D5 | framing code error | FCE | 0 | one framing code error allowed |
|  |  |  | 1 | no framing code errors allowed |
| D4 | amplitude searching | HUNT_N | 0 | amplitude searching active (default) |
|  |  |  | 1 | amplitude searching stopped |

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### 18.2.4.2 Subaddresses 41 H to 57 H

Table 183 Line control register; LCR2 to LCR24 ( 41 H to 57 H ); see Sections 9.2 and 9.4

| NAME | DESCRIPTION | FRAMING CODE | $\begin{gathered} \mathrm{D}[7: 4] \\ (41 \mathrm{H} \text { TO } 57 \mathrm{H}) \end{gathered}$ | $\begin{gathered} \mathrm{D}[3: 0] \\ (41 \mathrm{H} \text { TO } 57 \mathrm{H}) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \text { DT[3:0] 62H[3:0] } \\ \text { (FIELD 1) } \end{gathered}$ | $\begin{gathered} \mathrm{DT}[3: 0] 62 \mathrm{H}[3: 0] \\ \text { (FIELD 2) } \end{gathered}$ |
| WST625 | teletext EuroWST, CCST | 27H | 0000 | 0000 |
| CC625 | European Closed Caption | 001 | 0001 | 0001 |
| VPS | video programming service | 9951H | 0010 | 0010 |
| WSS | wide screen signalling bits | 1E3C1FH | 0011 | 0011 |
| WST525 | US teletext (WST) | 27H | 0100 | 0100 |
| CC525 | US Closed Caption (line 21) | 001 | 0101 | 0101 |
| Test line | video component signal, VBI region | - | 0110 | 0110 |
| Intercast | raw data | - | 0111 | 0111 |
| General text | teletext | programmable | 1000 | 1000 |
| VITC625 | VITC/EBU time codes (Europe) | programmable | 1001 | 1001 |
| VITC525 | VITC/SMPTE time codes (USA) | programmable | 1010 | 1010 |
| Reserved | reserved | - | 1011 | 1011 |
| NABTS | US NABTS | - | 1100 | 1100 |
| Japtext | MOJI (Japanese) | programmable (A7H) | 1101 | 1101 |
| JFS | Japanese format switch (L20/22) | programmable | 1110 | 1110 |
| Active video | video component signal, active video region (default) | - | 1111 | 1111 |

### 18.2.4.3 Subaddress 58 H

Table 184 Programmable framing code; slicer set 58H[7:0]; see Tables 44 and 183

| FRAMING CODE FOR PROGRAMMABLE DATA TYPES | CONTROL BITS D7 TO D0 |
| :--- | :---: |
| Default value | FC[7:0] $=40 \mathrm{H}$ |

### 18.2.4.4 Subaddress 59H

Table 185 Horizontal offset for slicer; slicer set 59H and 5BH

| HORIZONTAL OFFSET | CONTROL BITS 5BH[2:0] | CONTROL BITS 59H[7:0] |
| :--- | :---: | :---: |
| Recommended value | HOFF[10:8] $=3 \mathrm{H}$ | HOFF[7:0] $=47 \mathrm{H}$ |

### 18.2.4.5 Subaddress 5AH

Table 186 Vertical offset for slicer; slicer set 5AH and 5BH

| VERTICAL OFFSET | CONTROL BIT 5BH[4] <br> VOFF8 | CONTROL BITS 5AH[7:0] <br> VOFF[7:0] |
| :--- | :---: | :---: |
| Minimum value 0 | 0 | 00 H |
| Maximum value 312 | 1 | 38 H |
| Value for 50 Hz 625 lines input | 0 | 03 H |
| Value for 60 Hz 525 lines input | 0 | 06 H |

### 18.2.4.6 Subaddress 5BH

Table 187 Field offset, and MSBs for horizontal and vertical offsets; slicer set 5BH[7:6]
See Sections 18.2.4.4 and 18.2.4.5 for HOFF[10:8] 5BH[2:0] and VOFF8[5BH[4]].

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :--- | :---: | :---: | :--- |
| D7 | field offset | FOFF | 0 | no modification of internal field indicator (default for 50 Hz <br> 625 lines input sources) |
|  |  |  | 1 | invert field indicator (default for 60 Hz 525 lines input sources) |
|  |  | R6 | recode |  |
|  |  |  | 1 |  |
|  |  |  |  |  |

### 18.2.4.7 Subaddress 5DH

Table 188 Header and data identification (DID; ITU 656) code control; slicer set 5DH[7:0]

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| D7 | field ID and V-blank selection for text output (F and V reference selection) | FVREF | 0 | F and V output of slicer is LCR table dependent |
|  |  |  | 1 | F and V output is taken from decoder real time signals EVEN ITU and VBLNK ITU |
| D[5:0] | default; DID[5:0] = 00H | DID[5:0] | 000000 | ANC header framing; see Fig. 38 and Table 50 |
|  | special cases of DID programming |  | 111110 | DID[5:0] = 3EH SAV/EAV framing, with FVREF = 1 |
|  |  |  | 111111 | DID[5:0] = 3FH SAV/EAV framing, with FVREF $=0$ |

### 18.2.4.8 Subaddress 5EH

Table 189 Sliced data identification (SDID) code; slicer set 5EH[5:0]

| BIT | DESCRIPTION | SYMBOL | VALUE |  | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| D[5:0] | SDID codes | SDID[5:0] | OOH | default |  |

### 18.2.4.9 Subaddress 60 H

Table 190 Slicer status byte 0; 60H[6:2]; read only register

| BIT | DESCRIPTION | SYMBOL | VALUE | FUNCTION |
| :---: | :--- | :---: | :---: | :--- |
| D6 | framing code valid | FC8V | 0 | no framing code (0 error) in the last frame detected |
|  |  |  | 1 | framing code with 0 error detected |
| D5 | framing code valid | FC7V | 0 | no framing code (1 error) in the last frame detected |
|  |  |  | 1 | framing code with 1 error detected |
| D4 | VPS valid | VPSV | 0 | no VPS in the last frame |
|  |  |  | 1 | VPS detected |
| D3 | PALplus valid | PPV | 0 | no PALplus in the last frame |
|  |  |  | 0 | PALplus detected |
| D2 | Closed Caption valid |  | 1 | Closed Caption detected |
|  |  |  |  |  |

### 18.2.4.10 Subaddresses 61 H and 62 H

Table 191 Slicer status byte 1;61H[5:0] and slicer status byte 2; 62H[7:0]; read only registers

| SUBADDRESS | BIT | SYMBOL | DESCRIPTION |
| :---: | :---: | :---: | :--- |
| 61 H | D 5 | F21_N | field ID as seen by the VBI slicer; for field 1: D5 = 0 |
|  | $\mathrm{D}[4: 0]$ | LN[8:4] | line number |
| 62 H | $\mathrm{D}[7: 4]$ | LN[3:0] |  |
|  | $\mathrm{D}[3: 0]$ | $\mathrm{DT}[3: 0]$ | data type; according to Table 44 |

### 18.2.5 Programming register interfaces and scaler part

### 18.2.5.1 Subaddress 80 H

Table 192 Global control 1; global set 80H[6:4]
SWRST moved to subaddress $88 \mathrm{H}[5]$; note 1 .

| TASK ENABLE CONTROL | CONTROL BITS D6 TO D4 |  |  |
| :--- | :---: | :---: | :---: |
|  | SMOD | TEB | TEA |
| Task of register set A is disabled | X | X | 0 |
| Task of register set A is enabled | X | X | 1 |
| Task of register set B is disabled | X | 0 | X |
| Task of register set B is enabled | X | 1 | X |
| The scaler window defines the F and V timing of the scaler output | 0 | X | X |
| VBI-data slicer defines the F and V timing of the scaler output | 1 | X | X |

## Note

1. $X=$ don't care.

## PC-CODEC

Table 193 Global control 1; global set 80H[3:0]; note 1

| I PORT AND SCALER BACK-END CLOCK SELECTION | CONTROL BITS D3 TO D0 |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | ICKS3 | ICKS2 | ICKS1 | ICKS0 |
| ICLK output and back-end clock is line-locked clock LLC from decoder | X | X | 0 | 0 |
| ICLK output and back-end clock is XCLK from X port | X | X | 0 | 1 |
| ICLK output is LLC and back-end clock is LLC2 clock | X | $\mathrm{X}(2)$ | 1 | 0 |
| Back-end clock is the ICLK input | X | X | 1 | 1 |
| IDQ pin carries the data qualifier | X | 0 | X | X |
| IDQ pin carries a gated back-end clock (IDQ AND CLK) | X | 1 | X | X |
| IDQ generation only for valid data | 0 | X | X | X |
| IDQ qualifies valid data inside the scaling region and all data outside the <br> scaling region | 1 | X | X | X |

## Notes

1. Although the ICLKO I/O is independent of ICKS2 and ICKS3, this selection can only be used if ICKS2 = 1 .
2. $X=$ don't care.

### 18.2.5.2 Subaddresses 83 H to 87 H

Table 194 X port I/O enable and output clock phase control; global set 83H[5:4]

| OUTPUT CLOCK PHASE CONTROL | CONTROL BITS D5 AND D4 |  |
| :--- | :---: | :---: |
|  | XPCK1 | XPCK0 |
| XCLK default output phase, recommended value | 0 | 0 |
| XCLK output inverted | 0 | 1 |
| XCLK phase shifted by about 3 ns | 1 | 0 |
| XCLK output inverted and shifted by about 3 ns | 1 | 1 |

Table 195 X port I/O enable and output clock phase control; global set $83 \mathrm{H}[2: 0]$

| X PORT I/O ENABLE | CONTROL BITS D2 TO DO |  |  |
| :---: | :---: | :---: | :---: |
|  | XRQT | XPE1 | XPE0 |
| X port output is disabled by software | X ${ }^{(1)}$ | 0 | 0 |
| X port output is enabled by software | X | 0 | 1 |
| $X$ port output is enabled by pin XTRI at logic 0 | X | 1 | 0 |
| X port output is enabled by pin XTRI at logic 1 | X | 1 | 1 |
| XRDY output signal is A/B task flag from event handler ( $\mathrm{A}=1$ ) | 0 | X | X |
| XRDY output signal is ready signal from scaler path (XRDY $=1$ means SAA7108E; SAA7109E is ready to receive data) | 1 | X | X |

## Note

1. $X=$ don't care

## PC-CODEC

Table 196 I port signal definitions; global set 84H[7:6] and 86H[5]

| I PORT SIGNAL DEFINITIONS | CONTROL BITS |  |  |
| :--- | :---: | :---: | :---: |
|  | 86H[5] | $\mathbf{8 4 H [ 7 : 6 ] ~}$ |  |
|  | IDG02 | IDG01 | IDG00 |
| IGP0 is output field ID, as defined by OFIDC[90H[6]] | 0 | 0 | 0 |
| IGP0 is A/B task flag, as defined by CONLH[90H[7]] | 0 | 0 | 1 |
| IGP0 is sliced data flag, framing the sliced VBI-data at the I port | 0 | 1 | 0 |
| IGP0 is set to logic 0 (default polarity) | 0 | 1 | 1 |
| IGP0 is the output FIFO almost filled flag | 1 | 0 | 0 |
| IGP0 is the output FIFO overflow flag | 1 | 0 | 1 |
| IGP0 is the output FIFO almost full flag, level to be programmed in subaddress 86H | 1 | 1 | 0 |
| IGP0 is the output FIFO almost empty flag, level to be programmed in subaddress 86H | 1 | 1 | 1 |

Table 197 I port signal definitions; global set 84H[5:4] and 86H[4]

| I PORT SIGNAL DEFINITIONS | CONTROL BITS |  |  |
| :--- | :---: | :---: | :---: |
|  | 86H[4] | $84 \mathrm{H}[5: 4]$ |  |
|  | IDG12 | IDG11 | IDG10 |
| IGP1 is output field ID, as defined by OFIDC[90H[6]] | 0 | 0 | 0 |
| IGP1 is A/B task flag, as defined by CONLH[90H[7]] | 0 | 0 | 1 |
| IGP1 is sliced data flag, framing the sliced VBI-data at the I port | 0 | 1 | 0 |
| IGP1 is set to logic 0 (default polarity) | 0 | 1 | 1 |
| IGP1 is the output FIFO almost filled flag | 1 | 0 | 0 |
| IGP1 is the output FIFO overflow flag | 1 | 0 | 1 |
| IGP1 is the output FIFO almost full flag, level to be programmed in subaddress 86H | 1 | 1 | 0 |
| IGP1 is the output FIFO almost empty flag, level to be programmed in subaddress 86H | 1 | 1 | 1 |

Table 198 I port output signal definitions; global set $84 \mathrm{H}[3: 0]$; note 1

| I PORT OUTPUT SIGNAL DEFINITIONS | CONTROL BITS D3 TO D0 |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | IDV1 | IDVO | IDH1 | IDH0 |
| IGPH is a H-gate signal, framing the scaler output | X | X | 0 | 0 |
| IGPH is an extended H-gate (framing H-gate during scaler output and scaler <br> input H-reference outside the scaler window) | X | X | 0 | 1 |
| IGPH is a horizontal trigger pulse, on active going edge of H-gate | X | X | 1 | 0 |
| IGPH is a horizontal trigger pulse, on active going edge of extended H-gate | X | X | 1 | 1 |
| IGPV is a V-gate signal, framing scaled output lines | 0 | 0 | X | X |
| IGPV is the V-reference signal from scaler input | 0 | 1 | X | X |
| IGPV is a vertical trigger pulse, derived from V-gate | 1 | 0 | X | X |
| IGPV is a vertical trigger pulse derived from input V-reference | 1 | 1 | X | X |

## Note

1. $X=$ don't care.

## PC-CODEC

Table $199 \times$ port signal definitions text slicer; global set $85 \mathrm{H}[7: 5]$; note 1

| X PORT SIGNAL DEFINITIONS TEXT SLICER | CONTROL BITS D7 TO D5 |  |  |
| :---: | :---: | :---: | :---: |
|  | ISWP1 | ISWPO | ILLV |
| Video data limited to range 1 to 254 | X | X | 0 |
| Video data limited to range 8 to 247 | X | X | 1 |
| Dword byte swap, influences serial output timing D0 D1 D2 D3 $\Rightarrow$ FF 0000 SAV CB0 Y0 C $\mathrm{C}_{\mathrm{R}} 0 \mathrm{Y} 1$ | 0 | 0 | X |
| D1 D0 D3 D2 $\Rightarrow 00 \mathrm{FF}$ SAV $00 \mathrm{Y} 0 \mathrm{C}_{\mathrm{B}} 0 \mathrm{Y} 1 \mathrm{C}_{\mathrm{R}} 0$ | 0 | 1 | X |
| D2 D3 D0 D1 $\Rightarrow 00$ SAV FF $00 \mathrm{C}_{\mathrm{R}} 0 \mathrm{Y} 1 \mathrm{C}_{\mathrm{B}} 0 \mathrm{Y} 0$ | 1 | 0 | X |
| D3 D2 D1 D0 $\Rightarrow$ SAV 0000 FF Y1 C $\mathrm{R}^{0} 0 \mathrm{Y} 0 \mathrm{C}_{\mathrm{B}} 0$ | 1 | 1 | X |

## Note

1. $\mathrm{X}=$ don't care.

Table 200 I port reference signal polarities; global set $85 \mathrm{H}[4: 0]$; note 1

| I PORT REFERENCE SIGNAL POLARITIES |  | CONTROL BITS D4 TO DO |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | IG1P | IRVP | IRHP | IDQP |  |
| IDQ at default polarity (1 = active) | X | X | X | X | 0 |  |
| IDQ is inverted | X | X | X | X | 1 |  |
| IGPH at default polarity (1 = active) | X | X | X | 0 | X |  |
| IGPH is inverted | X | X | X | 1 | X |  |
| IGPV at default polarity (1 = active) | X | X | 0 | X | X |  |
| IGPV is inverted | X | X | 1 | X | X |  |
| IGP1 at default polarity | X | 0 | X | X | X |  |
| IGP1 is inverted | X | 1 | X | X | X |  |
| IGP0 at default polarity | 0 | X | X | X | X |  |
| IGP0 is inverted | 1 | X | X | X | X |  |

## Note

1. $X=$ don't care.

## PC-CODEC

Table 201 I port FIFO flag control and arbitration; global set 86H[7:4]; note 1

| FUNCTION | CONTROL BITS D7 TO D4 |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | VITX1 | VITX0 | IDG02 | IDG12 |
| See subaddress 84H: IDG11 and IDG10 | X | X | X | 0 |
|  | X | X | X | 1 |
| See subaddress 84H: IDG01 and IDG00 | X | X | 0 | X |
|  | X | X | 1 | X |
| I port signal definitions |  |  |  |  |
| I port data output inhibited | 0 | 0 | X | X |
| Only video data are transferred | 0 | 1 | X | X |
| Only text data are transferred (no EAV, SAV will occur) | 1 | 0 | X | X |
| Text and video data are transferred, text has priority | 1 | 1 | X | X |

## Note

1. $X=$ don't care.

Table 202 I port FIFO flag control and arbitration; global set 86H[3:0]; note 1

| I PORT FIFO FLAG CONTROL AND ARBITRATION |  | CONTROL BITS D3 TO DO |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | FFL1 | FFLO | FEL1 | FEL0 |  |
| FAE FIFO flag almost empty level |  |  |  |  |  |
| <16 Dwords | X | X | 0 | 0 |  |
| <8 Dwords | X | X | 0 | 1 |  |
| <4 Dwords | X | X | 1 | 0 |  |
| 0 Dwords | X | X | 1 | 1 |  |
| FAF FIFO flag almost full level |  |  |  |  |  |
| 216 Dwords | 0 | 0 | X | X |  |
| $\geq 24$ Dwords | 0 | 1 | X | X |  |
| $\geq 28$ Dwords | 1 | 0 | X | X |  |
| 32 Dwords | 1 | 1 | X | X |  |

## Note

1. $X=$ don't care.

## PC-CODEC

Table 203 I port I/O enable, output clock and gated clock phase control; global set 87H[7:4]; note 1

| OUTPUT CLOCK AND GATED CLOCK PHASE CONTROL | CONTROL BITS D7 TO D4 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | IPCK3 ${ }^{(2)}$ | IPCK2 ${ }^{(2)}$ | IPCK1 | IPCK0 |
| ICLK default output phase | X | X | 0 | 0 |
| ICLK phase shifted by $1 / 2$ clock cycle $\Rightarrow$ recommended for ICKS1 $=1$ and ICKS0 $=0$ (subaddress 80H) | X | X | 0 | 1 |
| ICLK phase shifted by about 3 ns | X | X | 1 | 0 |
| ICLK phase shifted by $1 / 2$ clock cycle + approximately $3 \mathrm{~ns} \Rightarrow$ alternatively to setting '01’ | X | X | 1 | 1 |
| IDQ = gated clock default output phase | 0 | 0 | X | X |
| IDQ = gated clock phase shifted by $1 / 2$ clock cycle $\Rightarrow$ recommended for gated clock output | 0 | 1 | X | X |
| IDQ = gated clock phase shifted by approximately 3 ns | 1 | 0 | X | X |
| IDQ = gated clock phase shifted by $1 / 2$ clock cycle + approximately $3 \mathrm{~ns} \Rightarrow$ alternatively to setting '01' | 1 | 1 | X | X |

## Notes

1. $X=$ don't care.
2. IPCK3 and IPCK2 only affects the gated clock (subaddress 80 H , bit ICKS2 = 1).

Table 204 I port I/O enable, output clock and gated clock phase control; global set 87H[1:0]

| I PORT I/O ENABLE |  | CONTROL BITS D1 AND D0 |  |
| :--- | :---: | :---: | :---: |
|  |  | IPE0 |  |
| I port output is disabled by software | 0 | 0 |  |
| I port output is enabled by software | 0 | 1 |  |
| I port output is enabled by pin ITRI at logic 0 | 1 | 0 |  |
| I port output is enabled by pin ITRI at logic 1 | 1 | 1 |  |

### 18.2.5.3 Subaddress 88 H

Table 205 Power save control; global set 88H[7:4]; note 1

| POWER SAVE CONTROL | CONTROL BITS D7 TO D4 |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | CH4EN | CH2EN | SWRST ${ }^{(2)}$ | DPROG |
| DPROG = 0 after reset | X | X | X | 0 |
| DPROG = 1 can be used to assign that the device has been <br> programmed; this bit can be monitored in the scalers status byte, <br> bit PRDON; if DPROG was set to logic 1 and PRDON status bit <br> shows a logic 0 a power-up or start-up fail has occurred | X | X | X | 1 |
| Scaler path is reset to its idle state, software reset |  |  |  |  |
| Scaler is switched back to operation | X | X | 0 | X |
| AD1x analog channel is in power-down mode | X | X | 1 | X |
| AD1x analog channel is active | X | 0 | X | X |
| AD2x analog channel is in power-down mode | X | 1 | X | X |
| AD2x analog channel is active | 0 | X | X | X |

## Notes

1. $\mathrm{X}=$ don't care.
2. Bit SWRST is now located here.

Table 206 Power save control; global set 88H[3] and 88H[1:0]; note 1

| POWER SAVE CONTROL | CONTROL BITS D3, D1 AND D0 |  |  |
| :--- | :---: | :---: | :---: |
|  | SLM3 | SLM1 | SLM0 |
| Decoder and VBI slicer are in operational mode | X | X | 0 |
| Decoder and VBI slicer are in Power-down mode; scaler only operates, if scaler <br> input and ICLK source is the X port (refer to subaddresses 80H and 91H/C1H) | X | X | 1 |
| Scaler is in operational mode | X | 0 | X |
| Scaler is in Power-down mode; scaler in Power-down stops I port output | X | 1 | X |
| Audio clock generation active | 0 | X | X |
| Audio clock generation in Power-down and output disabled | 1 | X | X |

## Note

1. $X=$ don't care.

## PC-CODEC

### 18.2.5.4 Subaddress 8FH

Table 207 Status information scaler part; 8FH[7:0]; read only register

| BIT | $\mathbf{I}^{2} \mathbf{C}$-BUS <br> STATUS BIT | FUNCTION(1) |
| :---: | :---: | :--- |
| D7 | XTRI | status on input pin XTRI, if not used for 3-state control, usable as hardware flag for software <br> use |
| D6 | ITRI | status on input pin ITRI, if not used for 3-state control, usable as hardware flag for software <br> use |
| D5 | FFIL | status of the internal 'FIFO almost filled' flag |
| D4 | FFOV | status of the internal 'FIFO overflow' flag |
| D3 | PRDON | copy of bit DPROG, can be used to detect power-up and start-up fails |
| D2 | ERROF | error flag of scalers output formatter, normally set, if the output processing needs to be <br> interrupted, due to input/output data rate conflicts, e.g. if output data rate is much too low and <br> all internal FIFO capacity used |
| D1 | FIDSCI | status of the field sequence ID at the scalers input |
| D0 | FIDSCO | status of the field sequence ID at the scalers output, scaler processing dependent |

## Note

1. Status information is unsynchronized and shows the actual status at the time of $\mathrm{I}^{2} \mathrm{C}$-bus read.

### 18.2.5.5 Subaddresses 90 H and COH

Table 208 Task handing control; register set A [90H[7:6]] and B [COH[7:6]]; note 1

| EVENT HANDLER CONTROL | CONTROL BITS D7 AND D6 |  |
| :--- | :---: | :---: |
|  | CONLH | OFIDC |
| Output field ID is field ID from scaler input | X | 0 |
| Output field ID is task status flag, which changes every time an selected task <br> is activated (not synchronized to input field ID) | X | 1 |
| Scaler SAV/EAV byte bit D7 and task flag = 1, default | 0 | X |
| Scaler SAV/EAV byte bit D7 and task flag =0 | 1 | X |

## Note

1. $X=$ don't care.

Table 209 Task handling control; register set A [90H[5:3]] and B [COH[5:3]]

| EVENT HANDLER CONTROL | CONTROL BITS D5 TO D3 |  |  |
| :--- | :---: | :---: | :---: |
|  | FSKP2 | FSKP1 | FSKP0 |
| Active task is carried out directly | 0 | 0 | 0 |
| 1 field is skipped before active task is carried out | 0 | 0 | 1 |
| $\ldots$ fields are skipped before active task is carried out | $\ldots$ | $\ldots$ | $\ldots$ |
| 6 fields are skipped before active task is carried out | 1 | 1 | 0 |
| 7 fields are skipped before active task is carried out | 1 | 1 | 1 |

## PC-CODEC

Table 210 Task handling control; register set A [90H[2:0]] and B [COH[2:0]]; note 1

| EVENT HANDLER CONTROL | CONTROL BITS D2 TO D0 |  |  |
| :--- | :---: | :---: | :---: |
|  | RPTSK | STRC1 | STRC0 |
| Event handler triggers immediately after finishing a task | X | 0 | 0 |
| Event handler triggers with next V-sync | X | 0 | 1 |
| Event handler triggers with field ID $=0$ | X | 1 | 0 |
| Event handler triggers with field ID $=1$ | X | 1 | 1 |
| If active task is finished, handling is taken over by the next task | 0 | X | X |
| Active task is repeated once, before handling is taken over by the next task | 1 | X | X |

## Note

1. $X=$ don't care.

### 18.2.5.6 Subaddresses 91 H to 93 H

Table 211 X port formats and configuration; register set $\mathrm{A}[91 \mathrm{H}[7: 3]$ ] and B [C1H[7:3]]; note 1

| SCALER INPUT FORMAT AND CONFIGURATION SOURCE SELECTION | CONTROL BITS D7 TO D3 |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | CONLV | HLDFV | SCSRC1 | SCSRC0 | SCRQE |
| Only if XRQT[83H[2]] = 1: scaler input source reacts on SAA7108E; SAA7109E request | X | X | X | X | 0 |
| Scaler input source is a continuous data stream, which cannot be interrupted (must be logic 1 if SAA7108E; SAA7109E decoder part is source of scaler or XRQT[83H[2]] = 0) | X | X | X | X | 1 |
| Scaler input source is data from decoder, data type is provided according to Table 44 | X | X | 0 | 0 | X |
| Scaler input source is $\mathrm{Y}-\mathrm{C}_{B}-\mathrm{C}_{\mathrm{R}}$ data from X port | X | X | 0 | 1 | X |
| Scaler input source is raw digital CVBS from selected analog channel, for backward compatibility only, further use is not recommended | X | X | 1 | 0 | X |
| Scaler input source is raw digital CVBS (or 16 -bit $Y+C_{B}-C_{R}$, if no 16-bit output are active) from $X$ port | X | X | 1 | 1 | X |
| SAV/EAV code bits D6 and D5 (F and V) may change between SAV and EAV | X | 0 | X | X | X |
| SAV/EAV code bits D6 and D5 (F and V) are synchronized to scalers output line start | X | 1 | X | X | X |
| SAV/EAV code bit D5 (V) and V gate on pin IGPV as generated by the internal processing; see Fig. 44 | 0 | X | X | X | X |
| SAV/EAV code bit D5 (V) and V gate are inverted | 1 | X | X | X | X |

## Note

1. $X=$ don't care.

## PC-CODEC

Table 212 X port formats and configuration; register set A [91H[2:0]] and B [C1H[2:0]]; note 1

| SCALER INPUT FORMAT AND CONFIGURATION FORMAT <br> CONTROL |  | CONTROL BITS D2 TO DO |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | FSC2 $^{(2)}$ | FSC1 $^{(2)}$ | FSC0 |  |
| Input is $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$ like sampling scheme | X | X | 0 |  |
| Input is $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 1: 1$ like sampling scheme | X | X | 1 |  |
| Chroma is provided every line, default | 0 | 0 | X |  |
| Chroma is provided every 2nd line | 0 | 1 | X |  |
| Chroma is provided every 3rd line | 1 | 0 | X |  |
| Chroma is provided every 4th line | 1 | 1 | X |  |

## Notes

1. $X=$ don't care.
2. FSC2 and FSC1 only to be used, if $X$ port input source don't provide chroma information for every input line. $X$ port input stream must contain dummy chroma bytes.

Table 213 X port input reference signal definitions; register set A [92H[7:4]] and B [C2H[7:4]]; note 1

| X PORT INPUT REFERENCE SIGNAL DEFINITIONS | CONTROL BITS D7 TO D4 |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | XFDV | XFDH | XDV1 | XDV0 |
| Rising edge of XRV input and decoder V123 is vertical reference | X | X | X | 0 |
| Falling edge of XRV input and decoder V123 is vertical reference | X | X | X | 1 |
| XRV is a V-sync or V gate signal | X | X | 0 | X |
| XRV is a frame sync, V pulses are generated internally on both edges of <br> FS input | X | X | 1 | X |
| X port field ID is state of XRH at reference edge on XRV (defined by <br> XFDV) | X | 0 | X | X |
| Field ID (decoder and X port field ID) is inverted | X | 1 | X | X |
| Reference edge for field detection is falling edge of XRV | 0 | X | X | X |
| Reference edge for field detection is rising edge of XRV | 1 | X | X | X |

## Note

1. $X=$ don't care.

## PC-CODEC

Table $214 \times$ port input reference signal definitions; register set A [92H[3:0]] and B [C2H[3:0]]; note 1

| X PORT INPUT REFERENCE SIGNAL DEFINITIONS | CONTROL BITS D3 TO DO |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | XCODE | XDH | XDQ | XCKS |
| XCLK input clock and XDQ input qualifier are needed | X | X | X | 0 |
| Data rate is defined by XCLK only, no XDQ signal used | X | X | X | 1 |
| Data are qualified at XDQ input at logic 1 | X | X | 0 | X |
| Data are qualified at XDQ input at logic 0 | X | X | 1 | X |
| Rising edge of XRH input is horizontal reference | X | 0 | X | X |
| Falling edge of XRH input is horizontal reference | X | 1 | X | X |
| Reference signals are taken from XRH and XRV | 0 | X | X | X |
| Reference signals are decoded from EAV and SAV | 1 | X | X | X |

## Note

1. $X=$ don't care.

Table 215 I port output format and configuration; register set $A$ [ $93 \mathrm{H}[7: 5]]$ and $\mathrm{B}[\mathrm{C} 3 \mathrm{H}[7: 5]]$; note 1

| I PORT OUTPUT FORMATS AND CONFIGURATION | CONTROL BITS D7 TO D5 |  |  |
| :--- | :---: | :---: | :---: |
|  | ICODE | I8_16 | FYSK |
| All lines will be output | X | X | 0 |
| Skip the number of leading Y only lines, as defined by FOI1 and FOI0 | X | X | 1 |
| Dwords are transferred byte wise, see subaddress 85H bits ISWP1 and ISWP0 | X | 0 | X |
| Dwords are transferred 16-bit word wise via IPD and HPD, see subaddress 85H bits <br> ISWP1 and ISWP0 | X | 1 | X |
| No ITU 656 like SAV/EAV codes are available | 0 | X | X |
| ITU 656 like SAV/EAV codes are inserted in the output data stream, framed by a <br> qualifier | 1 | X | X |

## Note

1. $X=$ don't care.

## PC-CODEC

Table 216 I port output format and configuration; register set A [93H[4:0]] and B [C3H[4:0]]; note 1

| I PORT OUTPUT FORMATS AND CONFIGURATION | CONTROL BITS D4 TO D0 |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | FOI1 | FOIO | FSI2 | FSI1 | FSIO |
| 4:2:2 Dword formatting | X | X | 0 | 0 | 0 |
| 4:1:1 Dword formatting | X | X | 0 | 0 | 1 |
| $4: 2: 0$, only every 2nd line $Y+C_{B}-C_{R}$ output, in between Y only output | X | X | 0 | 1 | 0 |
| 4:1:0, only every 4th line $Y+C_{B}-C_{R}$ output, in between Y only output | X | X | 0 | 1 | 1 |
| Y only | X | X | 1 | 0 | 0 |
| Not defined | X | X | 1 | 0 | 1 |
| Not defined | X | X | 1 | 1 | 0 |
| Not defined | X | X | 1 | 1 | 1 |
| No leading $Y$ only line, before 1 st $Y+C_{B}-C_{R}$ line is output | 0 | 0 | X | X | X |
| 1 leading $Y$ only line, before 1st $Y+C_{B}-C_{R}$ line is output | 0 | 1 | X | X | X |
| 2 leading $Y$ only lines, before 1st $Y+C_{B}-C_{R}$ line is output | 1 | 0 | X | X | X |
| 3 leading Y only lines, before 1st $\mathrm{Y}+\mathrm{C}_{B}-\mathrm{C}_{\mathrm{R}}$ line is output | 1 | 1 | X | X | X |

## Note

1. $X=$ don't care.

### 18.2.5.7 Subaddresses 94H to 9BH

Table 217 Horizontal input window start; register set A [94H[7:0]; 95H[3:0]] and B [C4H[7:0]; C5H[3:0]]

| HORIZONTAL INPUT ACQUISITION WINDOW DEFINITION OFFSET IN X (HORIZONTAL) DIRECTION ${ }^{(1)}$ | CONTROL BITS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { A [95H[3:0]] } \\ & \text { B [C5H[3:0]] } \end{aligned}$ |  |  |  | A [94H[7:0]] <br> B [C4H[7:0]] |  |  |  |  |  |  |  |
|  | X011 | X010 | XO9 | XO8 | X07 | XO6 | XO5 | XO4 | X03 | XO2 | X01 | XOO |
| A minimum of 2 should be kept, due to a line counting mismatch | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Odd offsets are changing the $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ sequence in the output stream to $\mathrm{C}_{R}-\mathrm{C}_{\mathrm{B}}$ sequence | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Maximum possible pixel offset $=4095$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Note

1. Reference for counting are luminance samples.

## PC-CODEC

Table 218 Horizontal input window length; register set A [96H[7:0]; 97H[3:0]] and B [C6H[7:0]; C7H[3:0]]

| HORIZONTAL INPUT ACQUISITION WINDOW DEFINITION INPUT WINDOW LENGTH IN X (HORIZONTAL) DIRECTION ${ }^{(1)}$ | CONTROL BITS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { A [97H[3:0]] } \\ & \text { B [C7H[3:0]] } \end{aligned}$ |  |  |  | A [96H[7:0]]B [C6H[7:0]] |  |  |  |  |  |  |  |
|  | XS11 | XS10 | XS9 | XS8 | XS7 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XSO |
| No output | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Odd lengths are allowed, but will be rounded up to even lengths | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Maximum possible number of input pixels $=4095$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Note

1. Reference for counting are luminance samples.

Table 219 Vertical input window start; register set A [98H[7:0]; 99H[3:0]] and B [C8H[7:0]; C9H[3:0]]

| VERTICAL INPUT ACQUISITION WINDOW DEFINITION OFFSET IN Y (VERTICAL) DIRECTION | CONTROL BITS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { A [99H[3:0]] } \\ & \text { B [C9H[3:0]] } \end{aligned}$ |  |  |  | A [98H[7:0]] <br> B [C8H[7:0]] |  |  |  |  |  |  |  |
|  | YO11 | YO10 | YO9 | YO8 | YO7 | YO6 | YO5 | YO4 | YO3 | YO2 | YO1 | YOO |
| Line offset $=0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Line offset = 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Maximum line offset $=4095$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Note

1. For trigger condition: STRC[1:0] $90 \mathrm{H}[1: 0]=00 ; \mathrm{YO}+\mathrm{YS}>$ (number of input lines per field -2 ), will result in field dropping. Other trigger conditions: $\mathrm{YO}>$ (number of input lines per field -2 ), will result in field dropping.

Table 220 Vertical input window length; register set A [9AH[7:0]; 9BH[3:0]] and B [CAH[7:0]; CBH[3:0]]

| VERTICAL INPUT ACQUISITION WINDOW DEFINITION INPUT WINDOW LENGTH IN Y (VERTICAL) DIRECTION ${ }^{(1)}$ | CONTROL BITS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | A [9BH[3:0]] <br> B [CBH[3:0]] |  |  |  | A [9AH[7:0]] <br> B [CAH[7:0]] |  |  |  |  |  |  |  |
|  | YS11 | YS10 | YS9 | YS8 | YS7 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YSO |
| No input lines | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 input line | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Maximum possible number of input lines $=4095$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Note

1. For trigger condition: $\operatorname{STRC}[1: 0] 90 \mathrm{H}[1: 0]=00 ; \mathrm{YO}+\mathrm{YS}>$ (number of input lines per field -2 ), will result in field dropping. Other trigger conditions: $\mathrm{YS}>$ (number of input lines per field - 2), will result in field dropping.

## PC-CODEC

### 18.2.5.8 Subaddresses 9CH to 9FH

Table 221 Horizontal output window length; register set A [9CH[7:0]; 9DH[3:0]] and B [CCH[7:0]; $\mathrm{CDH}[3: 0]$ ]

| HORIZONTAL OUTPUT ACQUISITION WINDOW DEFINITION NUMBER OF DESIRED OUTPUT PIXEL IN X (HORIZONTAL) DIRECTION ${ }^{(1)}$ | CONTROL BITS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { A [9DH[3:0]] } \\ & \text { B [CDH[3:0]] } \end{aligned}$ |  |  |  | $\begin{aligned} & \text { A [9CH[7:0]] } \\ & \text { В [CCH[7:0]] } \end{aligned}$ |  |  |  |  |  |  |  |
|  | XD11 | XD10 | XD9 | XD8 | XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XDO |
| No output | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Odd lengths are allowed, but will be filled up to even lengths | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Maximum possible number of input pixels = 4095; note 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Notes

1. Reference for counting are luminance samples.
2. If the desired output length is greater than the number of scaled output pixels, the last scaled pixel is repeated.

Table 222 Vertical output window length; register set A [9EH[7:0]; 9FH[3:0]] and B [CEH[7:0]; CFH[3:0]]

| VERTICAL OUTPUT ACQUISITION WINDOW DEFINITION NUMBER OF DESIRED OUTPUT LINES IN Y (VERTICAL) DIRECTION | CONTROL BITS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | A [9FH[3:0]] <br> B [CFH[3:0]] |  |  |  | A [9EH[7:0]] <br> B [CEH[7:0]] |  |  |  |  |  |  |  |
|  | YD11 | YD10 | YD9 | YD8 | YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YDO |
| No output | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 pixel | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Maximum possible number of output lines = 4095; note 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Note

1. If the desired output length is greater than the number of scaled output lines, the processing is cut.

### 18.2.5.9 Subaddresses AOH to A 2 H

Table 223 Horizontal prescaling; register set A [AOH[5:0]] and B [DOH[5:0]]

| HORIZONTAL INTEGER PRESCALING RATIO (XPSC) | CONTROL BITS D5 TO D0 |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  | XPSC5 | XPSC4 | XPSC3 | XPSC2 | XPSC1 | XPSC0 |
| Not allowed | 0 | 0 | 0 | 0 | 0 | 0 |
| Downscale $=1$ | 0 | 0 | 0 | 0 | 0 | 1 |
| Downscale $=1 / 2$ | 0 | 0 | 0 | 0 | 1 | 0 |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| Downscale $=1 / 63$ | 1 | 1 | 1 | 1 | 1 | 1 |

Table 224 Accumulation length; register set A [A1H[5:0]] and B [D1H[5:0]]

| HORIZONTAL PRESCALER ACCUMULATION <br> SEQUENCE LENGTH (XACL) | CONTROL BITS D5 TO D0 |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |

Table 225 Prescaler DC gain and FIR prefilter control; register set A [A2H[7:4]] and B [D2H[7:4]]; note 1

| FIR PREFILTER CONTROL | CONTROL BITS D7 TO D4 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | PFUV1 | PFUVO | PFY1 | PFYO |
| Luminance FIR filter bypassed | X | X | 0 | 0 |
| $H \_y(z)=1 / 4\left(\begin{array}{lll}1 & 1\end{array}\right)$ | X | X | 0 | 1 |
| H_y z$)=1 / 8(-111.754 .51 .751$-1) | X | X | 1 | 0 |
| $\mathrm{H} \_\mathrm{y}(\mathrm{z})=1 / 8$ (12221) | X | X | 1 | 1 |
| Chrominance FIR filter bypassed | 0 | 0 | X | X |
| H_uv(z) $=1 / 4(121)$ | 0 | 1 | X | X |
| H_uv $(z)=1 / 32$ (3 81083 ) | 1 | 0 | X | X |
| H_uv(z) = 1/8(12221) | 1 | 1 | X | X |

## Note

1. $X=$ don't care.

Table 226 Prescaler DC gain and FIR prefilter control; register set A [A2H[3:0]] and B [D2H[3:0]]; note 1

| PRESCALER DC GAIN | CONTROL BITS D3 TO D0 |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | XC2_1 | XDCG2 | XDCG1 | XDCG0 |
| Prescaler output is renormalized by gain factor $=1$ | X | 0 | 0 | 0 |
| Prescaler output is renormalized by gain factor $=1 / 2$ | X | 0 | 0 | 1 |
| Prescaler output is renormalized by gain factor $=1 / 4$ | X | 0 | 1 | 0 |
| Prescaler output is renormalized by gain factor $=1 / 8$ | X | 0 | 1 | 1 |
| Prescaler output is renormalized by gain factor $=1 / 16$ | X | 1 | 0 | 0 |
| Prescaler output is renormalized by gain factor $=1 / 32$ | X | 1 | 0 | 1 |
| Prescaler output is renormalized by gain factor $=1 / 64$ | X | 1 | 1 | 0 |
| Prescaler output is renormalized by gain factor $=1 / 128$ | X | 1 | 1 | 1 |
| Weighting of all accumulated samples is factor $1 ;$ <br> e.g. $\mathrm{XACL}=4 \Rightarrow$ sequence $1+1+1+1+1$ | 0 | X | X | X |
| Weighting of samples inside sequence is factor $2 ;$ <br> e.g. $\mathrm{XACL}=4 \Rightarrow$ sequence $1+2+2+2+1$ | 1 | X | X | X |

## Note

1. $X=$ don't care.

### 18.2.5.10 Subaddresses $A 4 H$ to $A 6 H$

Table 227 Luminance brightness control; register set A [A4H[7:0]] and B [D4H[7:0]]

| LUMINANCE <br>  | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | BRIG7 | BRIG6 | BRIG5 | BRIG4 | BRIG3 | BRIG2 | BRIG1 | BRIG0 |  |
| Value $=0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| Nominal value $=128$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| Value $=255$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |

Table 228 Luminance contrast control; register set A [A5H[7:0]] and B [D5H[7:0]]

| LUMINANCE CONTRAST <br> CONTROL | CONTROL BITS D7 TO DO |  |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | CONT7 | CONT6 | CONT5 | CONT4 | CONT3 | CONT2 | CONT1 | CONT0 |  |
| Gain $=0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| Gain $=1 / 64$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |
| Nominal gain $=64$ | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| Gain $=127 / 64$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |

Table 229 Chrominance saturation control; register set A [A6H[7:0]] and B [D6H[7:0]]

| CHROMINANCE <br> SATURATION CONTROL | CONTROL BITS D7 TO DO |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | SATN7 | SATN6 | SATN5 | SATN4 | SATN3 | SATN2 | SATN1 | SATN0 |
| Gain $=0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gain $=1 / 64$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Nominal gain $=64$ | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gain $=127 / 64$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

18.2.5.11 Subaddresses A8H to AEH

Table 230 Horizontal luminance scaling increment; register set A [A8H[7:0]; A9H[7:0]] and B [D8H[7:0]; D9H[7:0]]

| HORIZONTAL LUMINANCE <br> SCALING INCREMENT | A [A9H[7:4]] <br> B [D9H[7:4]] |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | A [A9H[3:0]] <br> B [D9H[3:0]] | A [A8H[7:4]] <br> B [D8H[7:4]] | A [A8H[3:0]] <br> B [D8H[3:0]] |  |
|  | XSCY[15:12] ${ }^{(1)}$ | XSCY[11:8] | XSCY[7:4] | XSCY[3:0] |
| Scale $=1024 / 1$ (theoretical) zoom | 0000 | 0000 | 0000 | 0000 |
| Scale $=1024 / 294, ~ l o w e r ~ l i m i t ~ d e f i n e d ~ b y ~$ <br> data path structure | 0000 | 0001 | 0010 | 0110 |
| Scale $=1024 / 1023$ zoom | 0000 | 0011 | 1111 | 1111 |
| Scale $=1$, equals 1024 | 0000 | 0100 | 0000 | 0000 |
| Scale $=1024 / 1025$ downscale | 0000 | 0100 | 0000 | 0001 |
| Scale $=1024 / 8191$ downscale | 0001 | 1111 | 1111 | 1111 |

## Note

1. Bits $\mathrm{XSCY}[15: 13]$ are reserved and are set to logic 0 .

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Table 231 Horizontal luminance phase offset; register set A [AAH[7:0]] and B [DAH[7:0]]

| HORIZONTAL LUMINANCE PHASE OFFSET | CONTROL BITS D7 TO DO |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | XPHY7 | XPHY6 | XPHY5 | XPHY4 | XPHY3 | XPHY2 | XPHY1 | XPHYO |
| Offset = 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Offset $=1 / 32$ pixel | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Offset $=32 / 32=1$ pixel | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Offset $=255 / 32$ pixel | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 232 Horizontal chrominance scaling increment; register set A [ACH[7:0]; ADH[7:0]] and B [DCH[7:0]; DDH[7:0]]

| HORIZONTAL CHROMINANCE SCALING INCREMENT | CONTROL BITS |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { A [ADH[7:4]] } \\ & \text { B [DDH[7:4]] } \end{aligned}$ | $\begin{aligned} & \text { A [ADH[3:0]] } \\ & \text { B [DDH[3:0]] } \end{aligned}$ | $\begin{aligned} & \text { A [ACH[7:4]] } \\ & \text { B [DCH[7:4]] } \end{aligned}$ | $\begin{aligned} & \text { A [ACH[3:0]] } \\ & \text { B [DCH[3:0]] } \end{aligned}$ |
|  | XSCC[15:12] ${ }^{(1)}$ | XSCC[11:8] | XSCC[7:4] | XSCC[3:0] |
| This value must be set to the luminance value $1 / 2 \mathrm{XSCY}[15: 0$ ] | 0000 | 0000 | 0000 | 0000 |
|  | 0000 | 0000 | 0000 | 0001 |
|  | 0001 | 1111 | 1111 | 1111 |

## Note

1. Bits XSCC[15:13] are reserved and are set to logic 0 .

Table 233 Horizontal chrominance phase offset; register set A [AEH[7:0]] and B [DEH[7:0]]

| HORIZONTAL CHROMINANCE PHASE OFFSET | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | XPHC7 | XPHC6 | XPHC5 | XPHC4 | XPHC3 | XPHC2 | XPHC1 | XPHCO |
| This value must be set to $1 / 2 \mathrm{XPHY}[7: 0]$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
|  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 18.2.5.12 Subaddresses BOH to BFH

Table 234 Vertical luminance scaling increment; register set $A[B 0 H[7: 0]$; $B 1 H[7: 0]]$ and $B[E 0 H[7: 0] ; E 1 H[7: 0]]$

| VERTICAL LUMINANCE SCALING INCREMENT | CONTROL BITS |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | A [B1H[7:4]] <br> B [E1H[7:4]] | $\begin{aligned} & \text { A [B1H[3:0]] } \\ & \text { B [E1H[3:0]] } \end{aligned}$ | A [BOH[7:4]] <br> B [EOH[7:4]] | A [BOH[3:0]] <br> B [EOH[3:0]] |
|  | YSCY[15:12] | YSCY[11:8] | YSCY[7:4] | YSCY[3:0] |
| Scale $=1024 / 1$ (theoretical) zoom | 0000 | 0000 | 0000 | 0001 |
| Scale = 1024/1023 zoom | 0000 | 0011 | 1111 | 1111 |
| Scale $=1$, equals 1024 | 0000 | 0100 | 0000 | 0000 |
| Scale $=1024 / 1025$ downscale | 0000 | 0100 | 0000 | 0001 |
| Scale $=1 / 63.999$ downscale | 1111 | 1111 | 1111 | 1111 |

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Table 235 Vertical chrominance scaling increment; register set A [B2H[7:0]; B3H[7:0]] and B [E2H[7:0]; E3H[7:0]]

| VERTICAL CHROMINANCE <br> SCALING INCREMENT | CONTROL BITS |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { A [B3H[7:4]] } \\ & \text { B [E3H[7:4]] } \end{aligned}$ | $\begin{aligned} & \text { A [B3H[3:0]] } \\ & \text { B [E3H[3:0]] } \end{aligned}$ | $\begin{aligned} & \text { A [B2H[7:4]] } \\ & \text { B [E2H[7:4]] } \end{aligned}$ | $\begin{aligned} & \text { A [B2H[3:0]] } \\ & \text { B [E2H[3:0]] } \end{aligned}$ |
|  | YSCC[15:12] | YSCC[11:8] | YSCC[7:4] | YSCC[3:0] |
| This value must be set to the luminance value YSCY[15:0] | 0000 | 0000 | 0000 | 0001 |
|  | 1111 | 1111 | 1111 | 1111 |

Table 236 Vertical scaling mode control; register set $A[B 4 H[4$ and 0$]$ ] and B [ $\mathrm{E} 4 \mathrm{H}[4$ and 0$]$ ]; note 1

| VERTICAL SCALING MODE CONTROL | CONTROL BITS D4 AND D0 |  |
| :--- | :---: | :---: |
|  | YMIR | YMODE |
| Vertical scaling performs linear interpolation between lines | X | 0 |
| Vertical scaling performs higher order accumulating interpolation, better alias <br> suppression | X | 1 |
| No mirroring | 0 | X |
| Lines are mirrored | 1 | X |

## Note

1. $X=$ don't care.

Table 237 Vertical chrominance phase offset '00'; register set A [B8H[7:0]] and B [E8H[7:0]]

| VERTICAL CHROMINANCE PHASE <br> OFFSET | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | YPC07 | YPC06 | YPC05 | YPC04 | YPC03 | YPC02 | YPC01 | YPC00 |  |
| Offset $=0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| Offset $=32 / 32=1$ line | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  |
| Offset $=255 / 32$ lines | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |

Table 238 Vertical luminance phase offset ' 00 '; register set A [ $\mathrm{BCH}[7: 0]$ ] and $\mathrm{B}[\mathrm{ECH}[7: 0]$ ]

| VERTICAL LUMINANCE PHASE <br> OFFSET | CONTROL BITS D7 TO D0 |  |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | YPY07 | YPY06 | YPY05 | YPY04 | YPY03 | YPY02 | YPY01 | YPY00 |  |
| Offset $=0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| Offset $=32 / 32=1$ line | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  |
| Offset $=255 / 32$ lines | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |

## PC-CODEC

## 19 PROGRAMMING START SET-UP OF DIGITAL VIDEO DECODER PART

### 19.1 Decoder part

The given values force the following behaviour of the SAA7108E; SAA7109E decoder part:

- The analog input AI11 expects an NTSC M, PAL B, D, G, H and I or SECAM signal in CVBS format; analog anti-alias filter and AGC active
- Automatic field detection enabled
- Standard ITU 656 output format enabled on the expansion port
- Contrast, brightness and saturation control in accordance with ITU standards
- Adaptive comb filter for luminance and chrominance activated
- Pins LLC, LLC2, XTOUTd, RTS0, RTS1 and RTCO are set to 3-state.

Table 239 Decoder part start set-up values for the three main standards

| $\begin{aligned} & \text { SUB } \\ & \text { ADDRESS } \\ & \text { (HEX) } \end{aligned}$ | REGISTER FUNCTION | BIT NAME ${ }^{(1)}$ | VALUES (HEX) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | NTSC M | PAL B, D, G, H AND I | SECAM |
| 00 | chip version | ID7 to ID4 | read only |  |  |
| 01 | increment delay | X, X, X, X, IDEL3 to IDEL0 | 08 | 08 | 08 |
| 02 | analog input control 1 | FUSE1, FUSE0, GUDL1, GUDL0 and MODE3 to MODE0 | C0 | C0 | C0 |
| 03 | analog input control 2 | X, HLNRS, VBSL, WPOFF, HOLDG, GAFIX, GAI28 and GAI18 | 10 | 10 | 10 |
| 04 | analog input control 3 | GAI17 to GAI10 | 90 | 90 | 90 |
| 05 | analog input control 4 | GAI27 to GAI20 | 90 | 90 | 90 |
| 06 | horizontal sync start | HSB7 to HSB0 | EB | EB | EB |
| 07 | horizontal sync stop | HSS7 to HSS0 | E0 | E0 | E0 |
| 08 | sync control | AUFD, FSEL, FOET, HTC1, HTC0, HPLL, VNOI1 and VNOIO | 98 | 98 | 98 |
| 09 | luminance control | BYPS, YCOMB, LDEL, LUBW and LUFI3 to LUFIO | 40 | 40 | 1B |
| 0A | luminance brightness control | DBRI7 to DBRI0 | 80 | 80 | 80 |
| OB | luminance contrast control | DCON7 to DCON0 | 44 | 44 | 44 |
| OC | chrominance saturation control | DSAT7 to DSAT0 | 40 | 40 | 40 |
| OD | chrominance hue control | HUEC7 to HUEC0 | 00 | 00 | 00 |
| OE | chrominance control 1 | CDTO, CSTD2 to CSTD0, DCVF, FCTC, $X$ and CCOMB | 89 | 81 | D0 |
| OF | chrominance gain control | ACGC and CGAIN6 to CGAIN0 | 2A | 2A | 80 |
| 10 | chrominance control 2 | OFFU1, OFFU0, OFFV1, OFFV0, CHBW and LCBW2 to LCBW0 | 0E | 06 | 00 |
| 11 | mode/delay control | COLO, RTP1, HDEL1, HDELO, RTP0 and YDEL2 to YDELO | 00 | 00 | 00 |

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| $\begin{aligned} & \text { SUB } \\ & \text { ADDRESS } \\ & \text { (HEX) } \end{aligned}$ | REGISTER <br> FUNCTION | BIT NAME ${ }^{(1)}$ | VALUES (HEX) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | NTSC M | PAL B, D, G, H AND I | SECAM |
| 12 | RT signal control | RTSE13 to RTSE10 and RTSE03 to RTSE00 | 00 | 00 | 00 |
| 13 | RT/X port output control | RTCE, XRHS, XRVS1, XRVS0, HLSEL and OFTS2 to OFTS0 | 00 | 00 | 00 |
| 14 | analog/ADC/compatibility control | CM99, UPTCV, AOSL1, AOSLO, XTOUTE, OLDSB, APCK1 and APCK0 | 00 | 00 | 00 |
| 15 | VGATE start, FID change | VSTA7 to VSTA0 | 11 | 11 | 11 |
| 16 | VGATE stop | VSTO7 to VSTO0 | FE | FE | FE |
| 17 | miscellaneous, VGATE configuration and MSBs | LLCE, LLC2E, X, X, X, VGPS, VSTO8 and VSTA8 | 40 | 40 | 40 |
| 18 | raw data gain control | RAWG7 to RAWG0 | 40 | 40 | 40 |
| 19 | raw data offset control | RAWO7 to RAWO0 | 80 | 80 | 80 |
| 1A to 1E | reserved | X, X, X, X, X, X, X, X | 00 | 00 | 00 |
| 1F | status byte video decoder $(\text { OLDSB = 0) }$ | INTL, HLVLN, FIDT, GLIMT, GLIMB, WIPA, COPRO and RDCAP | read only |  |  |

## Note

1. All $X$ values must be set to logic 0 .

## PC-CODEC

### 19.2 Audio clock generation part

The given values force the following behaviour of the SAA7108E; SAA7109E audio clock generation part:

- Used crystal is 24.576 MHz
- Expected field frequency is 59.94 Hz (e.g. NTSC M standard)
- Generated audio master clock frequency at pin AMCLK is $256 \times 44.1 \mathrm{kHz}=11.2896 \mathrm{MHz}$
- AMCLK is externally connected to AMXCLK (short-cut between pins K12 and J12)
- ASCLK $=32 \times 44.1 \mathrm{kHz}=1.4112 \mathrm{MHz}$
- ALRCLK is 44.1 kHz .

Table 240 Audio clock part set-up values

| SUB | REGISTER FUNCTION | BIT NAME ${ }^{(1)}$ | START VALUES |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (HEX) |  |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX |
| 30 | audio master clock cycles per field; bits 7 to 0 | ACPF7 to ACPF0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | BC |
| 31 | audio master clock cycles per field; bits 15 to 8 | ACPF15 to ACPF8 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | DF |
| 32 | audio master clock cycles per field; bits 17 and 16 | X, X, X, X, X, X, ACPF17 and ACPF16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| 33 | reserved | X, X, X, X, X, X, X, X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 34 | audio master clock nominal increment; bits 7 to 0 | ACNI7 to ACNIO | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | CD |
| 35 | audio master clock nominal increment; bits 15 to 8 | ACNI15 to ACNI8 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CC |
| 36 | audio master clock nominal increment; bits 21 to 16 | X, X, ACNI21 to ACNI16 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A |
| 37 | reserved | X, X, X, X, X, X, X, X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 38 | clock ratio AMXCLK to ASCLK | X, X, SDIV5 to SDIV0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| 39 | clock ratio ASCLK to ALRCLK | X, X, LRDIV5 to LRDIV0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| 3A | audio clock generator basic set-up | X, X, X, X, APLL, AMVR, LRPH, SCPH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 3B to 3F | reserved | X, X, X, X, X, X, X, X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |

## Note

1. All $X$ values must be set to logic 0 .

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### 19.3 Data slicer and data type control part

The given values force the following behaviour of the SAA7108E; SAA7109E VBI data slicer part:

- Closed captioning data is expected at line 21 of field 1 ( $60 \mathrm{~Hz} / 525$ line system)
- All other lines are processed as active video
- Sliced data are framed by ITU 656 like SAV/EAV sequence (DID[5:0] $=3 E H \Rightarrow$ MSB of SAV/EAV = 1).

Table 241 Data slicer start set-up values

| SUB ADDRESS (HEX) | REGISTER FUNCTION | BIT NAME ${ }^{(1)}$ | START VALUES |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX |
| 40 | slicer control 1 | $\begin{aligned} & \text { X, HAM_N, FCE, HUNT_N, X, X, } \\ & \text { X, X } \end{aligned}$ | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 |
| 41 to 53 | line control register 2 to 20 | LCRn_7 to LCRn_0 ( $\mathrm{n}=2$ to 20) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |
| 54 | line control register 21 | LCR21_7 to LCR21_0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F |
| 55 to 57 | line control register 22 to 24 | LCRn_7 to LCRn_0 ( $\mathrm{n}=22$ to 24) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |
| 58 | programmable framing code | FC7 to FC0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 59 | horizontal offset for slicer | HOFF7 to HOFF0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47 |
| 5A | vertical offset for slicer | VOFF7 to VOFF0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 ${ }^{(2)}$ |
| 5B | field offset and MSBs for horizontal and vertical offset | FOFF, RECODE, X, VOFF8, X, HOFF10 to HOFF8 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | $83^{(2)}$ |
| 5C | reserved | X, X, X, X, X, X, X, X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 5D | header and data identification code control | FVREF, X , DID5 to DID0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E |
| 5E | sliced data identification code | X, X, SDID5 to SDID0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 5F | reserved | X, X, X, X, X, X, X, X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 60 | slicer status byte 0 | -, FC8V, FC7V, VPSV, PPV, CCV, |  |  |  | ad-o |  | re | gist |  |  |
| 61 | slicer status byte 1 | -, -, F21_N, LN8 to LN4 |  |  |  | ad-o | only | re | gist |  |  |
| 62 | slicer status byte 2 | LN3 to LN0, DT3 to DT0 |  |  |  | ad-o | only | re | gist |  |  |

## Notes

1. All $X$ values must be set to logic 0 .
2. Changes for $50 \mathrm{~Hz} / 625$ line systems: subaddress $5 \mathrm{AH}=03 \mathrm{H}$ and subaddress $5 \mathrm{BH}=03 \mathrm{H}$.

### 19.4 Scaler and interfaces

Table 242 shows some examples for the scaler programming where:

- prsc = prescale ratio
- fisc = fine scale ratio
- vsc = vertical scale ratio.

The ratio is defined as: $\frac{\text { number of input pixel }}{\text { number of output pixel }}$
In the following settings the VBI data slicer is inactive.
To activate the VBI data slicer, VITX[1:0] 86H[7:6] has to be set to ' 11 '. Depending on the VBI data slicer settings, the sliced VBI data is inserted after the end of the scaled video lines, if the regions of the VBI data slicer and scaler overlap.

To compensate for the running-in of the vertical scaler, the vertical input window lengths are extended by 2 to 290 lines, respectively 242 lines for XS, but the scaler increment calculations are done with 288, respectively 240 lines.

### 19.4.1 Trigger condition

For trigger condition STRC[1:0] 90H[1:0] not equal '00'.
If the value of ( $\mathrm{YO}+\mathrm{YS}$ ) is $\geq 262$ (NTSC), and 312 (PAL) the output field rate is reduced to 30 Hz and 25 Hz respectively.

Horizontal and vertical offsets ( XO and YO ) have to be used to adjust the displayed video in the display window. As this adjustment is application dependent, the listed values are only dummy values.

### 19.4.2 MAXIMUM ZOOM FACTOR

The maximum zoom factor is dependent on the back-end data rate and is therefore back-end clock and data format dependent ( 8 or 16-bit output). The maximum horizontal zoom is limited to approximately 3.5 , due to internal data path restrictions.

### 19.4.3 EXAMPLES

Table 242 Example of configurations

| EXAMPLE NUMBER | SCALER SOURCE AND REFERENCE EVENTS | INPUT WINDOW | OUTPUT WINDOW | SCALE RATIOS |
| :---: | :---: | :---: | :---: | :---: |
| 1 | analog input to 8-bit I port output, with SAV/EAV codes, 8-bit serial byte stream decoder output at $X$ port; acquisition trigger at falling edge vertical and rising edge horizontal reference signal; H and V gates on IGPH and IGPV, IGPO $=$ VBI sliced data flag, IGP1 = FIFO almost full, level $\geq 24$, IDQ qualifier logic 1 active | $720 \times 240$ | $720 \times 240$ | $\begin{aligned} & \hline \text { prsc = 1; } \\ & \text { fisc = 1; } \\ & \text { vsc = 1 } \end{aligned}$ |
| 2 | analog input to 16-bit output, without SAV/EAV codes, Y on I port, $\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ on H port and decoder output at X port; acquisition trigger at falling edge vertical and rising edge horizontal reference signal; H and V pulses on IGPH and IGPV, output FID on IGP0, IGP1 fixed to logic 1, IDQ qualifier logic 0 active | $704 \times 288$ | $768 \times 288$ | $\begin{aligned} & \hline \text { prsc }=1 ; \\ & \text { fisc }=0.91667 ; \\ & \text { vsc }=1 \end{aligned}$ |
| 3 | $X$ port input 8 bit with SAV/EAV codes, no reference signals on XRH and XRV, XCLK as gated clock; field detection and acquisition trigger on different events; acquisition triggers at rising edge vertical and rising edge horizontal; I port output 8 -bit with SAV/EAV codes like example number 1; see Table 243 | $720 \times 240$ | $352 \times 288$ | $\begin{aligned} & \hline \text { prsc = 2; } \\ & \text { fisc = 1.022; } \\ & \text { vsc = } 0.8333 \end{aligned}$ |
| 4 | X port and H port for 16 -bit $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}} 4: 2: 2$ input (if no 16-bit output selected); XRH and XRV as references; field detection and acquisition trigger at falling edge of vertical and rising edge of horizontal; I port output 8-bit with SAV/EAV codes, but Y only output | $720 \times 288$ | $200 \times 80$ | $\begin{aligned} & \hline \text { prsc = } 2 ; \\ & \text { fisc = 1.8; } \\ & \text { vsc = 3.6 } \end{aligned}$ |

Table 243 Scaler and interface configuration examples

| $\begin{aligned} & \mathrm{I}^{2} \mathrm{C}-\mathrm{BUS} \\ & \text { ADDRESS } \\ & \text { (HEX) } \end{aligned}$ | MAIN FUNCTION | EXAMPLE 1 |  | EXAMPLE 2 |  | EXAMPLE 3 |  | EXAMPLE 4 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | HEX | DEC | HEX | DEC | HEX | DEC | HEX | DEC |
| Global settings |  |  |  |  |  |  |  |  |  |
| 80 | task enable, IDQ and back-end clock definition | 10 | - | 10 | - | 10 | - | 10 | - |
| 83 | XCLK output phase and X port output enable | 01 | - | 01 | - | 00 | - | 00 | - |
| 84 | IGPH, IGPV, IGP0 and IGP1 output definition | A0 | - | C5 | - | A0 | - | A0 | - |
| 85 | signal polarity control and I port byte swapping | 10 | - | 09 | - | 10 | - | 10 | - |
| 86 | FIFO flag thresholds and video/text arbitration | 45 | - | 40 | - | 45 | - | 45 | - |
| 87 | ICLK and IDQ output phase and I port enable | 01 | - | 01 | - | 01 | - | 01 | - |
| 88 | power save control and software reset | F0 | - | F0 | - | F0 | - | F0 | - |

Task A: scaler input configuration and output format settings

| 90 | task handling | 00 | - | 00 | - | 00 | - | 00 | - |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 91 | scaler input source and format definition | 08 | - | 08 | - | 18 | - | 38 | - |
| 92 | reference signal definition at scaler input | 10 | - | 10 | - | 10 | - | 10 | - |
| 93 | I port output formats and configuration | 80 | - | 40 | - | 80 | - | 84 | - |

Input and output window definition

| 94 | horizontal input offset (XO) | 10 | 16 | 10 | 16 | 10 | 16 | 10 | 16 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 95 |  | 00 | - | 00 | - | 00 | - | 00 | - |
| 96 | horizontal input (source) window length (XS) | D0 | 720 | C0 | 704 | D0 | 720 | D0 | 720 |
| 97 |  | 02 | - | 02 | - | 02 | - | 02 | - |
| 98 | vertical input offset (YO) | 0A | 10 | 0A | 10 | 0A | 10 | 0A | 10 |
| 99 |  | 00 | - | 00 | - | 00 | - | 00 | - |
| 9A | vertical input (source) window length (YS) | F2 | 242 | 22 | 290 | F2 | 242 | 22 | 290 |
| 9B |  | 00 | - | 01 | - | 00 | - | 01 | - |
| 9C | horizontal output (destination) window length (XD) | D0 | 720 | 00 | 768 | 60 | 352 | C8 | 200 |
| 9D |  | 02 | - | 03 | - | 01 | - | 00 | - |
| 9E | vertical output (destination) window length (YD) | F0 | 240 | 20 | 288 | 20 | 288 | 50 | 80 |
| 9F |  | 00 | - | 01 | - | 01 | - | 00 | - |

## Prefiltering and prescaling

| A0 | integer prescale (value '00' not allowed) | 01 | - | 01 | - | 02 | - | 02 | - |
| :---: | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | accumulation length for prescaler | 00 | - | 00 | - | 02 | - | 03 | - |
| A2 | FIR prefilter and prescaler DC normalization | 00 | - | 00 | - | AA | - | F2 | - |
| A4 | scaler brightness control | 80 | 128 | 80 | 128 | 80 | 128 | 80 | 128 |
| A5 | scaler contrast control | 40 | 64 | 40 | 64 | 40 | 64 | 11 | 17 |
| A6 | scaler saturation control | 40 | 64 | 40 | 64 | 40 | 64 | 11 | 17 |


| ${ }^{12} \mathrm{C}$-BUS | MAIN FUNCTION | EXAMPLE 1 |  | EXAMPLE 2 |  | EXAMPLE 3 |  | EXAMPLE 4 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (HEX) |  | HEX | DEC | HEX | DEC | HEX | DEC | HEX | DEC |
| Horizontal phase scaling |  |  |  |  |  |  |  |  |  |
| A8 | horizontal scaling increment for luminance | 00 | 1024 | AA | 938 | 18 | 1048 | 34 | 1844 |
| A9 |  | 04 | - | 03 | - | 04 | - | 07 | - |
| AA | horizontal phase offset luminance | 00 | - | 00 | - | 00 | - | 00 | - |
| AC | horizontal scaling increment for chrominance | 00 | 512 | D5 | 469 | 0C | 524 | 9A | 922 |
| AD |  | 02 | - | 01 | - | 02 | - | 03 | - |
| AE | horizontal phase offset chrominance | 00 | - | 00 | - | 00 | - | 00 | - |
| Vertical scaling |  |  |  |  |  |  |  |  |  |
| B0 | vertical scaling increment for luminance | 00 | 1024 | 00 | 1024 | 55 | 853 | 66 | 3686 |
| B1 |  | 04 | - | 04 | - | 03 | - | 0E | - |
| B2 | vertical scaling increment for chrominance | 00 | 1024 | 00 | 1024 | 55 | 853 | 66 | 3686 |
| B3 |  | 04 | - | 04 | - | 03 | - | 0E | - |
| B4 | vertical scaling mode control | 00 | - | 00 | - | 00 | - | 01 | - |
| B8 to BF | vertical phase offsets luminance and chrominance (needs to be used for interlace correct scaled output) | start with B 8 to BF at 00 H , if there are no problems with the interlaced scaled output optimize according to Section 9.3.3.2 |  |  |  |  |  |  |  |

## 20 PACKAGE OUTLINE

BGA156: plastic ball grid array package; 156 balls; body $15 \times 15 \times 1.15 \mathrm{~mm}$
DIMENSIONS (mm are the original dimensions)

| UNIT | $\mathbf{A}$ <br> $\mathbf{m a x}$. | $\mathbf{A}_{\mathbf{1}}$ | $\mathbf{A}_{\mathbf{2}}$ | $\mathbf{b}$ | $\mathbf{D}$ | $\mathbf{D}_{\mathbf{1}}$ | $\mathbf{E}$ | $\mathbf{E}_{\mathbf{1}}$ | $\mathbf{e}$ | $\mathbf{e}_{\mathbf{1}}$ | $\mathbf{k}$ | $\mathbf{v}$ | $\mathbf{w}$ | $\mathbf{y}$ | $\mathbf{y}_{\mathbf{1}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 1.75 | 0.5 | 1.25 | 0.6 | 15.2 | 13.7 | 15.2 | 13.7 | 1.0 | 13.0 | 1.65 | 0.3 | 0.1 | 0.15 | 0.35 |


| OUTLINE <br> VERSION | REFERENCES |  |  |  | EUROPEAN <br> PROJECTION | ISSUE DATE |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | EIAJ |  |  |  |
| SOT472-1 |  |  |  |  | $-99-12-02$ |  |
| $00-03-04$ |  |  |  |  |  |  |

## 21 SOLDERING

### 21.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 21.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to $250^{\circ} \mathrm{C}$. The top-surface temperature of the packages should preferable be kept below $220^{\circ} \mathrm{C}$ for thick/large packages, and below $235^{\circ} \mathrm{C}$ for small/thin packages.

### 21.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
- larger than or equal to 1.27 mm , the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm , the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a $45^{\circ}$ angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at $250^{\circ} \mathrm{C}$.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 21.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage ( 24 V or less) soldering iron applied to the flat part of the lead.
Contact time must be limited to 10 seconds at up to $300^{\circ} \mathrm{C}$.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and $320^{\circ} \mathrm{C}$.

### 21.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD |  |
| :--- | :--- | :--- |
|  | WAVE | REFLOW(1) |
| BGA, HBGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS | not suitable(2) | suitable |
| suitable |  |  |
| PLCC(3), SO, SOJ | suitable |  |
| LQFP, QFP, TQFP | nocommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | nocommended(5) | suitable |

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a $45^{\circ}$ angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm ; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm .
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm ; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm .

## 22 DATA SHEET STATUS

| DATA SHEET STATUS ${ }^{(1)}$ | PRODUCT <br> STATUS |  |
| :--- | :--- | :--- |
| Objective data | Development | This data sheet contains data from the objective specification for product <br> development. Philips Semiconductors reserves the right to change the <br> specification in any manner without notice. |
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## Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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## NOTES

## NOTES

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[^0]:    
    
    
    a. Y output range.
    b. $\mathrm{C}_{\mathrm{B}}$ output range.
    c. $C_{R}$ output range
    "ITU Recommendation 601/656" digital levels with default BCS (decoder) settings DCON[7:0] $=44 \mathrm{H}, \mathrm{DBRI[7:0]}=80 \mathrm{H}$ and DSAT[7:0] $=40 \mathrm{H}$. Equations for modification to the $\mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ levels via BCS control $\mathrm{I}^{2} \mathrm{C}$-bus bytes DBRI, DCON and DSAT.

    Luminance: $\quad Y_{\text {OUT }}=\operatorname{Int}\left[\frac{D C O N}{68} \times(Y-128)\right]+$ DBRI
    Chrominance: $\left(\mathrm{C}_{\mathrm{R}} \mathrm{C}_{\mathrm{B}}\right)_{\text {OUT }}=\operatorname{Int}\left[\frac{\mathrm{DSAT}}{64} \times\left(\mathrm{C}_{\mathrm{R}}, \mathrm{C}_{\mathrm{B}}-128\right)\right]+128$
    It should be noted that the resulting levels are limited to 1 to 254 in accordance with "ITU Recommendation 601/656".
    Fig. $25 \mathrm{Y}-\mathrm{C}_{\mathrm{B}}-\mathrm{C}_{\mathrm{R}}$ range for scaler input and X port output.

[^1]:    The programming of the horizontal increment delay is used to match internal processing delays to the delay of the ADC. Use recommended position only.

    Table 150 Horizontal increment delay; 01H[3:0]

    | FUNCTION | IDEL3 | IDEL2 | IDEL1 | IDELO |
    | :--- | :---: | :---: | :---: | :---: |
    | No update | 1 | 1 | 1 | 1 |
    | Minimum delay | 1 | 1 | 1 | 0 |
    | Recommended position | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |  |
    | Maximum delay | 0 | 0 | 0 | 0 |

