

# DATA SHEET

## **FB2031**

9-bit latched/registered/pass-thru  
Futurebus+ transceiver

Product specification

1995 May 25

IC19 Data Handbook

# 9-bit latched/registered/pass-thru Futurebus+ transceiver

# FB2031

## FEATURES

- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I<sub>CC</sub> current
- Tight output skew
- Supports live insertion

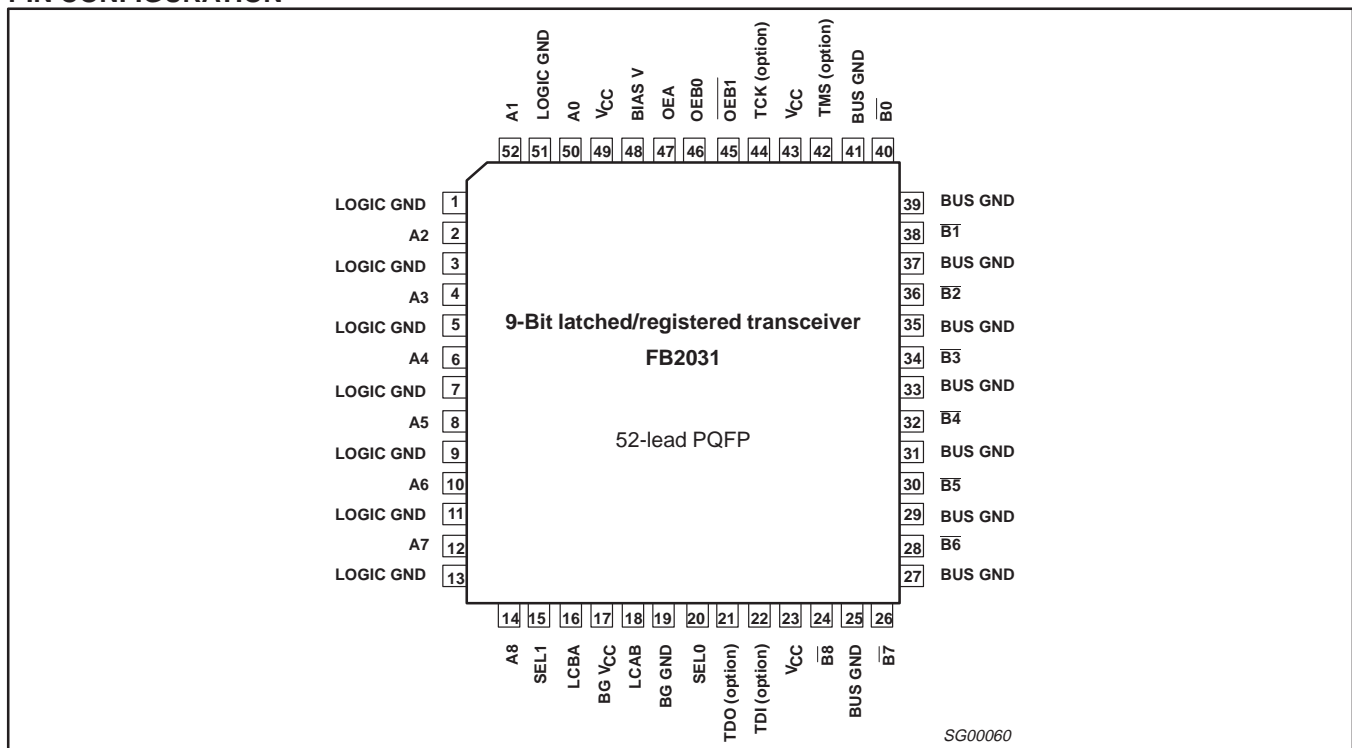
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYPICAL	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> to B <sub>n</sub>	2.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay B <sub>n</sub> to A <sub>n</sub>	4.4 4.2	ns
C <sub>O</sub>	Output capacitance (B <sub>0</sub> – B <sub>n</sub> only)	6	pF
I <sub>OL</sub>	Output current (B <sub>0</sub> – B <sub>n</sub> only)	100	mA
I <sub>CC</sub>	Supply current	A <sub>n</sub> to B <sub>n</sub> (outputs Low or High)	17
		B <sub>n</sub> to A <sub>n</sub> (outputs Low)	50
		B <sub>n</sub> to A <sub>n</sub> (outputs High)	25

## ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V <sub>CC</sub> = 5V±10%; T <sub>amb</sub> = 0°C to +70°C	INDUSTRIAL RANGE V <sub>CC</sub> = 5V±10%; T <sub>amb</sub> = -40°C to +85°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2031BB	CD3206BB	SOT379-1

## PIN CONFIGURATION



# 9-bit latched/registered/pass-thru Futurebus+ transceiver

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## DESCRIPTION

The FB2031 is a 9-bit latched/registered transceiver featuring a latched, registered or pass-thru mode in either the A-to-B or B-to-A direction. The FB2031 is intended to provide the electrical interface to a high performance wired-OR bus.

The TTL-level side (A port) has a common I/O. The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two mode select inputs (SEL0 and SEL1). A "00" configures latches in both directions. A "10" configures thru mode in both directions. A "01" configures register mode in both directions. A "11" configures register mode in the A-to-B direction and latch mode in the B-to-A direction.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the register mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-Low latch enables. Regardless of the mode, data is inverted from input to output.

The 3-State A port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and OEB1. Only when OEB0 is High and  $\overline{OEB1}$  is Low is the output enabled.

When either OEB0 is Low or  $\overline{OEB1}$  is High, the B port is inactive and is pulled to the level of the pullup voltage. New data can be entered in the register and latched modes or can be retained while the associated outputs are in 3-State (A port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The " $V_{OH}$ " clamp reduces inductive ringing effects during a Low-to-High transition. The " $V_{OH}$ " clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V  $V_{OL}$  level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch-free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while  $V_{CC}$  is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a  $V_{CC}$  pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be infrequent and impossible to troubleshoot.

**As with any high power device, thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.**

## PACKAGE THERMAL CHARACTERISTICS

PARAMETER	CONDITION	52-PIN PLASTIC QFP
$\theta_{ja}$	Still air	80°C/W
$\theta_{ja}$	300 Linear feet per minute air flow	58°C/W
$\theta_{jc}$	Thermally mounted on one side to heat sink	20°C/W

## PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
A0 – A8	50, 52, 2, 4, 6, 8, 10, 12, 14	I/O	BiCMOS data inputs/3-State outputs (TTL)
B0 – B8	40, 38, 36, 34, 32, 30, 28, 26, 24	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
OEB1	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	25, 27, 29, 31, 33, 35, 37, 39, 41	GND	Bus ground (0V)
LOGIC GND	51, 1, 3, 5, 7, 9, 11, 13	GND	Logic ground (0V)
$V_{CC}$	23, 43, 49	Power	Positive supply voltage
BIAS V	48	Power	Live insertion pre-bias pin
BG $V_{CC}$	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
SEL0	20	Input	Mode select
SEL1	15	Input	Mode select
LCAB	18	Input	A to B clock/latch enable (transparent latch when Low)
LCBA	16	Input	B to A clock/latch enable (transparent latch when Low)
TMS	42	Input	Test Mode Select (optional, if not implemented then no connect)
TCK	44	Input	Test Clock (optional, if not implemented then no connect)
TDI	22	Input	Test Data In (optional, if not implemented then no connect)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)

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## FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	An	Bn*	OEB0	OEB1	OEA	LCAB	LCBA	SEL0	SEL1	An	Bn
An to Bn thru mode	L	—	H	L	L	X	X	H	L	input	H**
	H	—	H	L	L	X	X	H	L	input	L
An to Bn transparent latch	L	—	H	L	L	L	X	L	L	input	H**
	H	—	H	L	L	L	X	L	L	input	L
An to Bn latch and read	l	—	H	L	L	↑	X	L	L	input	H**
	h	—	H	L	L	↑	X	L	L	input	L
Bn outputs latched and read (preconditioned latch)	X	—	H	L	X	H	X	L	L	X	latched data
An to Bn register	l	—	H	L	L	↑	X	X	H	input	H**
	h	—	H	L	L	↑	X	X	H	input	L
Bn to An thru mode	—	L	Disable		H	X	X	H	L	H	input
	—	H	Disable		H	X	X	H	L	L	input
Bn to An transparent latch	—	L	Disable		H	X	L	L	L	H	input
	—	H	Disable		H	X	L	L	L	L	input
	—	L	Disable		H	X	L	H	H	H	input
	—	H	Disable		H	X	L	H	H	L	input
	—	l	Disable		H	X	↑	L	L	H	input
	—	h	Disable		H	X	↑	L	L	L	input
Bn to An latch and read	—	l	Disable		H	X	↑	H	H	H	input
	—	h	Disable		H	X	↑	H	H	L	input
	—	l	Disable		H	X	↑	H	H	H	input
	—	h	Disable		H	X	↑	H	H	L	input
An outputs latched and read (preconditioned latch)	—	X	X	X	H	X	H	L	L	latched data	X
	—	X	X	X	H	X	H	H	H	latched data	X
Bn to An register	—	l	Disable		H	X	↑	L	H	H	input
	—	h	Disable		H	X	↑	L	H	L	input
Disable Bn outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	X	X	X	X	X	X	H**
Disable An outputs	X	X	X	X	L	X	X	X	X	Z	X

## FUNCTION SELECT TABLE

MODE SELECTED	SEL0	SEL1
Thru mode	H	L
Register mode (An to Bn)	X	H
Latch mode (An to Bn)	L	L
Register mode (Bn to An)	L	H
Latch mode (Bn to An)	L	L
	H	H

## NOTES:

H = High voltage level

L = Low voltage level

l = Low voltage level one set-up time prior to the Low-to-High LCXX transition

h = High voltage level one set-up time prior to the Low-to-High LCXX transition

X = Don't care

Z = High-impedance (OFF) state

— = Input not externally driven

↑ = Low-to-High transition

H\*\* = Goes to level of pull-up voltage

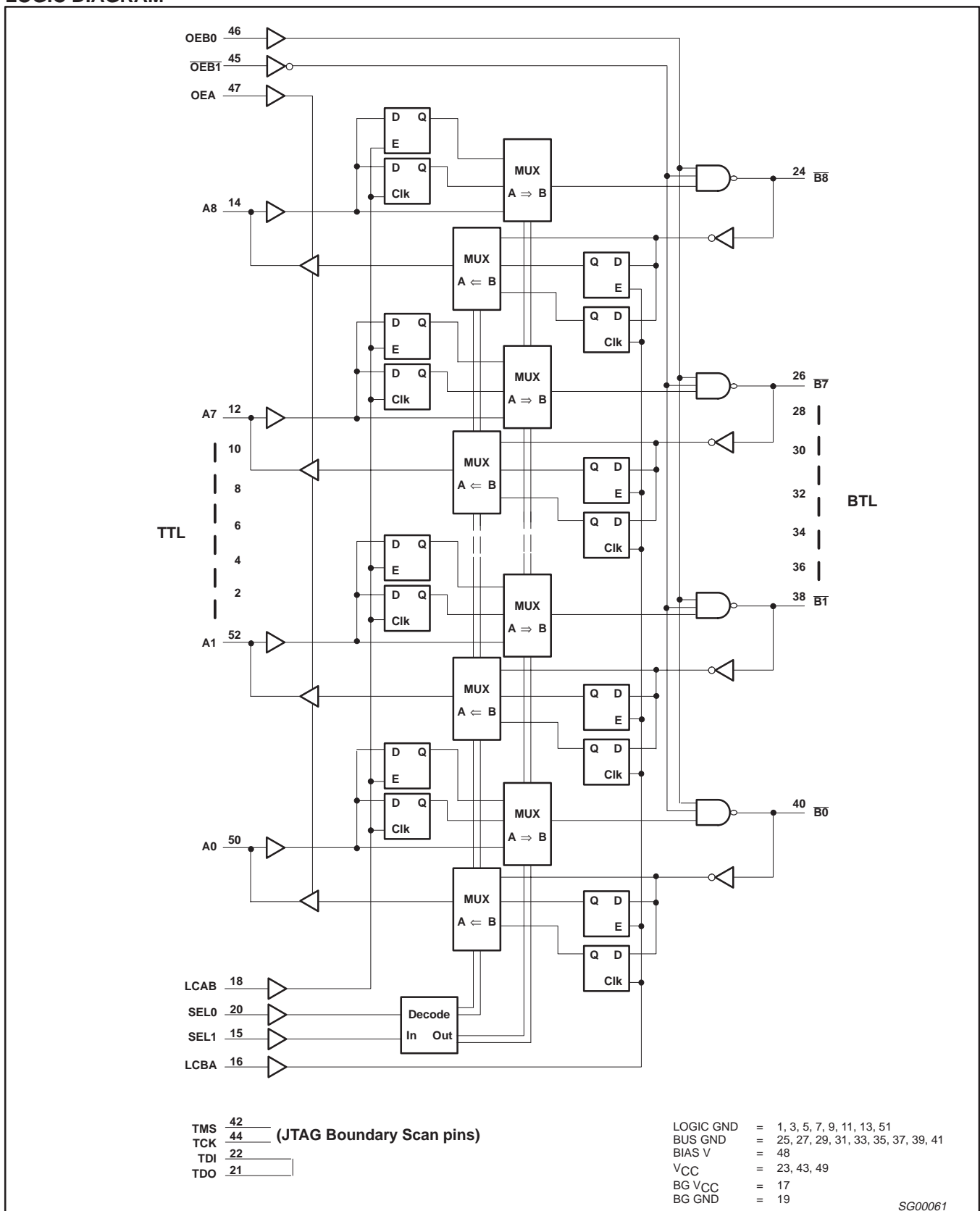
Bn\* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

Disable = OEB0 is Low or OEB1 is High.

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## LOGIC DIAGRAM



## 9-bit latched/registered/pass-thru Futurebus+ transceiver

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**ABSOLUTE MAXIMUM RATINGS**

Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
$V_{CC}$	Supply voltage		-0.5 to +7.0	V
$V_{IN}$	Input voltage	All inputs except $\overline{B0} - \overline{B8}$	-1.2 to +7.0	V
		$\overline{B0} - \overline{B8}$	-1.2 to +3.5	
$I_{IN}$	Input current		-40 to +5.0	mA
$V_{OUT}$	Voltage applied to output in High output state		-0.5 to + $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	A0 – A8	48	mA
		$\overline{B0} - \overline{B8}$	200	
$T_{STG}$	Storage temperature		-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS (Industrial)**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	Except $\overline{B0} - \overline{B8}$	2.0		V
		$\overline{B0} - \overline{B8}$	1.62	1.55	
$V_{IL}$	Low-level input voltage	Except $\overline{B0} - \overline{B8}$		0.8	V
		$\overline{B0} - \overline{B8}$		1.47	
$I_{IK}$	Input clamp current	Control inputs		-40	mA
		$\overline{B0} - \overline{B8}$ & A0 – A8		-18	
$I_{OH}$	High-level output current	A0 – A8		-3	mA
$I_{OL}$	Low-level output current	A0 – A8		24	mA
		$\overline{B0} - \overline{B8}$		100	
$I_{IA}$	Off device input current	Except $\overline{B0} - \overline{B8}$ , $V_I = 0$ to 5.5V, $V_{CC} = 0V$		100	μA
$C_{OB}$	Output capacitance of B port		6	7	pF
$T_{amb}$	Operating free-air temperature range		-40	+85	°C

**RECOMMENDED OPERATING CONDITIONS (Commercial)**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	Except $\overline{B0} - \overline{B8}$	2.0		V
		$\overline{B0} - \overline{B8}$	1.62	1.55	
$V_{IL}$	Low-level input voltage	Except $\overline{B0} - \overline{B8}$		0.8	V
		$\overline{B0} - \overline{B8}$		1.47	
$I_{IK}$	Input clamp current	Control inputs		-40	mA
		$\overline{B0} - \overline{B8}$ & A0 – A8		-18	
$I_{OH}$	High-level output current	A0 – A8		-3	mA
$I_{OL}$	Low-level output current	A0 – A8		24	mA
		$\overline{B0} - \overline{B8}$		100	
$I_{IA}$	Off device input current	Except $\overline{B0} - \overline{B8}$ , $V_I = 0$ to 5.5V, $V_{CC} = 0V$		100	μA
$C_{OB}$	Output capacitance of B port		6	7	pF
$T_{amb}$	Operating free-air temperature range		0	+70	°C

## 9-bit latched/registered/pass-thru Futurebus+ transceiver

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**DC ELECTRICAL CHARACTERISTICS (Industrial)**

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
I <sub>OH</sub>	High level output current	$\overline{B0} - \overline{B8}$	V <sub>CC</sub> = MAX, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, V <sub>OH</sub> = 1.9V			100	μA
I <sub>OFF</sub>	Power-off output current	$\overline{B0} - \overline{B8}$	V <sub>CC</sub> = 0.0V, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, V <sub>OH</sub> = 1.9V			200	μA
V <sub>OH</sub>	High-level output voltage	A0 – A8 <sup>4</sup>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = -24mA	2.0			V
			V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = -3mA	2.5	2.85		
V <sub>OL</sub>	Low-level output voltage	A0 – A8 <sup>4</sup>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 24mA			0.5	V
			V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 80mA	.75	1.0	1.1	
				V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 100mA			
			V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 80mA			1.15	
			V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 4mA	0.5			
V <sub>IK</sub>	Input clamp voltage	Control pins	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.5	V
		A0 – A8 $\overline{B0} - \overline{Bn}$	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18mA			-1.2	
I <sub>I</sub>	Input current at maximum input voltage	Except $\overline{B0} - \overline{B8}$	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V or 5.5V			±50	μA
I <sub>IH</sub>	High-level input current	Except $\overline{B0} - \overline{B8}$	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA
		$\overline{B0} - \overline{B8}$	V <sub>CC</sub> = MAX, V <sub>I</sub> = 1.9V			100	
			V <sub>CC</sub> = MAX, V <sub>I</sub> = 3.5V <sup>5</sup>	100			mA
I <sub>IL</sub>	Low-level input current	Except $\overline{B0} - \overline{B8}$	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-20	μA
		$\overline{B0} - \overline{B8}$	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.75V			-100	
I <sub>IH</sub> + I <sub>OZH</sub>	Off-state I/O High current	A0 – A8	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V			50	μA
I <sub>IL</sub> + I <sub>OZL</sub>	Off-state I/O Low current	A0 – A8	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V			-50	μA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	A0 – A8 only	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.0V	-45		-150	mA
I <sub>CC</sub>	Supply current (total)	An to $\overline{Bn}$	V <sub>CC</sub> = MAX, outputs Low or High		17	30	mA
		$\overline{Bn}$ to An	V <sub>CC</sub> = MAX, outputs Low		50	78	
		$\overline{Bn}$ to An	V <sub>CC</sub> = MAX, outputs High		25	45	
		I <sub>CCZ</sub>	V <sub>CC</sub> = MAX, outputs 3-State		28	50	
		Worst case	V <sub>CC</sub> = MAX, all A and B outputs on		50	78	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Due to test equipment limitations, actual test conditions are V<sub>IH</sub> = 1.8V and V<sub>IL</sub> = 1.3V for the B side.
- For B port input voltage between 3 and 5 volts I<sub>IH</sub> will be greater than 100μA, but the parts will continue to function normally.
- $\overline{B0} - \overline{B8}$  clamps remain active for a minimum of 80ns following a High-to-Low transition.
- Temperature range: 0 to +85°C.
- Temperature range: -40 to 0°C.

## 9-bit latched/registered/pass-thru Futurebus+ transceiver

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**DC ELECTRICAL CHARACTERISTICS** (Commercial)

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
$I_{OH}$	High level output current	$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 1.9\text{V}$			100	$\mu\text{A}$
$I_{OFF}$	Power-off output current	$\overline{B0} - \overline{B8}$	$V_{CC} = 0.0\text{V}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 1.9\text{V}$			100	$\mu\text{A}$
$V_{OH}$	High-level output voltage	A0 – A8 <sup>4</sup>	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OH} = -24\text{mA}$	2.0			V
			$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OH} = -3\text{mA}$	2.5	2.85		
$V_{OL}$	Low-level output voltage	A0 – A8 <sup>4</sup>	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = 24\text{mA}$			0.5	V
			$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = 80\text{mA}$	.75	1.0	1.1	
		$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = 100\text{mA}$			1.15	
			$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = 4\text{mA}$	0.5			
$V_{IK}$	Input clamp voltage	Control pins	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.5	V
		A0 – A8 $\overline{B0} - \overline{Bn}$	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.2	
$I_I$	Input current at maximum input voltage	Except $\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_I = 0.0\text{V}$ or $5.5\text{V}$			$\pm 50$	$\mu\text{A}$
$I_{IH}$	High-level input current	Except $\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	$\mu\text{A}$
		$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_I = 1.9\text{V}$			100	
			$V_{CC} = \text{MAX}, V_I = 3.5\text{V}$ <sup>5</sup>	100			mA
$I_{IL}$	Low-level input current	Except $\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-20	$\mu\text{A}$
		$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_I = 0.75\text{V}$			-100	
$I_{IH} + I_{OZH}$	Off-state I/O High current	A0 – A8	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$			50	$\mu\text{A}$
$I_{IL} + I_{OZL}$	Off-state I/O Low current	A0 – A8	$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$			-50	$\mu\text{A}$
$I_{OS}$	Short-circuit output current <sup>3</sup>	A0 – A8 only	$V_{CC} = \text{MAX}, V_O = 0.0\text{V}$	-45		-150	mA
$I_{CC}$	Supply current (total)	An to $\overline{Bn}$	$V_{CC} = \text{MAX}$ , outputs Low or High		17	30	mA
		$\overline{Bn}$ to An	$V_{CC} = \text{MAX}$ , outputs Low		50	78	
		$\overline{Bn}$ to An	$V_{CC} = \text{MAX}$ , outputs High		25	45	
		$I_{CCZ}$	$V_{CC} = \text{MAX}$ , outputs 3-State		28	50	
		Worst case	$V_{CC} = \text{MAX}$ , all A and B outputs on		50	78	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.
- Due to test equipment limitations, actual test conditions are  $V_{IH} = 1.8\text{V}$  and  $V_{IL} = 1.3\text{V}$  for the B side.
- For B port input voltage between 3 and 5 volts  $I_{IH}$  will be greater than  $100\mu\text{A}$ , but the parts will continue to function normally.
- $\overline{B0} - \overline{B8}$  clamps remain active for a minimum of 80ns following a High-to-Low transition.



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## LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS			UNIT		
		MIN	NOM	MAX			
V <sub>BIASV</sub>	Bias pin voltage	V <sub>CC</sub> = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0V		4.5	5.5	V	
I <sub>BIASV</sub>	Bias pin DC current	V <sub>CC</sub> = 0 to 4.75V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA	
		V <sub>CC</sub> = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			10	μA	
V $\overline{Bn}$	Bus voltage during prebias	$\overline{B0} - \overline{B8} = 0V$ , Bias V = 5.0V		1.62	2.1	V	
I <sub>LM</sub>	Fall current during prebias	$\overline{B0} - \overline{B8} = 2V$ , Bias V = 4.5 to 5.5V		1		μA	
I <sub>HM</sub>	Rise current during prebias	$\overline{B0} - \overline{B8} = 1V$ , Bias V = 4.5 to 5.5V		-1		μA	
I $\overline{Bn}$ PEAK	Peak bus current during insertion	V <sub>CC</sub> = 0 to 5.25V, $\overline{B0} - \overline{B8} = 0$ to 2.0V, Bias V = 4.5 to 5.5V, OE <sub>B0</sub> = 0.8V, t <sub>r</sub> = 2ns			10	mA	
I <sub>OLOFF</sub>	Power up current	V <sub>CC</sub> = 0 to 5.25V, OE <sub>B0</sub> = 0.8V			100	μA	
		V <sub>CC</sub> = 0 to 2.2V, OE <sub>B0</sub> = 0 to 5V			100		
t <sub>GR</sub>	Input glitch rejection	V <sub>CC</sub> = 5.0V			1.35	1.0	ns

## AC ELECTRICAL CHARACTERISTICS (Industrial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T <sub>amb</sub> = +25°C, V <sub>CC</sub> = 5V, C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = -40 to +85°C, V <sub>CC</sub> = 5V±10%, C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 4	120	150		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (thru mode) $\overline{Bn}$ to An	Waveform 1, 2	2.5	4.4	5.9	2.3	7.0	ns
			2.4	4.2	5.5	2.4	6.2	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (transparent latch) $\overline{Bn}$ to An	Waveform 1, 2	2.9	4.6	6.2	2.7	7.1	ns
			2.8	4.3	5.9	2.5	7.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LCBA to An	Waveform 1, 2	2.6	4.1	5.5	2.0	6.2	ns
			2.4	4.7	6.1	2.0	6.8	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SEL0 or SEL1 to An	Waveform 1, 2	1.5	3.8	5.2	1.2	6.2	ns
			1.7	3.9	6.0	1.5	6.5	
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time from High or Low OEA to An	Waveform 5, 6	2.1	3.5	4.8	1.8	6.0	ns
			2.0	3.8	5.3	1.7	6.3	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time to High or Low OEA to An	Waveform 5, 6	1.9	3.4	4.8	1.6	5.5	ns
			1.7	3.2	4.8	1.5	5.5	
t <sub>TLH</sub> t <sub>THL</sub>	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				3.0	7.5	ns
						1.7	4.0	
t <sub>SK(o)</sub>	Output to output skew for multiple channels <sup>1</sup>	Waveform 3		0.5	1.0		1.5	ns
t <sub>SK(p)</sub>	Pulse skew <sup>2</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>   <sub>MAX</sub>	Waveform 2		0.5	1.0		1.0	ns

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Due to test equipment limitations, actual test conditions are V<sub>IH</sub> = 1.8V and V<sub>IL</sub> = 1.3V for the B side.
- For B port input voltage between 3 and 5 volts I<sub>IH</sub> will be greater than 100μA, but the parts will continue to function normally.
- $\overline{B0} - \overline{B8}$  clamps remain active for a minimum of 80ns following a High-to-Low transition.

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## AC ELECTRICAL CHARACTERISTICS (Industrial)

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			$T_{amb} = +25^{\circ}\text{C}, V_{CC} = 5\text{V}, C_D = 30\text{pF}, R_U = 16.5\Omega$			$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}, V_{CC} = 5\text{V}\pm 10\%, C_D = 30\text{pF}, R_U = 16.5\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay (thru mode) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.0 2.7	5.0 4.0	1.5 1.5	5.7 4.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay (transparent latch) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.2 3.1	5.0 4.2	1.5 1.5	5.5 5.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	4.0 4.0	5.5 5.5	1.5 1.5	6.5 6.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay SEL0 or SEL1 to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	3.5 2.3	5.5 4.5	2.0 1.0	6.1 5.5	ns
$t_{PZH}$ $t_{PZL}$	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.5 1.2	3.0 2.4	5.0 4.5	1.0 1.0	5.7 5.5	ns
$t_{TLH}$ $t_{THL}$	Output transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.0 3.0	0.9 0.6	3.0 3.0	ns
$t_{SK(o)}$	Output to output skew for multiple channels <sup>1</sup>	Waveform 3	1.0	0.4		1.6	1.6	ns
$t_{SK(p)}$	Pulse skew <sup>2</sup> $ t_{PHL} - t_{PLH} _{MAX}$	Waveform 2		0.3	1.0		1.5	ns

## NOTES:

- $|t_{PNactual} - t_{PMactual}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature,  $V_{CC}$ , loading, etc.).
- $t_{SK(p)}$  is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

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## AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			$T_{amb} = +25^{\circ}\text{C}, V_{CC} = 5\text{V}, C_L = 50\text{pF}, R_L = 500\Omega$			$T_{amb} = 0 \text{ to } +70^{\circ}\text{C}, V_{CC} = 5\text{V} \pm 10\%, C_L = 50\text{pF}, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$f_{MAX}$	Maximum clock frequency	Waveform 4	120	150		100		MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay (thru mode) $\bar{B}_n$ to $A_n$	Waveform 1, 2	2.5 2.4	4.4 4.2	5.9 5.5	2.3 2.4	6.6 5.9	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay (transparent latch) $B_n$ to $A_n$	Waveform 1, 2	2.9 2.8	4.6 4.3	6.2 5.9	2.7 2.5	7.0 6.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay LCBA to $A_n$	Waveform 1, 2	2.6 2.4	4.1 4.7	5.5 6.1	2.0 2.0	6.0 6.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay SEL0 or SEL1 to $A_n$	Waveform 1, 2	1.5 1.7	3.8 3.9	5.2 6.0	1.2 1.5	6.0 6.5	ns
$t_{PZH}$ $t_{PZL}$	Output enable time from High or Low OEA to $A_n$	Waveform 5, 6	2.1 2.0	3.5 3.8	4.8 5.3	1.8 1.7	5.8 6.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time to High or Low OEA to $A_n$	Waveform 5, 6	1.9 1.7	3.4 3.2	4.8 4.8	1.6 1.5	5.4 5.4	ns
$t_{TLH}$ $t_{THL}$	Output transition time, $A_n$ Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				2.0 1.0	7.5 3.5	ns
$t_{SK(o)}$	Output to output skew for multiple channels <sup>1</sup>	Waveform 3		0.5	1.0		1.5	ns
$t_{SK(p)}$	Pulse skew <sup>2</sup> $ t_{PHL} - t_{PLH} _{MAX}$	Waveform 2		0.5	1.0		1.0	ns

## NOTES:

- $|t_{PNactual} - t_{PMactual}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature,  $V_{CC}$ , loading, etc.).
- $t_{SK(p)}$  is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

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## AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			$T_{amb} = +25^{\circ}\text{C}, V_{CC} = 5\text{V}, C_D = 30\text{pF}, R_U = 16.5\Omega$			$T_{amb} = 0 \text{ to } +70^{\circ}\text{C}, V_{CC} = 5\text{V}\pm 10\%, C_D = 30\text{pF}, R_U = 16.5\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay (thru mode) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.0 2.7	5.0 4.0	1.0 0.5	5.5 4.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay (transparent latch) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.2 3.1	5.0 4.2	1.0 0.8	5.5 4.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	4.0 4.0	5.5 5.5	1.5 1.0	6.0 6.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay SEL0 or SEL1 to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	3.5 2.3	5.5 4.5	2.0 1.0	6.0 5.0	ns
$t_{PZH}$ $t_{PZL}$	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.5 1.5	3.0 2.4	5.0 4.5	1.0 0.8	5.5 5.5	ns
$t_{TLH}$ $t_{THL}$	Output transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.0 3.0	1.0 0.6	2.3 2.3	ns
$t_{SK(o)}$	Output to output skew for multiple channels <sup>1</sup>	Waveform 3		0.4	1.0		1.6	ns
$t_{SK(p)}$	Pulse skew <sup>2</sup> $ t_{PHL} - t_{PLH} _{MAX}$	Waveform 2		0.3	1.0		1.5	ns

## NOTES:

- $|t_{PNactual} - t_{PMactual}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature,  $V_{CC}$ , loading, etc.).
- $t_{SK(p)}$  is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

## AC SETUP REQUIREMENTS (Industrial)

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_{amb} = +25^{\circ}\text{C}, V_{CC} = 5\text{V},$			$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}, V_{CC} = 5\text{V}\pm 10\%,$		
			$C_L = 50\text{pF}$ (A side) / $C_D = 30\text{pF}$ (B side) $R_L = 500\Omega$ (A side) / $R_U = 16.5\Omega$ (B side)					
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to LCAB	Waveform 4	1.0 1.0			1.5 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to LCAB	Waveform 4	1.0 1.0			2.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{Bn}$ to LCBA	Waveform 4	2.0 2.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			3.0 3.0		ns

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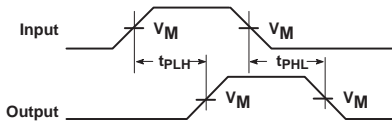
**AC SETUP REQUIREMENTS (Commercial)**

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_{amb} = +25^{\circ}C, V_{CC} = 5V,$			$T_{amb} = 0 \text{ to } +70^{\circ}C,$ $V_{CC} = 5V \pm 10\%,$		
			$C_L = 50pF \text{ (A side)} / C_D = 30pF \text{ (B side)}$ $R_L = 500\Omega \text{ (A side)} / R_U = 16.5\Omega \text{ (B side)}$					
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to LCAB	Waveform 4	1.0 1.0			1.5 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to LCAB	Waveform 4	1.0 1.0			2.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{Bn}$ to LCBA	Waveform 4	2.0 2.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			3.0 3.0		ns

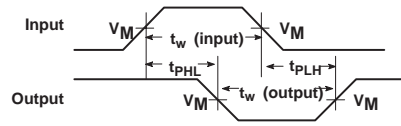
9-bit latched/registered/pass-thru Futurebus+ transceiver

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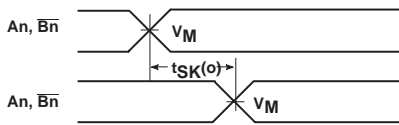
AC WAVEFORMS



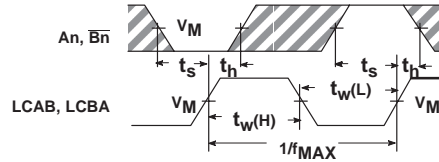
Waveform 1. Propagation Delay for Data or Output Enable to Output



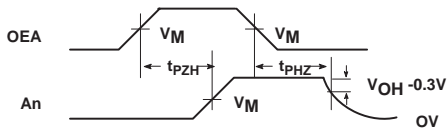
Waveform 2. Propagation Delay for Data or Output Enable to Output



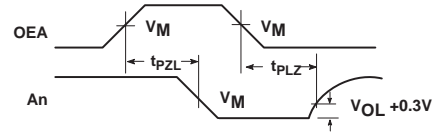
Waveform 3. Output to Output Skew



Waveform 4. Setup and Hold Times, Pulse Widths and Maximum Frequency



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

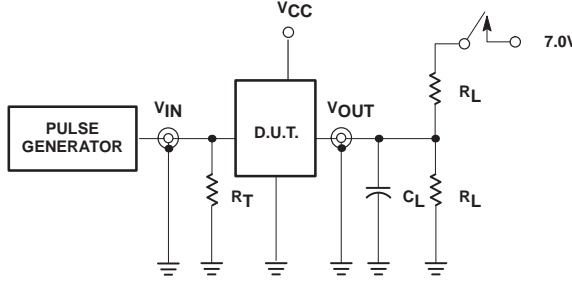
NOTE:  $V_M = 1.55V$  for  $\overline{Bn}$ ,  $V_M = 1.5V$  for all others.  
The shaded areas indicate when the input is permitted to change for predictable output performance.

SG00062

# 9-bit latched/registered/pass-thru Futurebus+ transceiver

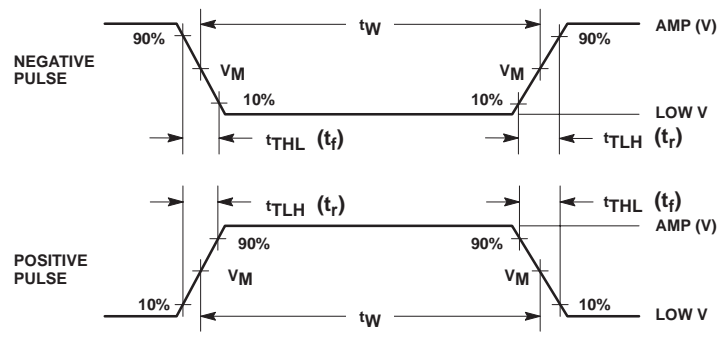
FB2031

## TEST CIRCUIT AND WAVEFORMS



**Test Circuit for 3-State Outputs on A Port**

The circuit shows a Pulse Generator connected to the input (VIN) of a D.U.T. through a termination resistor (RT). The output (VOUT) is connected to a load resistor (RL) and a load capacitor (CL). A switch is connected to the output through another load resistor (RL) and is controlled by a 7.0V signal. VCC is connected to the device.



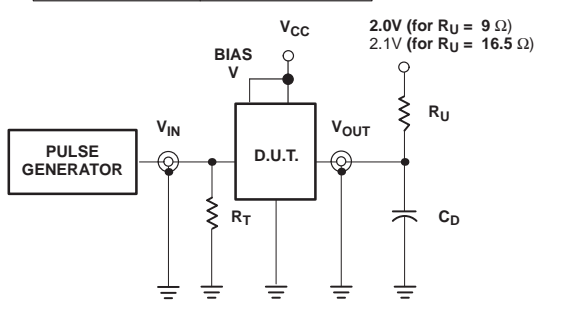
**Input Pulse Definitions**

VM = 1.55V for  $\overline{Bn}$ , VM = 1.5V for all others.

The waveforms show a negative pulse (top) and a positive pulse (bottom). Key parameters are labeled: tW (pulse width), tTHL (tr) (fall time), and tTLH (tr) (rise time). Voltage levels are marked at 90%, VM, and 10%.

**SWITCH POSITION**

TEST	SWITCH
tPLZ, tPZL	closed
All other	open



**Test Circuit for Outputs on B Port**

The circuit shows a Pulse Generator connected to the input (VIN) of a D.U.T. through a termination resistor (RT). The output (VOUT) is connected to a pull-up resistor (RU) and a load capacitor (CD). A BIAS V signal is connected to the device. VCC is connected to the device. RU values are specified as 2.0V for RU = 9Ω and 2.1V for RU = 16.5Ω.

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	tW	tTLH	tTHL
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

**DEFINITIONS:**

- RL = Load Resistor; see AC CHARACTERISTICS for value.
- CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- RT = Termination resistance should be equal to ZOUT of pulse generators.
- CD = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- RU = Pull up resistor; see AC CHARACTERISTICS for value.

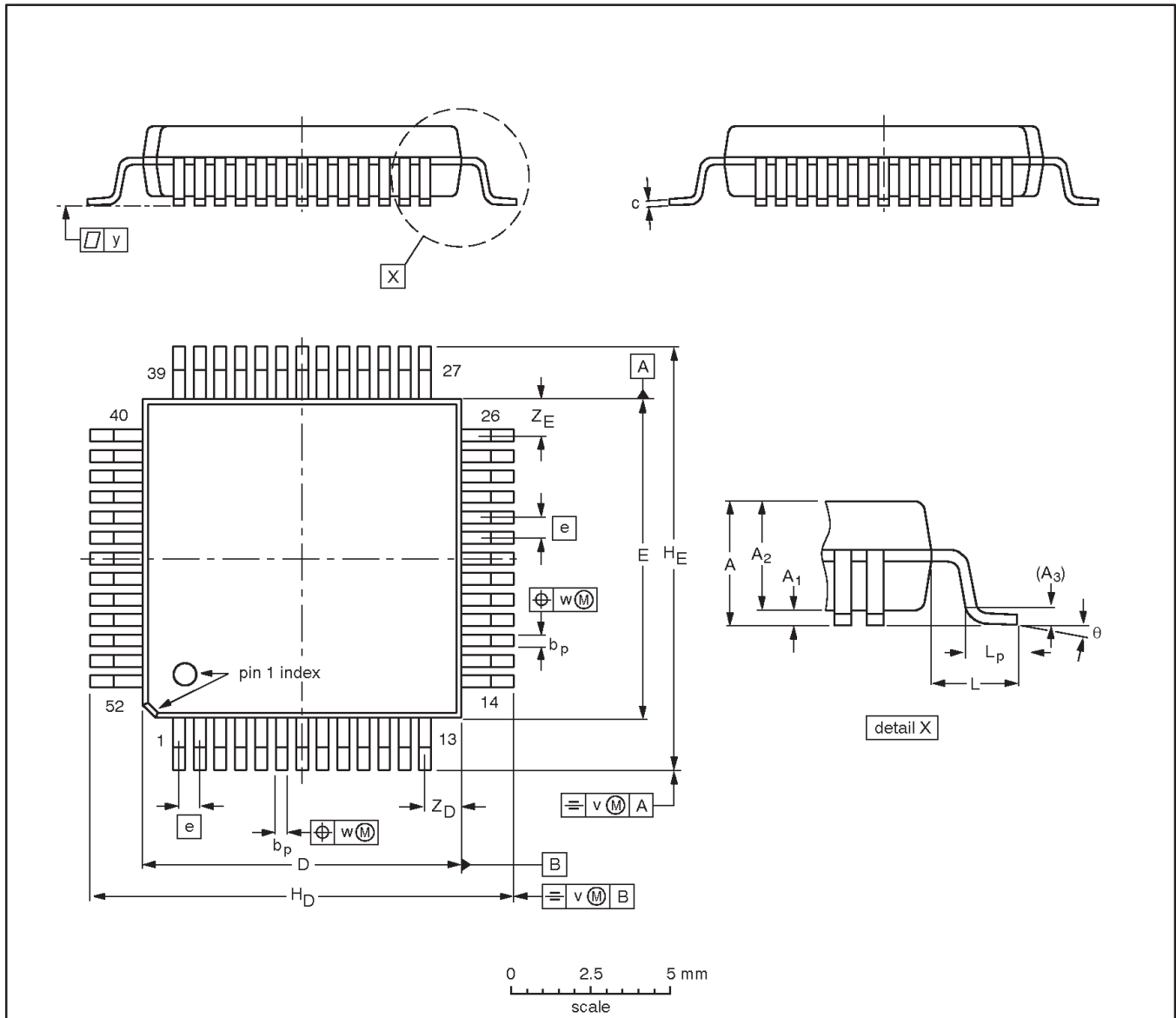
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QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT379-1		MO-108			-95-02-04 97-08-04



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**NOTES**

## 9-bit latched/registered/pass-thru Futurebus+ transceiver

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**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

**Definitions**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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