MOTOROLA
intelligence everywhere™

digitaldna™

The MPC8241 combines a MPC603e PowerPC™ core microprocessor with a PCI bridge. The PCI support on the MPC8241 will allow system designers to rapidly design systems using peripherals already designed for the PCI and other standard interfaces. The MPC8241 also integrates a high-performance memory controller which supports various types of ROM and SDRAM. The MPC8241 is the second of a family of products that provides system-level support for industry standard interfaces with a MPC603e processor core.

This document describes pertinent electrical and physical characteristics of the MPC8241. The MPC8241 is based on the MPC8245 design, so for functional characteristics of the processor, refer to the *MPC8245 Integrated Processor User's Manual* (MPC8245UM/D).

This document contains the following topics:

To locate any published errata or updates for this document, refer to the web site at http://www.motorola.com/semiconductors.

1.1 Overview

The MPC8241 integrated processor is comprised of a peripheral logic block and a 32-bit superscalar MPC603e core, as shown in Figure 1.

MPC8241

Additional Features:
- Prog I/O with Watchpoint
- JTAG/COP Interface
- Power Management

Processor Core Block

(64-Bit) Two-Instruction Fetch

Processor PLL

Branch Processing Unit (BPU)

Instruction Unit

(64-Bit) Two-Instruction Dispatch

System Register Unit (SRU)

Integer Unit (IU)

Load/Store Unit (LSU)

Floating-Point Unit (FPU)

Data MMU

64-Bit

Instruction MMU

16-Kbyte Data Cache

16-Kbyte Instruction Cache

Peripheral Logic Bus

Peripheral Logic Block

Message Unit (with I$_2$O)

Address (32-Bit)

Data (64-Bit)

Data Path ECC Controller

Data Bus (32- or 64-Bit) with 8-Bit Parity or ECC

DMA Controller

Central Control Unit

Memory Controller

Memory/ROM/ Port X Control/Address

I^{2}C

I^{2}C Controller

Performance Monitor

SDRAM_SYNC_IN

DLL

SDRAM Clocks

5 IRQs/ 16 Serial Interrupts

PIC Interrupt Controller/ Timers

Peripheral Logic PLL

PCI_SYNC_IN

Configuration Registers

DUART

PCI Bus Interface Unit

Watchpoint Facility

Address Translator

PCI Arbiter

Fanout Buffers

PCI Bus Clocks

32-Bit PCI Interface

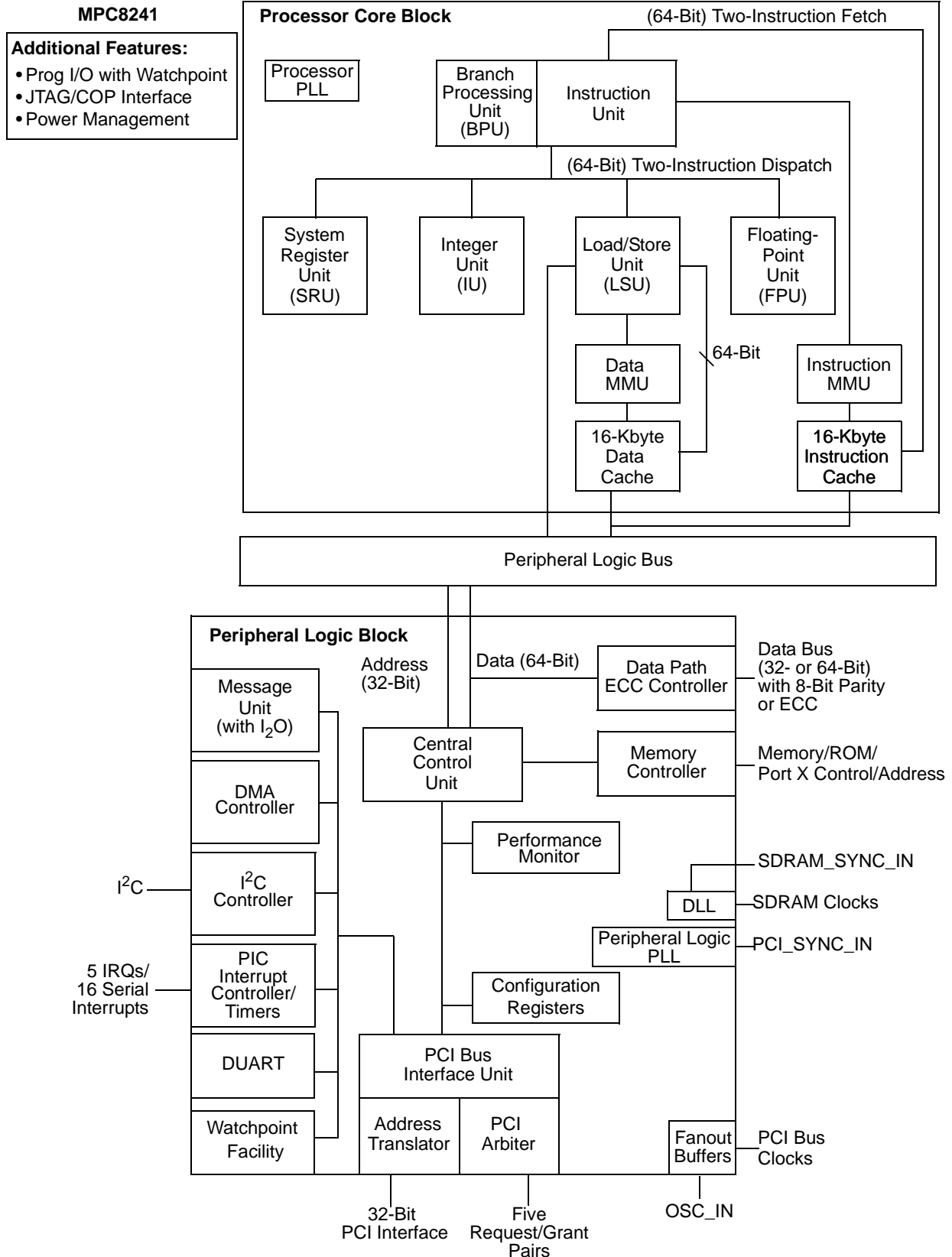Five Request/Grant Pairs

OSC_IN

Figure 1. MPC8241 Block Diagram

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I$_2$O interface), and an I^{2}C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

The MPC8241 contains an internal peripheral logic bus that interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade-off performance for power consumption. The processor core is clocked from a separate PLL, which is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies, while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8241 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The processor core and peripheral logic are general-purpose in order to serve a variety of embedded applications. The MPC8241 can be used as either a PCI host or PCI agent controller.

1.2   Features

Major features of the MPC8241 are as follows:

- Processor core
  - High-performance, superscalar processor core
  - Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
  - 16-Kbyte instruction cache
  - 16-Kbyte data cache
  - Lockable L1 caches—entire cache or on a per-way basis up to three of four ways
  - Dynamic power management—supports 60x nap, doze, and sleep modes
- Peripheral logic
  - Peripheral logic bus
    - Supports various operating frequencies and bus divider ratios
    - 32-bit address bus, 64-bit data bus
    - Supports full memory coherency
    - Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - Store gathering on peripheral logic bus-to-PCI writes
  - Memory interface
    - Supports up to 2 Gbytes of SDRAM memory
    - High-bandwidth data bus (32- or 64-bit) to SDRAM
    - Programmable timing supporting SDRAM
    - Supports 1 to 8 banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices
    - Write buffering for PCI and processor accesses
    - Supports normal parity, read-modify-write (RMW), or ECC
    - Data-path buffering between memory interface and processor

Features

- Low-voltage TTL logic (LVTTL) interfaces
- 272 Mbytes of base and extended ROM/Flash/Port X space
- Base ROM space supports 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- Extended ROM space supports 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- Port X: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects
— 32-bit PCI interface

- Operates up to 66 MHz
    - PCI 2.2-compatible
    - PCI 5.0-V tolerance
    - Support for dual address cycle (DAC) for 64-bit PCI addressing (master only)
    - Support for PCI locked accesses to memory
    - Support for accesses to PCI memory, I/O, and configuration spaces
    - Selectable big- or little-endian operation
    - Store gathering of processor-to-PCI write and PCI-to-memory write accesses
    - Memory prefetching of PCI read accesses
    - Selectable hardware-enforced coherency
    - PCI bus arbitration unit (five request/grant pairs)
    - PCI agent mode capability
    - Address translation with two inbound and outbound units (ATU)
    - Some internal configuration registers accessible from PCI
— Two-channel integrated DMA controller (writes to ROM/Port X not supported)
    - Supports direct mode or chaining mode (automatic linking of DMA transfers)
    - Supports scatter gathering—read or write discontinuous memory
    - 64-byte transfer queue per channel
    - Interrupt on completed segment, chain, and error
    - Local-to-local memory
    - PCI-to-PCI memory
    - Local-to-PCI memory
    - PCI memory-to-local memory
— Message unit
    - Two doorbell registers
    - Two inbound and two outbound messaging registers
    - I$_2$O message interface
— I^{2}C controller with full master/slave support that accepts broadcast messages
— Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
— Two (dual) universal asynchronous receiver/transmitters (UARTs)

— Integrated PCI bus and SDRAM clock generation

— Programmable PCI bus and memory interface output drivers

• System level performance monitor facility

• Debug features

— Memory attribute and PCI attribute signals

— Debug address signals

— $\overline{\text{MIV}}$ signal: marks valid address and data bus cycles on the memory bus

— Programmable input and output signals with watchpoint capability

— Error injection/capture on data path

— IEEE 1149.1 (JTAG)/test interface

1.3　General Parameters

The following list provides a summary of the general parameters of the MPC8241:

Technology	0.25 µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully static
Packages	Surface-mount 357 (thick substrate and thick mold cap) plastic ball grid array (PBGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 2 for details and recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8241.

1.4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other characteristics.

1.4.1.1 Absolute Maximum Ratings

This section describes the MPC8241 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	−0.3 to 2.1	V
Supply voltage—memory bus drivers PCI and standard I/O buffers	$GV_{DD}\_OV_{DD}$	−0.3 to 3.6	V
Supply voltage—PLLs	$AV_{DD}/AV_{DD}2$	−0.3 to 2.1	V
Supply voltage—PCI reference	LV_{DD}	−0.3 to 5.4	V
Input voltage [2]	V_{in}	−0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105	°C
Storage temperature range	T_{stg}	−55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.

1.4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Supply voltage	V_{DD}	1.8 ± 100 mV	V	1, 2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers	$GV_{DD}\_OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage	AV_{DD}	1.8 ± 100 mV		1, 2
PLL supply voltage—peripheral logic	$AV_{DD}2$	1.8 ± 100 mV	V	1, 2
PCI reference	LV_{DD}	5.0 ± 5%	V	4, 5, 6
		3.3 ± 0.3	V	5, 6, 7

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	°C	

Notes:
1. CPU speed limited to 266 MHz operation at this voltage. See Table 7.
2. **Caution:** $GV_{DD\_}OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD\_}OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD\_}OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD\_}OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD\_}OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

Electrical and Thermal Characteristics

Figure 2 shows supply voltage sequencing and separation cautions.
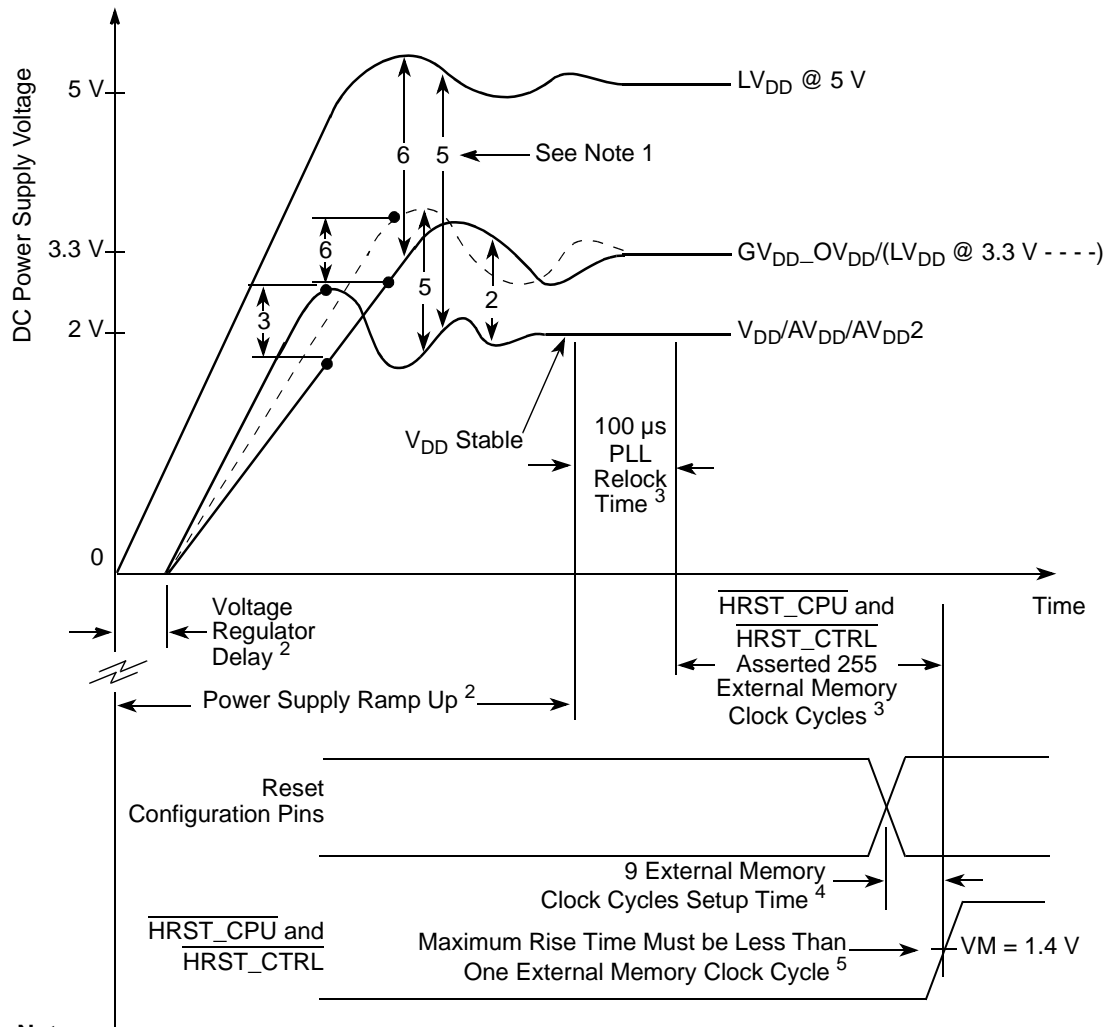
Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. Refer to Section 1.7.2, "Power Supply Sizing," for additional information on this topic.
3. Refer to Table 8 for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for additional information on reset configuration pin setup timing requirements.
5. HRST_CPU/HRST_CTRL must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the MPC8241memory interface.
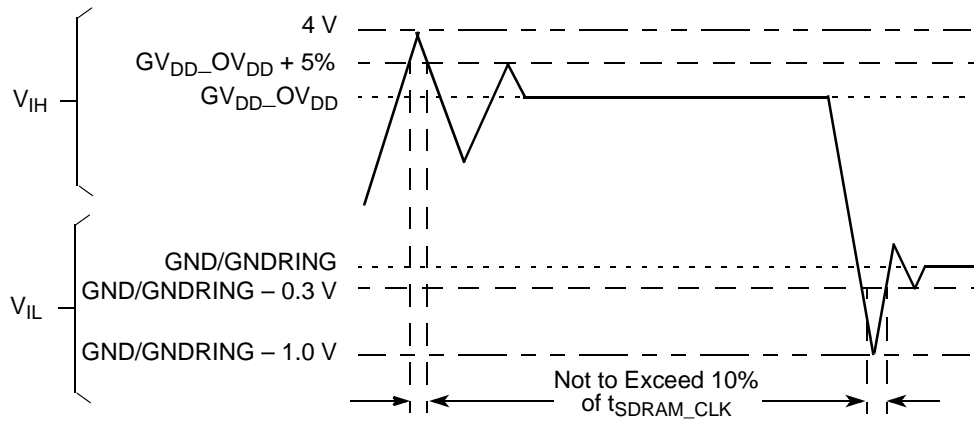
Figure 3. Overshoot/Undershoot Voltage

Figure 4 and Figure 5 show the undershoot and overshoot voltage of the MPC8241 PCI interface for 3.3- and 5-V signals, respectively.
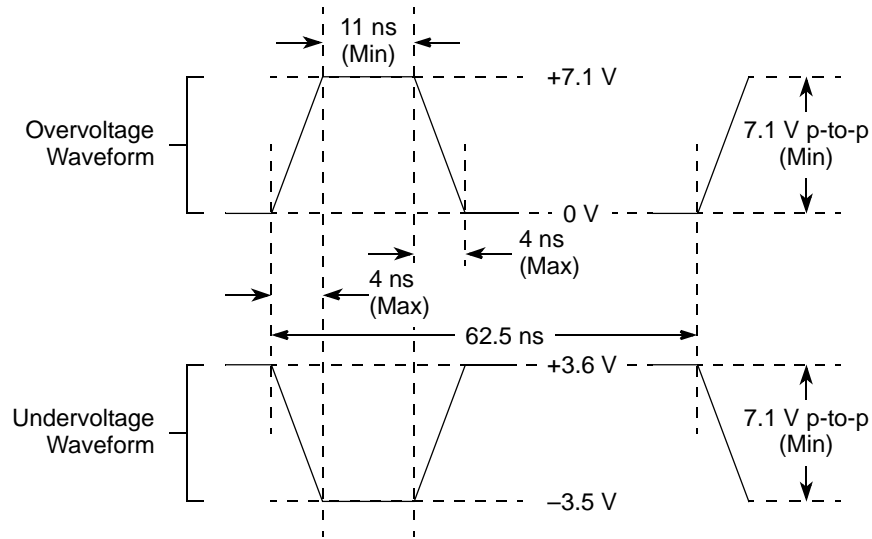
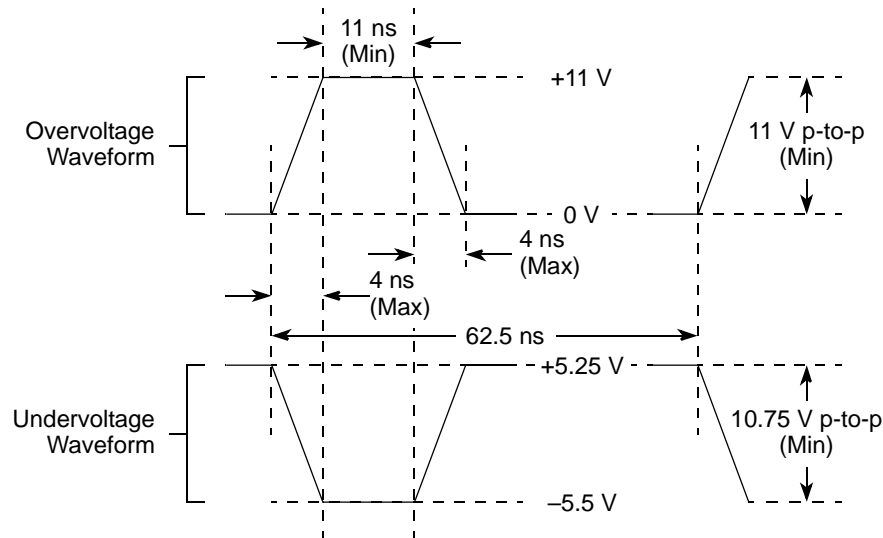

Figure 4. Maximum AC Waveforms for 3.3-V Signaling

Figure 5. Maximum AC Waveforms for 5-V Signaling

1.4.1.3 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8241 at recommended operating conditions.

Table 3. DC Electrical Specifications

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Input high voltage	PCI only	V_{IH}	$0.65 \times GV_{DD}\_OV_{DD}$	LV_{DD}	V	1
Input low voltage	PCI only	V_{IL}	—	$0.3 \times GV_{DD}\_OV_{DD}$	V	
Input high voltage	All other pins ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{IH}	2.0	3.3	V	
Input low voltage	All inputs except PCI_SYNC_IN	V_{IL}	GND/GNDRING	0.8	V	2
PCI_SYNC_IN input high voltage		CV_{IH}	2.4	—	V	
PCI_SYNC_IN input low voltage		CV_{IL}	GND/GNDRING	0.4	V	2
Input leakage current for pins using DRV_PCI driver	$0.5\ V \leq V_{in} \leq 2.7\ V$ @ LV_{DD} = 4.75 V	I_L	—	±70	µA	3
Input leakage current all others	LV_{DD} = 3.6 V $GV_{DD}\_OV_{DD} \leq 3.465\ V$	I_L	—	±10	µA	3
Output high voltage	I_{OH} = driver dependent ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{OH}	2.4	—	V	4
Output low voltage	I_{OL} = driver dependent ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{OL}	—	0.4	V	4

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1MHz	C_{in}	—	15.0	pF	

Notes:
1. See Table 17 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal $GV_{DD\_}OV_{DD}/LV_{DD}$ and V_{DD} or both $GV_{DD\_}OV_{DD}/LV_{DD}$ and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 17.

1.4.1.4 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 17. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20	$GV_{DD\_}OV_{DD}$ = 3.3 V	36.6	18.0	mA	2, 4
	40 (default)		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × $GV_{DD\_}OV_{DD}$ ($GV_{DD\_}OV_{DD}$ = 3.3 V) where table entry voltage = $GV_{DD\_}OV_{DD}$ – PCI V_{OH}.
2. For all others with $GV_{DD\_}OV_{DD}$ = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = $GV_{DD\_}OV_{DD}$ – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × $GV_{DD\_}OV_{DD}$ ($GV_{DD\_}OV_{DD}$ = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with $GV_{DD\_}OV_{DD}$ = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor User's Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

1.4.1.5 Power Characteristics

Table 5 provides preliminary estimated power consumption data for the MPC8241.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)							Unit	Notes
	33/66/133	33/66/166	33/66/200	33/100/200	66/100/200	66/66/266	66/133/266		
Typical	0.7	0.8	1.0	1.0	1.0	1.5	1.8	W	1, 5
Max—CFP	0.8	1.0	1.2	1.3	1.3	1.9	2.1	W	1, 2
Max—INT	0.8	0.9	1.0	1.2	1.2	1.6	1.8	W	1, 3
Doze	0.5	0.6	0.7	0.8	0.8	1.0	1.3	W	1, 4, 6
Nap	0.2	0.2	0.3	0.4	0.4	0.4	0.7	W	1, 4, 6
Sleep	0.2	0.2	0.2	0.2	0.3	0.2	0.4	W	1, 4, 6
I/O Power Supplies [7]									
Mode	Minimum			Maximum				Unit	Notes
$GV_{DD\_}OV_{DD}$	500			1100				mW	8

Notes:
1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power, see Section 1.7.2, "Power Supply Sizing," for information on $GV_{DD\_}OV_{DD}$ supply power.
2. Maximum—FP power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 1.9 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at V_{DD} = AV_{DD} = 1.8 V, $GV_{DD\_}OV_{DD}$ = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW, guaranteed by design, but not tested.
8. The typical maximum $GV_{DD\_}OV_{DD}$ value resulted from the MPC8241 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory and on 64-bit boundaries to local memory.

1.4.2 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8241. For further information, see Section 1.7.8, "Thermal Management Information."

Table 6. Thermal Characterization Data

Rating	Board Description	Symbol	Value [7] (166- and 200-MHz Parts)	Value [7] (266-MHz Part)	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	38	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JMA}$	25	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	31	22	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	22	17	°C/W	1, 3
Junction-to-board (bottom)	Four-layer board (2s2p)	$R_{\theta JB}$	17	11	°C/W	4
Junction-to-case (top)	Single-layer board (1s)	$R_{\theta JC}$	8	7	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	2	°C/W	6

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the board horizontal.
3. Per EIA/JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.
7. Note that the 166- and 200-MHz parts are in a two-layer package and the 266-MHz part is in a four-layer package. This results in different thermal characterization data for the two package types.

1.4.3 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC8241. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 1.9, "Ordering Information."

Table 7 provides the operating frequency information for the MPC8241 at recommended operating conditions (see Table 2) with $LV_{DD} = 3.3$ V $\pm$ 0.3 V.

Table 7. Operating Frequency

Characteristic	166 MHz		200 MHz		266 MHz		Unit
	$V_{DD}/AV_{DD}/AV_{DD}2 = 1.8 \pm 100$ mV						
	Min	Max	Min	Max	Min	Max	
Processor frequency (CPU)	100	166	100	200	100	266	MHz
Memory bus frequency	33	83	33	100	33	133	MHz
PCI input frequency	25–66						MHz

Caution: The PCI_SYNC_IN frequency and PLL_CFG[0:4] settings must be chosen such that the resulting peripheral logic/memory bus frequency and CPU (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.6, "PLL Configuration," for valid PLL_CFG[0:4] settings and PCI_SYNC_IN frequencies.

1.4.3.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications at recommended operating conditions, as defined in Section 1.4.3.2, "Input AC Timing Specifications." These specifications are for the default driver strengths indicated in Table 4. Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 2) with $LV_{DD} = 3.3$ V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
1a	Frequency of operation (PCI_SYNC_IN)	25	66	MHz	
2, 3	PCI_SYNC_IN rise and fall times	—	2.0	ns	1
4	PCI_SYNC_IN duty cycle measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN pulse width high measured at 1.4 V	6	9	ns	2
5b	PCI_SYNC_IN pulse width low measured at 1.4 V	6	9	ns	2
7	PCI_SYNC_IN jitter	—	150	ps	
8a	PCI_CLK[0:4] skew (pin-to-pin)	—	250	ps	
8b	SDRAM_CLK[0:3] skew (pin-to-pin)	—	190	ps	3
10	Internal PLL relock time	—	100	µs	2, 4, 5
15	DLL lock range with DLL_EXTEND = 0 disabled (default)	$(N \times T_{clk} - T_{dp}(max)) \le T_{loop}$ $\le (N \times T_{clk} - T_{dp}(min))$		ns	6
16	DLL lock range with DLL_EXTEND = 1 enabled	$((N - 0.5) \times T_{clk} - T_{dp}(max)) \le T_{loop}$ $\le ((N - 0.5) \times T_{clk} - T_{dp}(min))$		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. N is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. T_{dp}(max) and T_{dp}(min) are dependent on tap delay. See Table 9 for values of T_{dp}(max) and T_{dp}(min). See Figure 7 through Figure 10 for DLL locking ranges. Refer to Motorola Application Note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for more details on memory clock design.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram and Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation.
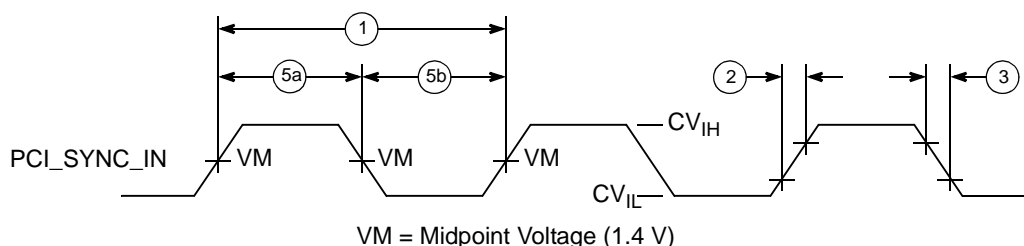

VM = Midpoint Voltage (1.4 V)

Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Table 9 lists the values of T_{dp}(min) and T_{dp}(max).

Table 9. T_{dp}(min) and T_{dp}(max)

Mode	T_{dp}(min)	T_{dp}(max)	Unit
Normal tap delay: bit 2 (DLL_MAX_DELAY) at offset 0x76 is cleared	7.58	12.97	ns
Maximum tap delay: bit 2 (DLL_MAX_DELAY) at offset 0x76 is set	8.28	17.57	ns

Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation. These graphs define the areas of DLL locking for various modes. The grey areas represent where the DLL will lock.

Note also that the DLL_MAX_DELAY bit can lengthen the amount of time through the delay line. This is accomplished by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock will be within the DLL lock range, it also means there may be slightly more jitter in the output clock of the DLL, should the phase comparator shift the clock between adjacent tap points. Refer to Motorola Application Note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for more details on memory design.
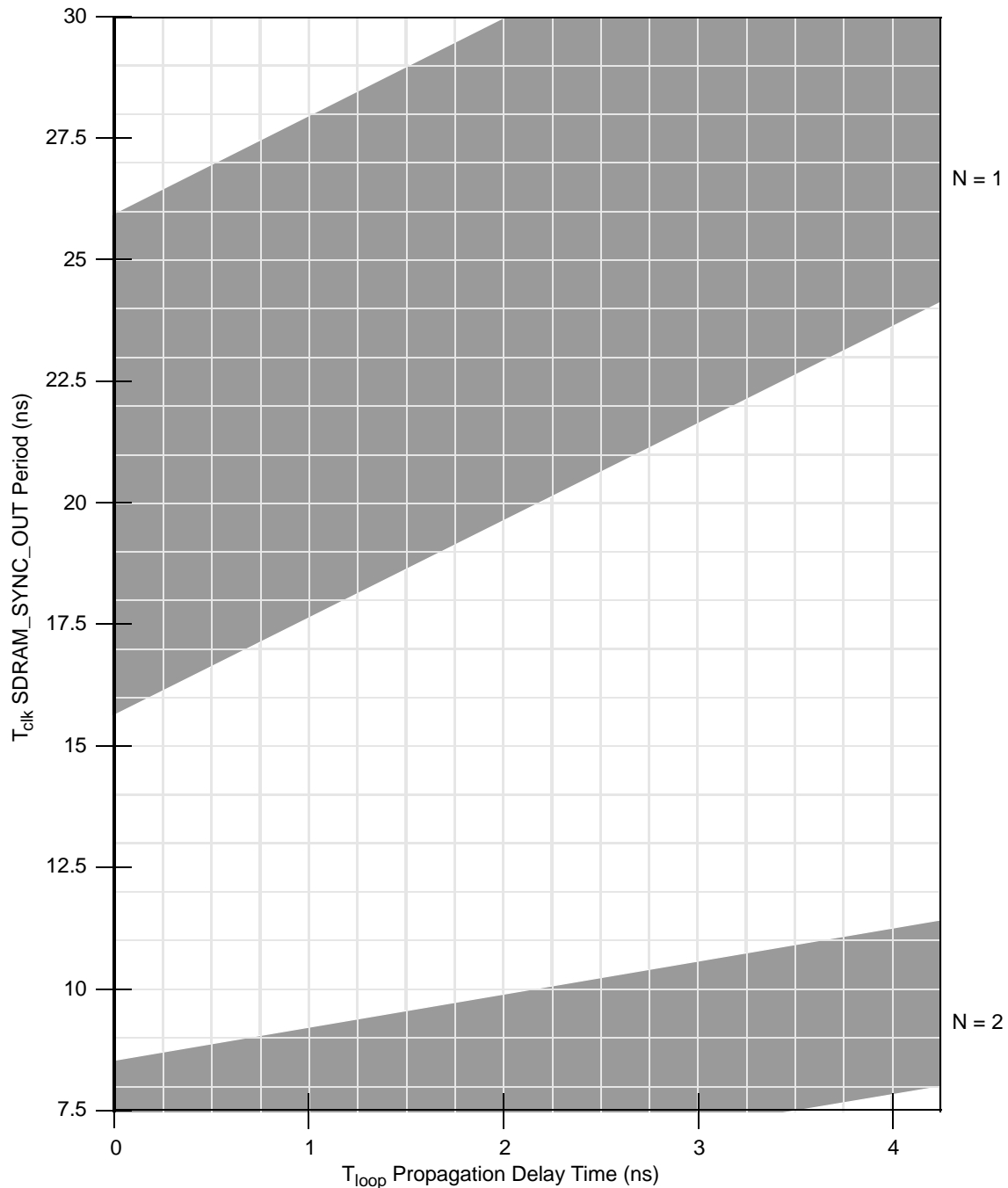
Figure 7. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend = 1 and Normal Tap Delay
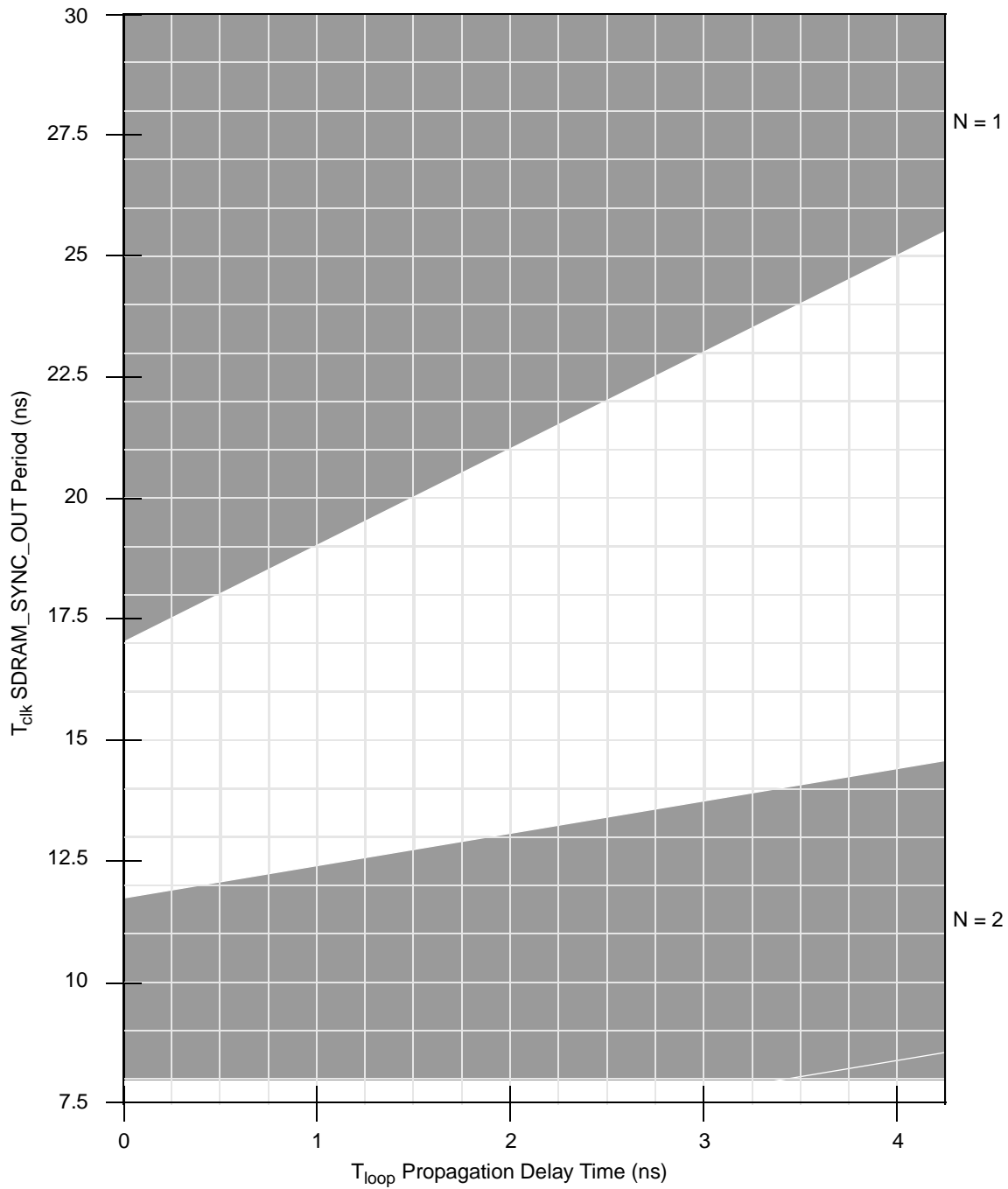
Figure 8. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend = 1 and Tap Max Delay
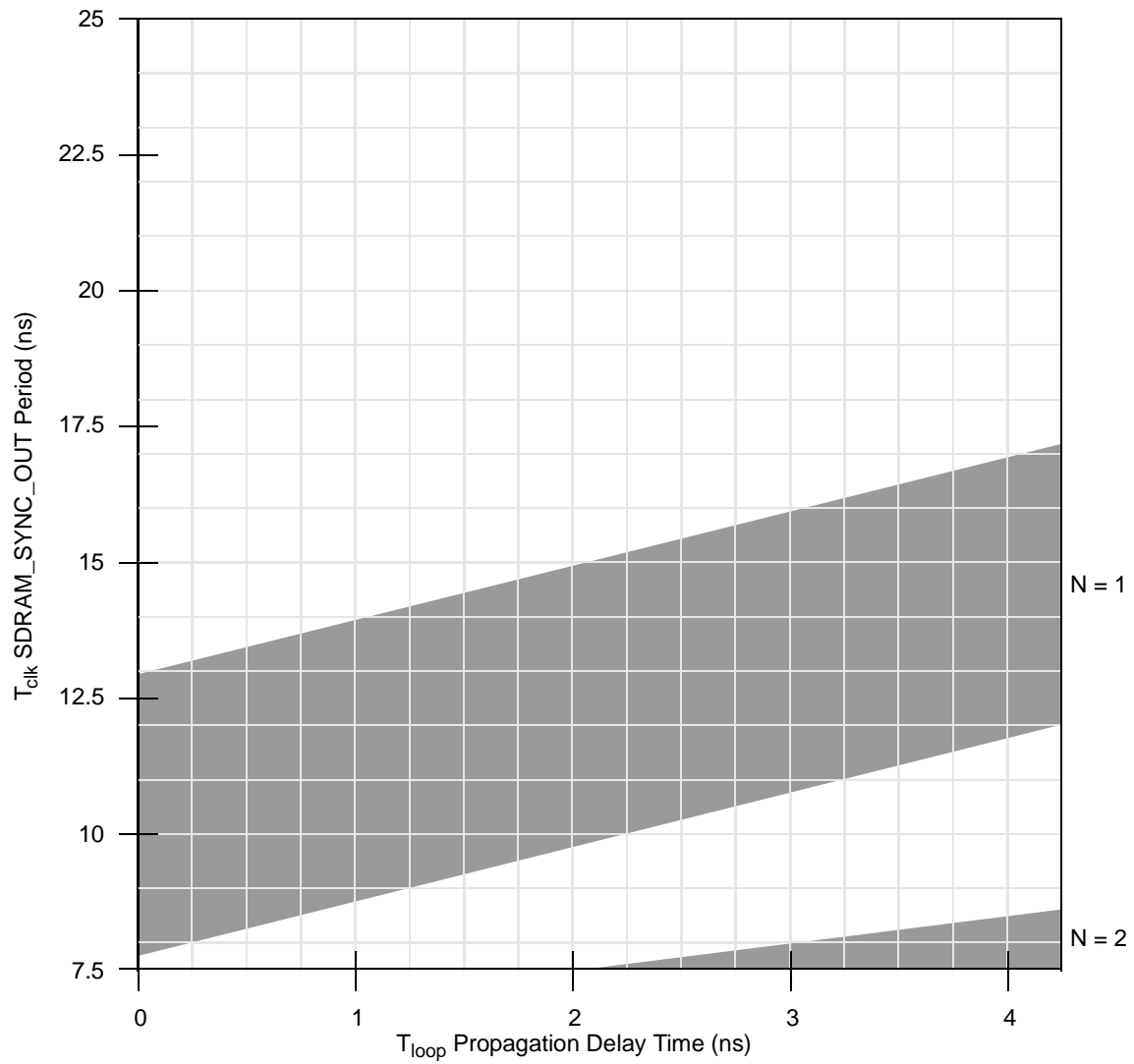
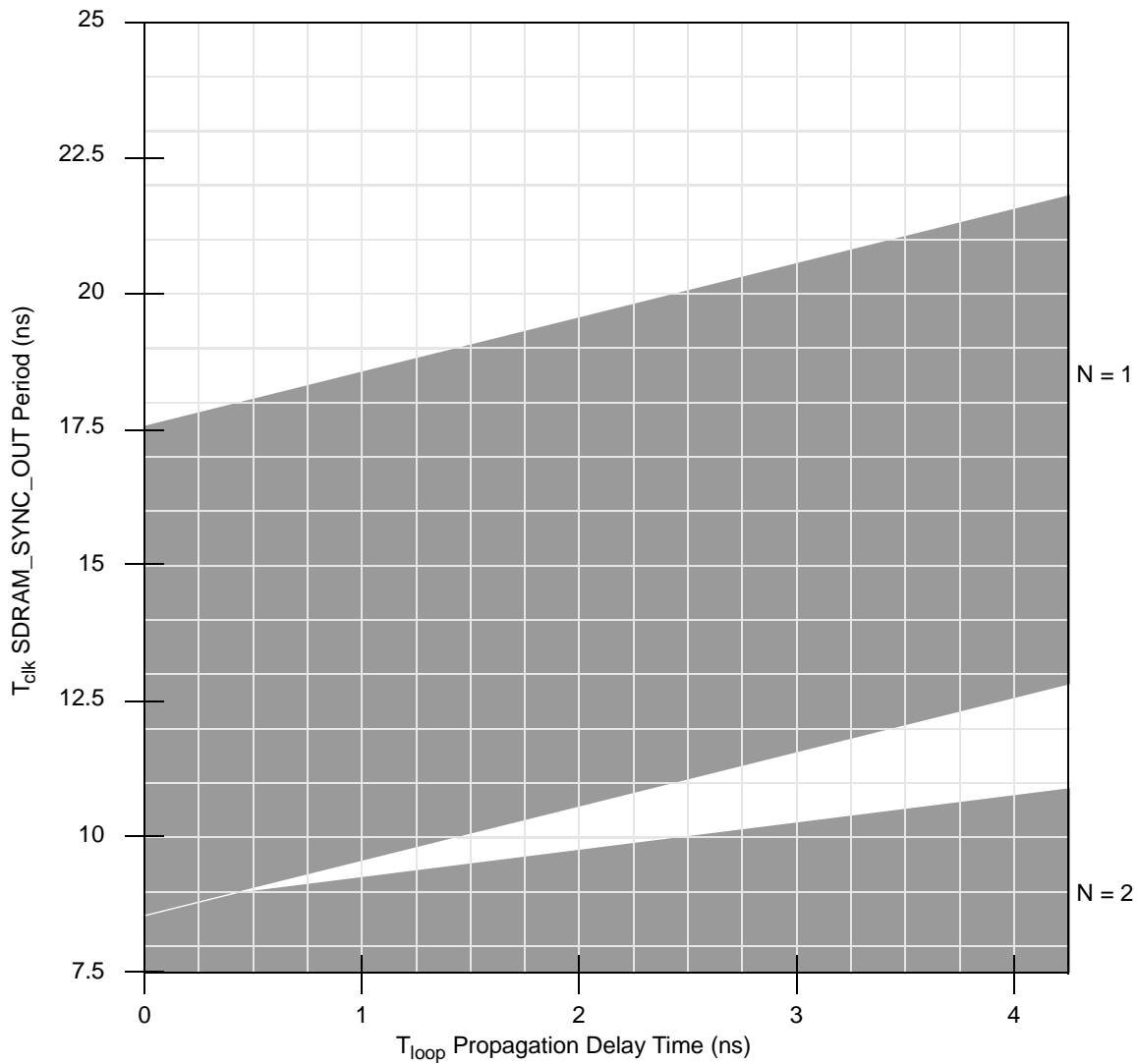**Figure 9. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend = 0 and Normal Tap Delay**

Figure 10. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend = 0 and Max Tap Delay

1.4.3.2   Input AC Timing Specifications

Table 10 provides the input AC timing specifications at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. See Figure 11 and Figure 12.

Electrical and Thermal Characteristics

Table 10. Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b	Memory input signals valid to SDRAM_SYNC_IN (input setup)				
10b0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	0.5	—		
10c	PIC, misc. debug input signals valid to SDRAM_SYNC_IN (input setup)	3.0	—	ns	2, 3
10d	I^{2}C input signals valid to SDRAM_SYNC_IN (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to sys_logic_clk offset time	0.65	1.0	ns	7
11a	SDRAM_SYNC_IN to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	2.1	—		
11b	$\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:
1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 12.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ signal. See Figure 13.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5:4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to sys_logic_clk. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the sys_logic_clk inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. The feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened by this amount relative to the SDRAM clock output trace lengths to maintain phase-alignment of the memory clocks with respect to sys_logic_clk. Note that the DLL locking range graphs of Figure 7 through Figure 10 compensate for T_{os} and there is no additional requirement to shorten T_{loop} by the duration of T_{os}. Refer to Motorola Application Note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for more details on accommodating for the problem of T_{os} and trace measurements in general.
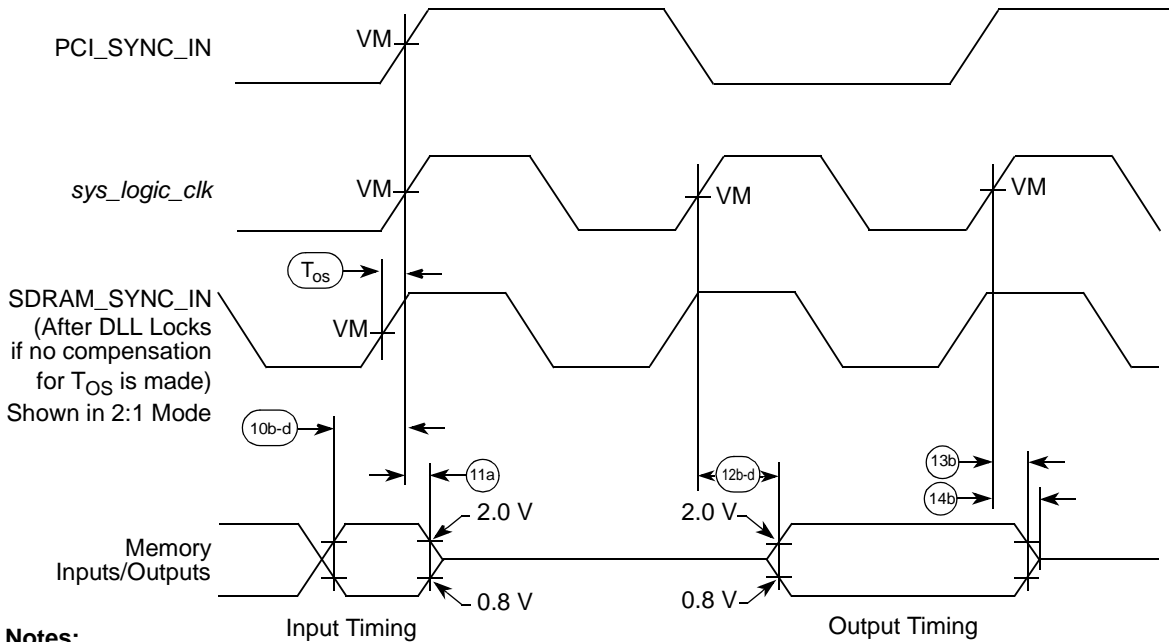
Notes:

VM = midpoint voltage (1.4 V).

10b-d = input signals valid timing.

11a = input hold time of SDRAM_SYNC_IN to memory.

12b-d = SDRAM_SYNC_IN to output valid timing.

13b = output hold time for non-PCI signals.

14b = SDRAM-SYNC_IN to output high-impedance timing for non-PCI signals.

T_{os} = offset timing required to align *sys_logic_clk* with SDRAM_SYNC_IN. The SDRAM_SYNC_IN signal is adjusted by the DLL to accommodate for internal delay. This causes SDRAM_SYNC_IN to be seen before *sys_logic_clk* once the DLL locks, if no other accommodation is made for the delay.

Figure 11. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN
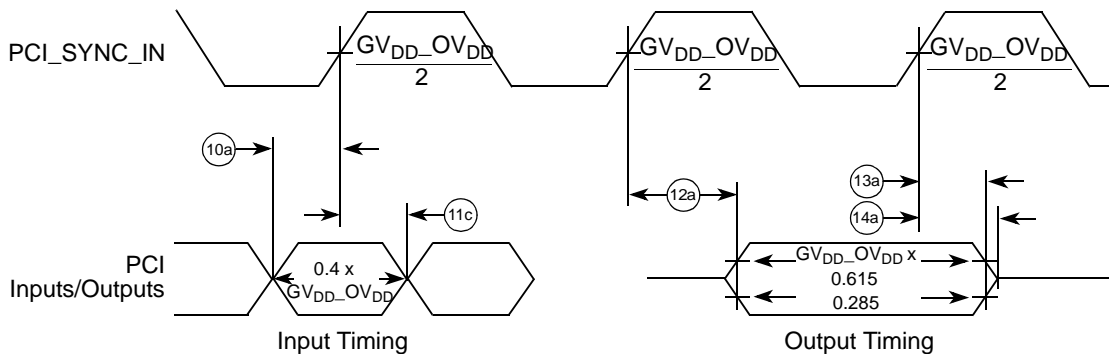
Figure 12. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

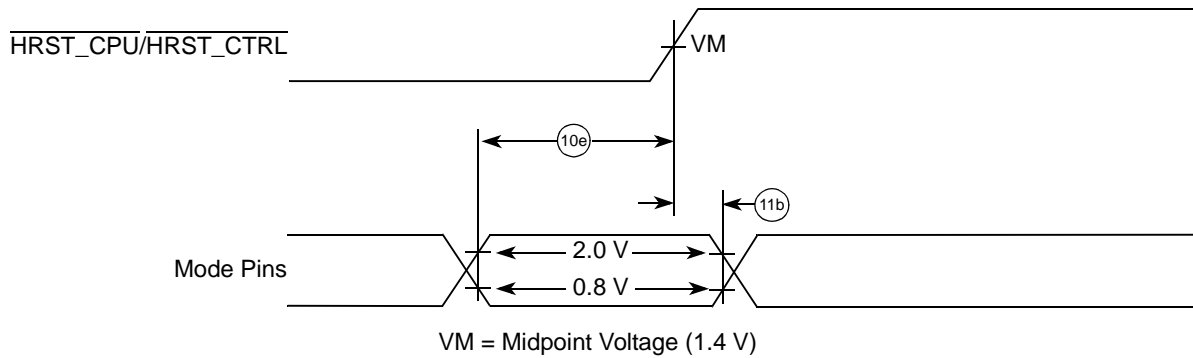VM = Midpoint Voltage (1.4 V)

Figure 13. Input Timing Diagram for Mode Select Signals

1.4.3.3   Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with $LV_{DD} = 3.3\ V \pm 0.3\ V$. See Figure 11. All output timings assume a purely resistive 50-Ω load (see Figure 14). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths indicated in Table 4.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{MCP}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{MCP}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{MCP}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{MCP}$,CKE] = 00	—	7.5		
12b	SDRAM_SYNC_IN to output valid (memory control and data signals)	—	4.5	ns	2
12c	SDRAM_SYNC_IN to output valid (for all others)	—	7.0	ns	2
12d	SDRAM_SYNC_IN to output valid (for I^{2}C)	—	5.0	ns	2
12e	SDRAM_SYNC_IN to output valid (ROM/Flash/Port X)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{MCP}$,CKE] = 11, 66 MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{MCP}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{MCP}$,CKE] = 01, 33 MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{MCP}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 11. Output AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
14b	SDRAM_SYNC_IN to output high impedance (for all others)	—	4.0	ns	2

Notes:
1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times GV_{DD}\_OV_{DD}$ or $0.615 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0 V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. PCI bused signals are composed of the following signals: $\overline{LOCK}$, $\overline{IRDY}$, C/BE[3:0], PAR, $\overline{TRDY}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$, AD[31:0], $\overline{REQ}$[4:0], $\overline{GNT}$[4:0], IDSEL, and $\overline{INTA}$.
4. In order to meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8241 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{MCP}$ and CKE reset configuration signals; the values on these two signals are inverted then stored as the initial settings of PCI_HOLD_DEL = PMCR2[5:4] (power management configuration register 2 <0x72>), respectively. Since $\overline{MCP}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. See Figure 15.
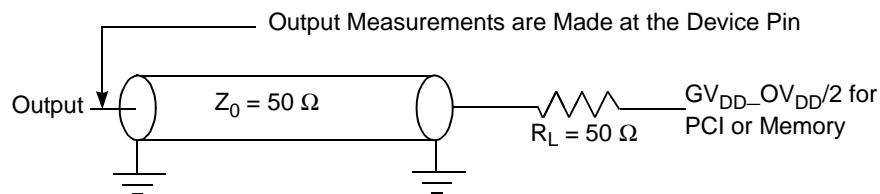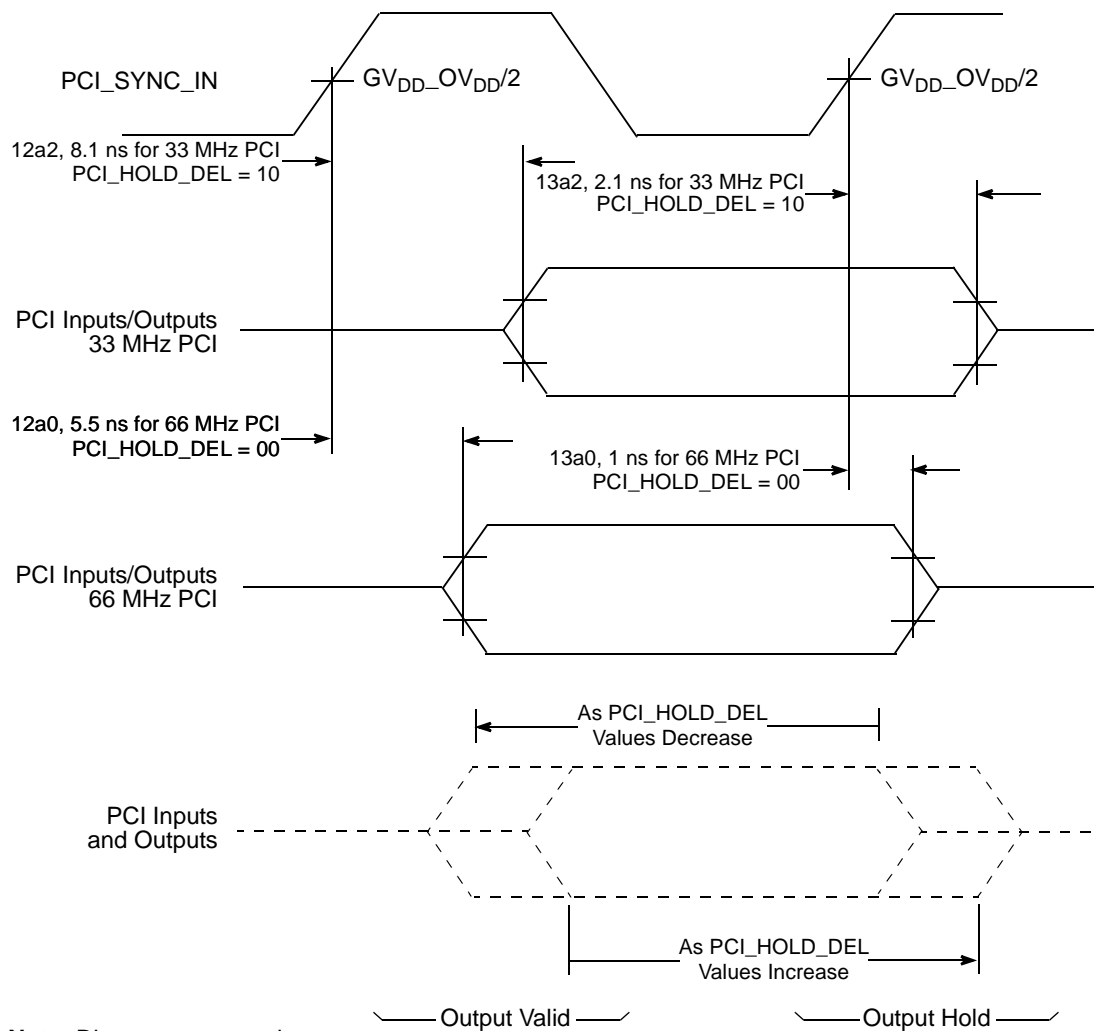

Figure 14. AC Test Load for the MPC8241

Figure 15. PCI_HOLD_DEL Affect on Output Valid and Hold Time

1.4.3.4 I²C AC Timing Specifications

Table 12 provides the I²C input AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with $LV_{DD} = 3.3$ V $\pm$ 0.3 V.

Table 12. I²C Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	4.0	—	CLKs	1, 2
2	Clock low period (time before the MPC8241 will drive SCL low as a transmitting slave after detecting SCL low as driven by an external master)	$8.0 + (16 \times 2^{FDR[4:2]}) \times (5 - 4(\{FDR[5],FDR[1]\} == b'10) - 3(\{FDR[5],FDR[1]\} == b'11) - 2(\{FDR[5],FDR[1]\} == b'00) - 1(\{FDR[5],FDR[1]\} == b'01))$	—	CLKs	1, 2, 4, 5
3	SCL/SDA rise time (from 0.5 to 2.4 V)	—	1	ms	
4	Data hold time	0	—	ns	2
5	SCL/SDA fall time (from 2.4 to 0.5 V)	—	1	ms	
6	Clock high period (time needed to either receive a data bit or generate a START or STOP)	5.0	—	CLKs	1, 2, 5
7	Data setup time	3.0	—	ns	3
8	Start condition setup time (for repeated start condition only)	4.0	—	CLKs	1,2
9	Stop condition setup time	4.0	—	CLKs	1, 2

Notes:

1. Units for these specifications are in SDRAM_CLK units.
2. The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I²C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK clock times DFFSR times two plus one SDRAM_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 17.
3. Timing is relative to the sampling clock (not SCL).
4. FDR[*x*] refers to the frequency divider register I2CFDR bit *x*.
5. Input clock low and high periods in combination with the FDR value in the frequency divider register (I2CFDR) determine the maximum I²C input frequency. See Table 13.

Table 13 provides the I^{2}C frequency divider register (I2CFDR) information for the MPC8241.

Table 13. MPC8241 Maximum I^{2}C Input Frequency

FDR Hex [2]	Divider [2] (Dec)	Max I^{2}C Input Frequency [1]			
		SDRAM_CLK @ 33 MHz	SDRAM_CLK @ 50 MHz	SDRAM_CLK @ 100 MHz	SDRAM_CLK [4] @ 133 MHz
20, 21	160, 192	1.13 MHz	1.72 MHz	3.44 MHz	4.58 MHz
22, 23, 24, 25	224, 256, 320, 384	733	1.11 MHz	2.22 MHz	2.95 MHz
0, 1	288, 320	540	819	1.63 MHz	2.18 MHz
2, 3, 26, 27, 28, 29	384, 448, 480, 512, 640, 768	428	649	1.29 MHz	1.72 MHz
4, 5	576, 640	302	458	917	1.22 MHz
6, 7, 2A, 2B, 2C, 2D	768, 896, 960, 1024, 1280, 1536	234	354	709	943
8, 9	1152, 1280	160	243	487	648
A, B, 2E, 2F, 30, 31	1536, 1792, 1920, 2048, 2560, 3072	122	185	371	494
C, D	2304, 2560	83	125	251	335
E, F, 32, 33, 34, 35	3072, 3584, 3840, 4096, 5120, 6144	62	95	190	253
10, 11	4608, 5120	42	64	128	170
12, 13, 36, 37, 38, 39	6144, 7168, 7680, 8192, 10240, 12288	31	48	96	128
14, 15	9216, 10240	21	32	64	85
16, 17, 3A, 3B, 3C, 3D	12288, 14336, 15360, 16384, 20480, 24576	16	24	48	64
18, 19	18432, 20480	10	16	32	43
1A, 1B, 3E, 3F	24576, 28672, 30720, 32768	8	12	24	32
1C, 1D	36864, 40960	5	8	16	21
1E, 1F	49152, 61440	4	6	12	16

Notes:
1. Values are in kHz unless otherwise specified.
2. FDR Hex and Divider (Dec) values are listed in corresponding order.
3. Multiple Divider (Dec) values will generate the same input frequency, but each Divider (Dec) value will generate a unique output frequency as shown in Table 14.
4. Only available for the 266-MHz part.

Electrical and Thermal Characteristics

Table 14 provides the I^{2}C output AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with $LV_{DD} = 3.3$ V ± 0.3 V.

Table 14. I^{2}C Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	(FDR[5] == 0) × (D$_{FDR}$/16)/2N + (FDR[5] == 1) × (D$_{FDR}$/16)/2M	—	CLKs	1–3
2	Clock low period	D$_{FDR}$/2	—	CLKs	1–3
3	SCL/SDA rise time (from 0.5 to 2.4 V)	—	—	ms	4
4	Data hold time	8.0 + (16 × 2$^{FDR[4:2]}$) × (5 – 4({FDR[5],FDR[1]} == b'10) – 3({FDR[5],FDR[1]} == b'11) – 2({FDR[5],FDR[1]} == b'00) – 1({FDR[5],FDR[1]} == b'01))	—	CLKs	1–3
5	SCL/SDA fall time (from 2.4 to 0.5 V)	—	< 5	ns	5
6	Clock high time	D$_{FDR}$/2	—	CLKs	1–3
7	Data setup time (MPC8241 as a master only)	(D$_{FDR}$/2) – (output data hold time)	—	CLKs	1, 3
8	Start condition setup time (for repeated start condition only)	D$_{FDR}$ + (output start condition hold time)	—	CLKs	1–3
9	Stop condition setup time	4.0	—	CLKs	1, 2

Notes:

1. Units for these specifications are in SDRAM_CLK units.
2. The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I^{2}C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK clock times DFFSR times two plus one SDRAM_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 17.
3. D$_{FDR}$ is the decimal divider number indexed by FDR[5:0] value. Refer to Table 10-5 in the *MPC8245 Integrated Processor User's Manual.* FDR[*x*] refers to the frequency divider register I2CFDR bit *x*. N is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 16. M is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 9.
4. Since SCL and SDA are open-drain type outputs, which the MPC8241 can only drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
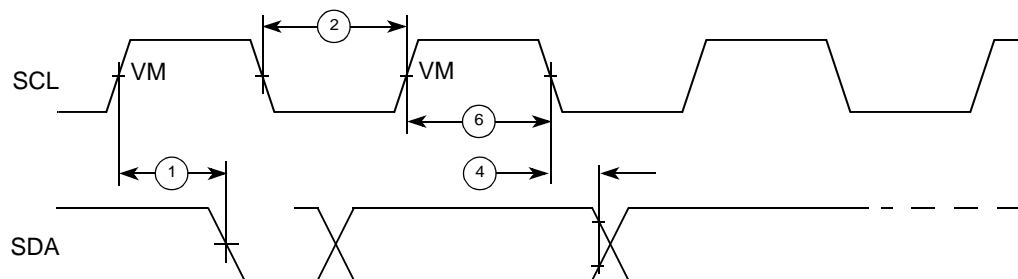5. Specified at a nominal 50 pF load.

Figure 16. I^{2}C Timing Diagram I

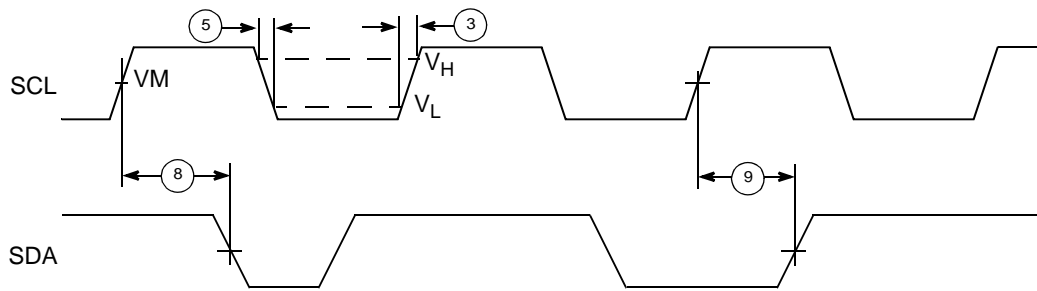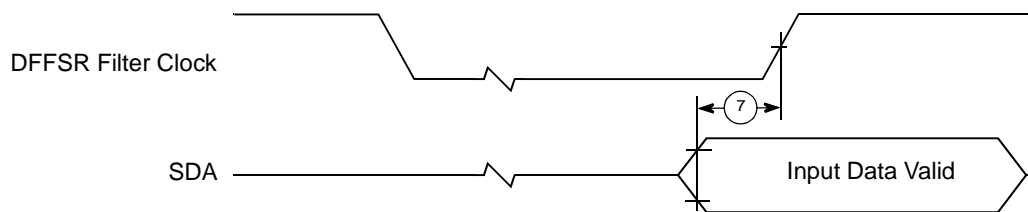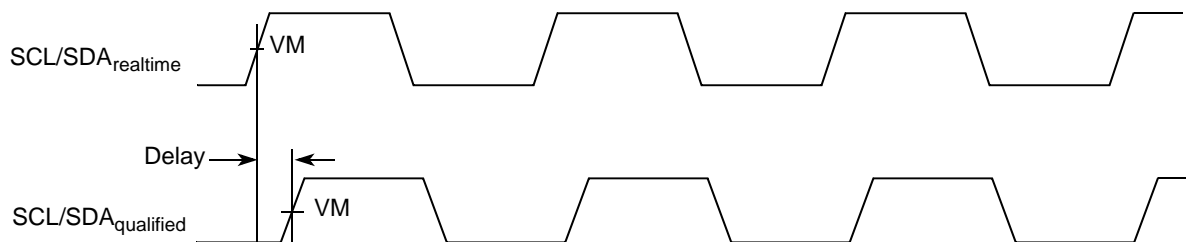**Figure 17. I^{2}C Timing Diagram II**

Note: DFFSR filter clock is the SDRAM_CLK clock times DFFSR value.

Figure 18. I^{2}C Timing Diagram III

Note: The delay is the local memory clock times DFFSR times two plus one local memory clock.

Figure 19. I^{2}C Timing Diagram IV (Qualified Signal)

1.4.3.5 PIC Serial Interrupt Mode AC Timing Specifications

Table 15 provides the PIC serial interrupt mode AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with $GV_{DD}\_OV_{DD} = 3.3$ V $\pm$ 5% and $LV_{DD} = 3.3$ V $\pm$ 0.3 V.

Table 15. PIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	—
3	S_CLK output valid time	—	6	ns	—
4	Output hold time	0	—	ns	—
5	$\overline{S\_FRAME}$, S_RST output valid time	—	1 *sys_logic_clk* period + 6	ns	2
6	S_INT input setup time to S_CLK	1 *sys_logic_clk* period + 2	—	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	—	0	ns	2

Notes:
1. See the *MPC8245 Integrated Processor User's Manual* for a description of the PIC interrupt control register (ICR) describing S_CLK frequency programming.
2. S_RST, $\overline{S\_FRAME}$, and S_INT shown in Figure 20 and Figure 21, depict timing relationships to *sys_logic_clk* and S_CLK and do not describe functional relationships between S_RST, $\overline{S\_FRAME}$, and S_INT. See the *MPC8245 Integrated Processor User's Manual* for a complete description of the functional relationships between these signals.
3. The *sys_logic_clk* waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; *sys_logic_clk* is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8245 Integrated Processor User's Manual* for a complete clocking description.
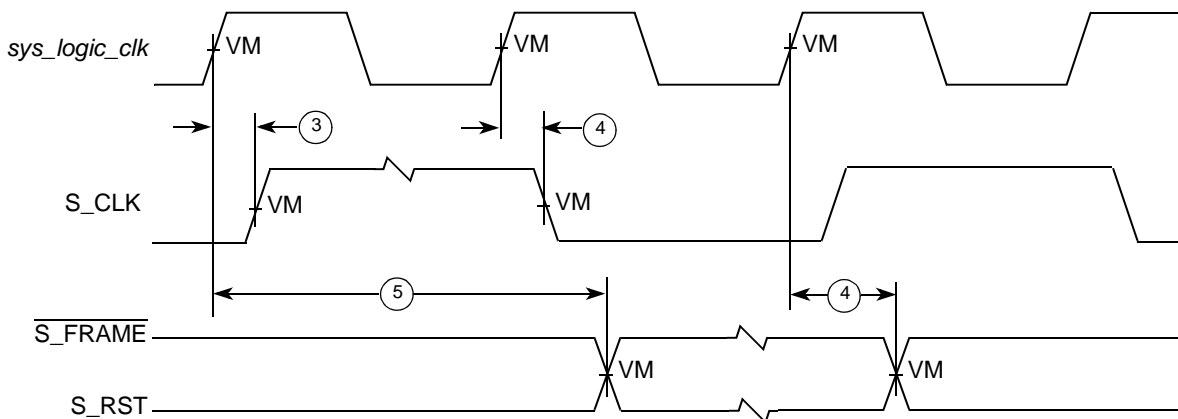

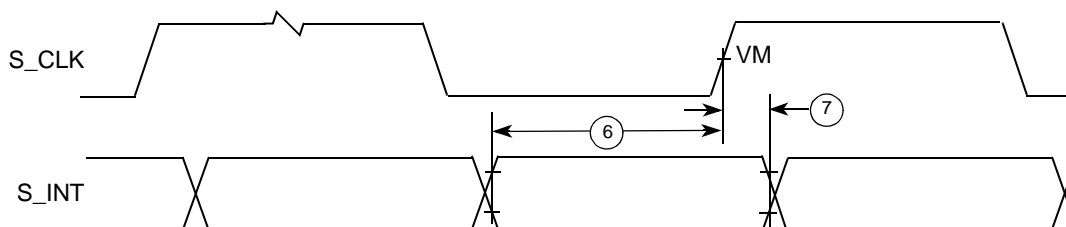**Figure 20. PIC Serial Interrupt Mode Output Timing Diagram**

Figure 21. PIC Serial Interrupt Mode Input Timing Diagram

1.4.3.6　IEEE 1149.1 (JTAG) AC Timing Specifications

Table 16 provides the JTAG AC timing specifications for the MPC8241 while in the JTAG operating mode at recommended operating conditions (see Table 2) with $LV_{DD} = 3.3$ V $\pm$ 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 16. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.5 V	20	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	0	15	ns	
13	TCK to TDO high impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
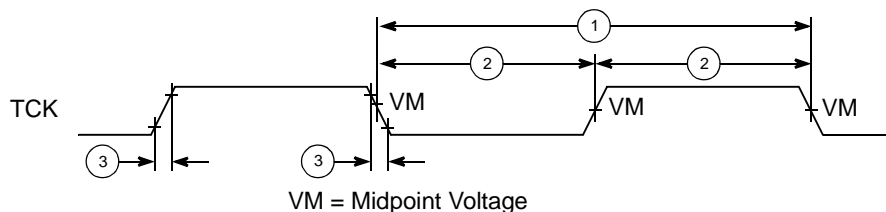3. Nontest (other than TDO) signal output timing with respect to TCK.

VM = Midpoint Voltage

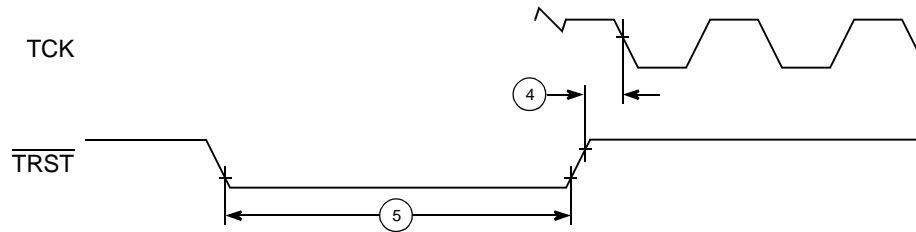**Figure 22. JTAG Clock Input Timing Diagram**
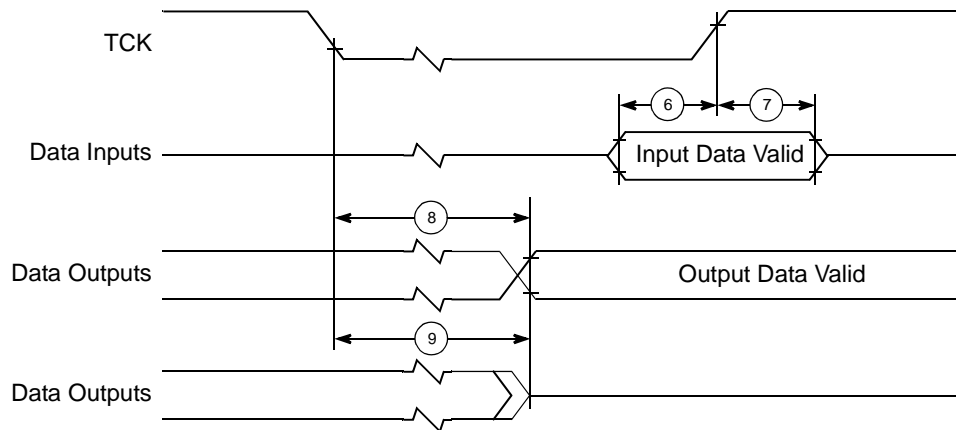
Figure 23. JTAG TRST Timing Diagram

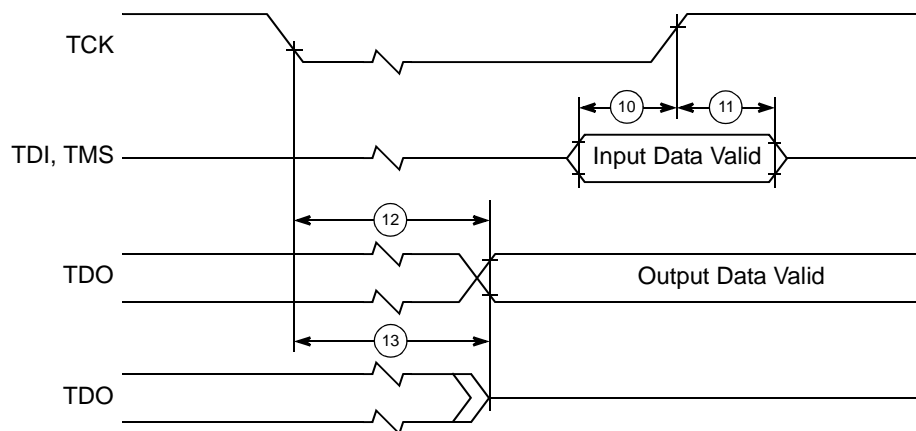**Figure 24. JTAG Boundary Scan Timing Diagram**

Figure 25. Test Access Port Timing Diagram

1.5 Package Description

This section details package parameters, pin assignments, and dimensions.

1.5.1 Package Parameters for the MPC8241

The MPC8241 uses a 25 mm × 25 mm, cavity up, 357-pin plastic ball grid array (PBGA) package. The package parameters are as follows.

Package Outline	25 mm × 25 mm
Interconnects	357
Pitch	1.27 mm
Solder Balls	ZQ (PBGA)—62 Sn/36 Pb/2 Ag
	VR (Lead free version of package)—95.5 Sn/4.0 Ag/0.5 Cu
Solder Ball Diameter	0.75 mm
Maximum Module Height	2.52 mm
Co-planarity Specification	0.15 mm
Maximum Force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

1.5.2 Pin Assignments and Package Dimensions

Figure 26 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA package.
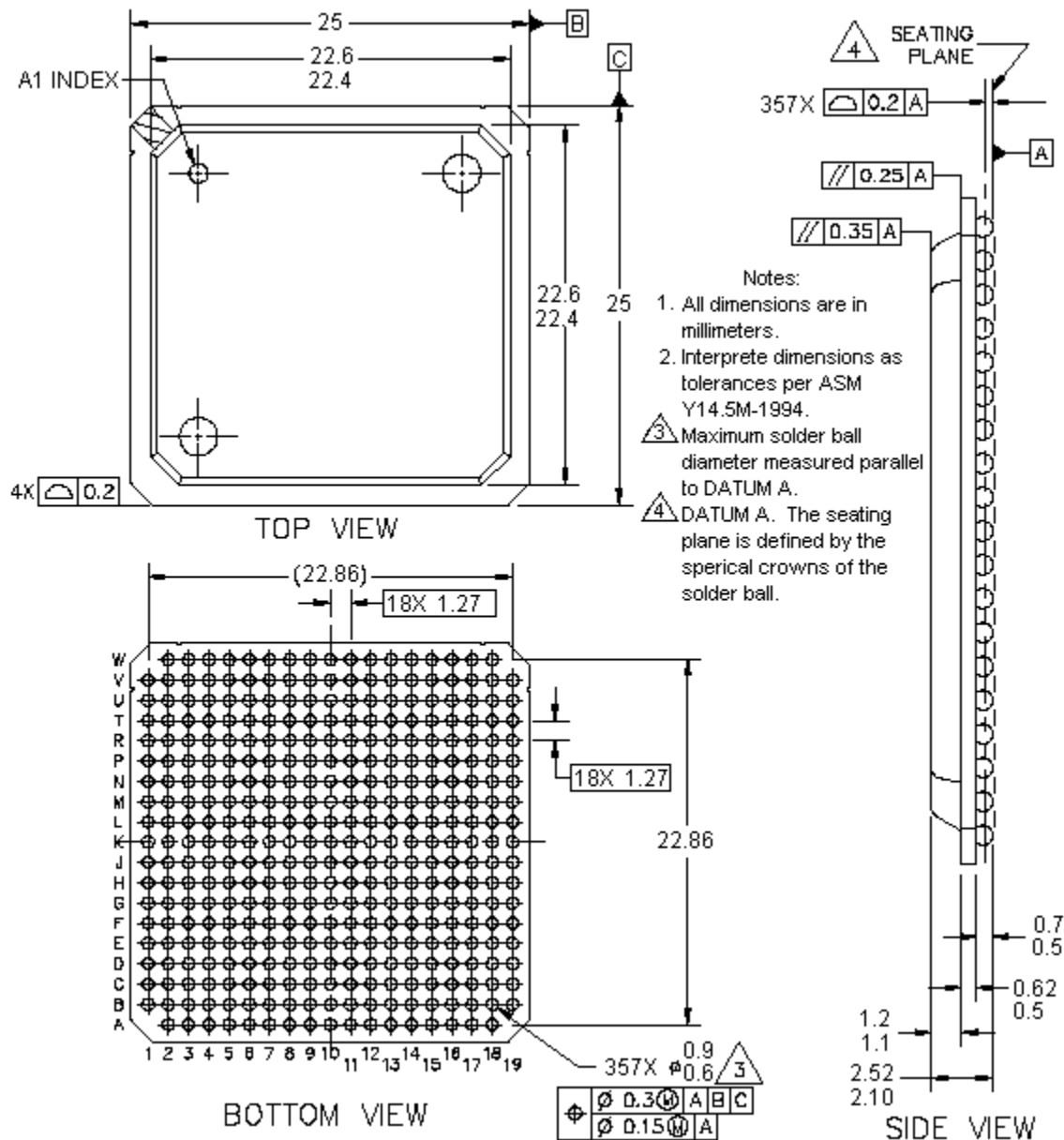

Figure 26. MPC8241 Package Dimensions and Pinout Assignments

1.5.3 Pinout Listings

Table 17 provides the pinout listing for the MPC8241, 357 PBGA package.

Table 17. MPC8241 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals						
$\overline{\text{C/BE}}$[3:0]	V11 V7 W3 R3	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{DEVSEL}}$	U6	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{FRAME}}$	T8	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{IRDY}}$	U7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{LOCK}}$	V6	Input	$GV_{DD}\_OV_{DD}$	—	3
AD[31:0]	U13 V13 U11 W14 V14 U12 W10 T10 V10 U9 V9 W9 W8 T9 W7 V8 V4 W4 V3 V2 T5 R6 V1 T2 U3 P3 T4 R1 T3 R4 U2 U1	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
PAR	R7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2
$\overline{\text{GNT}}$[3:0]	W15 U15 W17 V12	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{GNT}}$4/DA5	T11	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 4, 5
$\overline{\text{REQ}}$[3:0]	V16 U14 T15 V15	Input	$GV_{DD}\_OV_{DD}$	—	1, 6
$\overline{\text{REQ}}$4/DA4	W13	I/O	$GV_{DD}\_OV_{DD}$	—	5, 6
$\overline{\text{PERR}}$	T7	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3, 7
$\overline{\text{SERR}}$	U5	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3, 8
$\overline{\text{STOP}}$	W5	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{TRDY}}$	W6	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{INTA}}$	T12	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 8
IDSEL	U10	Input	$GV_{DD}\_OV_{DD}$	—	
Memory Interface Signals						
MDL[0:31]	M19 M17 L16 L17 K18 J18 K17 K16 J15 J17 H18 F16 H16 H15 G17 D19 B3 C4 C2 D3 G5 E1 H5 E2 F1 F2 G2 J5 H1 H4 J4 J1	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1, 9
MDH[0:31]	M18 L18 L15 K19 K15 J19 J16 H17 G19 G18 G16 D18 F18 E18 G15 E15 C3 D4 E5 F5 D1 E4 D2 E3 F4 G3 G4 G1 H2 J3 J2 K5	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1
DQM[0:7]	A18 B18 A6 C7 D15 D14 A9 B8	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1

Package Description

Table 17. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{CS}$[0:7]	A17 B17 C16 C17 C9 C8 A10 B10	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
FOE	A7	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{RCS0}$	C10	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{RCS1}$	B9	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	
$\overline{RCS2}$/TRIG_IN	P18	I/O	$GV_{DD}\_OV_{DD}$	—	5, 12
$\overline{RCS3}$/TRIG_OUT	N18	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	5
SDMA[1:0]	A15 B15	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1, 10, 11
SDMA[11:2]	A11 B12 A12 C12 B13 C13 D12 A14 C14 B14	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{DRDY}$	P1	Input	$GV_{DD}\_OV_{DD}$	—	5, 13
SDMA12/$\overline{SRESET}$	L3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA13/TBEN	K3	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA14/ $\overline{CHKSTOP\_IN}$	K2	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDBA1	C11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	
SDBA0	B11	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	
PAR[0:7]	E19 C19 D5 D6 E16 F17 B2 C1	I/O	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1
$\overline{SDRAS}$	B19	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
$\overline{SDCAS}$	D16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10
CKE	C6	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{WE}$	B16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	
$\overline{AS}$	A16	Output	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	10, 11
PIC Control Signals					
IRQ0/S_INT	P4	Input	$GV_{DD}\_OV_{DD}$	—	
IRQ1/S_CLK	R2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	
IRQ2/S_RST	U19	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	
IRQ3/$\overline{S\_FRAME}$	P15	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	
IRQ4/$\overline{L\_INT}$	P2	I/O	$GV_{DD}\_OV_{DD}$	DRV_PCI	

Package Description

Table 17. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
I²C Control Signals					
SDA	P17	I/O	GV_{DD}_OV_{DD}	DRV_STD_MEM	8, 12
SCL	R19	I/O	GV_{DD}_OV_{DD}	DRV_STD_MEM	8, 12
DUART Control Signals					
SOUT1/PCI_CLK0	T16	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
SIN1/PCI_CLK1	U16	I/O	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
SOUT2/$\overline{RTS1}$/ PCI_CLK2	W18	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
SIN2/$\overline{CTS1}$/ PCI_CLK3	V19	I/O	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
Clock-Out Signals					
PCI_CLK0/SOUT1	T16	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
PCI_CLK1/SIN1	U16	I/O	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
PCI_CLK2/$\overline{RTS1}$/ SOUT2	W18	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
PCI_CLK3/$\overline{CTS1}$/ SIN2	V19	I/O	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
PCI_CLK4/DA3	V17	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5, 14
PCI_SYNC_OUT	U17	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	
PCI_SYNC_IN	V18	Input	GV_{DD}_OV_{DD}	—	
SDRAM_CLK[0:3]	D7 B7 C5 A5	Output	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	1, 22
SDRAM_SYNC_OUT	B4	Output	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	
SDRAM_SYNC_IN	A4	Input	GV_{DD}_OV_{DD}	—	
CKO/DA1	L1	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5
OSC_IN	R17	Input	GV_{DD}_OV_{DD}	—	15
Miscellaneous Signals					
$\overline{HRST\_CTRL}$	M2	Input	GV_{DD}_OV_{DD}	—	
$\overline{HRST\_CPU}$	L4	Input	GV_{DD}_OV_{DD}	—	
$\overline{MCP}$	K4	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	10, 11, 16
NMI	M1	Input	GV_{DD}_OV_{DD}	—	
$\overline{SMI}$	L2	Input	GV_{DD}_OV_{DD}	—	12
$\overline{SRESET}$/SDMA12	L3	I/O	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	5, 12
TBEN/SDMA13	K3	I/O	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	5, 12
$\overline{QACK}$/DA0	A3	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5, 10, 11

Package Description

Table 17. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{\text{CHKSTOP\_IN}}$/ SDMA14	K2	I/O	$GV_{DD}\_OV_{DD}$	DRV_MEM_CTRL	5, 12
TRIG_IN/$\overline{\text{RCS2}}$	P18	I/O	$GV_{DD}\_OV_{DD}$	—	5, 12
TRIG_OUT/$\overline{\text{RCS3}}$	N18	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	5, 12
MAA[0:2]	E17 D17 C18	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1, 10, 11
$\overline{\text{MIV}}$	K1	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	23
PMAA[0:1]	N19 N17	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1, 2, 10, 11
PMAA[2]	M15	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	1, 2, 11
Test/Configuration Signals					
PLL_CFG[0:4]/ DA[10:6]	N3 N2 N1 M4 M3	I/O	$GV_{DD}\_OV_{DD}$	—	1, 5, 20
$\overline{\text{TEST0}}$	P16	Input	$GV_{DD}\_OV_{DD}$	—	13, 21
$\overline{\text{DRDY}}$	P1	Input	$GV_{DD}\_OV_{DD}$	—	5, 13
RTC	D13	Input	$GV_{DD}\_OV_{DD}$	—	12
TCK	T19	Input	$GV_{DD}\_OV_{DD}$	—	6, 13
TDI	N15	Input	$GV_{DD}\_OV_{DD}$	—	6, 13
TDO	T17	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	23
TMS	T18	Input	$GV_{DD}\_OV_{DD}$	—	6, 13
$\overline{\text{TRST}}$	R16	Input	$GV_{DD}\_OV_{DD}$	—	6, 13
Power and Ground Signals					
GNDRING/GND	F07 F08 F09 F10 F11 F12 F13 G07 G08 G09 G10 G11 G12 G13 H07 H08 H09 H10 H11 H12 H13 J07 J08 J09 J10 J11 J12 J13 K07 K08 K09 K10 K11 K12 K13 L07 L08 L09 L10 L11 L12 L13 M07 M08 M09 M10 M11 M12 M13 N07 N08 N09 N10 N11 N12 N13 P08 P09 P10 P11 P12 P13 R15	Ground		—	17
LV_{DD}	R18 U18 T1 U4 T6 W11 T14	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	

Table 17. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$GV_{DD}\_OV_{DD}/$ PWRRING	D09 D10 D11 E06 E07 E08 E09 E10 E11 E12 E13 E14 F06 F14 G06 G14 H06 H14 J06 J14 K06 K14 L06 L14 M06 M14 N06 N14 P06 P07 P14 R08 R09 R10 R11 R12	Power for memory drivers and PCI/Stnd 3.3 V	$GV_{DD}\_OV_{DD}$	—	18
V_{DD}	F03 H3 L5 N4 P5 V5 U8 W12 W16 R13 P19 L19 H19 F19 F15 C15 A13 A8 B5 A2	Power for core 1.8 V	V_{DD}	—	
No Connect	N5 W2 B1	—	—	—	
AV_{DD}	M5	Power for PLL (CPU core logic) 1.8 V	AV_{DD}	—	
$AV_{DD}2$	R14	Power for PLL (peripheral logic) 1.8 V	$AV_{DD}2$	—	
Debug/Manufacturing Pins					
DA0/$\overline{QACK}$	A3	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	5, 10, 11
DA1/CKO	L1	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	5
DA2	R5	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	19
DA3/PCI_CLK4	V17	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI_CLK	5
DA4/$\overline{REQ4}$	W13	I/O	$GV_{DD}\_OV_{DD}$	—	5, 6
DA5/$\overline{GNT4}$	T11	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	2, 4, 5
DA[10:6]/ PLL_CFG[0:4]	N3 N2 N1 M4 M3	I/O	$GV_{DD}\_OV_{DD}$	—	1, 5, 20
DA[11]	T13	Output	$GV_{DD}\_OV_{DD}$	DRV_PCI	1, 19
DA[12:13]	M16 N16	Output	$GV_{DD}\_OV_{DD}$	DRV_STD_MEM	19

Table 17. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
DA[14:15]	B6 D8	Output	GV$_{DD}$_OV$_{DD}$	DRV_MEM_CTRL	1, 19

Notes:
1. Multi-pin signals such as AD[31:0] or MDL[0:31] have their physical package pin numbers listed in order corresponding to the signal names. Ex: AD0 is on pin U1, AD1 is on pin U2,..., AD31 is on pin U13.
2. This pin is affected by programmable PCI_HOLD_DEL parameter.
3. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this PCI control pin to LV$_{DD}$.
4. $\overline{\text{GNT4}}$ is a reset configuration pin and has an internal pull-up resistor which is enabled only when the MPC8241 is in the reset state.
5. This pin is a multiplexed signal and appears more than once in this table.
6. This pin has an internal pull-up resistor which is enabled at all times. The value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
7. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification* (Rev. 2.2).
8. This pin is an open drain signal.
9. DL[0] is a reset configuration pin and has an internal pull-up resistor which is enabled only when the MPC8241 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
10. This pin has an internal pull-up resistor which is enabled only when the MPC8241 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
11. This pin is a reset configuration pin.
12. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to GV$_{DD}$_OV$_{DD}$.
13. V$_{IH}$ and V$_{IL}$ for these signals are the same as the PCI V$_{IH}$ and V$_{IL}$ entries in Table 3.
14. External PCI clocking source or fanout buffer may be required for system if using the MPC8241 DUART functionality since PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
15. OSC_IN utilizes the 3.3-V PCI interface driver which is 5-V tolerant, see Table 2 for details.
16. This pin can be programmed to be driven (default) or can be programmed (in PMCR2) to be open drain.
17. All grounded pins are connected together; connections should not be made to individual pins. The list represents the balls that are connected to Ground.
18. GV$_{DD}$_OV$_{DD}$ must not exceed V$_{DD}$/AV$_{DD}$/AV$_{DD}$2 by more than 1.8 V at any time including during power-on reset. Note that GV$_{DD}$_OV$_{DD}$ pins are all shorted together, PWRRING. The list represents the balls that are connected to PWRRING. Connections should not be made to individual PWRRING pins.
19. Treat these pins as No Connects unless using debug address functionality.
20. PLL_CFG signals must be driven on reset.
21. Place a pull-up resistor of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
22. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev 1.1 (A). These signals use DRV_MEM_CLK for chip Rev 1.2B.
23. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.

1.6 PLL Configuration

The internal PLLs of the MPC8241 are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations for the MPC8241 is shown in Table 18 and Table 19.

PLL Configuration

Table 18. PLL Configurations for the 166 and 200 MHz parts of MPC8241

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2] PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	200-MHz Part [2] PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	Multipliers PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	Not available			$25\text{-}26^5$	75-78	188-195	3 (2)	2.5 (2)
2	00010	$34^4–37^5$	34–37	153–166	$34^4–44^5$	34–44	153–200	1 (4)	4.5 (2)
3	00011^6	$50^7–66^3$	50–66	100–132	$50^7–66^3$	50–66	100–132	1 (Bypass)	2 (4)
4	00100	$25–41^5$	50–82	100–164	$25–44^{8,10}$	50–88	100–176	2 (4)	2 (4)
5	00101^6	$60–66^3$	60–66	150–165	$60–66^3$	60–66	150–165	1 (Bypass)	2.5 (2)
6	00110^9	Bypass			Bypass			Bypass	Bypass
7 Rev B	00111^6	$50^4–55^{\,5}$	50–55	150–166	$50^4–66^3$	50–66	150–198	1 (Bypass)	3 (2)
7 Rev D	00111	Not available							
8	01000	$50^4–55^5$	50–55	150–166	$50^4–66^3$	50–66	150–198	1 (4)	3 (2)
9	01001	$38^4–41^{5,11}$	76–82	152–164	$38^4–50^{5,12}$	76–100	152–200	2 (2)	2 (2)
B	01011	Not available			44^5	66	198	2(2)	2.5(2)
C	01100	$30^4–33^5$	60–66	150–165	$30^4–40^5$	60–80	150–200	2 (4)	2.5 (2)
E	01110	$25–27^5$	50–54	150–162	$25–33^5$	60–66	150–198	2 (4)	3 (2)
10	10000	$25–27^{5,11}$	75–83	150–166	$25–33^{5,12}$	75–100	150–200	3 (2)	2 (2)
12	10010	$50^4–55^{5,11}$	75–83	150–166	$50^4–66^3$	75–99	150–198	1.5 (2)	2 (2)
14	10100	Not available			$25–28^5$	50–56	175–196	2 (4)	3.5 (2)
16	10110				25^5	50	200	2(4)	4(2)
17	10111				25^5	100	200	4(2)	2(2)
19	11001	$33^{5,13}$	66	165	$33^{13}–40^5$	66–80	165–200	2(2)	2.5(2)
1A	11010	$37^4–41^5$	37–41	150–166	$37^4–50^5$	37–50	150–200	1 (4)	4 (2)
1B	11011	Not available			$33^{5,13}$	66	198	2(2)	3(2)
1C	11100				$44^{5,13}$	66	198	1.5(2)	3(2)
1D	11101	$44^{5,13}$	66	166	$44^{13}–53^5$	66–80	165–200	1.5 (2)	2.5 (2)
1E	11110^{14}	Not usable			Not usable			Off	Off

PLL Configuration

Table 18. PLL Configurations for the 166 and 200 MHz parts of MPC8241 (continued)

Ref [2]	PLL_ CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_ SYNC_IN) Range [3] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_ SYNC_IN) Range [3] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[14]	Not usable			Not usable			Off	Off

Notes:
1. PLL_CFG[0:4] settings not listed are reserved. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value. Note the impact of the relevant revisions for mode 7.
2. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
3. Limited by maximum PCI input frequency (66 MHz).
4. Limited by minimum CPU VCO frequency (300 MHz).
5. Limited by maximum CPU operating frequency.
6. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.
7. Limited by minimum CPU operating frequency (100 MHz).
8. Limited due to maximum memory VCO frequency (352 MHz).
9. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in dual PLL bypass mode.
10. Limited by maximum CPU VCO frequency (704 MHz).
11. Limited by maximum system memory interface operating frequency (83 MHz @ 166 MHz CPU bus speed).
12. Limited by maximum system memory interface operating frequency (100 MHz @ 200 MHz CPU bus speed).
13. Limited by minimum memory VCO frequency (132 MHz).
14. In clock off mode, no clocking occurs inside the MPC8241 regardless of the PCI_SYNC_IN input.

Table 19. PLL Configurations (266-MHz Parts)

Ref [2]	PLL_ CFG[0:4] [10,13]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–35[5]	75–105	188–263	3 (2)	2.5 (2)
1	00001[12]	25–29[5]	75–88	225–264	3 (2)	3 (2)
2	00010[11]	50[18]–59[5]	50–59	225–266	1 (4)	4.5 (2)
3	00011[11,14]	50[17]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100[12]	25–44[4]	50–88	100–176	2 (4)	2 (4)
5	00101	Reserved			Note 20	
6	00110[15]	Bypass			Bypass	

PLL Configuration

Table 19. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,13]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
7 (Rev B)	00111[14]	50[6]–66[1]	50–66	150–198	1 (Bypass)	3 (2)
7 (Rev D)	00111[14]	Not Available				
8	01000[12]	50[6]–66[1]	50–66	150–198	1 (4)	3 (2)
9	01001[19]	38[6]–66[1]	76–132	152–264	2 (2)	2 (2)
A	01010[12]	25–29[5]	50–58	225–261	2 (4)	4.5 (2)
B	01011[19]	45[3]–59[5]	68–88	204–264	1.5 (2)	3 (2)
C	01100[12]	30[6]–44[4]	60–88	150–220	2 (4)	2.5 (2)
D	01101[19]	45[3]–50[5]	68–75	238–263	1.5 (2)	3.5 (2)
E	01110[12]	25–44[5]	50–88	150–264	2 (4)	3 (2)
F	01111[19]	25[5]	75	263	3 (2)	3.5 (2)
10	10000[12]	25–44[16,5]	75–132	150–264	3 (2)	2 (2)
11	10001[19]	25–26[5]	100–106	250–266	4 (2)	2.5 (2)
12	10010[12]	50[6]–66[1]	75–99	150–198	1.5 (2)	2 (2)
13	10011[19]	Not available			4 (2)	3 (2)
14	10100[12]	25–38[5]	50–76	175–266	2 (4)	3.5 (2)
15	10101[19]	Not available			2.5 (2)	4 (2)
16	10110[12]	25–33[5]	50–66	200–264	2 (4)	4 (2)
17	10111[19]	25–33[5]	100–132	200–264	4 (2)	2 (2)
18	11000[12]	27[3]–35[5]	68–88	204–264	2.5 (2)	3 (2)
19	11001[19]	33[3]–53[5]	66–106	165–265	2 (2)	2.5 (2)
1A	11010[12]	50[18]–66[1]	50–66	200–264	1 (4)	4 (2)
1B	11011[19]	34[3]–44[5]	68–88	204–264	2 (2)	3 (2)
1C	11100[12]	44[3]–59[5]	66–88	198–264	1.5 (2)	3 (2)
1D	11101[12]	44[3]–66[1]	66–99	165–248	1.5 (2)	2.5 (2)
1E (Rev B)	11110[8]	Not usable			Off	Off
1E (Rev D)	11110	33[3]–38[5]	66-76	231-266	2(2)	3.5(2)

PLL Configuration

Table 19. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,13]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Off	Off

Notes:
1. Limited by maximum PCI input frequency (66 MHz).
2. Note the impact of the relevant revisions for modes 7 and 1E.
3. Limited by minimum memory VCO frequency (132 MHz).
4. Limited due to maximum memory VCO frequency (352 MHz).
5. Limited by maximum CPU operating frequency.
6. Limited by minimum CPU VCO frequency (300 MHz).
7. Limited by maximum CPU VCO frequency (704 MHz).
8. In clock off mode, no clocking occurs inside the MPC8241 regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings not listed are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting are different from the MPC8240 and are not backwards-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting is different from the MPC8240 and may not be fully backwards-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in dual PLL bypass mode.
16. Limited by maximum system memory interface operating frequency (133 MHz @ 266 MHz CPU).
17. Limited by minimum CPU operating frequency (100 MHz).
18. Limited by minimum memory bus frequency (50 MHz).
19. PCI_SYNC_IN range for this PLL_CFG[0:4] setting does not exist on the MPC8240 and may not be fully backwards-compatible.
20. No longer supported.

1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8241.

1.7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals are provided on the MPC8241 to provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 27 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over using multiple values.

The circuits should be placed as close as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing directly as possible from the capacitors to the input signal pins with minimal inductance of vias is important.
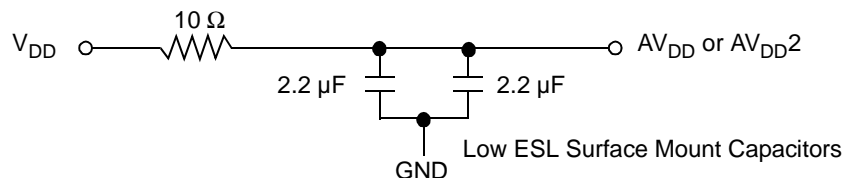
Figure 27. PLL Power Supply Filter Circuit

1.7.2 Power Supply Sizing

The power consumption numbers provided in Table 5 do not reflect power from the $GV_{DD}\_OV_{DD}$ power supply which are non-negligible for the MPC8241.

1.7.3 Decoupling Recommendations

Due to its dynamic power management feature, the large address and data buses, and its high operating frequencies, the MPC8241 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8241 system, and the MPC8241 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, $GV_{DD}\_OV_{DD}$, and LV_{DD} pin of the MPC8241. It is also recommended that these decoupling capacitors receive their power from dedicated power planes in the PCB, utilizing short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $GV_{DD}\_OV_{DD}$, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two

vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active-low inputs should be tied to OV_{DD}. Unused active-high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}_OV_{DD}, LV_{DD}, and GND pins of the MPC8241.

The PCI_SYNC_OUT signal is intended to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input of the MPC8241.

The SDRAM_SYNC_OUT signal is intended to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC8241. The trace length may be used to skew or adjust the timing window as needed. See Motorola application notes AN1849/D, *MPC107 Design Guide,* and AN2164/D, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for more information on this topic. Note that there is an SDRAM_SYNC_IN to PCI_SYNC_IN time requirement (see Table 10).

1.7.5 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected by the system to minimize possible output switching.

The $\overline{TEST0}$ pin requires a pull-up resistor of 120 Ω or less connected to GV_{DD}_OV_{DD}.

It is recommended that RTC have weak pull-up resistors (2–10 kΩ) connected to GV_{DD}_OV_{DD}.

It is recommended that the following signals be pulled up to GV_{DD}_OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{SMI}$, $\overline{SRESET}$/SDMA12, TBEN/SDMA13, $\overline{CHKSTOP\_IN}$/SDMA14, TRIG_IN/$\overline{RCS2}$, and $\overline{DRDY}$.

It is recommended that the following PCI control signals be pulled up to LV_{DD} with weak pull-up resistors (2–10 kΩ): $\overline{DEVSEL}$, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{LOCK}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{STOP}$, and $\overline{TRDY}$. The resistor values may need to be adjusted stronger to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{REQ}$[3:0], $\overline{REQ4}$/DA4, TCK, TDI, TMS, and $\overline{TRST}$. See Table 17 for more information.

The following pins have internal pull-up resistors enabled only while device is in the reset state: $\overline{GNT4}$/DA5, MDL0, $\overline{FOE}$, $\overline{RCS0}$, $\overline{SDRAS}$, $\overline{SDCAS}$, CKE, $\overline{AS}$, $\overline{MCP}$, MAA[0:2], PMAA[0:2], and $\overline{QACK}$/DA0. See Table 17 for more information.

The following pins are reset configuration pins: $\overline{GNT4}$/DA5, MDL[0], $\overline{FOE}$, $\overline{RCS0}$, CKE, $\overline{AS}$, $\overline{MCP}$, $\overline{QACK}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{HRST\_CPU}$ and $\overline{HRST\_CTRL}$.

Reset configuration pins should be tied to GND via 1-kΩ pull-down resistors to ensure a logic zero level is read into the configuration bits during reset if the default logic-one level is not desired.

Any other unused active low input pins should be tied to a logic-one level via weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 17. Unused active high input pins should be tied to GND via weak pull-down resistors (2–10 kΩ).

1.7.6 PCI Reference Voltage—LV$_{DD}$

The MPC8241 PCI reference voltage (LV$_{DD}$) pins should be connected to 3.3 ± 0.3 V power supply if interfacing the MPC8241 into a 3.3-V PCI bus system. Similarly, the LV$_{DD}$ pins should be connected to 5.0 V $\pm 5\%$ power supply if interfacing the MPC8241 into a 5-V PCI bus system. For either reference voltage, the MPC8241 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8241 tolerates 5-V signals when interfaced into a 5-V PCI bus system. (See Errata No. 18 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*).

1.7.7 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 28 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on.

The COP header shown in Figure 28 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 28; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 28 is common to all known emulators.
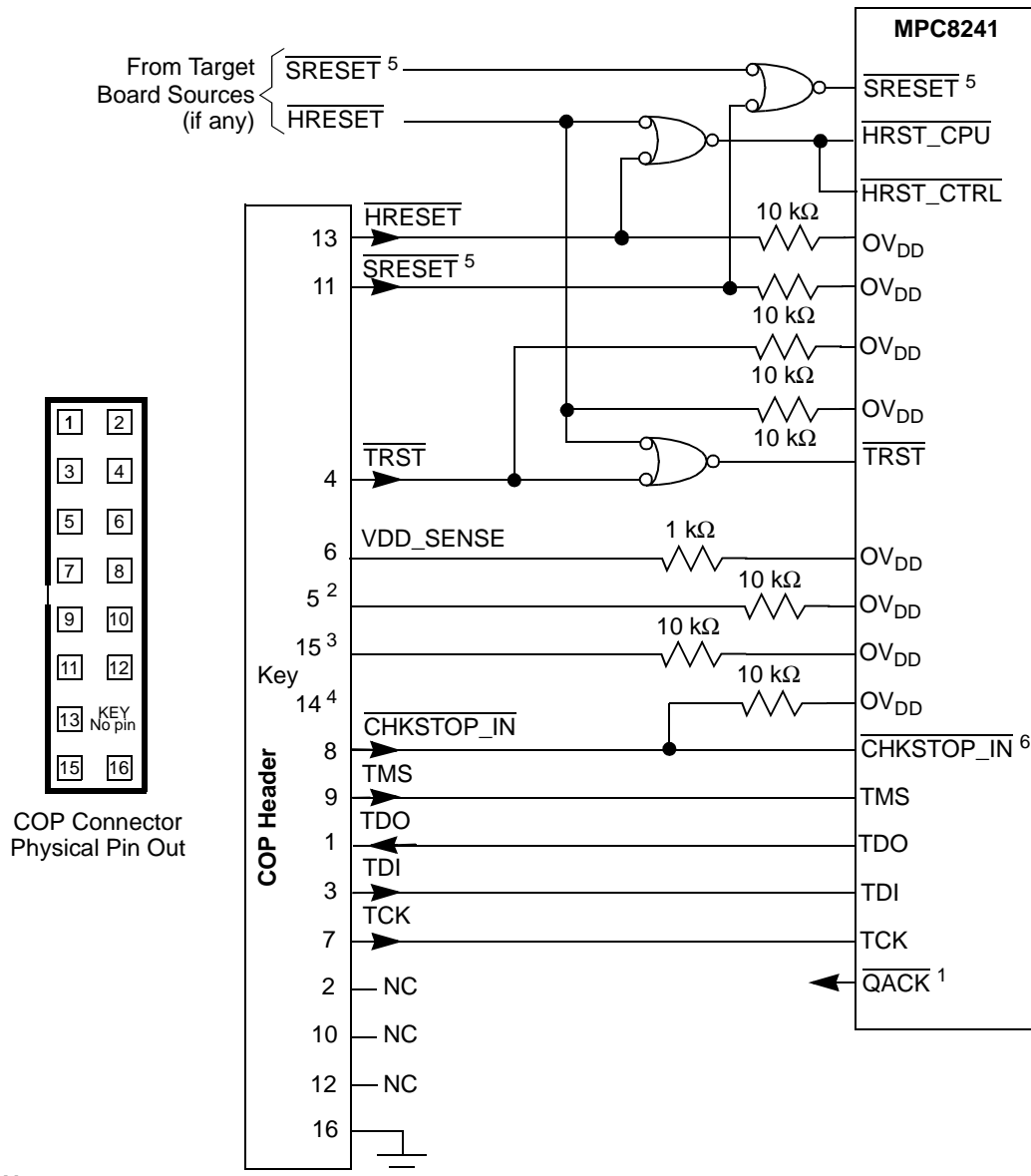
Figure 28. COP Connector Diagram

Notes:

1. $\overline{\text{QACK}}$ is an output on the MPC8241 and is not required at the COP header for emulation.
2. RUN/STOP normally found on pin 5 of the COP header is not implemented on the MPC8241. Connect pin 5 of the COP header to OV_{DD} with a 1-kΩ pull-up resistor.
3. $\overline{\text{CKSTP\_OUT}}$ normally found on pin 15 of the COP header is not implemented on the MPC8241 Connect pin 15 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
4. Pin 14 is not physically present on the COP header.
5. $\overline{\text{SRESET}}$ functions as output SDMA12 in extended ROM mode.
6. CHKSTOP_IN functions as output SDMA14 in extended ROM mode.

1.7.8   Thermal Management Information

This section provides thermal management information for the plastic ball grid array (PBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, a heat sink may be required to maintain junction temperature within specifications. Proper thermal control design is primarily dependent on the system-level design: heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly; see Figure 29.
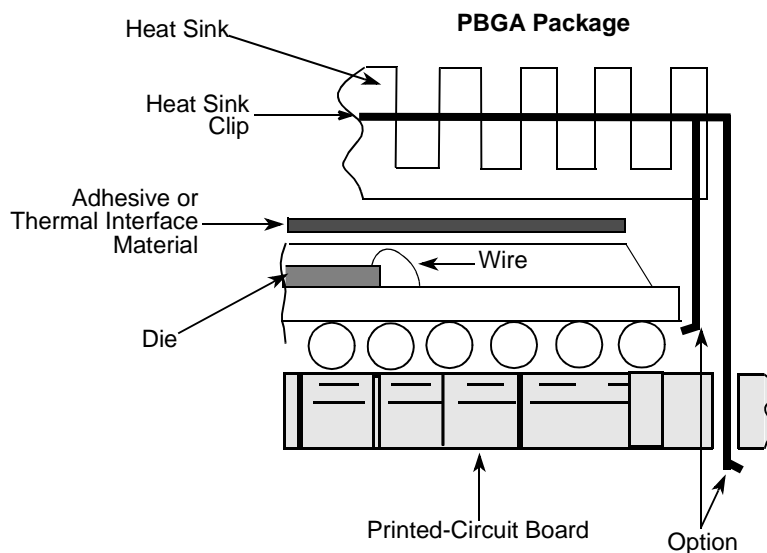
Figure 29. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 30 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the PBGA package and there exists a high board level thermal loading from adjacent components. (Label used—1s.)
- A heat sink is not attached to the PBGA package and there exists a low board level thermal loading from adjacent components. (Label used—2s2p.)
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and there exists high board level thermal loading from adjacent components. (Label used—1s/sink.)
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and there exists low board level thermal loading from adjacent components. (Label used—2s2p/sink.)
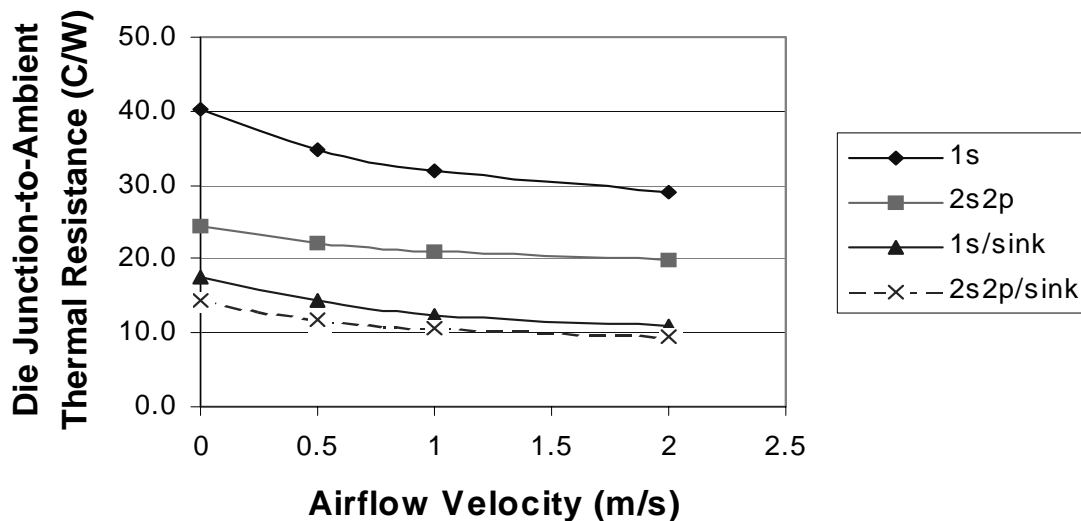
Figure 30. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8241. There are several commercially available heat sinks for the MPC8241 provided by the following vendors:

Aavid Thermalloy   603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech   408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC)   818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics   800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering   603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

1.7.8.1 Internal Package Conduction Resistance

For the PBGA, die-up, packaging technology, shown in Figure 29, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-ball thermal resistance

Figure 31 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

(Note the internal versus external package resistance)
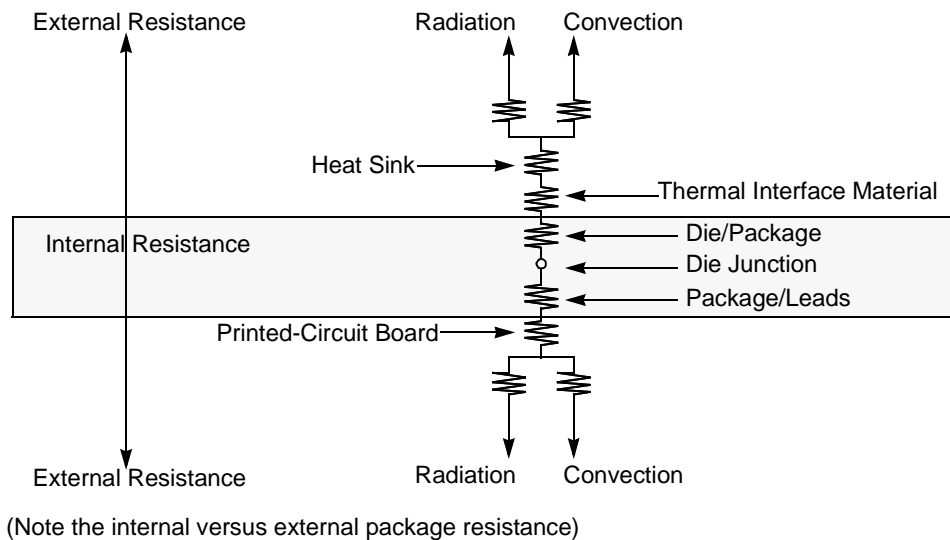
Figure 31. PBGA Package with Heat Sink Mounted to a Printed-Circuit Board

For this die-up, wire-bond PBGA package, heat generated on the active side of the chip is conducted mainly through the mold cap, the heat sink attach material (or thermal interface material), and finally through the heat sink where it is removed by forced-air convection.

1.7.8.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended between the top of the mold cap and the bottom of the heat sink to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 32 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 29). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors: thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.
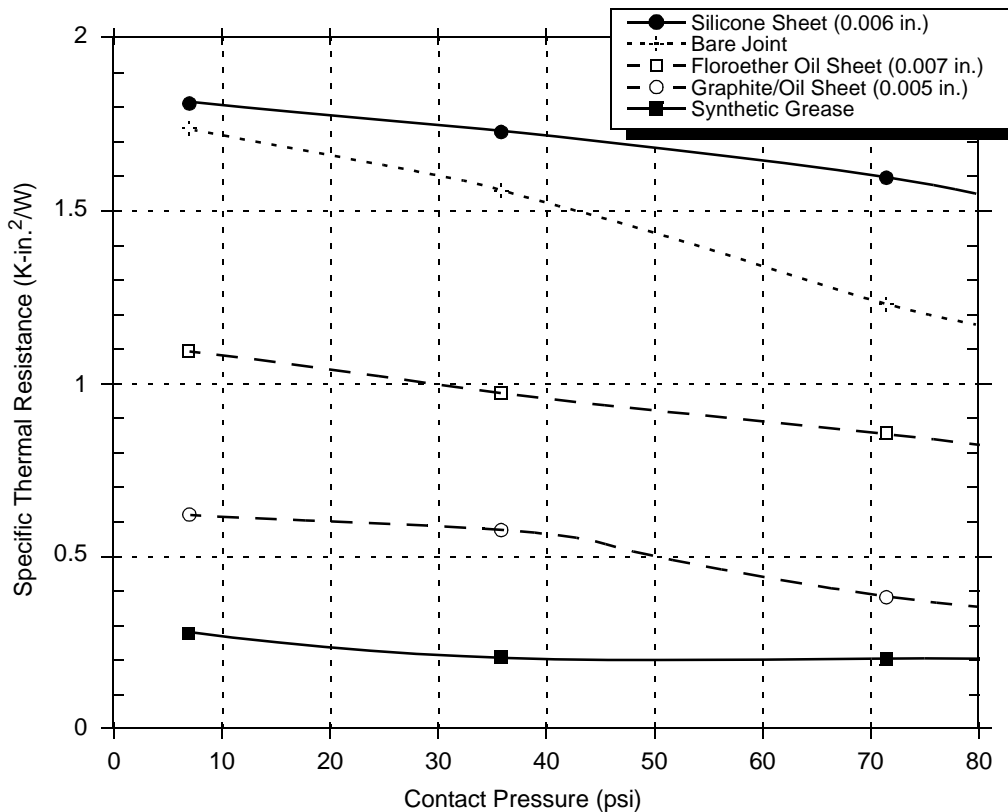
Figure 32. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company	800-347-4572
18930 West 78th St.	
Chanhassen, MN 55317	
Internet: www.bergquistcompany.com	
Chomerics, Inc.	781-935-4850
77 Dragon Ct.	
Woburn, MA 01888-4014	
Internet: www.chomerics.com	
Dow-Corning Corporation	800-248-2481
Dow-Corning Electronic Materials	
2200 W. Salzburg Rd.	
Midland, MI 48686-0997	
Internet: www.dow.com	
Shin-Etsu MicroSi, Inc.	888-642-7674
10028 S. 51st St.	
Phoenix, AZ 85044	
Internet: www.microsi.com	

Thermagon Inc.   888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

1.7.8.3   Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature atop the package (°C)
ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

1.7.9   References

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1.8 Document Revision History

Table 20 provides a revision history for this hardware specification.

Table 20. Revision History Table

Rev. No.	Substantive Change(s)
0	Initial release.
0.1	Updated Features list in Section 1.2. Corrected pin assignments in Table 16 for DA[15] and DQM[3] signals. Added vendor (Cool Innovations, Inc.) to list of heat sink vendors.
0.2	Table 16—Corrected pin number for PLL_CFG0/DA10 to N3. The pin was already correctly listed for DA10/PLL_CFG0. Updated note 1 to reflect pin assignments for the MPC8241. Updated footnotes throughout document. Section 1.4.3.3—Updated note 4 to correct bit values of PCI_HOLD_DEL in PMCR2. Section 1.6—Updated notes in Table 17. Included memory VCO minimum and maximum numbers. Section 1.7.8—Updated description of bits PCI_HOLD_DEL in PMCR2. Section 1.7.10.3—Replaced thermal characterization parameter (YJT) with correct thermal characterization parameter (ψ_{JT}). Changed ψ_π symbol to ψ_{JT}.
0.3	Corrected solder ball information in Section 1.5.1 to 62 Sn/36 Pb/2 Ag. Section 1.4.3.1—Corrected DLL_EXTEND labeling in Figures 5 through 8. Removed note for pin TRIG_OUT/RCS3 in Table 16, as well as from the list of pins needing to be pulled up to IV_{DD} in Section 1.7.6. Corrected order information labeling in Section 1.9 to MPC8241XZPXXXX. Also corrected label description of ZU=PBGA to ZP=PBGA.
1	Updated document template. Section 1.4.1.5—Updated driver type names in Table 4 so that they are consistent with the driver types referred to in the *MPC8245 Integrated Processor User's Manual*. Added notes 5 and 6 to Table 4. Section 1.4.3.1—Added reference to AN2164 in note 7. Labeled N value in Figures 5 through 8. Section 1.4.3.2—Updated Figure 9 to show T_{os}. Table 9—Changed default for 0x77 bits 5:4 to 0b10. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid Timing. Updated Figure 13 to state GVdd_OVdd instead of OVdd. Section 1.5.3—Updated driver type names to match those used in Table 4. Updated notes for the following signals: $\overline{DRDY}$, SDRAM_CLK[0:3], $\overline{MIV}$, RTC, TDO, and DA[11]. Section 1.6—Updated PLL table and notes. Removed old Section 1.7.2 on voltage sequencing requirements. Added cautions regarding voltage sequencing to the end of Table 2 in Section 1.4.1.2. Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors. Section 1.7.5—Added reference to AN2164. Section 1.7.6—Added sentence regarding the PLL_CFG signals. Removed old Section 1.7.8 since the MPC8241 cannot be used as a drop in replacement for the MPC8240 because of pin compatibility issues. Section 1.7.8—Updated $\overline{TRST}$ information in this section and Figure 26. Section 1.7.9—Updated list for heat sink and thermal interface vendors. Section 1.9—Changed format of ordering information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.

Table 20. Revision History Table

Rev. No.	Substantive Change(s)
2	Section 1.4.1.2—Updated note 1 to include 266-MHz part. Added a line to cautions 2 and 3 in the notes section of Table 2. Added Figures 4 and 5 to show the overshoot and undershoot requirements for the PCI interface. Section 1.4.1.3—Table 3: Updated minimum value for input high voltage, and maximum value for capacitance. Section 1.4.3.2—Appended Figures 9 and 10. Section 1.4.3.4—Added a column to Table 13 to include 133-MHz memory bus speed for 266-MHz part. Section 1.5.2—Changed Figure 24 to accommodate new package offerings. Section 1.6—Added Table 19 for PLL of the 266-MHz part. Section 1.7.7—Corrected note numbering in COP connector diagram. Section 1.9.1—Updated package description in part marking nomenclature.
3	Section 1.4.1.2—Changed recommended value in Table 2 for I/O buffer supply to 3.3 ± 0.3 V. Changed wording referencing Figure 4 to refer to the MPC8241. Section 1.4.2—Table 6: Updated values for thermal characterization data as per the new packaging and 266-MHz part. Added note 7 for the difference between 166/200 MHz and the 266-MHz packaging. Section 1.4.3—Corrected the voltage listing for the 266 MHz to 1.8 ± 0.1 V in Table 7. Section 1.5—Changed package parameters and illustration based on new packaging. Section 1.6—Table 18: Modified PLL configuration for 166- and 200-MHz parts for Mode 7 to specify that this mode is not available for Rev . D of the part. Added sentence to note 1 referencing update for Mode 7. Table 19: Made several range updates for various modes to accommodate VCO limits. Added Mode 7 and 1E updates for Rev. D. Updated VCO limits listed in notes 4, 6, and 7.

1.9   Ordering Information

Ordering information for the parts fully covered by this document is provided in Section 1.9.1, "Part Numbers Fully Addressed by This Document." Section 1.9.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

1.9.1   Part Numbers Fully Addressed by This Document

Table 21 provides the Motorola part numbering nomenclature for the MPC8241. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.The revision level can be determined by reading the Revision ID register at address offset 0x08.

Table 21. Part Numbering Nomenclature

XPC	*nnnn*	L	*xx*	*nnn*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package** [1]	**Processor Frequency** [2]	**Revision Level**
MPC	8241	L = Standard Spec. 1.8 V ± 100 mV 0° to 105°C	ZQ = thick substrate and thick mold cap PBGA VR = Lead free version of package	166 MHz 200 MHz 266 MHz	Contact local Motorola Sales Office

Notes:
1. See Section 1.5, "Package Description," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

1.9.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document; see Table 22.

Table 22. Part Numbers with Separate Documentation

Part Number Series	Operating Conditions	Document Order Number of Applicable Specification
XPC8241TZP*nnnx*	1.8 V ± 100 mV, –40° to 105°C 166 MHz, 200 MHz, 266 MHz	MPC8241TZPPNS/D

Note: For other differences, see applicable specifications.

Ordering Information

1.9.3 Part Marking

Parts are marked as the example shown in Figure 33.
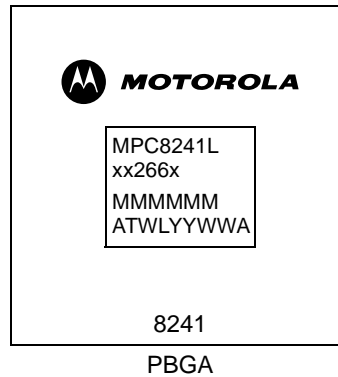
PBGA

Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 33. Part Marking for PBGA Device

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-480-768-2130
(800) 521-6274

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre, 2 Dai King Street
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

(800) 521-6274

HOME PAGE:

www.motorola.com/semiconductors

MOTOROLA

MPC8241EC/D