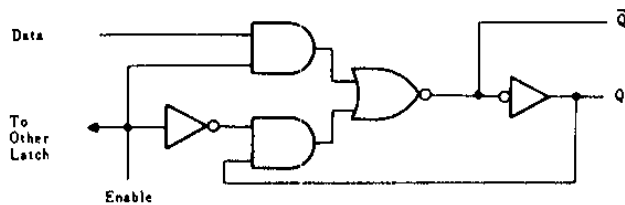


HD74LS75 • Quadruple Bistable Latches

The HD74LS75 is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data(D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high. This device features complementary Q and \bar{Q} outputs from a 4-bit latch.

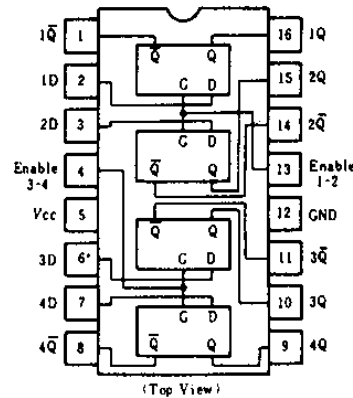
■ BLOCK DIAGRAM (1/4)



■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Pulse width	t_w	20	—	—	ns
Setup time	t_{su}	15	—	—	ns
Hold time	t_h	5	—	—	ns

■ PIN ARRANGEMENT



■ FUNCTION TABLE

Inputs		Outputs	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

Notes) H; high level, L; low level, X; irrelevant
 Q_0 ; level of Q before the indicated steady-state input conditions were established.
 \bar{Q}_0 ; complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established.

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V_{IH}		2.0	—	—	V	
	V_{IL}		—	—	0.8	V	
Output voltage	V_{OH}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$	2.7	—	—	V	
	V_{OL}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OL}=4\text{mA}$	—	—	0.4	V
			$I_{OL}=8\text{mA}$	—	—	0.5	
Input current	I_{IH}	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	D input	—	—	20	μA
			G input	—	—	80	
	I_{IL}	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	D input	—	—	-0.4	mA
			G input	—	—	-1.6	
	I_I	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	D input	—	—	0.1	mA
G input	—	—	0.4				
Short-circuit output current	I_{OS}	$V_{CC}=5.25\text{V}$	-20	—	-100	mA	
Supply current **	I_{CC}	$V_{CC}=5.25\text{V}$	—	6.3	12	mA	
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V	

* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

** I_{CC} is measured with all outputs open and all inputs grounded.

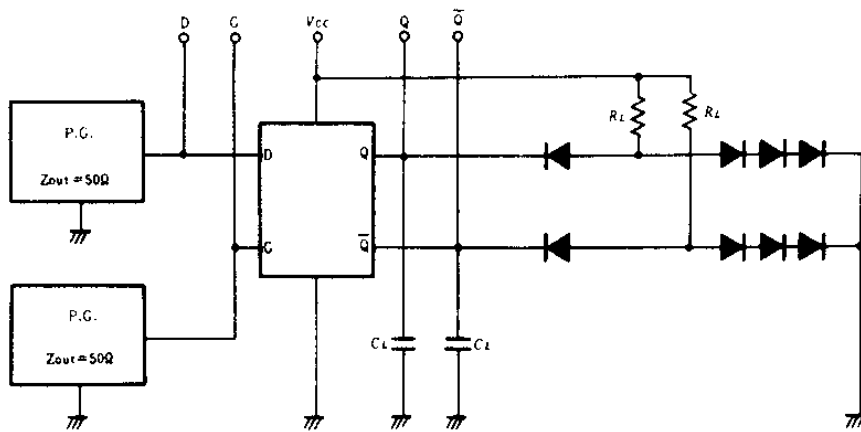
HD74LS75

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	D	Q	$C_L = 15pF$, $R_L = 2k\Omega$	—	15	27	ns
	t_{PHL}				—	9	17	
	t_{PLH}	D	\bar{Q}		—	12	20	ns
	t_{PHL}				—	7	15	
	t_{PLH}	G	Q		—	15	27	ns
	t_{PHL}				—	14	25	
	t_{PLH}	G	\bar{Q}		—	16	30	ns
	t_{PHL}				—	7	15	

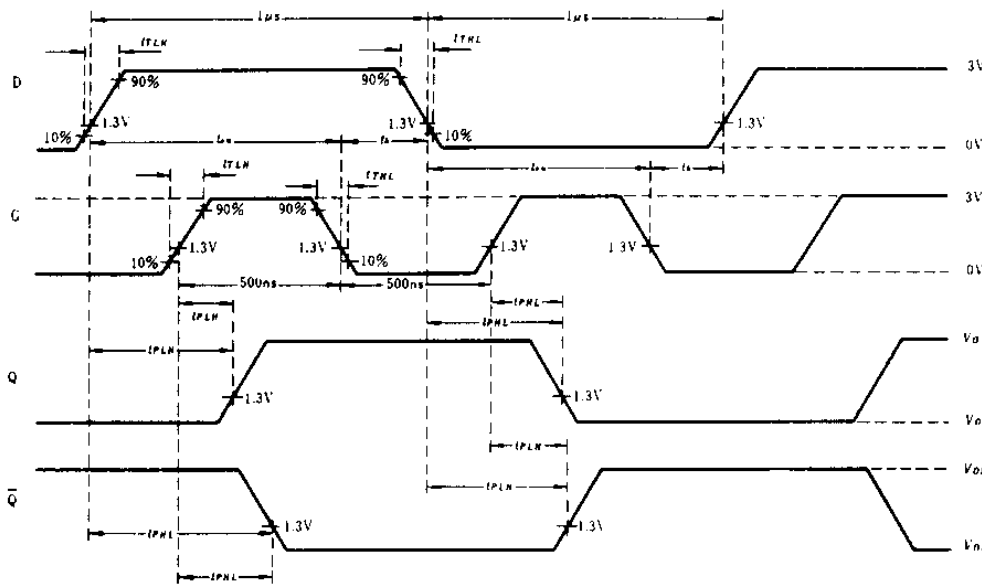
TESTING METHOD

1) Test Circuit



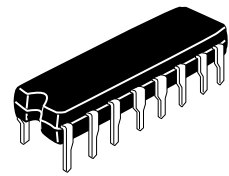
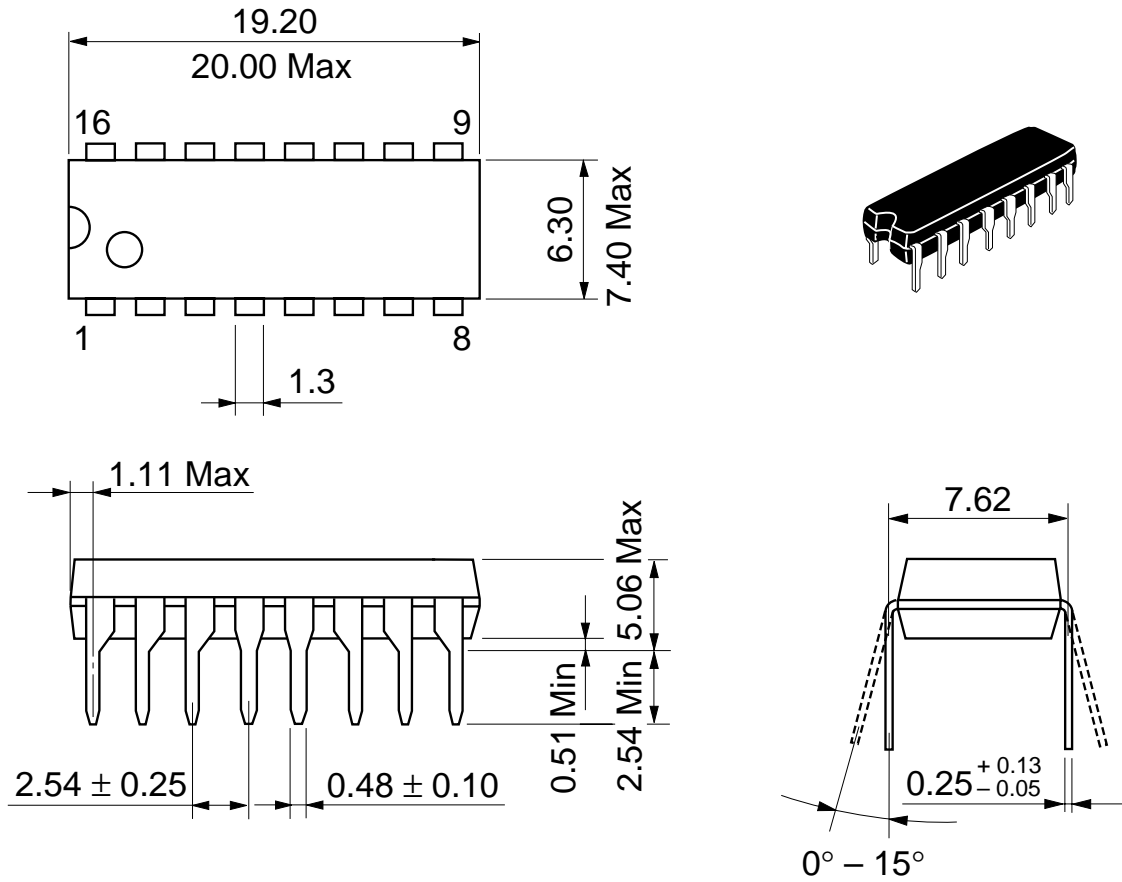
- Notes) 1. Test is put into the each latch
 2. All diodes are 1S2074 \oplus .
 3. C_L includes probe and jig capacitance.

Waveform



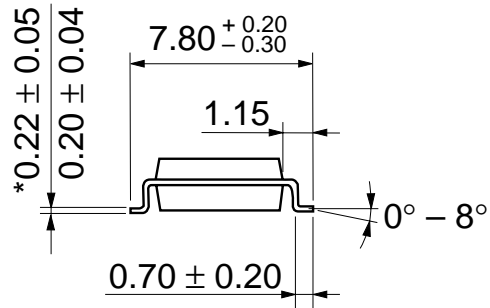
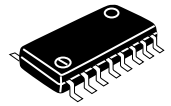
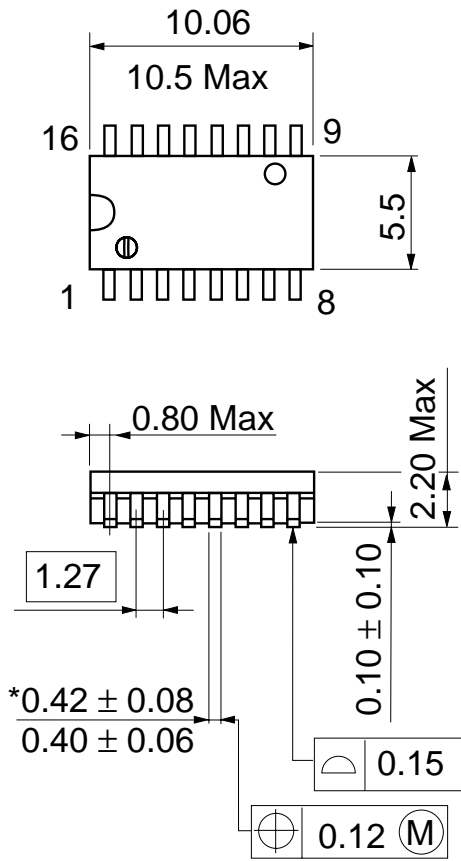
- Notes) 1. Input pulse; D input; $PRR=500kHz$, G input; $PRR=1MHz$, $t_{THL} \leq 10ns$, $t_{TLH} \leq 10ns$.
 2. When measuring propagation delay times from the D input, the corresponding G input must be held high.

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

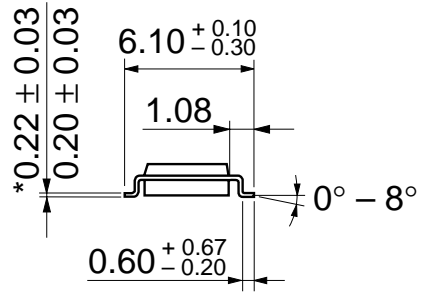
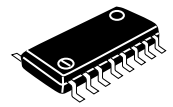
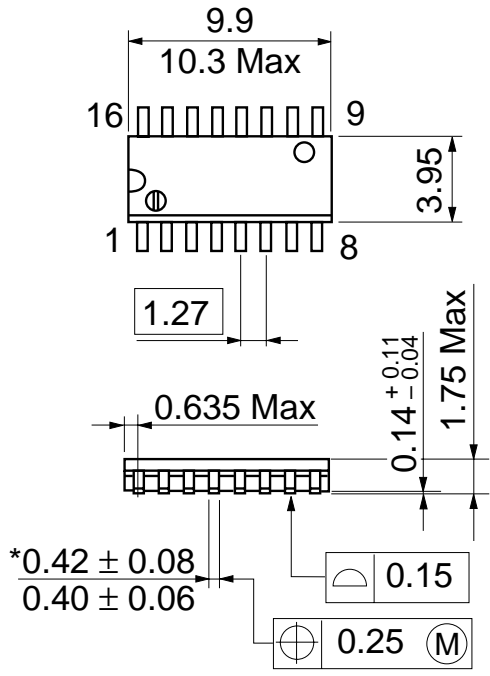
Unit: mm



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher StraÙe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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