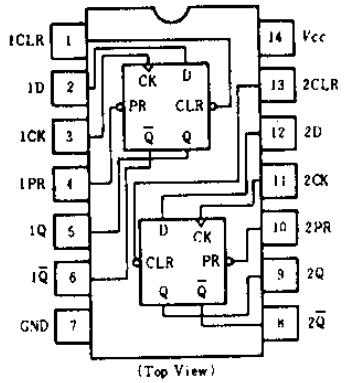
HD74LS74A ●Dual D-type Positive Edge-triggered Flip-Flops (with Preset and Clear)

■FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	Q_0	$\overline{Q}_0$

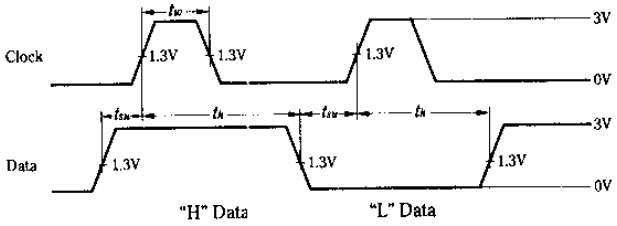
Notes) H; high level, L; low level, X; irrelevant
↑; transition from low to high level
Q_0; level of Q before the indicated steady-state conditions were established.
$\overline{Q}_0$; complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.
*; This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■PIN ARRANGEMENT



(Top View)

■TIMING DEFINITION



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	←	25	MHz
Pulse width	Clock High	t_W	25	–	–	ns
	Clear Preset		25	–	–	
Setup time	"H" Data	t_{su}	20↑	–	–	ns
	"L" Data		20↑	–	–	
Hold time		t_h	5↑	–	–	ns

Note) ↑; The arrow indicates the rising edge.

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{IH}=2V$	$I_{OL}=8mA$	–	–	0.5	V
				$I_{OL}=4mA$	–	–	0.4	
Input current	D	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	Clear				–	–	40	
	Preset				–	–	40	
	Clock				–	–	20	
	D	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	Clear				–	–	−0.8	
	Preset				–	–	−0.8	
	Clock				–	–	−0.4	
	D	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	Clear				–	–	0.2	
	Preset				–	–	0.2	
	Clock				–	–	0.1	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current		I_{CC}**	$V_{CC}=5.25V$		–	4	8	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$
** With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

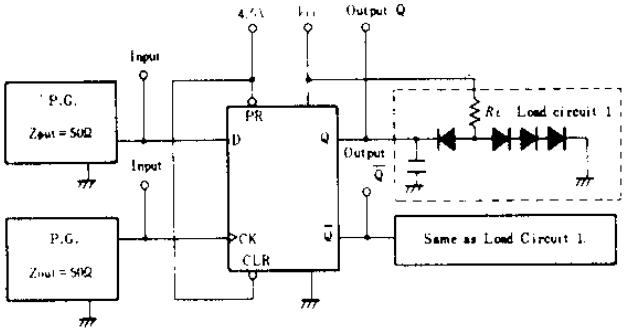
■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

Item	Symbol	Inputs	Outputs	Test Condition	min	typ	max	Unit
Maximum clock frequency	f_{max}			C_L=15pF, R_L=2kΩ	25	33	–	MHz
Propagation delay time	t_{PLH}	Clock, Clear or Preset	Q, $\bar{Q}$		–	13	25	ns
	t_{PHL}				–	25	40	ns

■TESTING METHOD

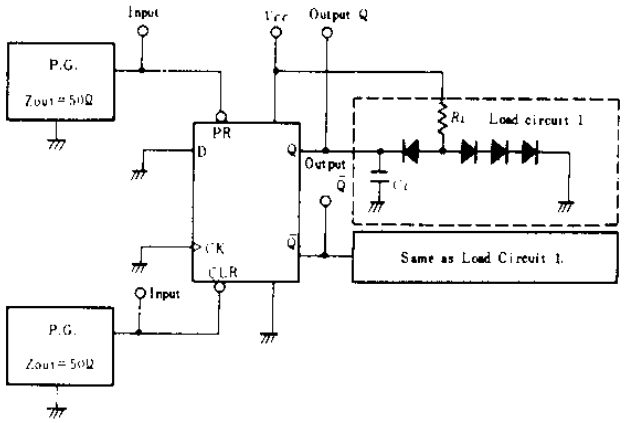
1) Test Circuit

1.1) f_{max}, t_{PLH}, t_{PHL} (Clock→Q,$\bar{Q}$)



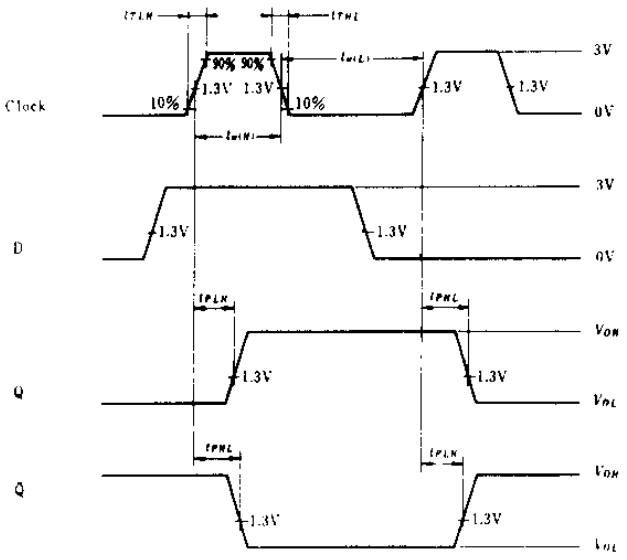
Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

1.2) t_{PHL}, t_{PLH} (Clear or Preset→Q,$\bar{Q}$)



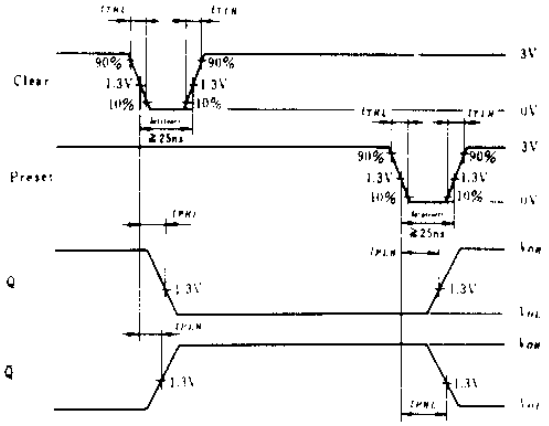
Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

Waveform



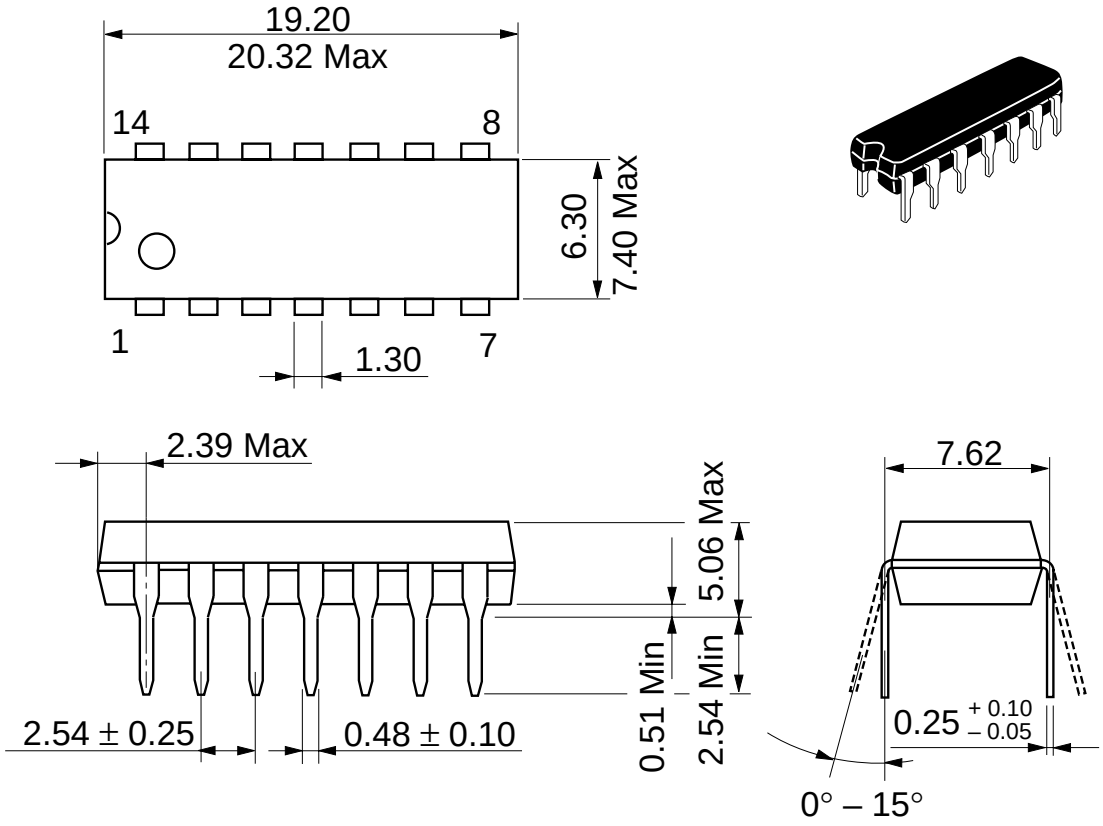
Note) Clock input pulse; t_{TLH}≦15ns, t_{THL}≦6ns, PRR=1MHz, duty cycle=50% and: for f_{max}, t_{TLH}=t_{THL}≦2.5ns.

Waveform



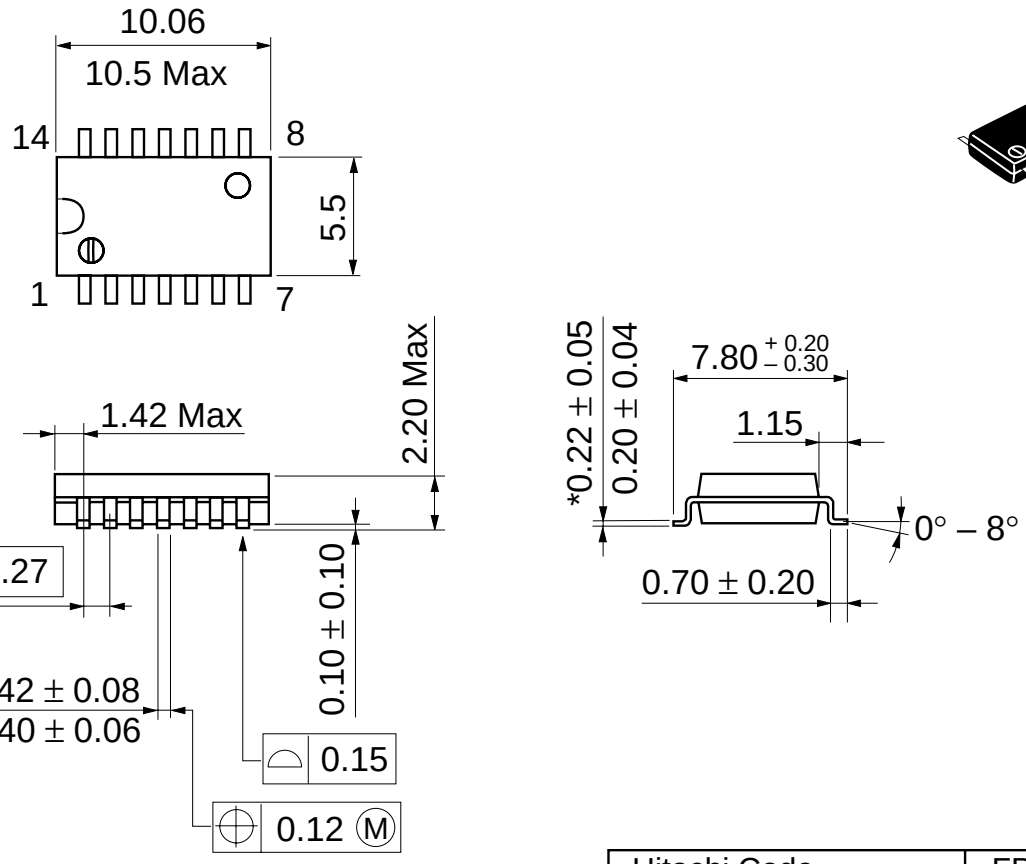
Note) Clear and preset input pulse; t_{TLH}≦15ns, t_{THL}≦6ns, PRR=1MHz

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

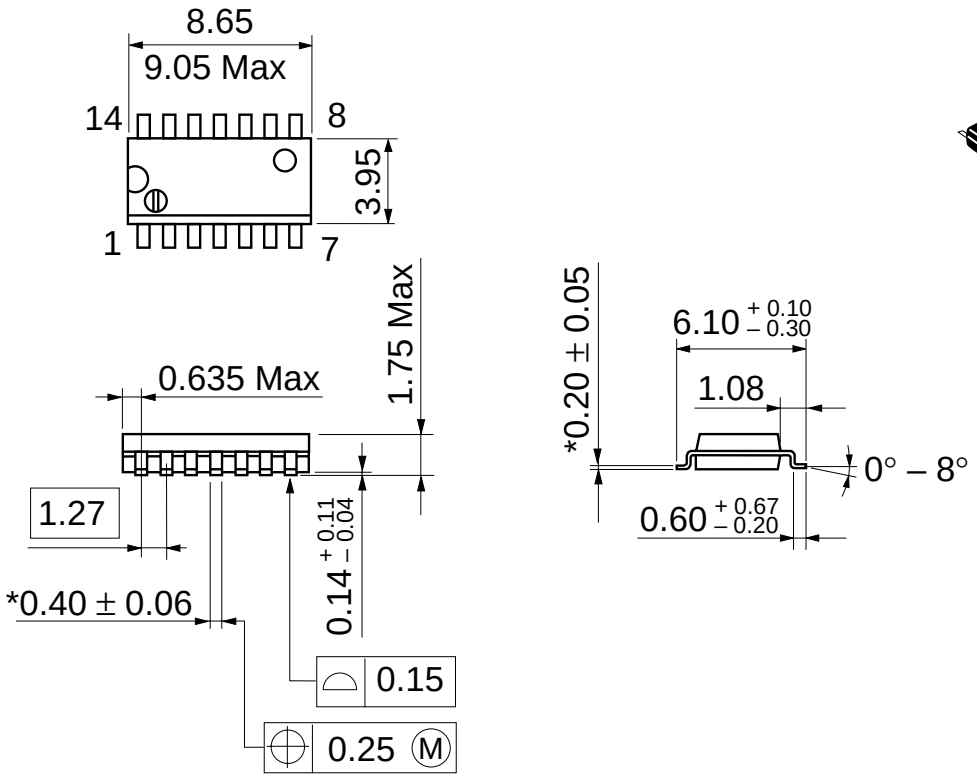
Unit: mm

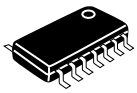


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

Unit: mm





*Pd plating

Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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