# **R&E** INTERNATIONAL, INC.

## **FEATURES**

- ♦ 3-State Output with Disable Control
- ♦ Separate Inhibit Input
- ♦ Selects One of Eight Data Sources
- Performs Parallel-To-Serial Conversion

## DESCRIPTION

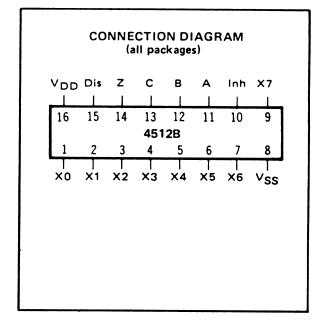
The 4512B is an 8-Channel Data Selector with Function Inhibit and Output Disable controls. One of eight binary inputs is selected by Select inputs A, B, and C, and is routed to the output Z. A high on the Disable input causes the Z output to assume a high-impedance state, regardless of other input conditions. This allows the output to interface directly with bus-oriented systems. When the Inhibit input is high, it forces the output low, providing the Disable input is low. By manipulation of the inputs, the 4512B can provide any logic functions of four variables (see Applications Information).

TRUTH TABLE

С	В	Α	INHIBIT	DISABLE	Z
0	0	0	0	٥	×o
0	0	1 .	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	хз
1	0	0	0	0	X4
1	0	1	0	0	×5
1	1	0	0	0	×6
1	1	1	0	0	X7
•	•	•	1	0	0
•	•	•	•	1	High Impedance

# = Don't Care

# **CMOS 8-CHANNEL DATA SELECTOR**

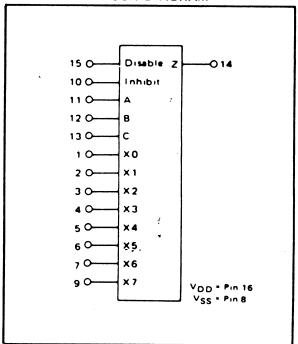


## **RECOMMENDED OPERATING CONDITIONS**

## For maximum reliability:

DC Supply Voltage  $V_{DD}$  -  $V_{SS}$  3 to 15 Vdc Operating Temperature  $T_A$  C -55 to +125 °C E -40 to +85 °C

## **BLOCK DIAGRAM**



## **ELECTRICAL CHARACTERISTICS**

## STATIC CHARACTERISTICS'

PARAMETER		(Vdc) CONDITIONS	CONDITIONS	T <sub>LOW</sub> <sup>2</sup>		+25°C		THIGH <sup>2</sup>		Units	
			Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Onits	
QUIESCENT DEVICE CURRENT	اموا										
	"	5	VIN = VSS or VDD	_	5	_	0.05	5	_	150	μAdc
		10	All valid input	-	10	-	0.1	10	_	300	
		15	combinations	_	20	_	0.2	20	_	600	
3-STATE OUTPUT LEAKAGE	卢니										
CURRENT		15		_	±0.1	-	± 10 <sup>-4</sup>	±0.1	-	±1.0	μAdc

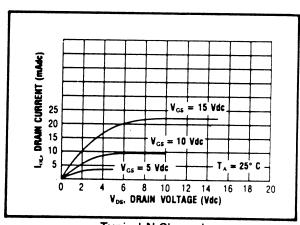
NOTES: 1 Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

TLOW = -55°C for C
= -40°C for E

THIGH = +125°C for C
= + 85°C for E

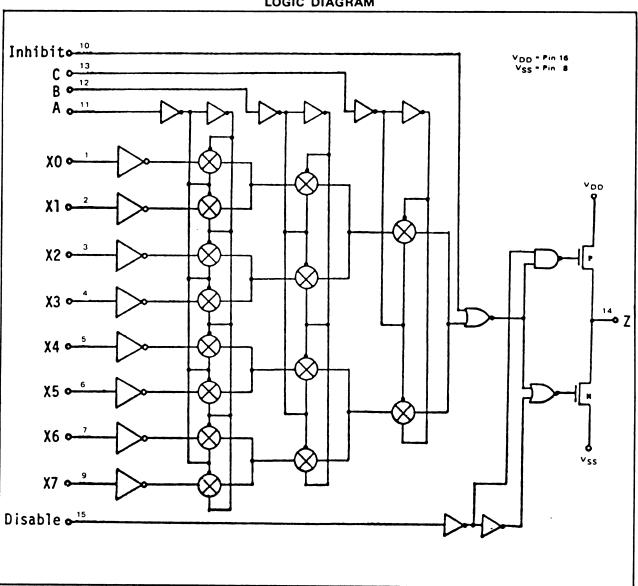
## DYNAMIC CHARACTERISTICS (C<sub>L</sub> = 50pF, T<sub>A</sub> = 25°C)

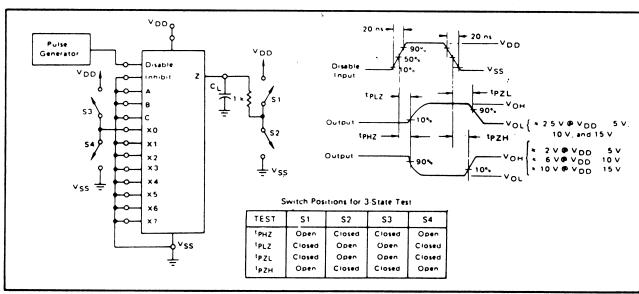
PARAMETER	V <sub>DD</sub> (Vdc)	Min.	Тур.	Max.	Units	
PROPAGATION DELAY TIME From Inhibit						
	<sup>t</sup> PLH, <sup>t</sup> PHL	5	_	120	240	ns
	l i	10	_	55	110	113
		15	_	40	80	
From Select Input	tout tout					
•	<sup>t</sup> PLH, <sup>t</sup> PHL	5	_	225	450	ns
		10	_	100	200	115
		15	-	75	150	
From Data Input	tnu tnu					
·	<sup>t</sup> PLH, <sup>t</sup> PHL	5	_	200	400	
		10	_	80	160	ns
		15	-	60	120	
From Disable	tpHZ, tpZH					
	terz, tezh					
	1,55,1,55	5		60	120	ns
		10	_	30	60	
		15	-	25	50	
OUTPUT TRANSITION TIME	t <sub>TLH</sub> , t <sub>THL</sub>					
		5	_	100	200	ns
		10	_	50	100	
		15	_	40	80	



Typical N-Channel Sink Current Characteristics

## LOGIC DIAGRAM





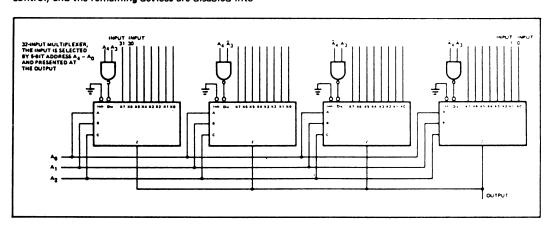
3-State AC Test Circuit and Waveform

## **APPLICATIONS INFORMATION**

### 32-INPUT MULTIPLEXER

Output terminals of several 4512B devices can be connected to a single data bus. One 4512B is selected by the 3-state Disable control, and the remaining devices are disabled into

a high-impedance state, A 32-input multiplexer utilizing four 4512B data selectors and a single 4011B is shown.



### LOGIC FUNCTION GENERATORS

In addition to the standard application of multiplexers in data conversion techniques, these circuits can also be used in generating logic functions, which in many cases can reduce system package count.

A multiplexer is a multiple-position single-pole switch. One set of inputs selects the position of the switch. The second set of inputs collects the input data, which is transferred through the circuit to one output. By using the binary select inputs and the data inputs, the 4512B can generate any of the 65,536 different functions of four variables.

Assume the four binary inputs are A, B, C, and D, and that Z is the desired function. Using the

INPUT VARIABLES				REQUIRED FUNCTION
A	В	С	D	z
L	L	L	L	н
L	L	L	н	L
L	L	н	L	н
L	L	н	н	Н
L	н	L	L	L.
L	н	L	н	Н
L	н	н	L	L
L	н	н	н	L
н	L	L	L	
	•			
		<u>`</u>		i .
		_	_	
			H = HIG L = LOW	

select inputs as the first three variables, any combination of A, B, and C will select a data input (assuming the output is enabled). For each combination of A, B, and C, the required output, as a function of the fourth variable D, can be HIGH or LOW or the same as D or the inverse of D. Therefore, the truth table may be examined and each data input of the 4512B is connected to  $V_{DD}$ ,  $V_{SS}$ , D, or  $\overline{D}$  as required. In such fashion, the function is generated.

In the example shown, the first two outputs are the inverse of D, so XO is connected to  $\overline{D}$ . The next two are HIGH, so X1 is connected to  $V_{\overline{DD}}$ , etc.

