# SIEMENS

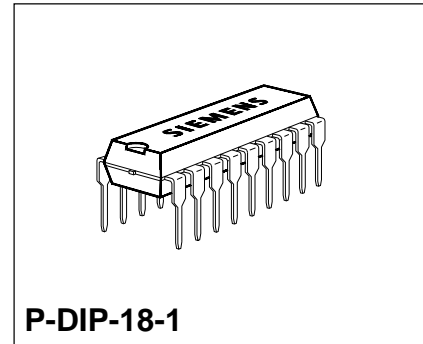## Quad Driver Incl. Short-Circuit Signaling          FZL 4145 D

**Bipolar IC**

### Features

● Short-circuit shutdown with clock generator
● Four driver circuits for controlling
  power transistors
● Overload and short-circuit signaling

**P-DIP-18-1**

| Type | Ordering Code | Package |
|------|---------------|---------|
| FZL 4145 D | Q67000-H8437 | P-DIP-18-1 |

### General Description

The IC comprises four driver circuits capable of driving power transistors for high output currents. The output transistors are protected against short-circuit to ground and supply voltage. The input threshold can be adjusted between 1.5 V and 7 V. Overload or short-circuit failure at an output will be indicated at pin SQ (signaling output).
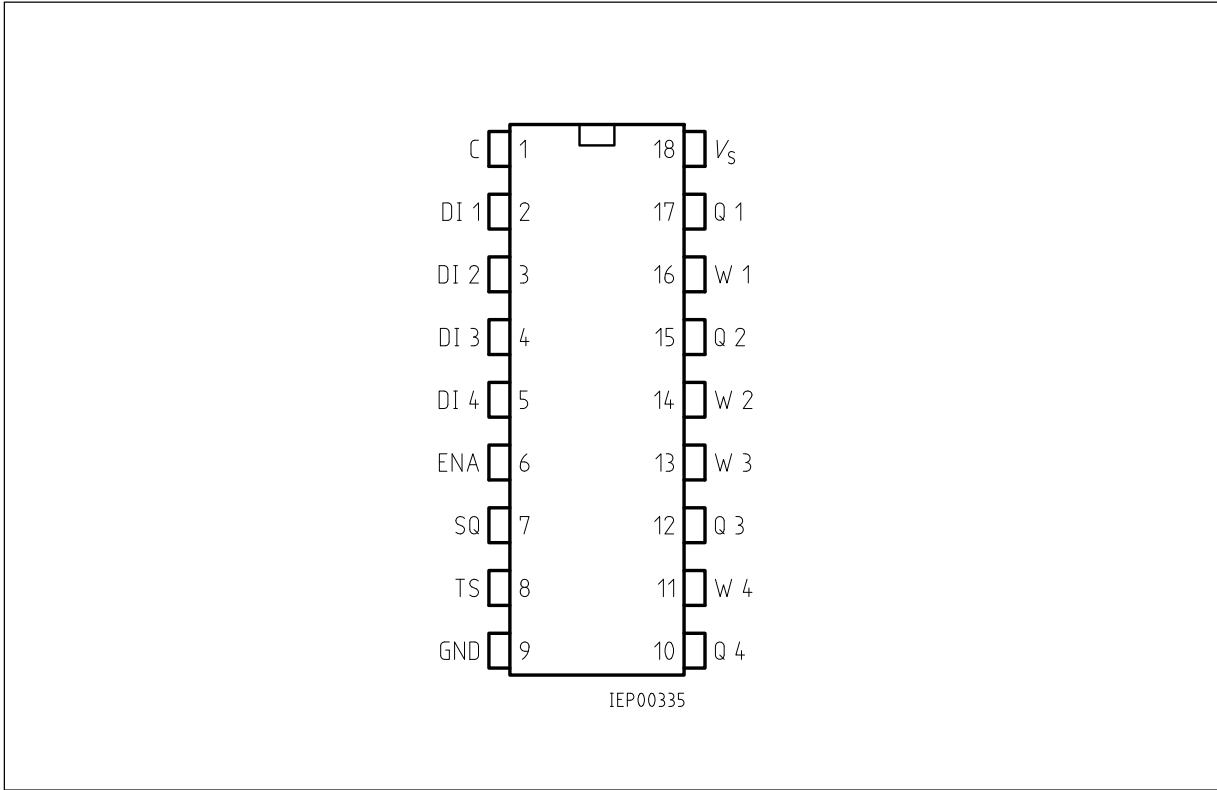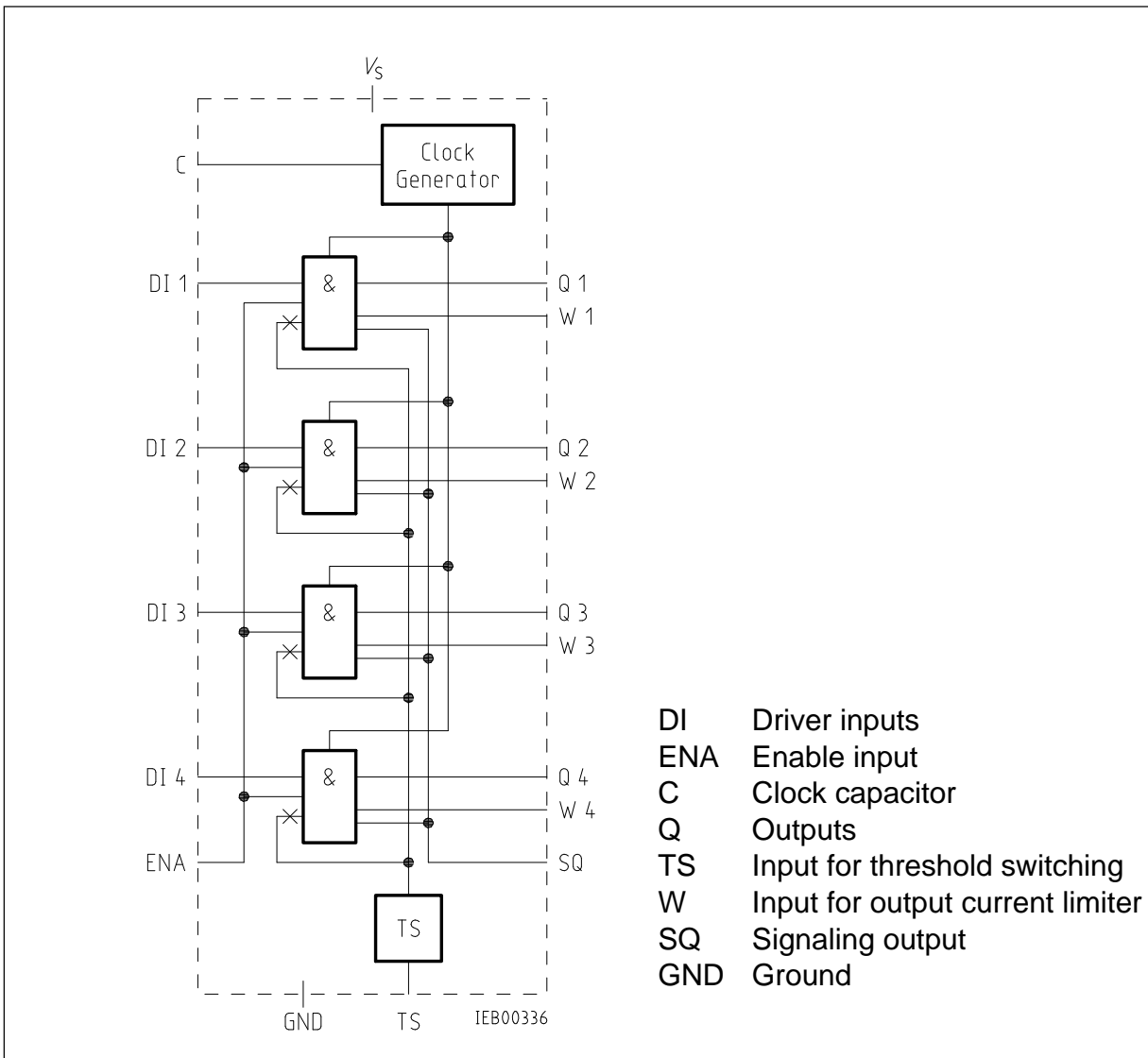
### Functional Description

Each driver circuit has one active high driver input DI and a common enable input (ENA) (active high) is provided for all stages. The (Q) outputs are designed to drive the output transistors. The load current is sampled via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-on again is provided by the built-in clock generator. Its operation requires an external capacitor $C_T$ at pin C. If $C_T$ is bridged by a break-key, switching on can only be carried out by operating a key. The duty cycle of the clock generator is 1:50 (e.g. 40 µs/2 ms with $C_T$ = 33 nF).

In case of overcurrent or short-circuit failure at any output stage the signaling output (SQ) will go low. In clock-governed operation (i.e. when there is automatic switching on by the clock and not by a key), SQ goes high and low at the clock rate as long as a short-circuit or overload exists. SQ is an open-collector output.

Unused W pins must be connected to $V_s$. Open W pins would simulate a short-circuit and activate the signaling output.

## Pin Configuration
(top view)



```
        C   1         18   Vs
      DI 1  2         17   Q 1
      DI 2  3         16   W 1
      DI 3  4         15   Q 2
      DI 4  5         14   W 2
       ENA  6         13   W 3
        SQ  7         12   Q 3
        TS  8         11   W 4
       GND  9         10   Q 4
                IEP00335
```

**Block Diagram**

The switching threshold at inputs DI and ENA can be adjusted between 1.5 V and 7 V via connection TS:

| | |
|---|---|
| $V_{TS}$ = 0 V; | input threshold = 1.5 V (for 5 V logic) |
| $V_{TS}$ = 0 to 5 V; | input threshold = $V_{TS}$ + 1.5 V |
| $V_{TS}$ = $V_S$: | input threshold = 7 V (for 12/15 V and 24/28 V logic) |

If the output is disabled due to the logic states of inputs DI or ENA this disable is effective over the total supply voltage range between $V_S$ = 0 V and $V_S$ = 35 V.

The inputs are protected with clamp diodes.

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## Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | **min.** | **max.** | | |
| Supply voltage | $V_S$ | – 0.3 | 35 | V | |
| | $V_S$ | – 0.3 | 45 | V | 100 ms duration, 1 s interval |
| Input voltage at DI and ENA | $V_{DI, ENA}$ | – 0.3 | 35 | V | [1] |
| Voltage at TS and SQ | $V_{TS, SQ}$ | – 0.3 | 45 | V | |
| Output voltage $V_Q$ and voltage at C | $V_Q, V_C$ | – 0.3 | $V_S$ | V | |
| Voltage at W | $V_W$ | $V_S – 5$ | $V_S$ | V | [3] |
| Input current at DI and ENA | $I_{DI, ENA}$ | – 3 | 1 | mA | [2] |
| | $I_{DI, ENA}$ | – 6 | 2 | mA | [2] 100 ms duration, 1 s interval |
| | $I_{DI, ENA}$ | – 6 | 5 | mA | [2] 100 µs duration, 1 ms interval |
| Output current at SQ | $I_{SQ}$ | | 8 | mA | |
| Power dissipation of all input diodes | $P_{tot}$ | | 50 | mW | |
| Storage temperature | $T_{stg}$ | – 65 | 125 | °C | |
| Thermal resistance system - air | $R_{th\,SA}$ | | 65 | K/W | |
| system - case | $R_{th\,SC}$ | | 45 | K/W | |

## Operating Range

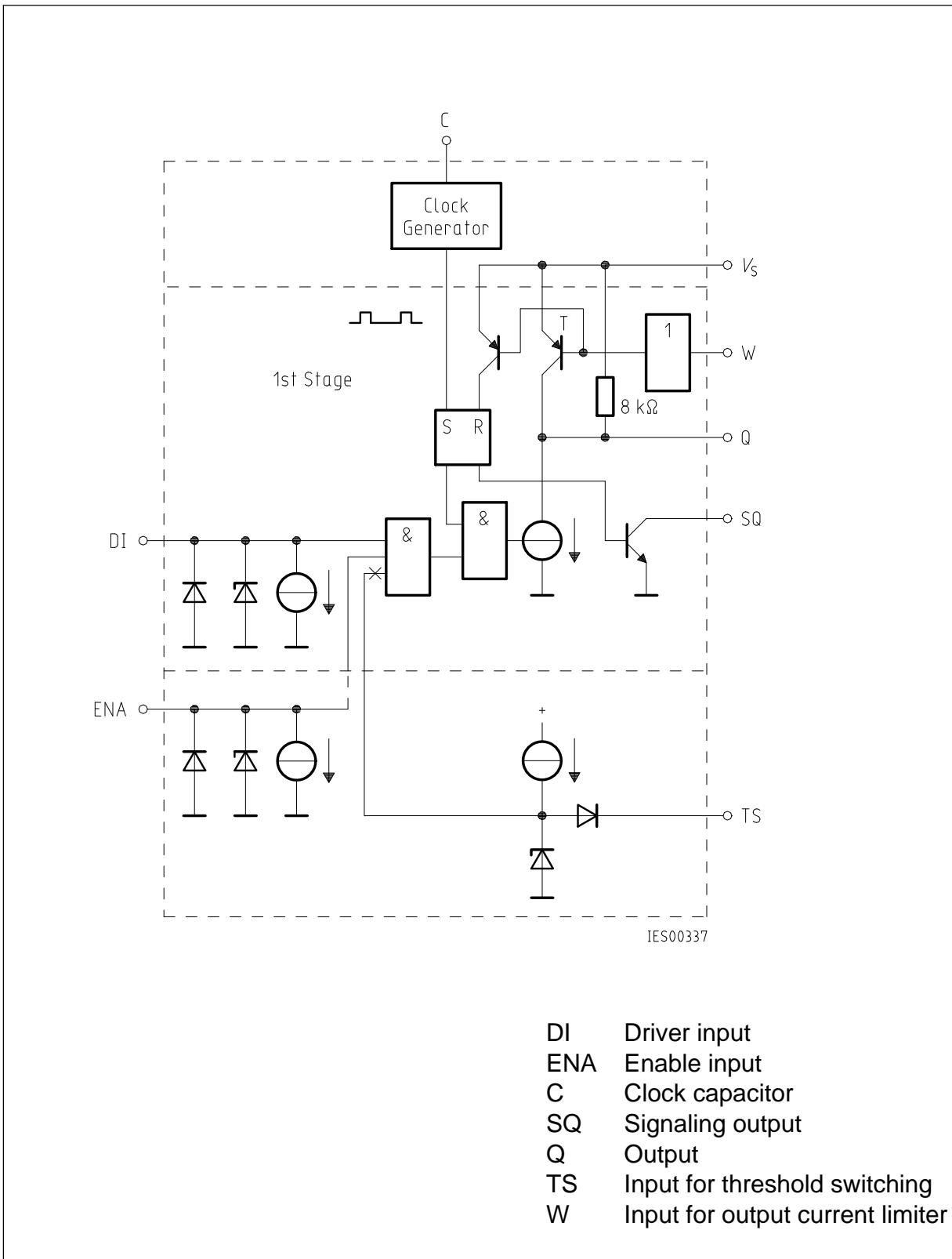| Parameter | Symbol | | | Unit | Remarks |
|---|---|---|---|---|---|
| Supply voltage for input threshold | | | | | |
| 1.5 V | $V_S$ | 4.5 | 35 | V | $V_{TS} = 0$ V |
| 1.5 V to 6.5 V | $V_S$ | $V_{TS} + 4.5$ | 35 | V | $V_{TS} = 0$ V to 5 V |
| 7 V | $V_S$ | 10 | 35 | V | $V_{TS} = V_S$ |
| Ambient temperature | $T_A$ | – 25 | 85 | °C | |

**Notes:** [1] $V_{DI, ENA} > 35$ V requires a protective resistor before DI, ENA.
[2] $V_{DI, ENA}$ may increase to more than 35 V during current nodes.
[3] Unused W connections must be connected to $V_S$.

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## Characteristics

Supply voltage $4.5\ \text{V} \le V_S \le 30\ \text{V}$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Supply current | $I_S$ | | 6 | 8.5 | mA | $V_{ENA} = 0\ \text{V}$, $V_W = V_S$ |
| H-input voltage at DI, ENA | $V_{IH}$ | 2 | | | V | $V_{TS} = 0\ \text{V}$ |
| H-input voltage at DI, ENA | $V_{IH}$ | 8 | | | V | $V_{TS} = V_S$ |
| L-input voltage at DI, ENA | $V_{IL}$ | | | 0.7 | V | $V_{TS} = 0\ \text{V}$ |
| L-input voltage at DI, ENA | $V_{IL}$ | | | 6 | V | $V_{TS} = V_S$ |
| Input current at DI, ENA | $I_{DI,\ ENA}$ | 50 | | 200 | µA | $0.5\ \text{V} \le V_{DI,\ ENA} \le 30\ \text{V}$ |
| L-output voltage at SQ | $V_{SQ\ L}$ | | | 0.5 | V | $I_{SQ} = 5\ \text{mA}$ |
| Output current available[1] | $I_Q$ | 1.5 | 2.5 | | mA | $V_Q = V_S - 1.5\ \text{V}$ |
| | $I_Q$ | 1.7 | | | mA | $T_A = 0\ °\text{C}$ $V_Q = V_S - 1.5\ \text{V}$ |
| Current from TS | $-I_{TS}$ | | 2 | 10 | µA | $V_{TS} = 0\ \text{V}$ |
| Switching threshold at W | $V_W$ | $V_S - 0.6$ | $V_S - 0.5$ | $V_S - 0.4$ | V | |
| Current in W | $I_W$ | | | 100 | µA | |
| Current from C | $-I_C$ | 12 | 20 | 34 | µA | $T_A = 20\ °\text{C}$ |
| Current in C | $I_C$ | 0.6 | 1 | 1.7 | mA | $T_A = 20\ °\text{C}$ |
| Upper switching threshold at C | $V_{CU}$ | 1.6 | 2.1 | 1.7 | V | $T_A = 20\ °\text{C}$ |
| Lower switching threshold at C | $V_{CL}$ | 0.6 | 0.9 | 1.2 | V | $T_A = 20\ °\text{C}$ |
| Saturation voltage at T[2] | $V_{Q\ R}$ | | $V_S - 0.3$ | | V | $V_W = V_S - 2\ \text{V}$, $I_Q = 0$ |
| H-output voltage | $V_{Q\ H}$ | $V_S - 0.25$ | $V_S - 0.02$ | | V | $V_{ENA} = 0\ \text{V}$ |

[1] The actual output current is typically 0.5 mA higher, a value which is required as current for the short-circuit protection. However, only the value specified above is available to drive the external output transistors.
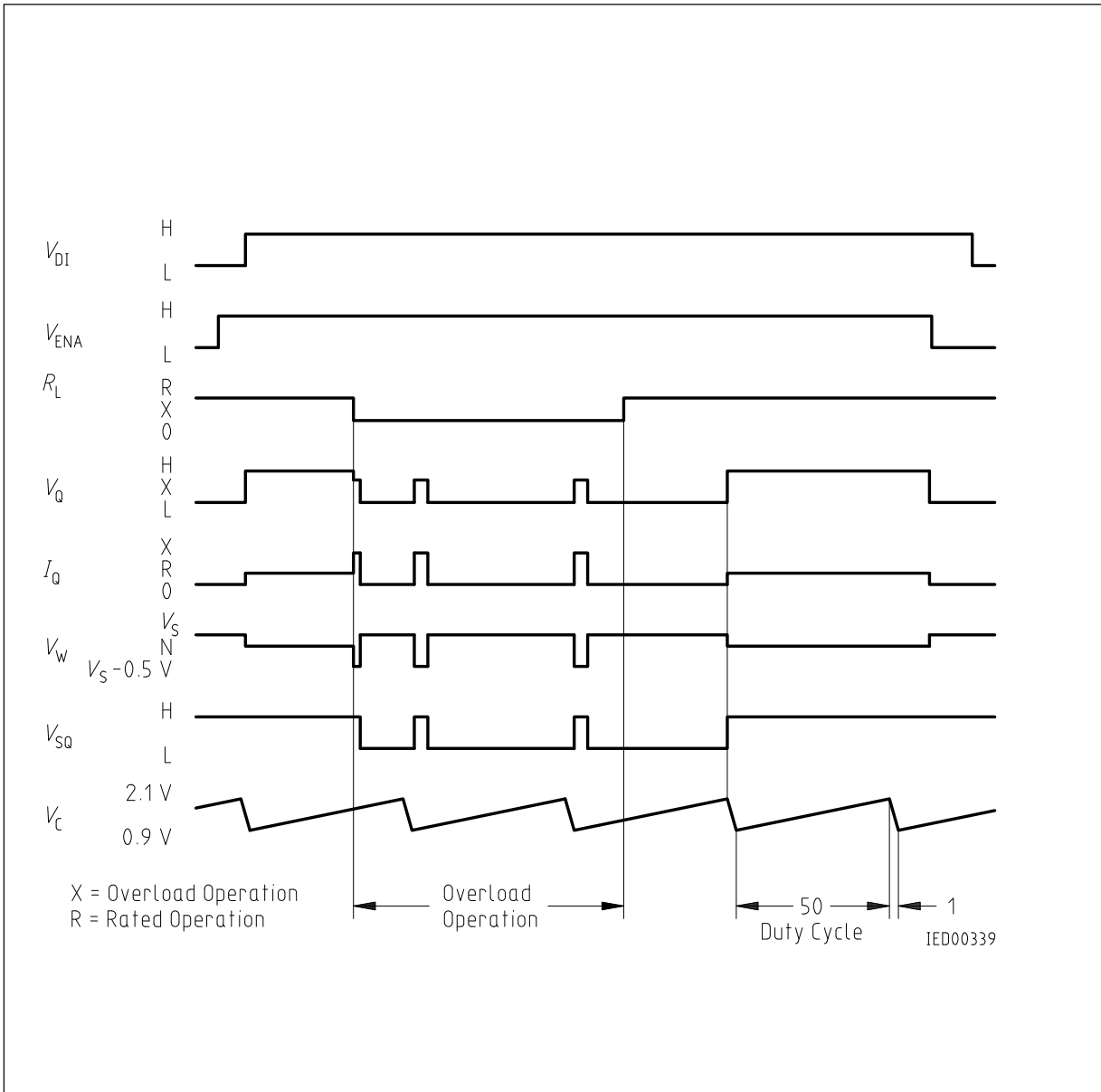
[2] See block diagram

IES00337

| | |
|---|---|
| DI | Driver input |
| ENA | Enable input |
| C | Clock capacitor |
| SQ | Signaling output |
| Q | Output |
| TS | Input for threshold switching |
| W | Input for output current limiter |

**Schematic Circuit Diagram of One Stage**
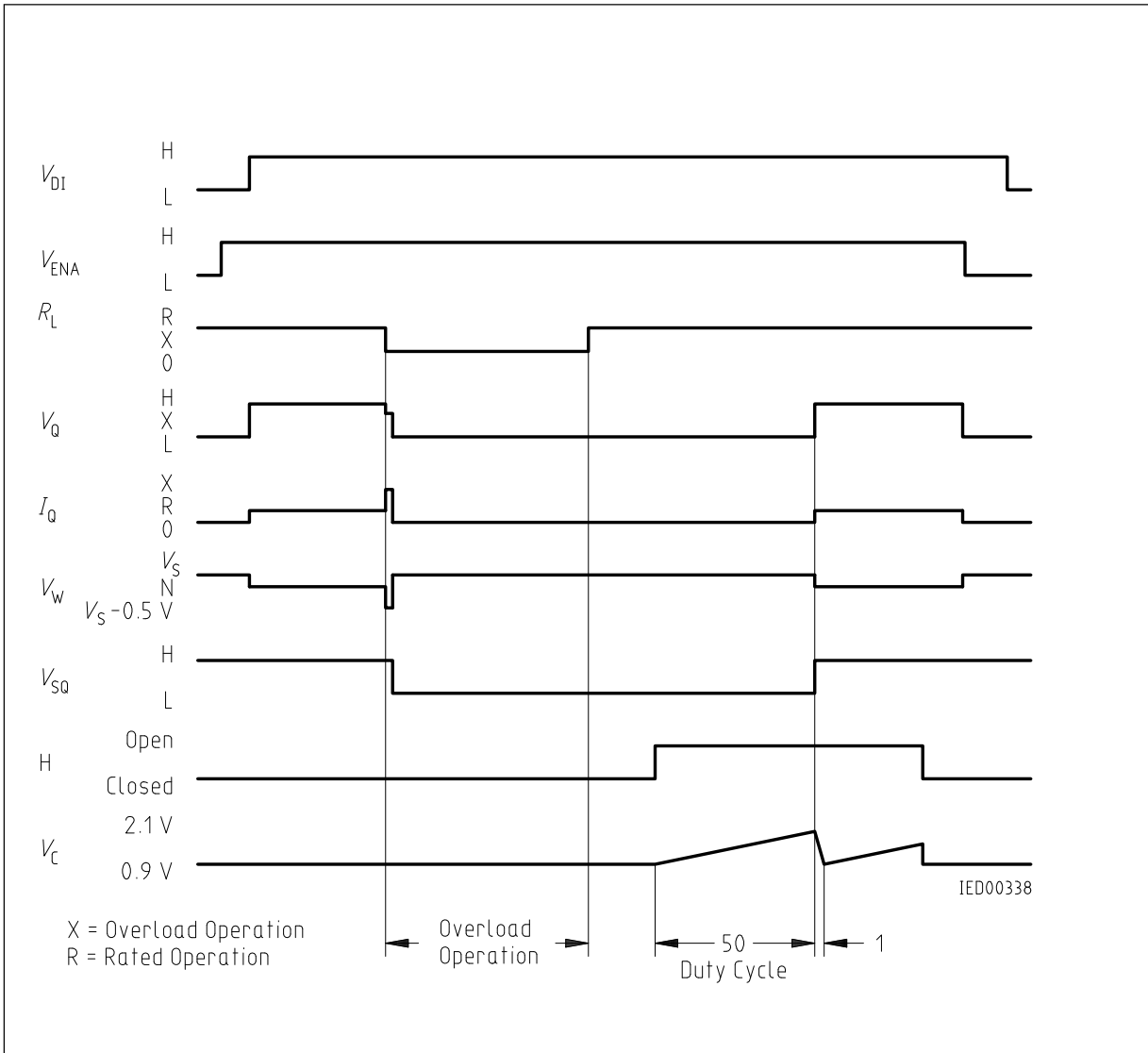
**Mode of Operation: Switching-ON again after Overload with Key H**

**Mode of Operation: Automatic Switching-ON again after Overload**

## Typical Application Circuits

The load conditions at Q depend on the permissible power dissipation of the used power transistors. The pulsed power dissipation in case of a short circuit must be observed.

In order to suppress oscillations of the power stage in case of a short circuit, a capacitor $C$ at Q1 to Q4 is necessary if e.g. fast switching transistors are used.

Typical value X of $C$: approx. 20 nF.

The output circuit 1 is suited for currents up to approx. $I_Q$ = 100 mA.

The output circuit 2 and 3 are suited for currents up to approx. $I_Q$ = 2 A. A minimum power dissipation can be achieved with circuit 3.

A break key in parallel to $C_T$ allows a manual switch-on in case of short-circuit.



IES00340
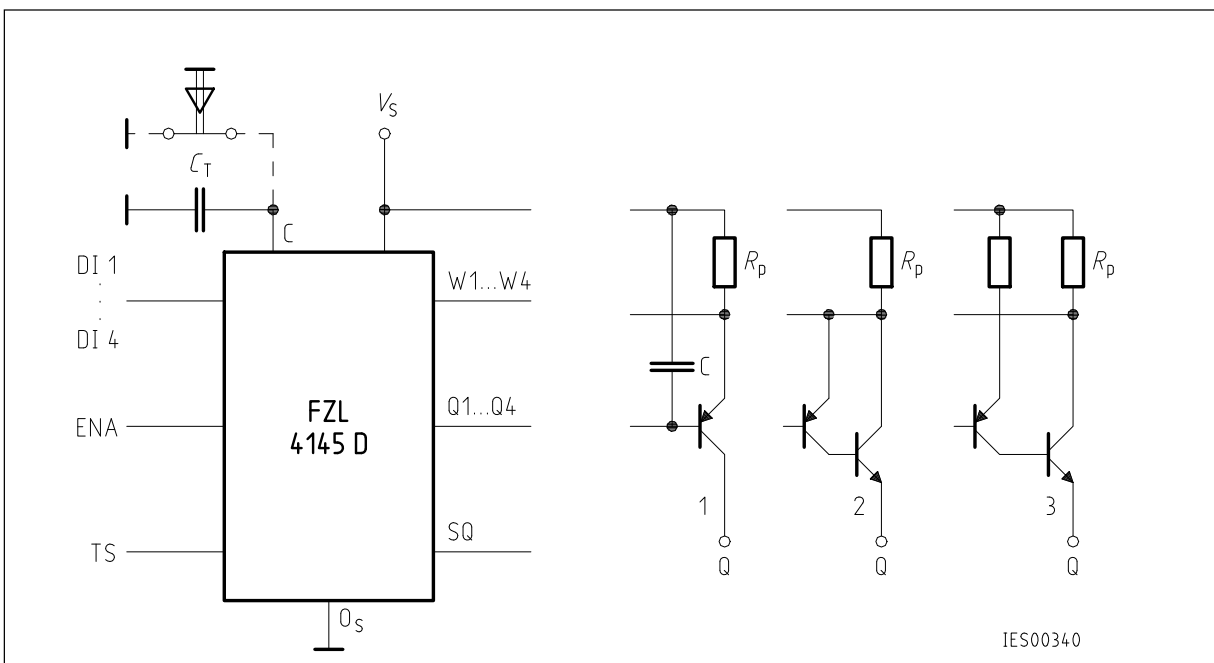
$R_P$ = Precision resistor (current measurement)
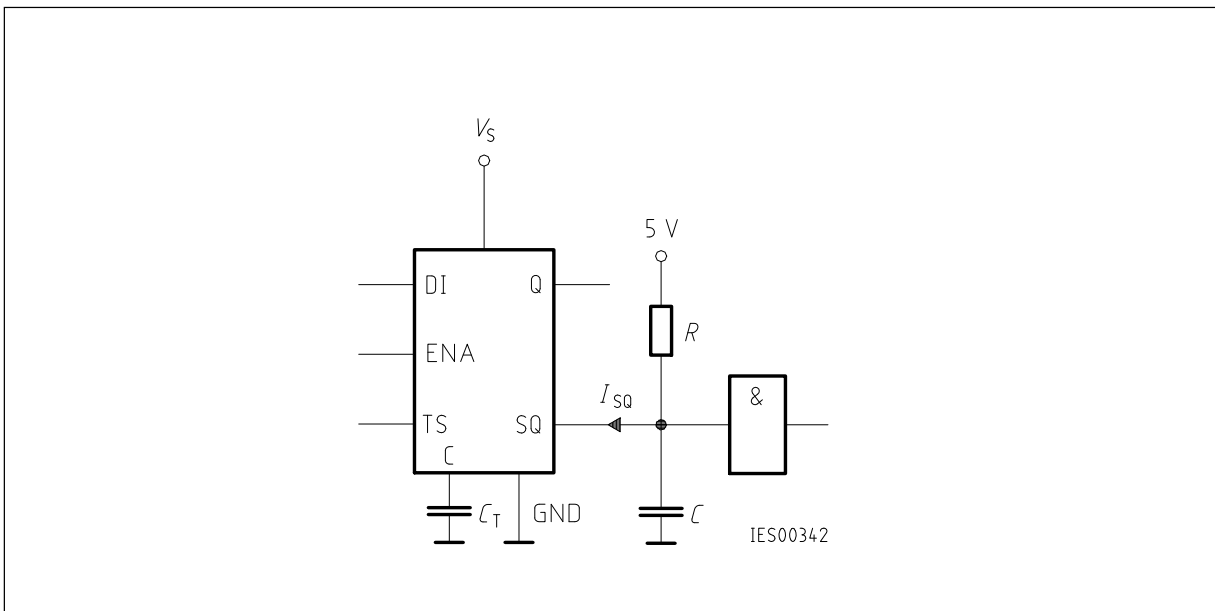$C_T$ = 0.8 x $t_p$ (nF, µs)
$t_p$ = Short-circuit current pulse length

**Note:** Circuit 1 does not permit a capacitor between Q1 and Q4 and the collector.
Circuit 2 does not permit a capacitor between Q1 and Q4 and base or emitter, respectively.
Otherwise too high current spikes would arise in case of a short circuit.

## Typical Application of Short-Circuit Signaling Output SQ
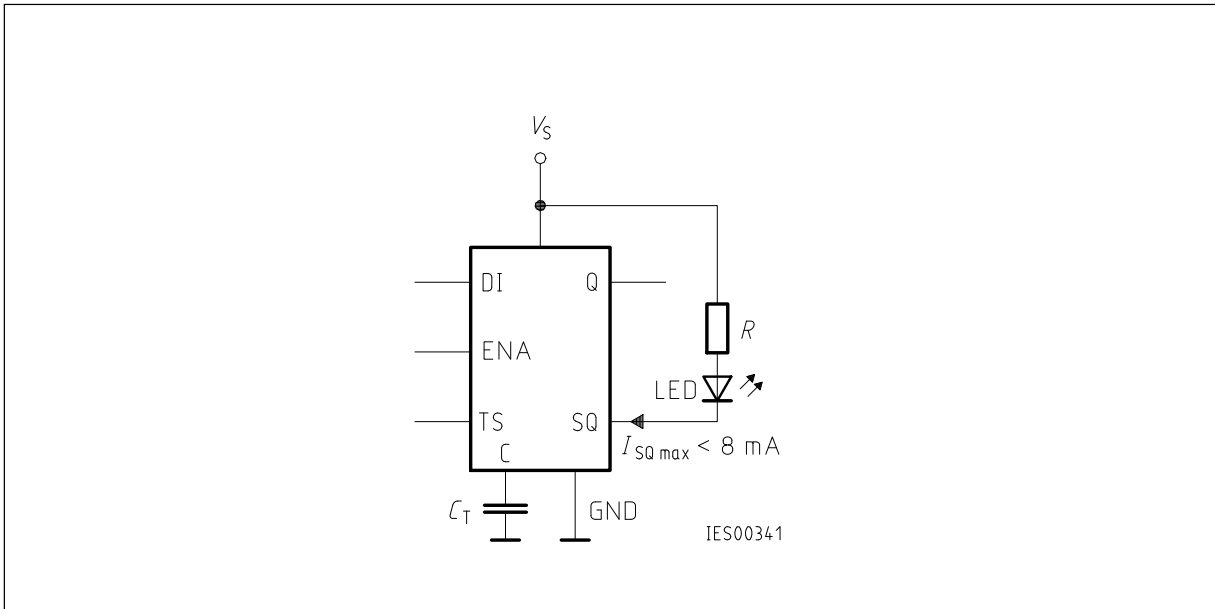


**1. LED Display**



## 2. TTL/CMOS/LSL Driving

If the pulses appearing at SQ during clocked operation disturb the remainder of the circuit, a lowpass filter will be necessary. For a load current of $I_{SQ} = 1$ mA a capacitor $C$ of approx. 10 nF is necessary to limit the output pulses of up to 10 µs (depending on $C_T$) to 1 V. Signaling occurs after approx. 50 µs.

Semiconductor Group                    10