To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

GENERAL DESCRIPTION

The M62320P/FP is a CMOS 8-bit I/O expander which has serial to parallel and parallel to serial data converting functions.

It can communicate with a microcontroller via few wiring thanks to the adoption of the two-line I^{2}C BUS.

Parallel data I/O terminal can be set to input or output mode alternatively in individual bits.

Maximum 8 ICs can be connected to a bus by using three chip-select pins, so that it is possible to handle up to 64 bits data.
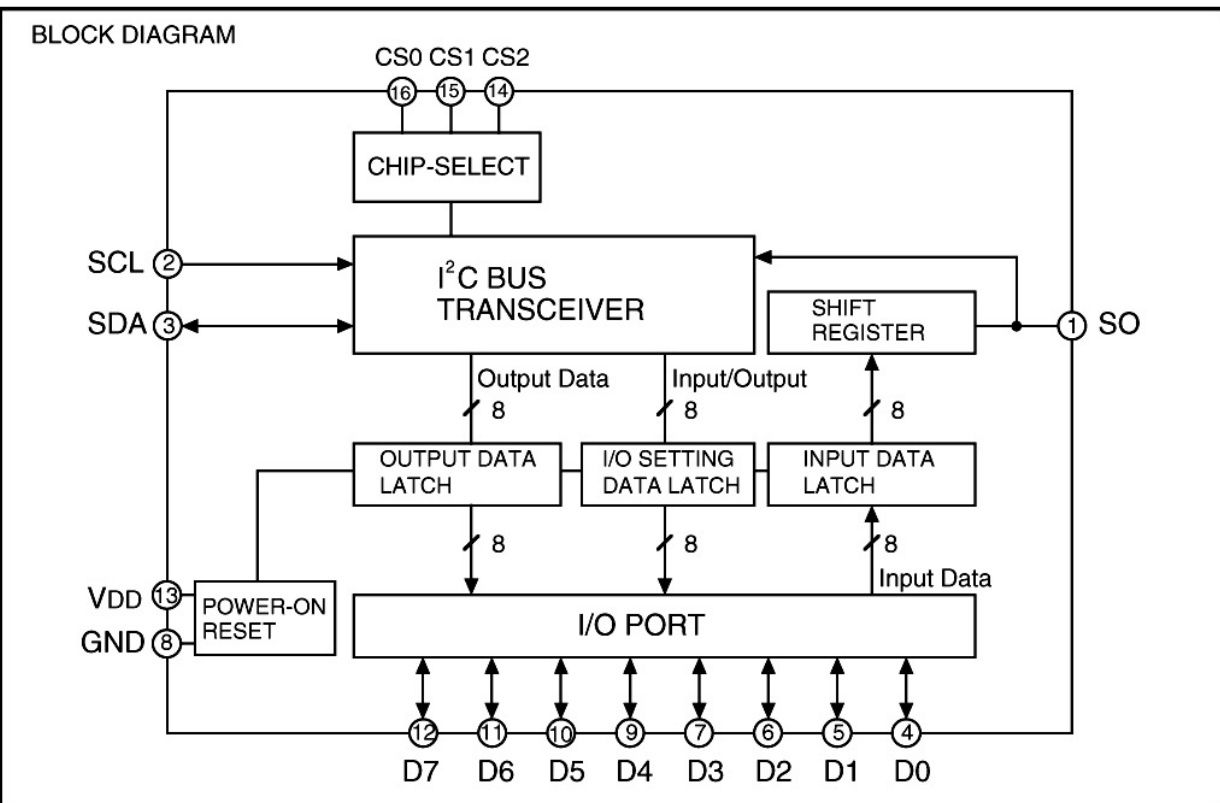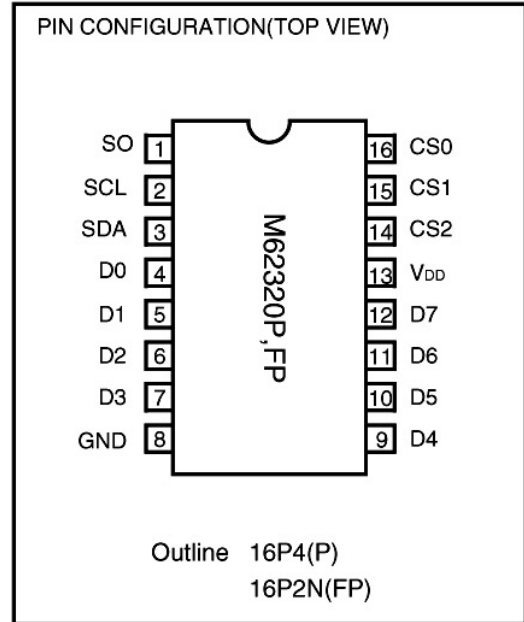
FEATURES

- Simple two-line (SCL and SDA) communication with a microcontroller.
- 8-bit data conversion between serial and parallel by I^{2}C BUS.
- Built-in power-on reset.

APPLICATION

I/O port expansion for a microcontroller.
Data conversion between serial and parallel in microcontroller peripherals.

PIN CONFIGURATION(TOP VIEW)

Pin	Signal		Pin	Signal
1	SO		16	CS0
2	SCL		15	CS1
3	SDA		14	CS2
4	D0		13	V$_{DD}$
5	D1		12	D7
6	D2		11	D6
7	D3		10	D5
8	GND		9	D4

M62320P,FP

Outline   16P4(P)
16P2N(FP)

BLOCK DIAGRAM

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PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
2	SCL	Input	Serial clock input
3	SDA	Input/Output	Serial data input/output
1	SO	Output	Serial data output
16	CS0	Input	Chip select data input
15	CS1		
14	CS2		
4	D0	Input/Output	Parallel data input/output
5	D1		
6	D2		
7	D3		
9	D4		
10	D5		
11	D6		
12	D7		
13	VDD	——	Power supply
8	GND	——	GND

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VDD	Supply voltage		−0.3 to 7.0	V
VI	Input voltage		−0.3 to VDD+0.3	V
VO	Output voltage		−0.3 to VDD+0.3	V
IOH	Output current "Low"	D0 to D7	- 5 to 0	mA
IOL	Output current "High"	D0 to D7	0 to 30	mA
Pd	Power dissipation	Ta = 25°C	1220(P) / 980(FP)	mW
Topr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

- Supply voltage………VDD=5V±10%
- Input high voltage……VIH=0.8VDD to VDD
- Input low voltage………VIL=0 to 0.2VDD

## ELECTRICAL CHARACTERISTICS (VDD=5V ±10%, GND=0V,Ta=20 to 85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
IDD	Circuit current	V_{IH} = VDD,V_{IL} = GND, f_{SCL} = 400kHZ		0.05	0.5	mA
		V_{IH} = VDD,V_{IL} = GND, f_{SCL} = stop		0.1	1.0	μA
IILK	Input leak current		-10		10	μA
VIH	Input high voltage		0.8VDD			V
VIL	Input low voltage				0.2VDD	V
VOH	Output high voltage	IOH = -1mA	VDD-0.4			V
VOL	Output low voltage	IOL = 5mA			0.4	V
IOL	Output current "Low"	VOL = 0.4V	5	10		mA
		VOL = 1.0V	15	25		mA

I²C BUS CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	KHz
t_{BUF}	Free time: the bus must be free before a new transmission can start	4.7	-	µs
$t_{HD:STA}$	Hold time START Condition. After this period,the first clock pulse is generated.	4.0	-	µs
t_{LOW}	LOW period of the clock	4.7	-	µs
t_{HIGH}	HIGh period of the clock	4.0	-	µs
$t_{SU:STA}$	Set-up time for START condition (Only relevant for a repeated START condition)	4.7	-	µs
$t_{HD:DAT}$	Data Hold time	0	-	µs
$t_{SU:DAT}$	Data Set-up time	250	-	ns
t_R	Rise time of SDA and SCL signals	-	1000	ns
t_F	Fall time of SDA and SCL signals	-	300	ns
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	µs

• Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max.300 ns) of the falling edge of SCL.

TIMING CHART
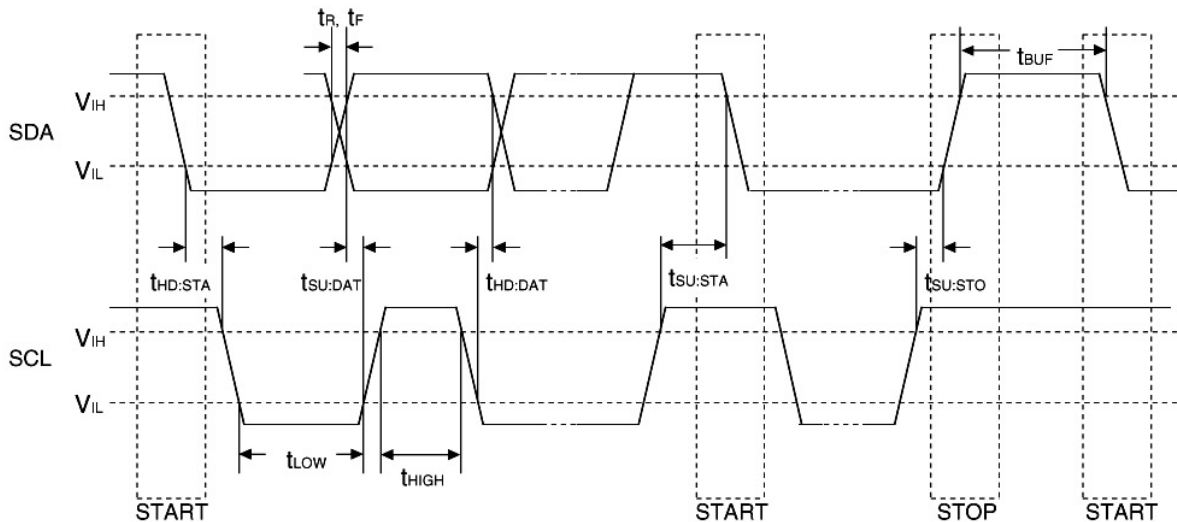
FUNCTIONAL BLOCKS

I^{2}C BUS interface

The I^{2}C BUS interface recognizes start/stop conditions, a slave address and a write/read mode selection by receiving SDA,SCL,CS0,CS1 and CS2 signals and then the latch pulses, dedicated to each data latch are generated.

Data Latch
This IC has 3 types of data latch : the I/O setting data latch, the input data latch and the output data latch and each latch is controlled by the I^{2}C BUS interface.

• I/O setting data latch
These latches set input- or output-state of each parallel data terminals (D$_0$ to D$_7$). They are set at the next byte after receiving the slave address byte in the write mode from the master. In case this latch is set to high, the data is transferred from the I^{2}C BUS interface to the parallel data terminals. In the opposite transmission : from the parallel data terminals to the I^{2}C BUS, it is set to low.

• Output data latch
In the write mode, the data from the I^{2}C BUS to the parallel data terminals is latched. When the master transmits output data after a setting in write mode, the output data is taken into the latches.

• Input data latch
In the read mode, the data of parallel data terminals is latched in the input data latches. The input data is taken into the latches from the parallel data terminals on every 8th negative edge of SCL clock . The latched data is output to the master through the sift resistor. On the output terminal assigned by the I / O setting latch, the input data latch takes the state of the output terminal.

Parallel input / output port
In case I/O setting latch is set to low (the input mode), each parallel terminal becomes hi-impedance and is able to accept a input. In another case I/O setting latch is set to high (output mode), each parallel terminal outputs a data according to the state of the output data latch.
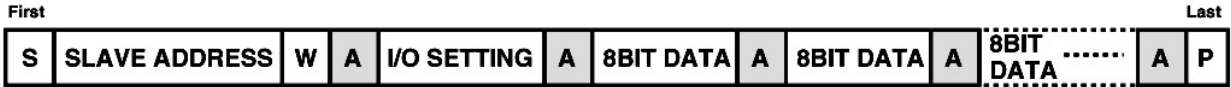
Power on reset
When power is turned on, each latch is reset and then the parallel data I/O terminals become hi-impedance (input mode).

DIGITAL DATA FORMAT

1. Write mode : I²C BUS data input to Parallel data output

First   Last

| S | SLAVE ADDRESS | W | A | I/O SETTING | A | 8BIT DATA | A | 8BIT DATA | A | 8BIT DATA | ------- | A | P |

2. Read mode : Parallel data input to I²C BUS data output

First   Last

| S | SLAVE ADDRESS | W | A | 8BIT DATA | A | 8BIT DATA | A | 8BIT DATA | A | ------- | 8BIT DATA | A̅ | P |

☐ Transmission from Master (MCU etc.) to Slave (M62320)

▓ Transmission from Slave (M62320) to Master (MCU etc.)

- **S : Start Condition**
  While SCL level is high, SDA line level should be changed from high to low.

- **Slave address**

First MSB ──────────────→ Last LSB

| 0 | 1 | 1 | 1 | A2 | A1 | A0 |
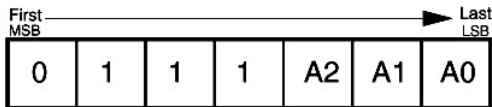
Lower three bits (A0,A1,A2) are a programmable address.
This IC is accessed only when the lower 3 bits data of slave
address coincide with the data of CS0 to CS2. (refer to the
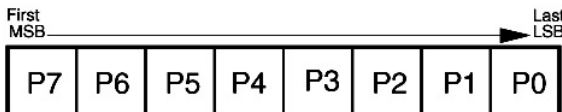right table)

- **Chip select data**

MSB		LSB			
A2	A1	A0	CS2	CS1	CS0
0	0	0	L	L	L
0	0	1	L	L	H
0	1	0	L	H	L
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	H	H	H

(L=Low,H=High)

- **W: Write (SDA = LOW), R : Read (SDA = HIGH)**

- **A: Acknowledge bit**

- **I/O setting data (I/O setting of parallel data I/O terminals.)**

First MSB ──────────────→ Last LSB

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

DATA INPUT from parallel data terminals = Low
DATA OUTPUT to parallel data terminals = High

- Each bit data corresponds to the I/O state of
  the parallel data terminals.

- **8bit data**

First MSB ──────────────→ Last LSB

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
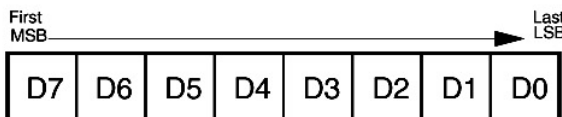
- **P : Stop condition**
  While SCL level is high, SDA level should be changed from low to high.

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FUNCTIONAL DESCRIPTION

All parallel data I/O terminals are set to the input-state after power-on. In case any terminals need to be set to the output state, the corresponding terminals should be set during the write mode. This setting is hold until a next setting.

In the write mode, 8 bits data can be transmitted from the I²C BUS interface to the parallel ports continually after the slave address and I/O setting.

In the read mode, 8 bits data can be transmitted from the parallel ports to the I²C BUS interface continually after the slave address setting.

In the case of a changing between the write- and read-mode, the data must be transmitted again from the starting condition.

• In a case of a data conversion from serial to parallel.
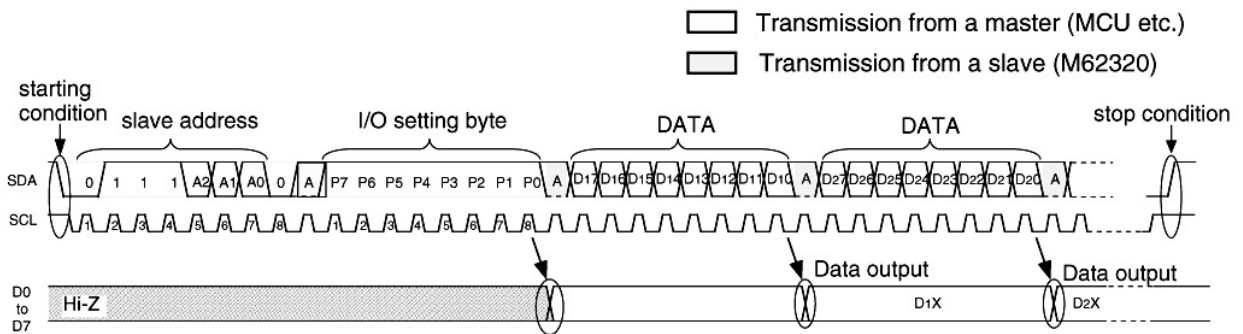
• In a case of a data conversion from parallel to serial.

All I/O setting resistors are set to low (input) in the write mode, before a parallel data is read. (All I/O setting resistors are set to the input mode after power-on.)
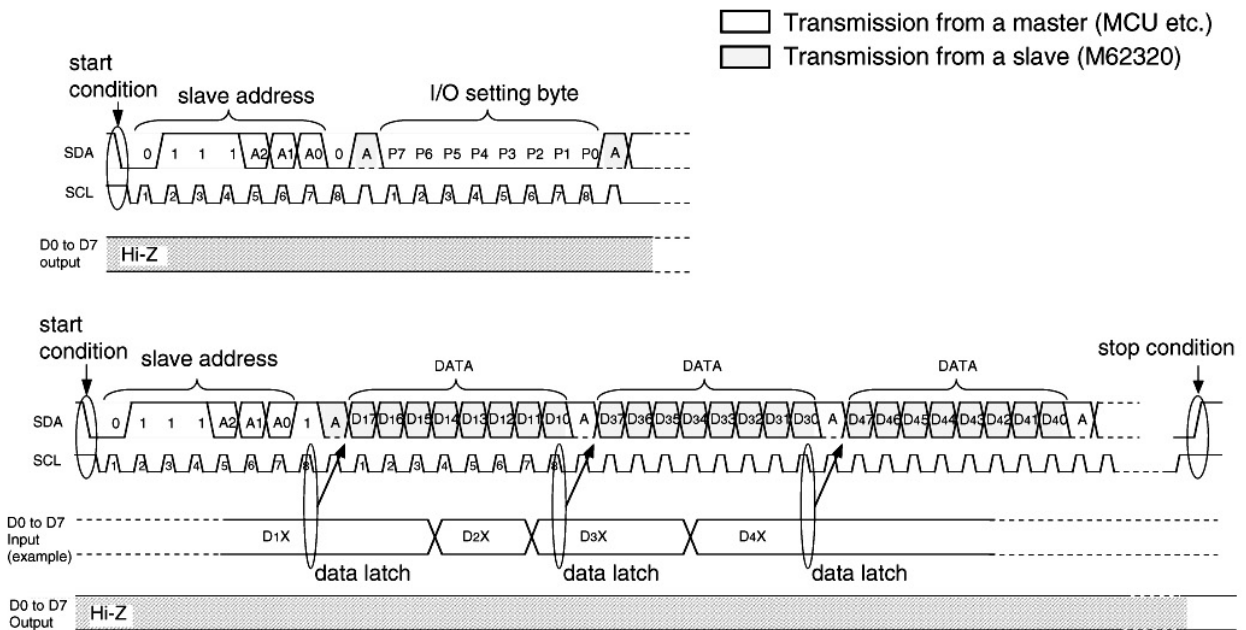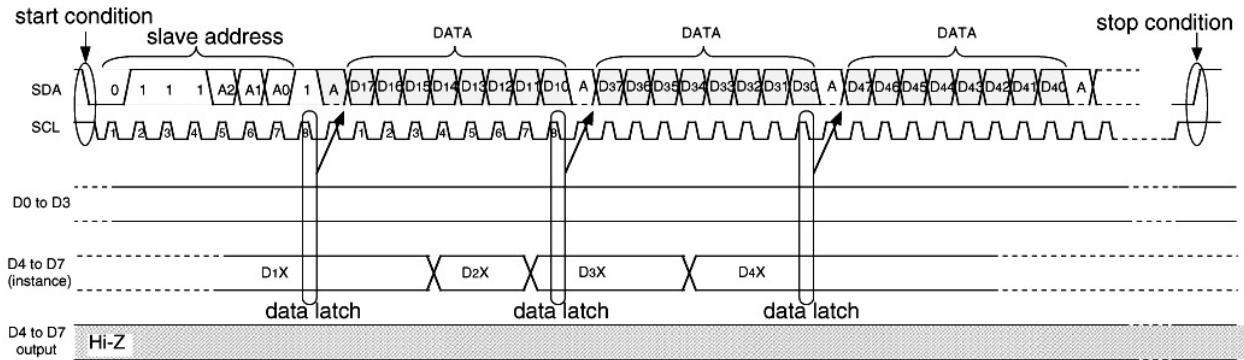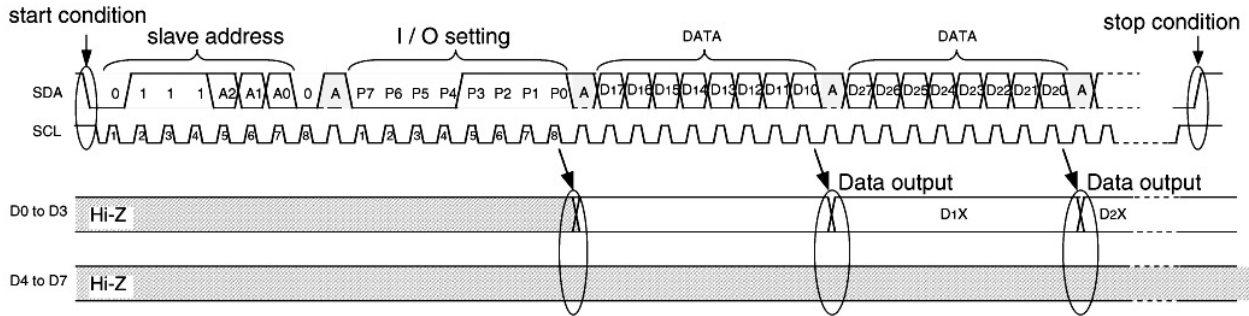
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• In case the I/O setting is different between each terminals.

An example : the parallel port terminals of D0 to D3 and D4 to D7 are assigned as output and input terminals, respectively.

• Write mode

The terminal assigned as an output provides the data written in the output data latch.
After power-on, all terminals are reset to the input-state.   Then an initial data low of the output latch are output after the I/O setting has been done. Finally the assigned output are provided after the 8-bit data transmission.
The terminal assigned as an input keeps the input condition (high-impedance) regardless of 8-bit data setting.

• Read mode

The input data is taken into the input latch on every 8th negative-going edge of the SCL clock through the terminal assigned as an input, and then the latched data is output via the SDA line.
The data of the output assigned terminal is also handled in the same procedures as above.

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TYPICAL APPLICATION
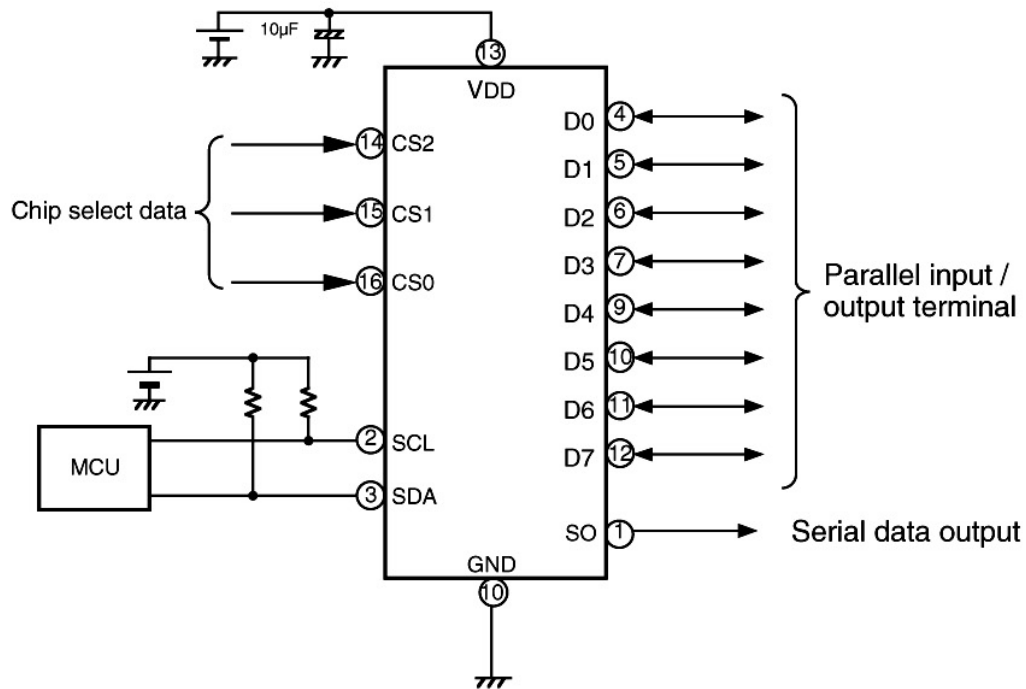
PRECAUTION FOR USE

- Purchase of MITSUBISHI ELECTRIC CORPORATION's I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system, provided that the system conforms to I²C Standard Specification as defined by Philips.

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury,fire or property damage. Remember to give due consideration to safety when making your circuit design, in order to prevent fires from spreading, redundancy, malfunction or other mishap.