Ordering number : ENN4363D

CMOS IC

LC6527N/F/L, 6528N/F/L

Single Chip 4-Bit Microcontroller for Small-Scale Control-Oriented Applications

The LC6527N / F / L, LC6528N / F / L belong to our single-chip 4-bit microcontroller LC6500 series fabicated using CMOS process technology and are suited for use in small-scale control-oriented applications. Their basic asrchitecture and instruction set are the same. Application areas include the standard logic circuits and applications where the number of controls is small. The LC6527N / F / L, LC6528N / F / L have relation to the LC6527C / H, LC6528C / H. The C version can be replaced by N version, and the H version (a part of the function is different). The L version is added as a low voltage version. The following show the careful difference of C and N version when you replace C version with N version.

			C version	N version
Operating Temperature			-30°C to +70°C	-40°C to +85°C
1-pin C oscillation			exist	not exist
CF Oscillation Constant	400kHz	MURATA	C1=C2=330pF R=0Ω	C1=C2=220pF R=2.2kΩ
	800kHz	MURATA	C1=C2=220pF R=0Ω	C1=C2=100pF R=2.2kΩ
		KYOCERA	C1=C2=220pF R=0Ω	C1=C2=110pF
	1MHz	MURATA	C1=C2=220pF R=0Ω	C1=C2=100pF R=2.2kΩ

(Note) The suffix of recommend oscillation is changed C version and N version, but the characteristic is no change.

Features

1) CMOS technology for a low-power operation (with instruction-controlled standby function)
2) ROM / RAM
   LC6527N / F / L ROM : 1K × 8bits, RAM : 64 × 4bits
   LC6528N / F / L ROM : 0.5K × 8bits, RAM : 32 × 4bits
3) Instruction set : 51 kinds selectable from 80 instructions common to the LC6500 series
4) Wide operating voltage range from 2.2V to 6.0V (L version)
5) Instruction cycle time of 0.92μs (F version)

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

6) Flexible I / O port
- Number of ports : 4 ports / 13 pins max.
- All ports : Input / output common
  Input / output voltage 15V max. (open drain type)
  Output current 20mA max. (sink current) (LED direct drivable)
- Option selectable for your intended system
  A. Open drain output, pull-up resistor : Single-bit select for all ports
  B. Output level at the reset mode : 4-bit select of H / L level for port C / D

7) Stack level : 4 levels
8) Timer : 4-bit prescaler+8-bit programmable timer
9) Clock oscillation option selectable for your intended system
- Oscillator option : 2-pin RC oscillation (N, L version)
  2-pin ceramic resonator oscillation, 1-pin external clock input (N, F, L version)
- Predivider option : No predivider, 1 / 3 predivider, 1 / 4 predivider (N, L version)

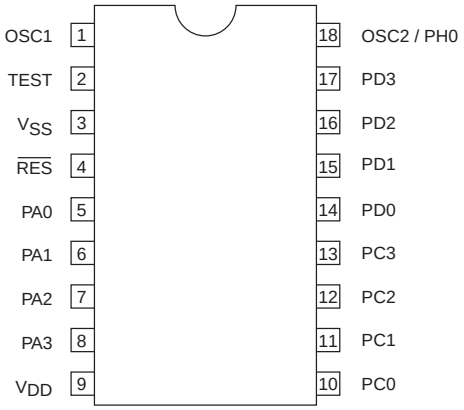
Function Table

Item		LC6527N / 28N	LC6527F / 28F	LC6527L / 28L
Memory	ROM	1024 × 8 bits (27N) 512 × 8 bits (28N)	1024 × 8 bits (27F) 512 × 8 bits (28F)	1024 × 8 bits (27L) 512 × 8 bits (28L)
	RAM	64 × 4 bits (27N) 32 × 4 bits (28N)	64 × 4 bits (27F) 32 × 4 bits (28F)	64 × 4 bits (27L) 32 × 4 bits (28L)
Instruc-tion	Instruction set	51	51	51
On-chip function	Timer	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer
	Stack level	4	4	4
	Standby function	Standby available by HALT instruction	Standby available by HALT instruction	Standby available by HALT instruction
Input / output port	Number of ports	I / O 13 max.	I / O 13 max.	I / O 13 max.
	I / O voltage	15V max.	15V max.	15V max.
	Output current	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.
	I / O circuit configuration	Open drain (N-channel) or pull-up resistor-provided output selectable bit by bit.		
	Output level at reset mode	"H" or "L" level selectable port by port (port C, D only)		
Charac-teristic	Minimum cycle time	2.77μs (V_{DD}≥4V) 6.0μs (V_{DD}≥3V)	0.92μs (V_{DD}≥4.5V)	3.84μs (V_{DD}≥2.2V)
	Supply voltage	3 to 6V	4.5 to 6V	2.2 to 6V
	Current dissipation	2.5mA typ.	4mA typ.	2.5mA typ.
Oscillation	Resonator	RC (850kHz, 400kHz typ.) ceramic (400k, 800k,1MHz, 4MHz)	ceramic 4MHz	RC (400kHz typ.) ceramic (400k, 800k,1MHz, 4MHz)
	predivider option	1 / 1, 1 / 3, 1 / 4	1 / 1	1 / 1, 1 / 3, 1 / 4
Other	Package	DIP18, MFP18*	DIP18, MFP18*	DIP18, MFP18*

(Note) Information on the resonator and oscillation circuit constants will be presented as soon as the recommended circuit is determined.
*MFP18 : under development

Pin Assignment

LC6527N / F / L
LC6528N / F / L



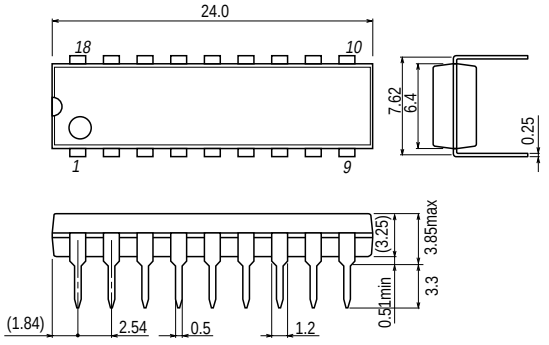
ILC00139

Common to DIP • MFP

• Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

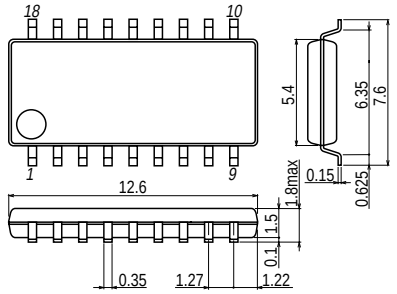
Package Dimentions

unit : mm
3007B



SANYO : DIP18(300mil)

unit : mm
3095



SANYO : MFP-18(300mil)

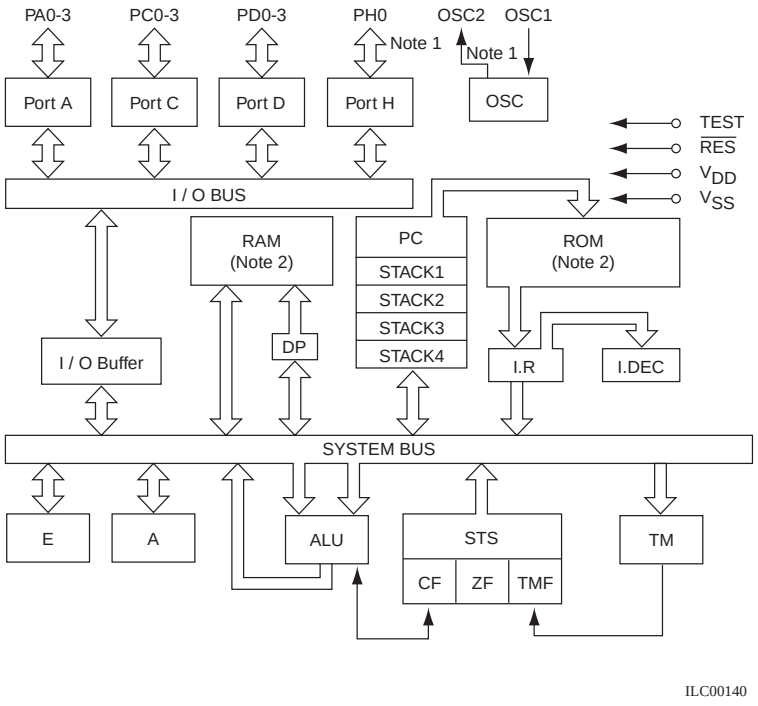
(Note) The package is the reference figure without the description of the rank. Please inquire us for the formal package.

Pin Name

OSC1, OSC2 : R, C or ceramic resonator for OSC
$\overline{RES}$: Reset
PA 0-3 : Input / output common port A 0-3
PC 0-3 : Input / output common port C 0-3
PD 0-3 : Input / output common port D 0-3
PH0 : Input / output common port H 0
TEST : Test

System Block Diagram

LC6527N / F / L, LC6528N / F / L



Note1. The PH0 pin or OSC2 pin is selected by the mask option.
Note2. LC6527N / F / N ROM : 1024 bytes RAM : 64 words
LC6528N / F / N ROM : 512 bytes RAM : 32 words

Development Support Tools

The following are available to support the program development for the LC6527, LC6528.

(1) User's Manual

"LC6527, LC6528 User's Manual" No. 24-6016 ('86.10.1.)

Note : Do not use "LC6523 Series User's Manual" No.16A-7015 and No.16-9064.

(2) Development Tool Manual

For the EVA-800 or the EVA-850 system, refer to "EVA-800. LC6527, LC6528 Development Tool Manual".

(3) Development Tools

A. For program evaluation

1. Piggy back (LC65PG23 / 26)
2. 23T27 ; The pin-to-pin conversion socket for the piggy back LC65PG23 / 26.

B. EVA-86000 system for program development is on development.

C. For program evaluation

microcontroller built-in EPROM (LC65E29)+conversion substrate (29T027)

Note. For notes for program evaluation, do not fail to refer to '4-3. Notes when evaluating programs'in "LC6527, LC6528 User's Manual".

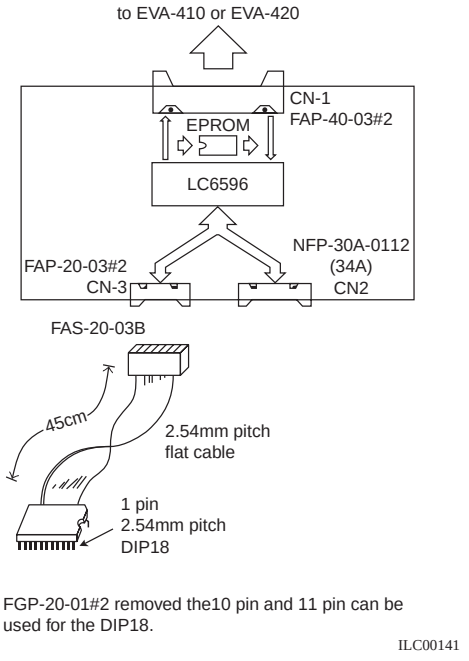


Fig.1 Evaluation kit terget board (EVA-TB6523C / 26C / 27C / 28C)

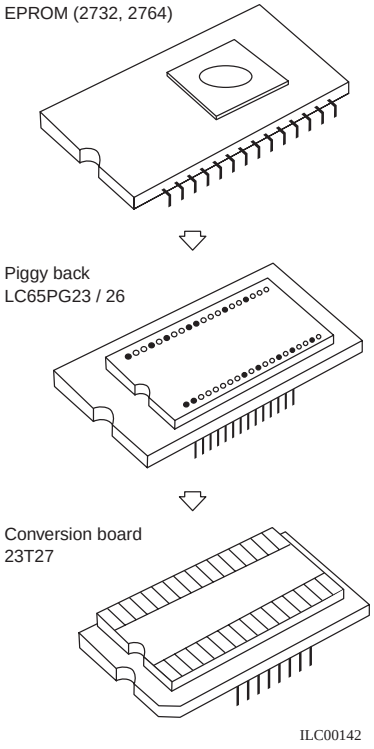
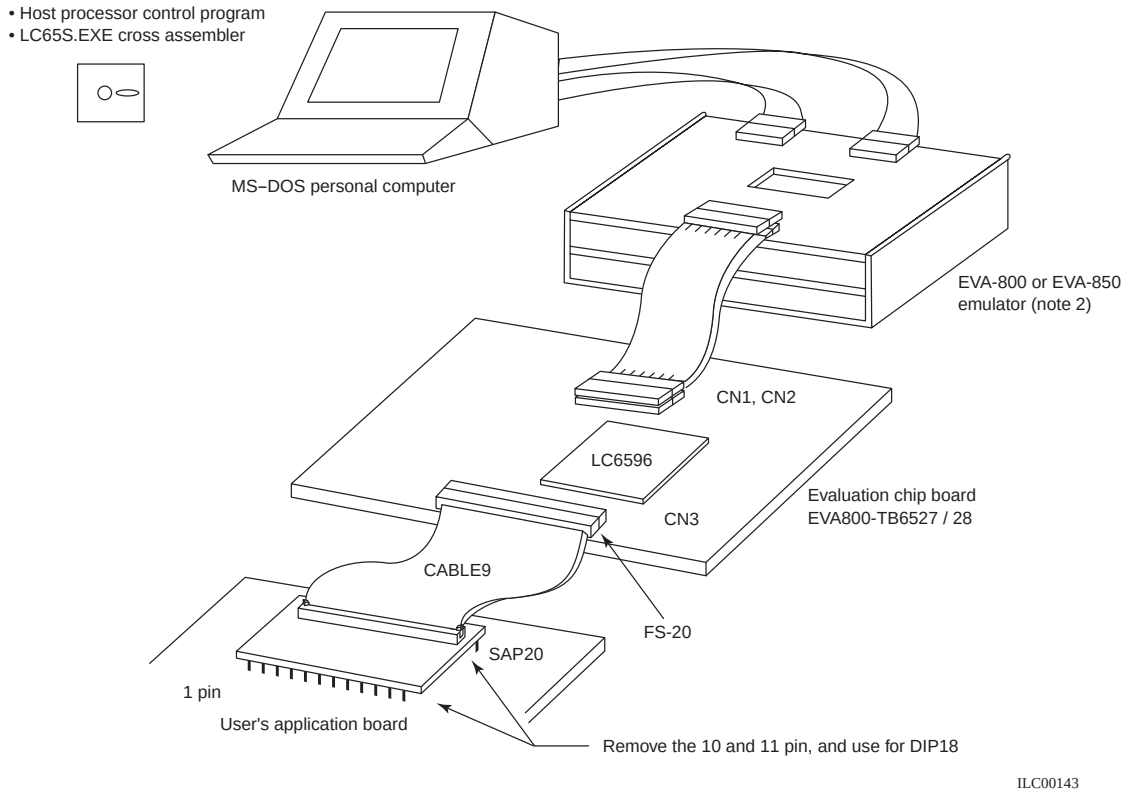


Fig. 2 Program evaluation

D. For program development (EVA-800 or EVA-850 system)

1. MS-DOS for host system (Note 1)
2. Cross assembler.....MS-DOS base cross assembler : <LC65S.EXE>
3. Host control program
4. Evaluation chip : LC6596
5. Emulator : EVA-800 or EVA-850 emulator and evaluation boards EVA800-TB6527 / 28

Appearance of Development Support System



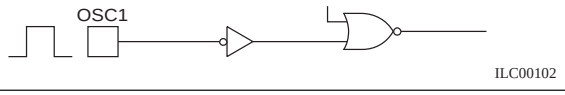
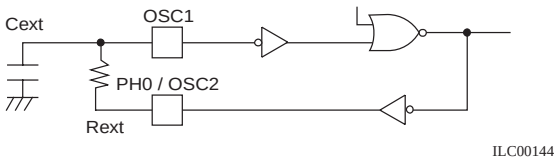
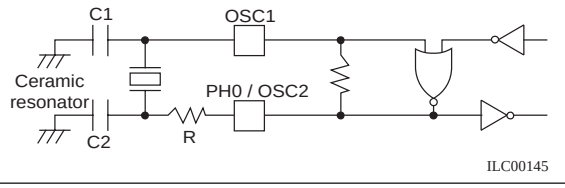
(Note 1) MS-DOS : Trademark of Microsoft Corporation

(Note 2) The EVA-800, EVA-850 are general term for emulator. A suffix (A, B,...) is added at the end of EVA-800 and EVA-850 as they are improved to be a newer version. Do not use the EVA-800 and EVA-850 with no suffix added.

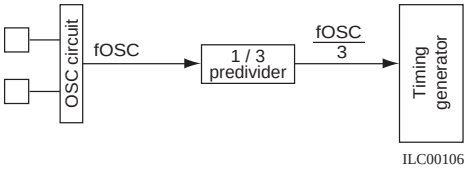
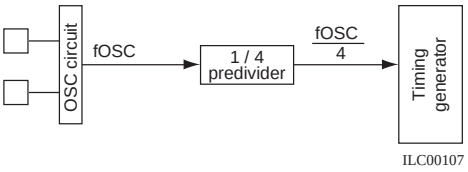
Pin Description

Pin name	Pins	I / O	Function	Option	Reset Mode
V_{DD} V_{SS}	1 1	– –	Power supply	–	–
OSC1	1	Input	• Pin for externally connecting RC, ceramic resonator for system clock generation. • For 1-pin external clock input, the PH0 / OSC2 pin is used as I / O port PH0. • For 2-pin RC OSC, 2-pin ceramic resonator OSC, the PH0 / OSC2 pin is used as OSC pin OSC2.	1) 1-pin external clock input 2) 2-pin RC OSC 3) 2-pin ceramic resonator OSC 4) Predivider option 1. No predivider 2. 1 / 3 predivider 3. 1 / 4 predivider	–
PA 0 to PA3	4	Input / output	• I / O port A0 to 3 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instruction) Single-bit set / reset (SPB, RPB instruction) • Standby is controlled by PA3. • The PA3 pin must be free from chattering during the HALT instruction execution cycle.	1) Open drain type output 2) With pull-up resistor 1), 2) : Specified bit by bit	• “H” output (Output Nch transistor : OFF)
PC0 to PC3	4	Input / output	• I / O port C0 to 3 same as for PA0 to 3 (Note) • Option permits output at the reset mode to be “H” or “L”. (Note) No standby control function is provided.	1) Open drain type output 2) With pull-up resistor 3) Output at reset mode : “H” 4) Output at reset mode : “L” • 1), 2) : Specified bit by bit • 3), 4) : Specified in a group of 4 bits	• “H” output • “L” output (Option-selectable)
PD0 to PD3	4	Input / output	• I / O port D0 to 3 Same as for PC0 to 3	Same as for PC0 to 3	Same as for PC0 to 3
PH0 / OSC2	1	Input / output	• I / O port H0 Same as for PA0 to 3 (Note) • Single-bit configuration • For 2-pin OSC, this pin is used as the OSC2 pin, providing no function as I / O port. (Note) No standby control function is provided	Same as for PA0 to 3	Same as for PA0 to 3
$\overline{RES}$	1	Input	• System reset input • For power-up reset, C is connected externally. • For reset restart, “L” level is applied for 4 clock cycles or more.		
TEST	1	Input	• LSI test pin Normally connected to V_{SS}		

Oscillator circuit option

Option Name	Circuit	Conditions, etc.
1. External clock		The PH0 / OSC2 pin is used as port PH0.
2. 2-pin RC OSC		The PH0 / OSC2 pin is used as OSC pin OSC2, providing no function as port.
3. Ceramic resonator OSC		The PH0 / OSC2 pin is used as OSC pin OSC2, providing no function as port.

Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider (1 / 1)		• Applicable to all of 3 OSC options. • The OSC frequency, external clock do not exceed 1444kHz. (LC6527N, 6528N) • The OSC frequency, external clock do not exceed 4330kHz. (LC6527F, 6528F) • The OSC frequency, external clock do not exceed 1040kHz. (LC6527L, 6528L)
2. 1 / 3 predivider		• Applicable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz.
3. 1 / 4 predivider		• Applicable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz.

Note : The OSC option and predivider option are summarized below. Full care must be exercised.

Table of OSC, predivider Option of LC6527N / 28N, 27F / 28F and 27L / 28L

LC6527N, LC6528N

Circuit Configuration	Frequency	Predivider Option (Cycle time)	V_{DD} Range	Remarks
Ceramic resonator OSC	400kHz	1 / 1 (10µs)	3 to 6V	Unusable with 1 / 3, 1 / 4 predivider
	800kHz	1 / 1 (5µs) 1 / 3 (15µs) 1 / 4 (20µs)	4 to 6V 4 to 6V 4 to 6V	
	1MHz	1 / 1 (4µs) 1 / 3 (12µs) 1 / 4 (16µs)	4 to 6V 4 to 6V 4 to 6V	
	4kHz	1 / 3 (3µs) 1 / 4 (4µs)	4 to 6V 4 to 6V	Unusable with 1 / 1 predivider
1-pin external clock	200k to 677kHz 600k to 2000kHz 800k to 2667kHz 200k to 1444kHz 600k to 4330kHz 800k to 4330kHz	1 / 1 (20 to 6µs) 1 / 3 (20 to 6µs) 1 / 4 (20 to 6µs) 1 / 1 (20 to 2.77µs) 1 / 3 (20 to 2.77µs) 1 / 4 (20 to 3.70µs)	3 to 6V 3 to 6V 3 to 6V 4 to 6V 4 to 6V 4 to 6V	
External clock by 2-pin RC OSC circuit	Same as above			
2-pin RC	Used with 1 / 1 predivider, recommended constants. If used with other than recommended constants, the frequency, predivider option, V_{DD} range must be the same as for 1-pin external clock.		3 to 6V 4 to 6V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option or the 2-pin RC option.			

LC6527F, LC6528F

Circuit Configuration	Frequency	Predivider Option (Cycle time)	V_{DD} Range	Remarks
Ceramic resonator OSC	4MHz	1 / 1 (1µs)	4.5 to 6V	
1-pin external clock	200k to 4330kHz	1 / 1 (20 to 0.92µs)	4.5 to 6V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option.			

LC6527L, LC6528L

Circuit Configuration	Frequency	Predivider Option (Cycle time)	V_{DD} Range	Remarks
Ceramic resonator OSC	400kHz	1 / 1 (10µs)	2.2 to 6V	Unusable with 1 / 3, 1 / 4 predivider
	800kHz	1 / 1 (5µs) 1 / 3 (15µs) 1 / 4 (20µs)	2.2 to 6V 2.2 to 6V 2.2 to 6V	
	1MHz	1 / 1 (4µs) 1 / 3 (12µs) 1 / 4 (16µs)	2.2 to 6V 2.2 to 6V 2.2 to 6V	
	4kHz	1 / 4 (4µs)	2.2 to 6V	Unusable with 1 / 1, 1 / 3 predivider
1-pin external clock	200k to 1040kHz 600k to 3120kHz 800k to 4160kHz	1 / 1 (20 to 3.84µs) 1 / 3 (20 to 3.84µs) 1 / 4 (20 to 3.84µs)	2.2 to 6V 2.2 to 6V 2.2 to 6V	
External clock by 2-pin RC OSC circuit	Same as above			
2-pin RC	Used with 1 / 1 predivider, recommended constants. If used with other than recommended constants, the frequency, predivider option, V_{DD} range must be the same as for 1-pin external clock.		2.2 to 6V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option or the 2-pin RC option.			

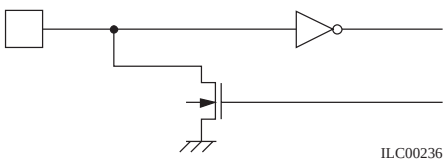
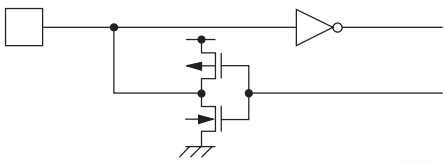
Option of ports C, D Output Level at the Reset Mode

For input / output common ports C, D either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output at the reset mode : “H”level	All of 4 bits of ports C, D
2. Output at the reset mode : “L”level	All of 4 bits of ports C, D

Option of port Output Configuration

For each input / output common port, either of the following two output configurations may be selected by option.

Option Name	Circuit	Conditions, etc.
1. Open drain output	 ILC00236	• Unapplicable to port PH0 / OSC2 when 2-pin RC OSC or ceramic resonator OSC is selected.
2. Output with pull-up resistor	 ILC00237	

LC6527N, LC6528N

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions	Limits	unit
Maximum supply voltage	V_{DD} max	V_{DD}		-0.3 to +7.0V	V
Output voltage	V_O	OSC2		Allowable up to voltage generated	V
Input voltage	V_I(1)	OSC1 (*1)		-0.3 to V_{DD}+0.3	V
	V_I(2)	TEST, $\overline{RES}$		-0.3 to V_{DD}+0.3	V
Input / output voltage	V_{IO}(1)	Port of OD type		-0.3 to +15	V
	V_{IO}(2)	Port of PU type		-0.3 to V_{DD}+0.3	V
Peak output current	I_{OP}	I / O port		-2 to +20	mA
Average output current	I_{OA}	I / O port	Per pin over the period of 100ms	-2 to +20	mA
	∑IOA(1)	PA0 to 3	Total current of PA0 to 3, (*2)	-6 to +40	mA
	∑IOA(2)	PC0 to 3 PH0 PD0 to 3	Total current of PC0 to 3, PD0 to 3 PH0 (*2)	-14 to +90	mA
Allowable power dissipation	Pd max(1)		Ta=-40 to +85°C (DIP package)	300	mW
	Pd max(2)		Ta=-40 to +85°C (MFP package)*	200	mW
Operating temperature	Topg			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

*……Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

2. Allowable Operating Conditions at Ta=-40°C to +85°C, V_{SS}= 0V, V_{DD}=3.0 to 6.0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min	typ	max	
Operating supply voltage	V_{DD}	V_{DD}			3.0		6.0	V
Standby supply voltage	VST	V_{DD}	RAM, register hold (*3)		1.8		6.0	V
"H"-level input voltage	V_{IH}(1)	Port of OD type (except H0)	Output Nch Tr. OFF		0.7V_{DD}		+13.5	V
	V_{IH}(2)	Port of PU type (except H0)	Output Nch Tr. OFF		0.7V_{DD}		V_{DD}	V
	V_{IH}(3)	H0 of OD type	Output Nch Tr. OFF		0.8V_{DD}		+13.5	V
	V_{IH}(4)	H0 of PU type	Output Nch Tr. OFF		0.8V_{DD}		V_{DD}	V
	V_{IH}(5)	$\overline{RES}$			0.8V_{DD}		V_{DD}	V
	V_{IH}(6)	OSC1	External clock mode		0.8V_{DD}		V_{DD}	V
"L"-level input voltage	V_{IL}(1)	Port	Output Nch Tr. OFF	V_{DD}=4 to 6	V_{SS}		0.3V_{DD}	V
	V_{IL}(2)	Port	Output Nch Tr. OFF	V_{DD}=3 to 6	V_{SS}		0.25V_{DD}	V
	V_{IL}(3)	OSC1	External clock mode	V_{DD}=4 to 6	V_{SS}		0.25V_{DD}	V
	V_{IL}(4)	OSC1	External clock mode	V_{DD}=3 to 6	V_{SS}		0.2V_{DD}	V
	V_{IL}(5)	TEST		V_{DD}=4 to 6	V_{SS}		0.3V_{DD}	V
	V_{IL}(6)	TEST		V_{DD}=3 to 6	V_{SS}		0.25V_{DD}	V
	V_{IL}(7)	$\overline{RES}$		V_{DD}=4 to 6	V_{SS}		0.25V_{DD}	V
	V_{IL}(8)	$\overline{RES}$		V_{DD}=3 to 6	V_{SS}		0.2V_{DD}	V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min	typ	max	
Operating frequency (cycle time)	fop (Tcyc)		When the 1 / 3 or 1 / 4 predivider option is selected, clock must not exceed 4.33MHz.	V_{DD}=4 to 6	200 (20)		1444 (2.77)	kHz (µs)
					200 (20)		667 (6.0)	kHz (µs)
External clock conditions			Fig.1.					
Frequency	text	OSC1	When clock exceeds 1.444MHz, the 1 / 3 or 1 / 4 predivider option is selected.	V_{DD}=4 to 6	200		4330	kHz
				3 to 6	200		2667	kHz
Pulse width	textH, textL	OSC1		V_{DD}=4 to 6	69			ns
				3 to 6	180			ns
Rise / Fall time	textR, textF	OSC1		V_{DD}=4 to 6			50	ns
				3 to 6			100	ns
Oscillation guaranty constants								
2-pin RC oscillation	Cext	OSC1, OSC2	Fig.2	V_{DD}=3 to 6		220±5%		pF
	Cext	OSC1, OSC2	Fig.2	V_{DD}=4 to 6		220±5%		pF
	Rext	OSC1, OSC2	Fig.2	V_{DD}=3 to 6		12±1%		kΩ
	Rext	OSC1, OSC2	Fig.2	V_{DD}=4 to 6		4.7±1%		kΩ
Ceramic resonator OSC			Fig.3			Table 1		

3. Electrical Characteristics at Ta=-40°C to +85°C, V_{SS}= 0V, V_{DD}=3.0V to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
"H"-level input current	I_{IH}(1)	Port of OD type	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) V_{IN}=±13.5V			+5.0	µA
	I_{IH}(2)	OSC1	External clock mode, V_{IN}=V_{DD}			+1.0	µA
"L"-level input current	I_{IL}(1)	Port of OD type	Output Nch Tr. OFF V_{IN}=V_{SS}	-1.0			µA
	I_{IL}(2)	Port of PU type	Output Nch Tr. OFF V_{IN}=V_{SS}	-1.3	-0.35		mA
	I_{IL}(3)	$\overline{RES}$	V_{IN}=V_{SS}	-45	-10		µA
	I_{IL}(4)	OSC1	External clock mode, V_{IN}=V_{SS}	-1.0			µA
"H"-level output voltage	V_{OH}(1)	Port of PU type	I_{OH}=-50µA V_{DD}=4.0V to 6.0V	V_{DD}-1.2			V
	V_{OH}(2)	Port of PU type	I_{OH}=-10µA	V_{DD}-0.5			V
"L"-level output voltage	V_{OL}(1)	Port	I_{OL}=10mA V_{DD}=4.0V to 6.0V			1.5	V
	V_{OL}(2)	Port	I_{OL}=1.8mA, I_{OL} of each port : 1mA or less			0.4	V
Hysteresis voltage	VHIS	$\overline{RES}$, OSC1 of schmitt type(*4)			0.1V_{DD}		V

Parameter	Symbol	Pins	Conditions	Ratings min	Ratings typ	Ratings max	unit
Current dissipation 2-pin RC oscillation	IDDOP(1)	V_{DD}	Output Nch Tr. OFF at operating, Port=V_{DD} Fig.2 fosc=850kHz (TYP) V_{DD}=4 to 6V		1.5	4	mA
	IDDOP(2)	V_{DD}	Fig.2 fosc=400kHz (TYP)		1.0	4	mA
Ceramic resonator oscillation	IDDOP(3)	V_{DD}	Fig.3 4MHz, 1 / 3 predivider V_{DD}=4 to 6V		2.0	5	mA
	IDDOP(4)	V_{DD}	Fig.3 4MHz, 1 / 4 predivider V_{DD}=4 to 6V		2.0	4	mA
	IDDOP(5)	V_{DD}	Fig.3 400kHz		0.5	2	mA
	IDDOP(6)	V_{DD}	Fig.3 800kHz V_{DD}=4 to 6V		1.5	4	mA
External clock	IDDOP(7)	V_{DD}	200kHz to 667kHz, 1 / 1 predivider 600kHz to 2000kHz, 1 / 3 predivider 800kHz to 2667kHz, 1 / 4 predivider		1.5	4	mA
	IDDOP(8)	V_{DD}	200kHz to 1444kHz, 1 / 1 predivider 600kHz to 4330kHz, 1 / 3 predivider 800kHz to 4330kHz, 1 / 4 predivider V_{DD}=4 to 6V		2.0	5	mA
Standby mode	IDDst	V_{DD} V_{DD}	Output Nch Tr. OFF V_{DD}=6V Port=V_{DD} V_{DD}=3V		0.05 0.025	10 5	μA μA
Oscillation characteristics Ceramic OSC Frequency	fCFOSC (*5)	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	Fig.3 fo=400kHz Fig.3 fo=800kHz, V_{DD}=4 to 6V Fig.3 fo=1MHz, V_{DD}=4 to 6V Fig.3 fo=4MHz, 1 / 3 predivider 1 / 4 predivider, V_{DD}=4 to 6V	384 768 960 3840	400 800 1000 4000	416 832 1040 4160	kHz kHz kHz kHz
Stable time	tCFS		Fig.4 fo=400kHz Fig.4 fo=800kHz, 1MHz, 4MHz, 1 / 3 predivider, 1 / 4 predivider V_{DD}=4 to 6V			10 10	ms ms
2-pin RC oscillation Frequency	fMOSC	OSC1, OSC2	Fig.2 Cext=220pF±5% Fig.2 Rext=4.7kΩ±1% V_{DD}=4 to 6V	646	850	1117	kHz
		OSC1, OSC2	Fig.2 Cext=220pF±5% Fig.2 Rext=12kΩ±1% V_{DD}=3 to 6V	304	400	580	kHz

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Pull-up resistance I / O port pull-up resistance	RPP	Port of PU type	V_{DD}=5V		14		kΩ
External reset characteristics Reset time	tRST				See Fig.5		
Pin capacitance	Cp		f=1MHz Other than pins to be tested, V_{IN}=V_{SS}		10		pF

(*1) When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.
(*2) Average over the period of 100ms.
(*3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
(*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option or external clock oscillation option has been selected.
(*5) fCFOSC : oscillation frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

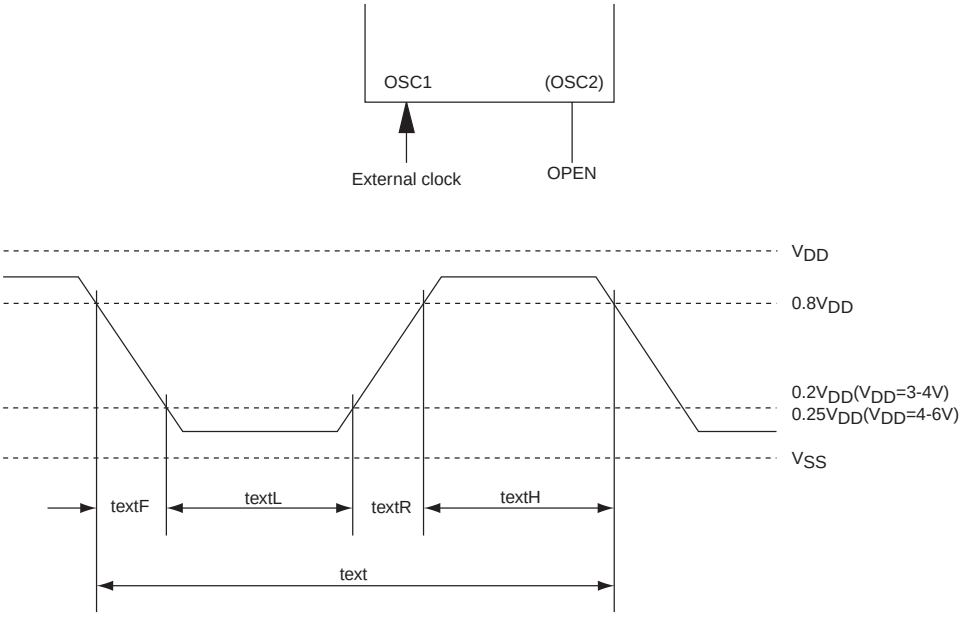


Fig. 1 External Clock Input Waveform ILC00146

*External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

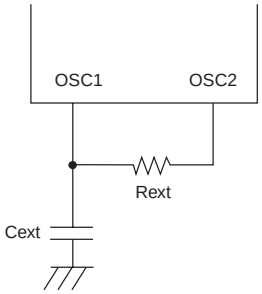


Fig. 2 2-pin RC Oscillation Circuit ILC00088

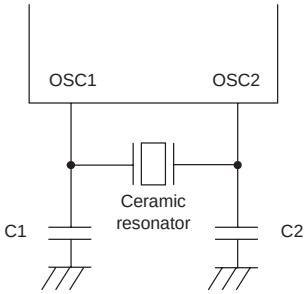


Fig. 3 Ceramic Resonator Oscillation Circuit ILC00147

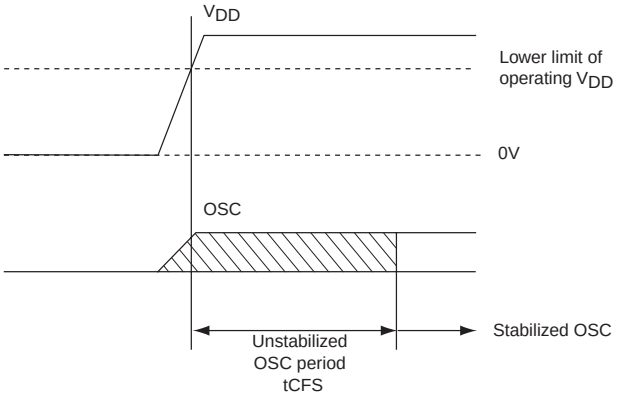


Fig. 4 Oscillation Stabilizing Period ILC00148

Table 1 Constants Guaranteed for Ceramic Resonator OSC

4MHz (Murata)	C1	33pF±10%
CSA4.00MG	C2	33pF±10%
CST4.00MGW (built-in C)	R	0Ω
4MHz (Kyocera)	C1	33pF±10%
KBR4.0MSA	C2	33pF±10%
KBR4.0MKS (built-in C)	R	0Ω
1MHz (Murata)	C1	100pF±10%
CSB1000J	C2	100pF±10%
	R	2.2Ω
1MHz (Kyocera)	C1	100pF±10%
KBR1000F	C2	100pF±10%
	R	0Ω
800kHz (Murata)	C1	100pF±10%
CSB800J	C2	100pF±10%
	R	2.2Ω
800kHz (Kyocera)	C1	100pF±10%
KBR800F	C2	100pF±10%
	R	0Ω
400kHz (Murata)	C1	220pF±10%
CSB400P	C2	220pF±10%
	R	2.2Ω
400kHz (Kyocera)	C1	330pF±10%
KBR400BK	C2	330pF±10%
	R	0Ω

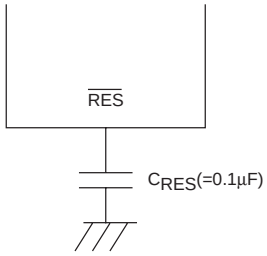


Fig. 5 Reset Circuit ILC00240

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

RC Oscillation Characteristics of the LC6527N, LC6528N

Fig. 6 shows the RC oscillation characteristics of the LC6527N, LC6528N. For the variation range of RC OSC frequency of the LC6527N, LC6528N, the following are guaranteed at the external constants only shown below.

1) V_{DD}=3.0V to 6.0V, Ta=-40°C to +85°C
   External constants Cext=220pF
   Rext=12kΩ
   304kHz≤fMOSC≤580kHz
2) V_{DD}=4.0V to 6.0V, Ta=-40°C to +85°C
   Cext=220pF
   Rext=4.7kΩ
   646kHz≤fMOSC≤1117kHz

If any other constants than specified above are used, the range of Rext=3kΩ to 20kΩ, Cext=150pF to 390pF must be observed. (See Fig.6.)

(*6) : The oscillation frequency at V_{DD}=5.0V, Ta=+25°C must be in the range of 350kHz to 750kHz.
(*7) : The oscillation frequency at V_{DD}=4.0V to 6.0V, Ta=-40°C to +85°C and V_{DD}=3.0V to 6.0V, Ta=-40°C to 85°C must be within the operation clock frequency range.

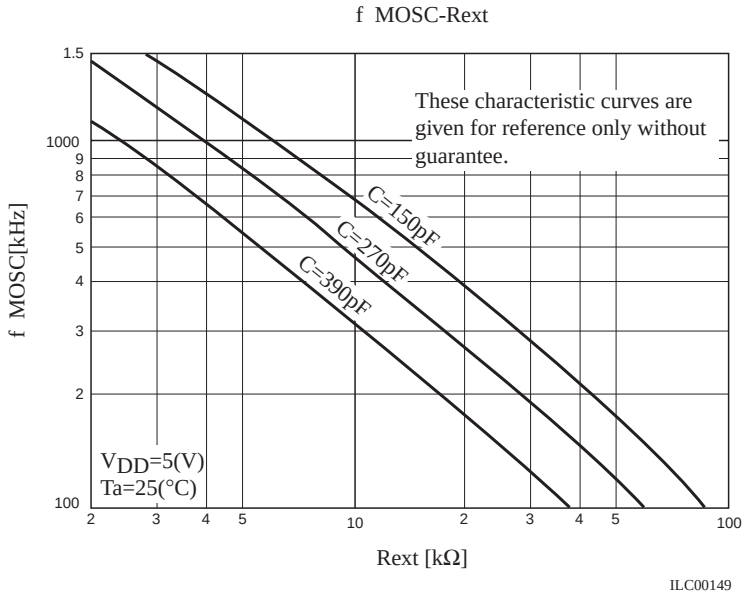


Fig. 6 RC Oscillation Frequency Data (Typ.)

LC6527F, LC6528F

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions	Limits	unit
Maximum supply voltage	V_{DD} max	V_{DD}		-0.3 to +7.0V	V
Output voltage	V_O	OSC2		Allowable up to voltage ganerated	V
Input voltage	V_I(1)	OSC1 (*1)		-0.3 to V_{DD}+0.3	V
	V_I(2)	TEST, $\overline{RES}$		-0.3 to V_{DD}+0.3	V
Output voltage	V_{IO}(1)	Port of OD type		-0.3 to +15	V
	V_{IO}(2)	Port of PU type		-0.3 to V_{DD}+0.3	V
Peak output current	I_{OP}	I / O port		-2 to +20	mA
Average output current	I_{OA}	I / O port	Per pin over the period of 100ms	-2 to +20	mA
	∑IOA(1)	PA0 to 3	Total current of PA0 to 3, (*2)	-6 to +40	mA
	∑IOA(2)	PC0 to 3 PH0 PD0 to 3	Total current of PC0 to 3, PD0 to 3, PH0 (*2)	-14 to +90	mA
Allowable power dissipation	Pd max(1)		Ta=-40 to +85°C (DIP package)	300	mW
	Pd max(2)		Ta=-40 to +85°C (MFP package)*	200	mW
Operating temperature	Topg			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

*……Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

2. Allowable Operating Conditions at Ta=-40°C to +85°C, V_{SS}= 0V, V_{DD}=4.5 to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating supply voltage	V_{DD}	V_{DD}		4.5		6.0	V
Standby supply voltage	VST	V_{DD}	RAM, register hold (*3)	1.8		6.0	V
"H"-level input voltage	V_{IH}(1)	Port of OD type (except H0)	Output Nch Tr. OFF	0.7V_{DD}		+13.5	V
	V_{IH}(2)	Port of PU type (except H0)	Output Nch Tr. OFF	0.7V_{DD}		V_{DD}	V
	V_{IH}(3)	H0 of OD type	Output Nch Tr. OFF	0.8V_{DD}		+13.5	V
	V_{IH}(4)	H0 of PU type	Output Nch Tr. OFF	0.8V_{DD}		V_{DD}	V
	V_{IH}(5)	$\overline{RES}$		0.8V_{DD}		V_{DD}	V
	V_{IH}(6)	OSC1	External clock mode	0.8V_{DD}		V_{DD}	V
"L"-level input voltage	V_{IL}(1)	Port	Output Nch Tr. OFF	V_{SS}		0.3V_{DD}	V
	V_{IL}(2)	OSC1	External clock mode	V_{SS}		0.25V_{DD}	V
	V_{IL}(3)	TEST		V_{SS}		0.3V_{DD}	V
	V_{IL}(4)	$\overline{RES}$		V_{SS}		0.25V_{DD}	V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating frequency (Cycle time)	fop (Tcyc)			200 (20)		4330 (0.92)	kHz (μs)
External clock conditions Frequency Pulse width Rise / Fall time	 text textH, textL textR, textF	 OSC1 OSC1 OSC1	 Fig.1	 200 69		 4330 50	 kHz ns ns
Oscillation guaranteed constants ceramic resonator OSC			Fig.2	See Table 1			

3. Electrical Characteristics at Ta=-40°C to +85°C, V_{SS}= 0V, V_{DD}=4.5V to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
"H"-level input current	I_{IH}(1)	Port of OD type	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) V_{IN}=±13.5V			+5.0	μA
	I_{IH}(2)	OSC1	External clock mode, V_{IN}=V_{DD}			+1.0	μA
"L"-level input current	I_{IL}(1)	Port of OD type	Output Nch Tr. OFF V_{IN}=V_{SS}	-1.0			μA
	I_{IL}(2)	Port of PU type	Output Nch Tr. OFF V_{IN}=V_{SS}	-1.3	-0.35		mA
	I_{IL}(3)	$\overline{RES}$	V_{IN}=V_{SS}	-45	-10		μA
	I_{IL}(4)	OSC1	External clock mode, V_{IN}=V_{SS}	-1.0			μA
"H"-level output voltage	V_{OH}(1)	Port of PU type	I_{OH}=-50μA	V_{DD}-1.2			V
	V_{OH}(2)	Port of PU type	I_{OH}=-10μA	V_{DD}-0.5			V
"L"-level output voltage	V_{OL}(1)	Port	I_{OL}=10mA			1.5	V
	V_{OL}(2)	Port	I_{OL}=1.8mA, I_{OL} of each port : 1mA or less			0.4	V
Hysteresis voltage	VHIS	$\overline{RES}$, OSC1 of schmitt type(*4)			0.1V_{DD}		V

Parameter	Symbol	Pins	Conditions	Ratings min	Ratings typ	Ratings max	unit
Current dissipation Ceramic resonator OSC	IDDOP(1)	V_{DD}	Fig.2 4MHz *1		1.5	3.5	mA
External clock	IDDOP(2)	V_{DD}	200kHz to 4330kHz *1 *1 Output Nch Tr.OFF at Operating mode Port=V_{DD}		1.5	3.5	mA
Standby mode	IDDst	V_{DD} V_{DD}	Output Nch Tr. OFF V_{DD}=6V Port=V_{DD} VDD=3V		0.05 0.025	10 5	μA μA
Oscillation characteristics Ceramic OSC Frequency	fCFOSC	OSC1, OSC2	Fig.2 fo=4MHz (*5)	3840	4000	4160	kHz
Stable time	tCFS		Fig.3 fo=4MHz			10	ms
Pull-up resistance I / O port pull-up resistance	RPP	Port of PU type	V_{DD}=5V		14		kΩ
External reset characteristics Reset time	tRST				See Fig.4		
Pin capacitance	Cp		f=1MHz, other than pins to be tested, V_{IN}=V_{SS}		10		pF

(*1) When oscillated internally under the oscillating conditions in Fig.2, up to the oscillation amplitude generated is allowable.
(*2) Average over the period of 100ms.
(*3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
(*4) The OSC1 pin can be schmitt-triggered when the external clock oscillation option has been selected.
(*5) fCFOSC : Oscillatable frequency.

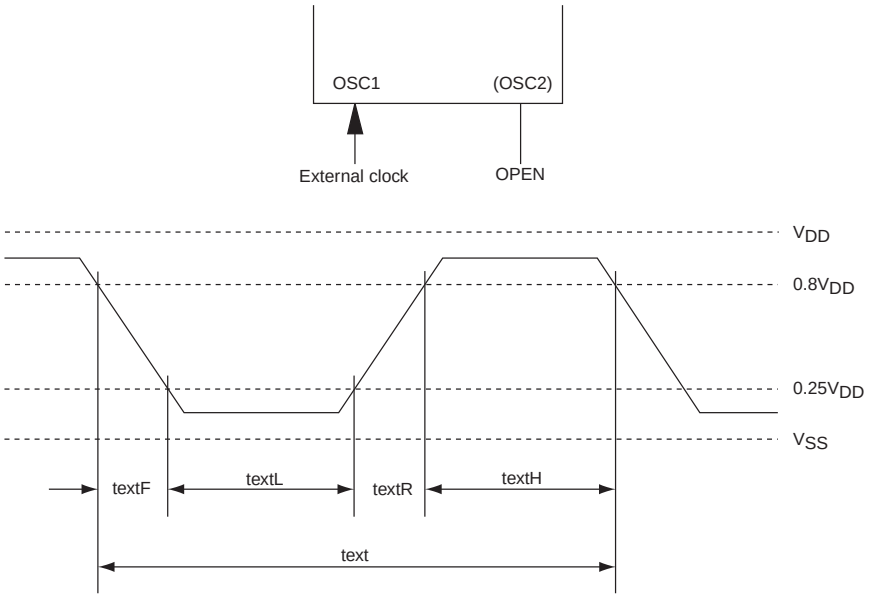


Fig. 1 External Clock Input Waveform ILC00150

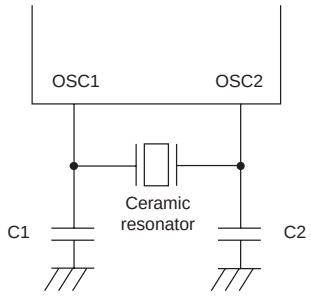


Fig. 2 Ceramic Resonator OSC Circuit ILC00151

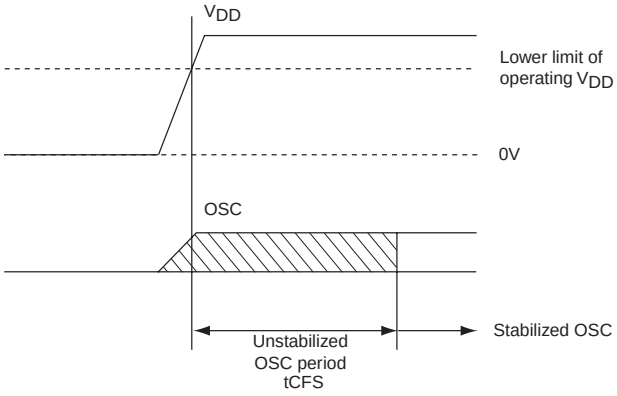


Fig. 3 OSC Stabilizing Period ILC00152

Table 1 Constants Guaranteed for Ceramic Resonator OSC

4MHz (Murarta)	C1	33pF±10%
CSA4.00MG	C2	33pF±10%
CST4.00MGW (built-in C)	R	0Ω
4MHz (Kyocera)	C1	33pF±10%
KBR4.0MSA	C2	33pF±10%
KBR4.0MKS (built-in C)	R	0Ω

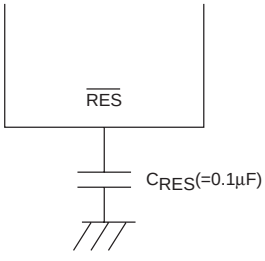


Fig. 4 Reset Circuit ILC00153

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1µF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

LC6527L, LC6528L

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions	Limits	unit
Maximum supply voltage	V_{DD} max	V_{DD}		-0.3 to +7.0	V
Output voltage	V_O	OSC2		Allowable up to votage ganerated	V
Input voltage	V_I(1)	OSC1 (*1)		-0.3 to V_{DD}+0.3	V
	V_I(2)	TEST, $\overline{RES}$		-0.3 to V_{DD}+0.3	V
Input / output voltage	V_{IO}(1)	Port of OD type		-0.3 to +15	V
	V_{IO}(2)	Port of PU type		-0.3 to V_{DD}+0.3	V
Peak output current	I_{OP}	I / O port		-2 to +20	mA
Average output current	I_{OA}	I / O port	Per pin over the period of 100ms	-2 to +20	mA
	∑IOA(1)	PA0 to 3	Total current of PA0 to 3, (*2)	-6 to +40	mA
	∑IOA(2)	PC0 to 3 PH0 PD0 to 3	Total current of PC0 to 3, PD0 to 3 PH0 (*2)	-14 to +90	mA
Allowable power dissipation	Pd max(1)		Ta=-40 to +85°C (DIP package)	250	mW
	Pd max(2)		Ta=-40 to +85°C (MFP package)*	150	mW
Operating temperature	Topg			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

*……Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

2. Allowable Operating Conditions at Ta=-40°C to 85°C, V_{SS}= 0V, V_{DD}=2.2 to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating supply voltage	V_{DD}	V_{DD}		2.2		6.0	V
Standby supply voltage	VST	V_{DD}	RAM, register hold (*3)	1.8		6.0	V
"H"-level input voltage	V_{IH}(1)	Port of OD type (except H0)	Output Nch Tr. OFF	0.7V_{DD}		+13.5	V
	V_{IH}(2)	Port of PU type (except H0)	Output Nch Tr. OFF	0.7V_{DD}		V_{DD}	V
	V_{IH}(3)	H0 of OD type	Output Nch Tr. OFF	0.8V_{DD}		+13.5	V
	V_{IH}(4)	H0 of PU type	Output Nch Tr. OFF	0.8V_{DD}		V_{DD}	V
	V_{IH}(5)	$\overline{RES}$		0.8V_{DD}		V_{DD}	V
	V_{IH}(6)	OSC1	External clock	0.8V_{DD}		V_{DD}	V
"L"-level input voltage	V_{IL}(1)	Port	Output Nch Tr. OFF	V_{SS}		0.2V_{DD}	V
	V_{IL}(2)	OSC1	External clock	V_{SS}		0.15V_{DD}	V
	V_{IL}(3)	TEST		V_{SS}		0.2V_{DD}	V
	V_{IL}(4)	$\overline{RES}$		V_{SS}		0.15V_{DD}	V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating frequency (cycle time)	fop (Tcyc)		When the 1 / 3 or 1 / 4 predivider option is selected, clock must not exceed 4.16MHz.	200 (20)		1040 (3.84)	kHz (μs)
External clock conditions							
Frequency	text	OSC1	Fig.1 When clock exceeds 1.040MHz, the 1 / 3 or 1 / 4 predivider option is selected.	200		4160	kHz
Pulse width	textH, textL	OSC1		100			ns
Rise / fall time	textR, textF	OSC1				100	ns
Oscillation guaranteed constants 2-pin RC oscillation	Cext	OSC1, OSC2	Fig.2	220±5%			pF
	Rext			12±1%			kΩ
Ceramic oscillation			Fig.3	See Table 1.			

3. Electrical Characteristics at Ta=-40°C to +85°C, V_{SS}= 0V, V_{DD}=2.2V to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
"H"-level input current	I_{IH}(1)	Port of OD type	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) V_{IN}=±13.5V			+5.0	μA
	I_{IH}(2)	OSC1	External clock mode, V_{IN}=V_{DD}			+1.0	μA
"L"-level input current	I_{IL}(1)	Port of OD type	Output Nch Tr. OFF V_{IN}=V_{SS}	-1.0			μA
	I_{IL}(2)	Port of PU type	Output Nch Tr. OFF V_{IN}=V_{SS}	-1.3	-0.35		mA
	I_{IL}(3)	$\overline{RES}$	V_{IN}=V_{SS}	-45	-10		μA
	I_{IL}(4)	OSC1	External clock mode, V_{IN}=V_{SS}	-1.0			μA
"H"-level output voltage	V_{OH}	Port of PU type	I_{OH}=-10μA	V_{DD}-0.5			V
"L"-level output voltage	V_{OL}(1)	Port	I_{OL}=3mA			1.5	V
	V_{OL}(2)	Port	I_{OL}=1mA, I_{OL} of each port : 1mA or less			0.4	V
Hysteresis voltage	VHIS	$\overline{RES}$, OSC1 of schmitt type(*4)			0.1V_{DD}		V

Parameter	Symbol	Pins	Conditions	Ratings min	Ratings typ	Ratings max	unit
Current dissipation 2-pin RC OSC	IDDOP(1)	V_{DD}	Output Nch Tr. OFF at operating, Port=V_{DD} Fig.2 fOSC=400kHz (TYP)		0.8	2.5	mA
Ceramic OSC	IDDOP(2)	V_{DD}	Fig.3 4MHz, 1 / 4 predivider		1.2	2.5	mA
	IDDOP(3)	V_{DD}	Fig.3 4MHz, 1 / 4 predivider V_{DD}=2.2V		0.5	1	mA
	IDDOP(4)	V_{DD}	Fig.3 400kHz		0.5	2	mA
	IDDOP(5)	V_{DD}	Fig.3 800kHz		1.0	2.5	mA
External clock	IDDOP(6)	V_{DD}	200kHz to 667kHz, 1 / 1 predivider 600kHz to 2000kHz, 1 / 3 predivider 800kHz to 2667kHz, 1 / 4 predivider		1.0	2.5	mA
Standby mode	IDDst	V_{DD}	Output Nch Tr. OFF V_{DD}=6V		0.05	10	μA
		V_{DD}	Port=V_{DD} V_{DD}=2.2V		0.025	5	μA
Oscillation characteristics Ceramic OSC Frequency	fCFOSC (*5)	OSC1, OSC2	Fig.3 fo=400kHz	384	400	416	kHz
		OSC1, OSC2	Fig.3 fo=800kHz	768	800	832	kHz
		OSC1, OSC2	Fig.3 fo=1MHz	960	1000	1040	kHz
		OSC1, OSC2	Fig.3 fo=4MHz 1 / 4 predivider	3840	4000	4160	kHz
Stable time	tCFS		Fig.4 fo=400kHz			10	ms
			Fig.4 fo=800kHz, 1MHz, 4MHz, 1 / 4 predivider			10	ms
2-pin RC OSC Frequency	fMOSC	OSC1, OSC2	Fig.2 Cext=220pF±5% Fig.2 Rext=12kΩ±1%	281	400	580	kHz
Pull-up resistance I / O port pull-up resistance	RPP	Port of PU type	V_{DD}=5V		14		kΩ
External reset characteristics Reset time	tRST		See Fig.5.				
Pin capacitance	Cp		f=1MHz Other than pins to be tested, V_{IN}=V_{SS}		10		pF

(*1) When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.

(*2) Average over the period of 100ms.

(*3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.

(*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option or external clock oscillation option has been selected.

(*5) fCFOSC : Oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

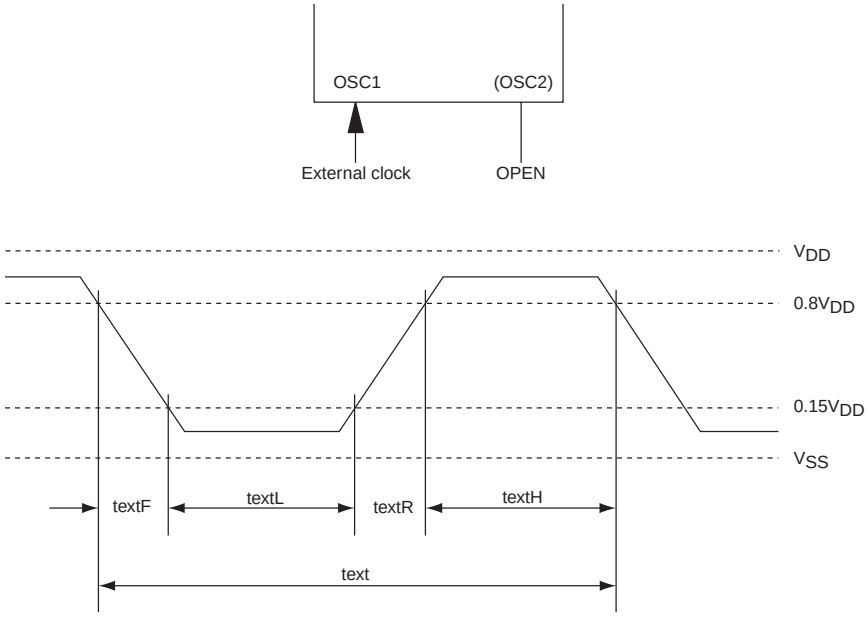


Fig. 1 External Clock Input Waveform ILC00154

*External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

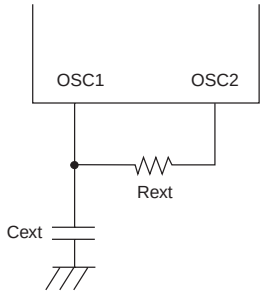


Fig. 2 2-pin RC Oscillation Circuit ILC00088

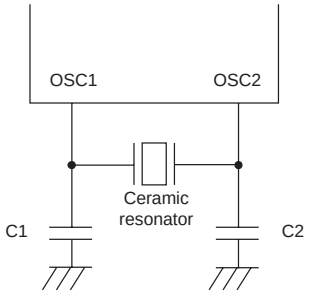


Fig. 3 Ceramic Resonator Oscillation Circuit ILC00147

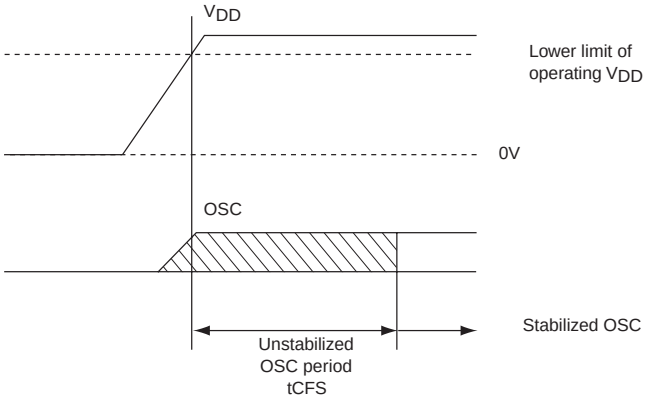


Fig. 4 Oscillation Stabilizing Period ILC00148

Table 1 Constants Guaranteed for Ceramic Resonator OSC

4MHz (Murata) CSA4.00MGU CST4.00MGWU (built-in C)	C1	33pF±10%
	C2	33pF±10%
	R	0Ω
1MHz (Murata) CSB1000J	C1	100pF±10%
	C2	100pF±10%
	R	2.2Ω
1MHz (Kyocera) KBR1000F	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
800kHz (Murata) CSB800J	C1	100pF±10%
	C2	100pF±10%
	R	2.2Ω
800kHz (Kyocera) KBR800F	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
400kHz (Murata) CSB400P	C1	220pF±10%
	C2	220pF±10%
	R	2.2Ω
400kHz (Kyocera) KBR400BK	C1	330pF±10%
	C2	330pF±10%
	R	0Ω

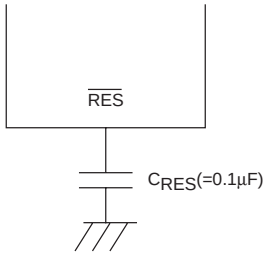


Fig. 5 Reset Circuit ILC00240

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

RC Oscillation Characteristic of the LC6527L, LC6528L

Fig. 6 shows the RC oscillation characteristic of the LC6527L, 6528L. For the variation range of RC OSC frequency of the LC6527L, 6528L, the following are guaranteed at the external constants only shown below.

V_{DD}=2.2V to 6.0V, Ta=-40°C to +85°C

External constants Cext=220pF

Rext=12kΩ

281kHz≤fMOSC≤580kHz

If any other constants than specified above are used, the range of Rext=3kΩ to 20kΩ, Cext=150pF to 390pF must be observed. (See Fig.6.)

(*6) : The oscillation frequency at V_{DD}=5.0V, Ta=+25°C must be in the range of 350kHz to 500kHz.

(*7) : The oscillation frequency at V_{DD}=2.2V to 6.0V, Ta=-40°C to +85°C must be within the operation clock frequency range.

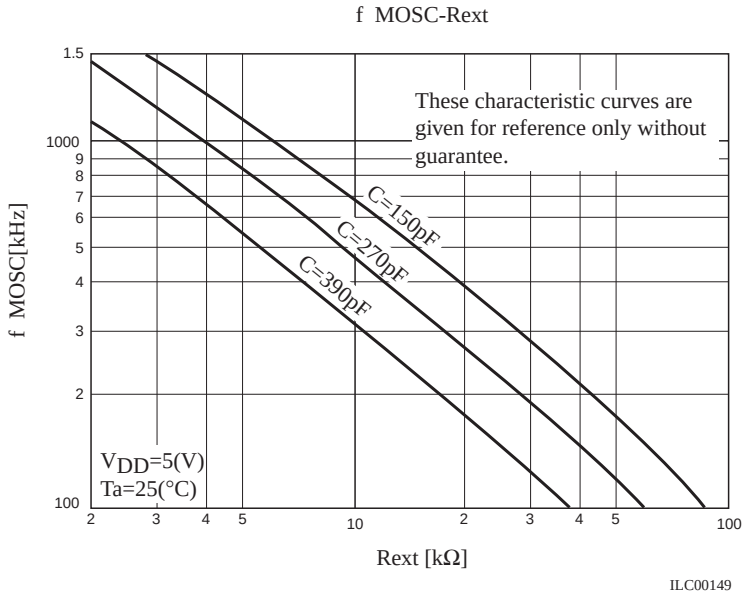


Fig. 6 RC Oscillation Frequency Data (Typ.)

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