M50253P/M50255P

12-BIT/16-BIT SERIAL PARALLEL CONVERTER

DESCRIPTION

M50253P/M50255P is a semiconductor integrated circuit designed for serial parallel converter with N-ch opendrain output. (V_O 12V max.)
M50253P and M50255P serves as serial parallel converter of 12-bit and 16-bit, respectively.

FEATURES

- Single 5V supply voltage
- High voltage breakdown output (12V)
- Controllable by only 2 pin: CLK, DATA

APPLICATION

Extension of I/O ports for microcomputer

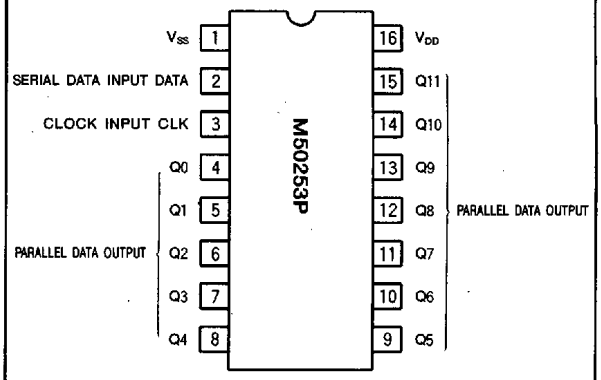
RECOMMENDED OPERATING CONDITION

Supply voltage range ..... 4.5~5.5V

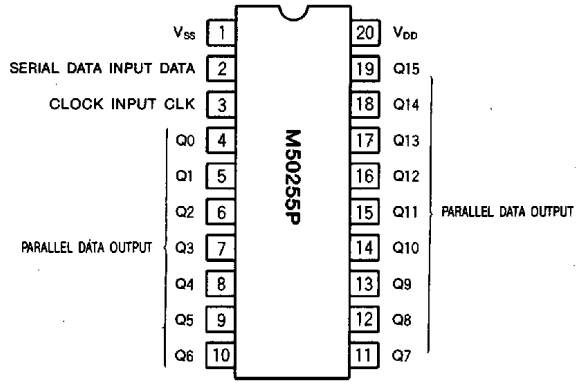
"H" input voltage ..... $0.7 \times V_{DD} \sim V_{DD}$

"L" input voltage ..... $0 \sim 0.3 \times V_{DD}$

PIN CONFIGURATION (TOP VIEW)

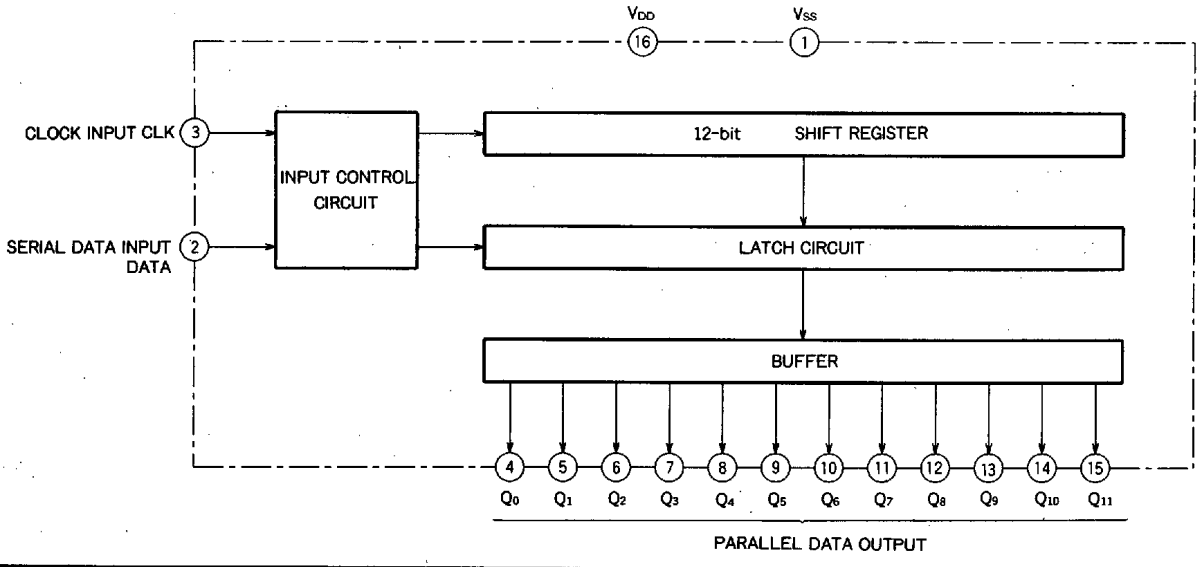


Outline 16P4

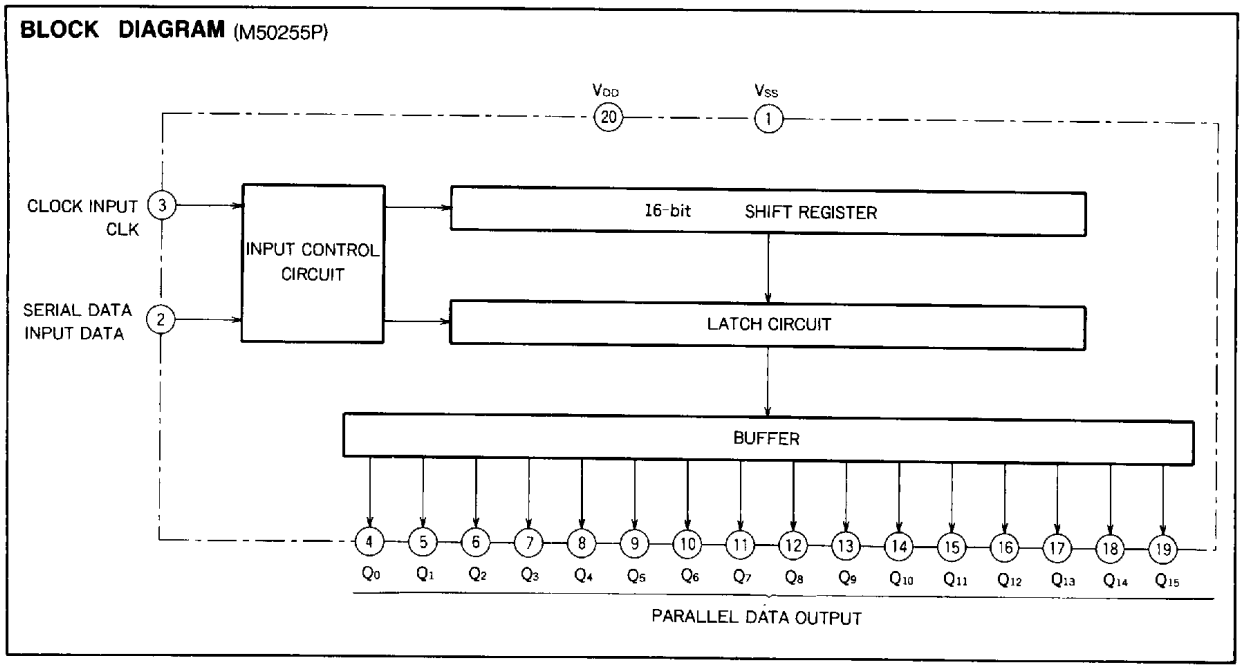


Outline 20P4

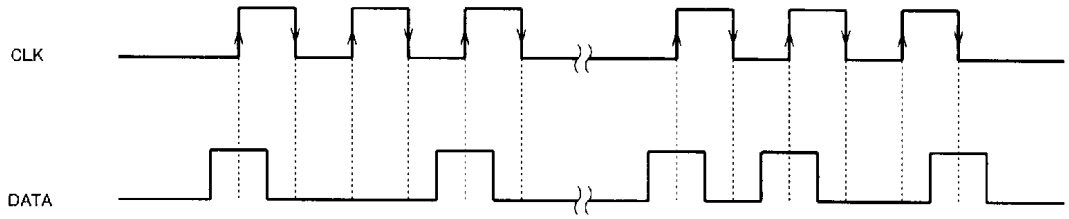
BLOCK DIAGRAM (M50253P)



BLOCK DIAGRAM (M50255P)



TIMING DIAGRAM



When CLK rises, the DATA is read.
When CLK falls and the DATA is "H," the contents of the shift register are transfered to the latch circuit.

ABSOLUTE MAXIMUM RATINGS

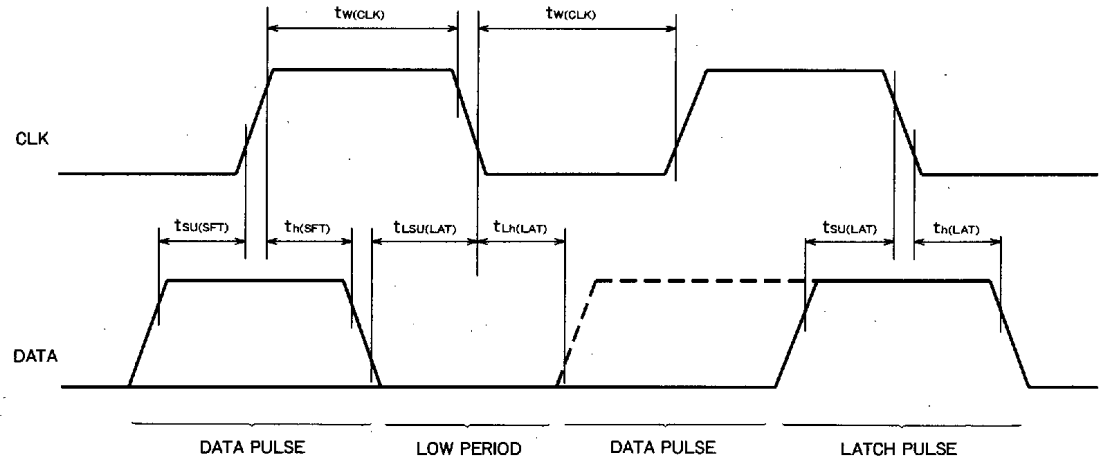
Symbol	Parameter	Ratings	Unit
V_{DD}-V_{SS}	Supply voltage	−0.3~7	V
V_I	Input voltage	$V_{SS}-0.3 \leqq V_I \leqq V_{DD}+0.3$	V
V_O	Output voltage	$V_{SS} \leqq V_O \leqq 13$	V
I_O	Output current	20	mA
Pd	Power dissipation	350	mW
Topr	Operating temperature	−20~70	℃
Tstg	Storage temperature	−40~125	℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply current	Input pin : V_{SS} or V_{DD} level Output pin : open			5	μA
I_{DD}	Supply current	f_{CLK} = 500kHz, DATA : V_{SS} or V_{DD} Output pin : open			5	mA
V_{OL}	"L" output voltage	I_{OL}=20mA			2	V
I_{OZH}	Off-state "H" output current	V_O =12V			12	μA
I_{OZL}	Off-state "L" output current	V_O =0V			−5	μA

Note : The sum of power dissipation should remain below 350 mW, the absolute maximum rating.

TIMING DIAGRAM



Note: Broken line shows DATA "High" before latch pulse.

TIMING REQUIREMENT

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{w\,(CLK)}$	CLK pulse width		500			ns
$t_{SU\,(SFT)}$	Data shift setup time		200			ns
$t_{h\,(SFT)}$	Data shift hold time		200			ns
$t_{SU\,(LAT)}$	Data latch setup time		50			ns
$t_{h\,(LAT)}$	Data latch hold time		250			ns
$t_{LSU\,(LAT)}$	Data latch low setup time		200			ns
$t_{Lh\,(LAT)}$	Data latch low hold time		250			ns