

CMOS QUAD LATCH

FEATURES

- ◆ Common Clock
- ◆ Positive- or Negative-Edge Clocking
- ◆ Q and \bar{Q} Outputs Available from Each Latch

DESCRIPTION

4042B devices contain four Latch circuits, each strobed by a common Clock. Complementary buffered outputs are available from each circuit.

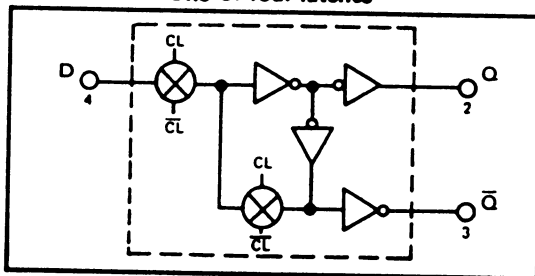
Information present at the Data input is transferred to outputs Q and \bar{Q} during the Clock level which is programmed by the Polarity input. For Polarity = 0 the transfer occurs during the 0 Clock level and for Polarity = 1 the transfer occurs during the 1 Clock level. The outputs follow the Data inputs providing the Clock and Polarity levels defined above are present. When a Clock transition occurs (positive for Polarity = 0 and negative for Polarity = 1) the information present at the input during the Clock transition is retained at the outputs until an opposite Clock transition occurs.

TRUTH TABLE

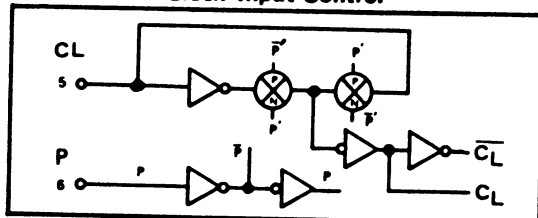
| CLOCK | POLARITY | Q |
|-------|----------|-------|
| 0 | 0 | D |
| | 0 | LATCH |
| 1 | 1 | D |
| | 1 | LATCH |

LOGIC DIAGRAMS

One of four latches

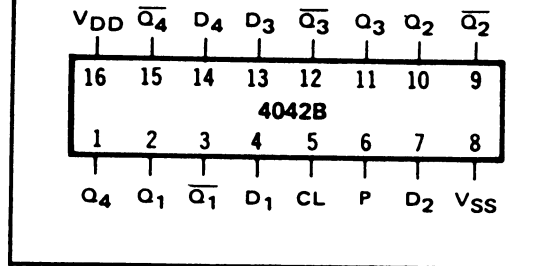


Clock Input Control



CONNECTION DIAGRAM

(all packages)



RECOMMENDED OPERATING CONDITIONS

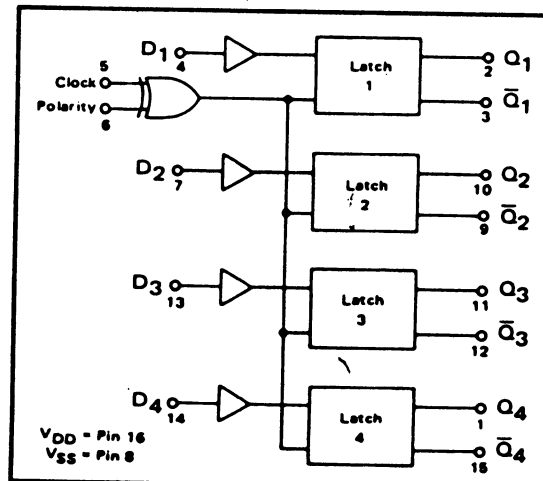
For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C -55 to +125 °C
E -40 to +85 °C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

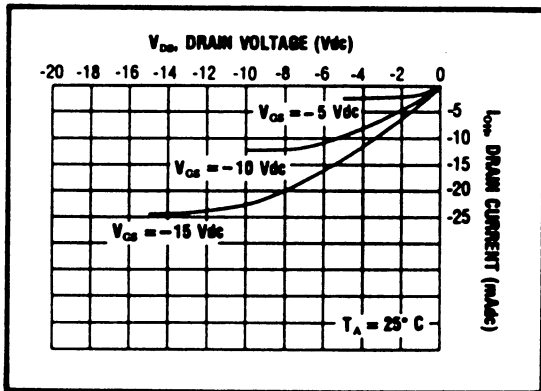
| PARAMETER | V _{DD} (Vdc) | CONDITIONS | T _{LOW} ² | | +25°C | | | T _{HIGH} ² | | Units |
|--------------------------|--------------------------|---|-------------------------------|------|-------|------|------|--------------------------------|------|-------|
| | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| QUIESCENT DEVICE CURRENT | I _{DD} | V _{IN} =V _{SS} or V _{DD} All valid input combinations | - | 5 | - | 1.0 | 5 | - | 150 | μAdc |
| | | | - | 10 | - | 2.0 | 10 | - | 300 | |
| | | | - | 15 | - | 4.0 | 20 | - | 600 | |

NOTES: ¹ Remaining Static Characteristics are listed under "4000B Series Family Specifications".

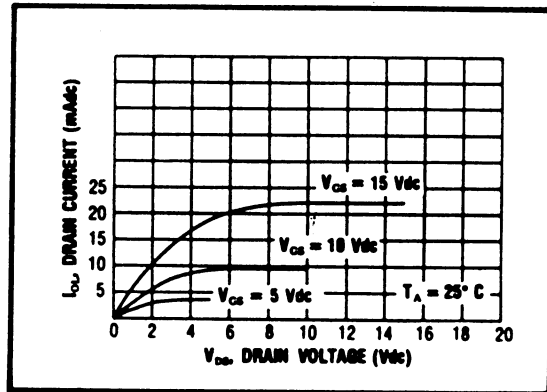
² T_{LOW} = -55°C for C
 = -40°C for E
 T_{HIGH} = +125°C for C
 = + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

| PARAMETER | | V _{DD} (Vdc) | Min. | Typ. | Max. | Units |
|--|-------------------------------------|--------------------------|------|------|------|-------|
| PROPAGATION DELAY TIME From Data Inputs | t _{PLH} , t _{PHL} | 5 | - | 110 | 220 | ns |
| | | 10 | - | 55 | 110 | |
| | | 15 | - | 40 | 80 | |
| From Clock Polarity Inputs | t _{PLH} , t _{PHL} | 5 | - | 150 | 300 | ns |
| | | 10 | - | 75 | 150 | |
| | | 15 | - | 50 | 100 | |
| OUTPUT TRANSITION TIME | t _{TLH} , t _{THL} | 5 | - | 100 | 200 | ns |
| | | 10 | - | 50 | 100 | |
| | | 15 | - | 40 | 80 | |
| MINIMUM CLOCK PULSE WIDTH | PW _{CL} | 5 | - | 100 | 200 | ns |
| | | 10 | - | 50 | 100 | |
| | | 15 | - | 30 | 60 | |
| MAXIMUM CLOCK RISE AND FALL TIME | t _{rCL} , t _{fCL} | 5 | 15 | - | - | μs |
| | | 10 | 5 | - | - | |
| | | 15 | 3 | - | - | |
| MINIMUM DATA INPUT SETUP TIME | t _{setup} | 5 | - | -20 | 50 | ns |
| | | 10 | - | -10 | 30 | |
| | | 15 | - | -5 | 25 | |
| MINIMUM DATA INPUT HOLD TIME | t _{hold} | 5 | - | 0 | 100 | ns |
| | | 10 | - | 0 | 50 | |
| | | 15 | - | 0 | 40 | |



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics