SM5840A/B

For Digital Audio Multi-function Digital Filter

77 ■ OVERVIEW

The SM5840 is a digital oversampling filter fabricated using NPC's proprietary Molybdenum gate CMOS technology. It is designed for use in digital audio playback systems, and supports 32.0, 44.1 and 48.0 kHz input sample rates and four- or eight-times oversampling. In addition to the oversampling filters, the SM5840 also incorporates digital de-emphasis, attenuation and soft mute functions for improved system performance and simpler design. Input and output data are in 2's complement, MSB-first, bit-serial form. The input data word length is 16 bits, and the output data word length is 16, 18 or 20 bits selectable. A separate serial interface is used to set the mode control flags and the attenuation coefficient. The SM5840 can operate from a standard 5 V supply or from a low-voltage supply with a rating as low as 3.2 V. It is available in 18-pin plastic DIPs and 22-pin SOPs.

■ FEATURES

- Selectable 4- or 8-times oversampling
- Three-stage stereo digital oversampling filter consisting of 69-, 13-, and 9-tap FIR filters
- First-order noise shaper
- Selectable attenuation, digital de-emphasis, and soft mute functions
- 19 bit × 14 bit multiplier with 24-bit accumulation
- IIS bus compatible input
- TTL-compatible inputs and outputs
- 0.8% DC offset (SM5840B only)
- Low voltage operation
- Molybdenum gate CMOS process

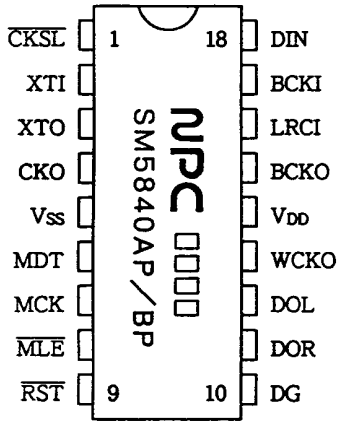
■ APPLICATIONS

- CD playback systems
- DAT playback systems
- PCM playback systems

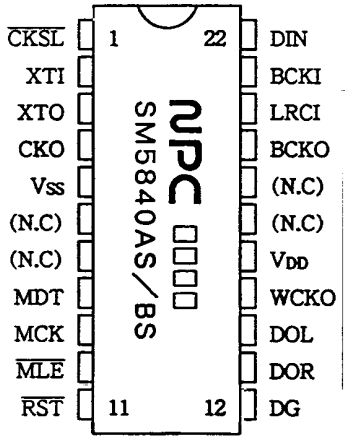
■ PIN CONFIGURATION

TOP VIEW

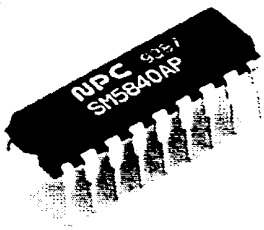
• 18 pin DIP



• 22 pin SOP



• 18 pin DIP



• 22 pin SOP

■ FILTER CHARACTERSTICS

SM5840A 4-times interpolation filter

Parameter	Value
Passband	0～0.4535fs
Stopband	0.5465～3.4535fs
Passband ripple	0.125 ± 0.03dB
Stopband attenuation	Greater than 55 dB
Group delay time	Constant

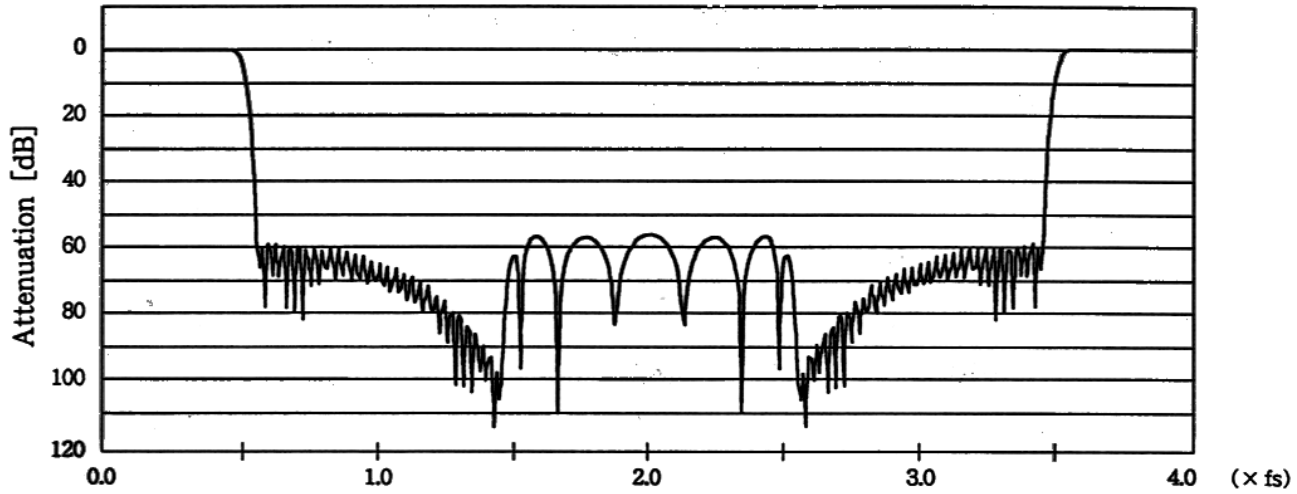


Fig. 1 SM5840A 4fs Frequency Characteristics

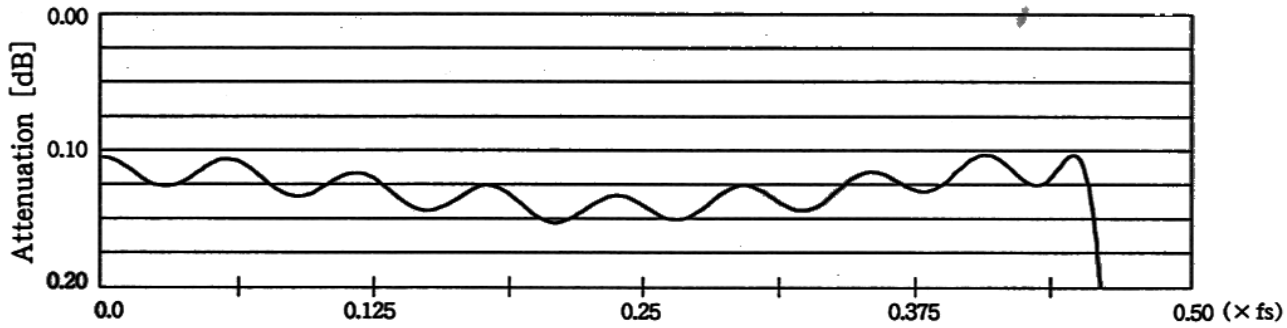
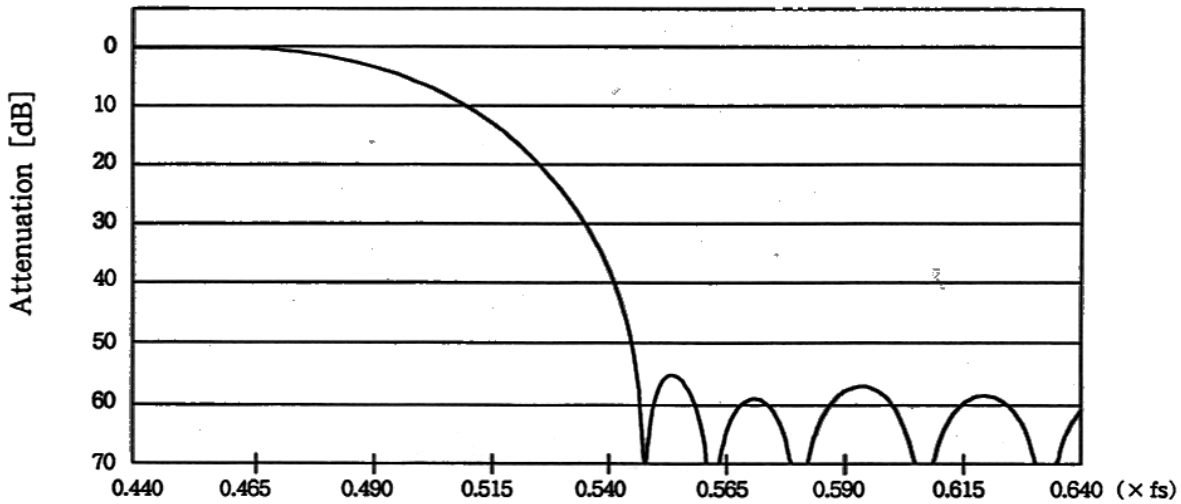


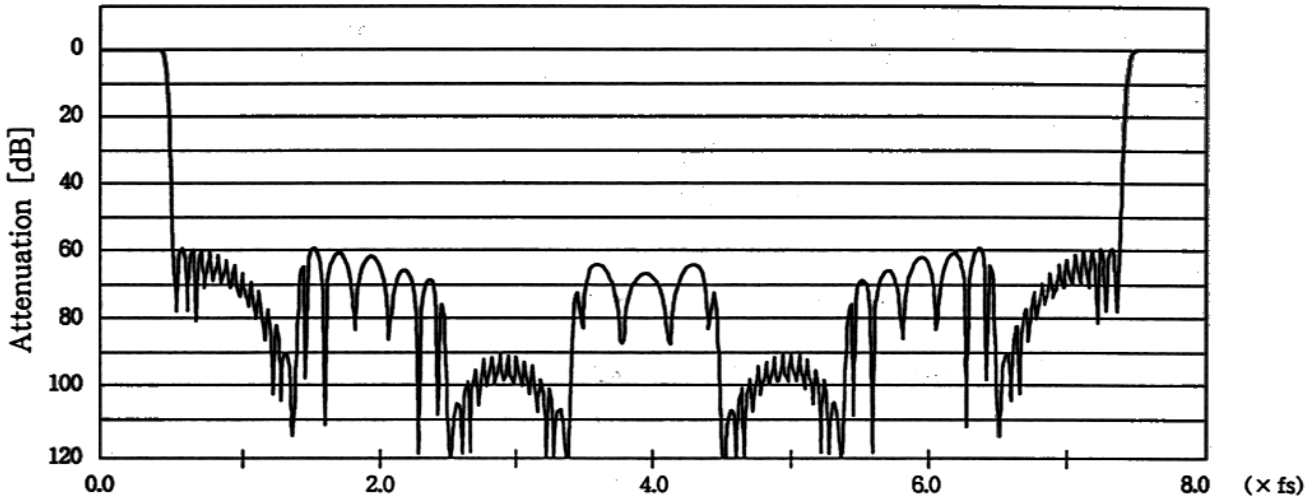
Fig. 2 SM5840A 4fs Passband Characteristics



3 SM5840A 4fs Transition Characteristics

SM5840A 8-times interpolation filter

Parameter	Value
Passband	0～0.4535fs
Stopband	0.5465～7.4535fs
Passband ripple	0.125 ± 0.03dB
Stopband attenuation	Greater than 55 dB
Group delay time	Constant



4 SM5840A 8fs Frequency Characteristics

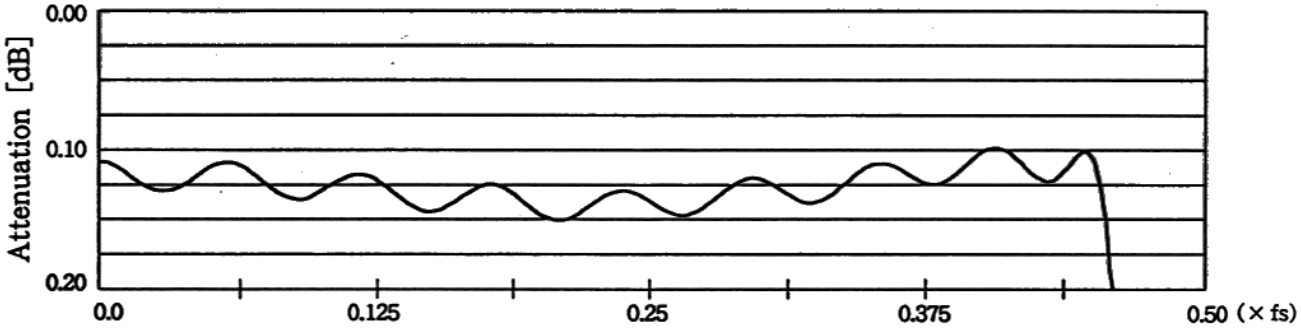
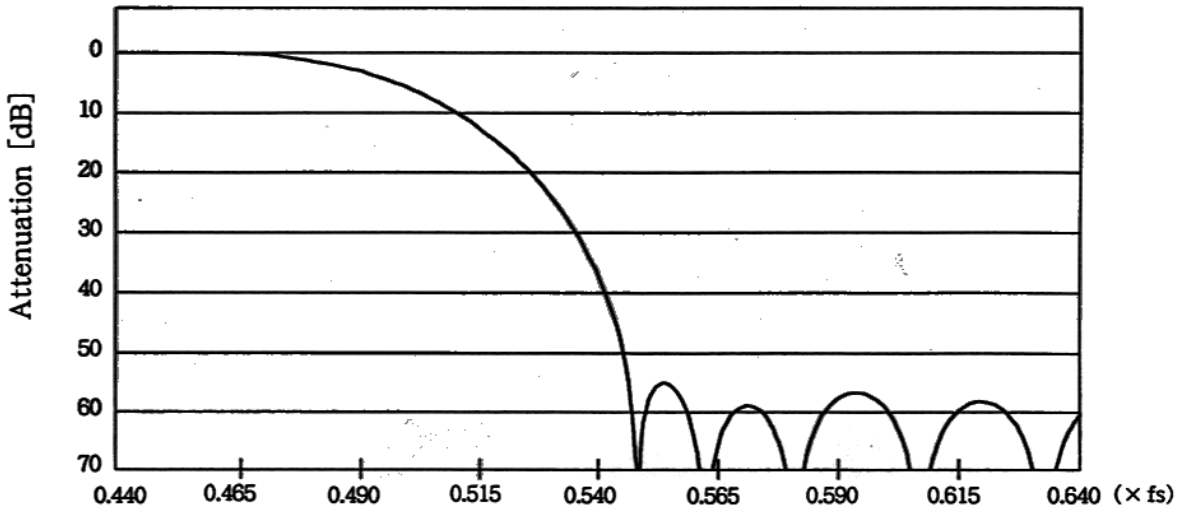


Fig. 5 SM5840A 8fs Passband Characteristics



6 SM5840A 8fs Transition Characteristics

SM5840B 4-times interpolation filter

Parameter	Value
Passband	0～0.4535fs
Stopband	0.5465～3.4535fs
Passband ripple	0.20 ± 0.03dB
Stopband attenuation	Greater than 55 dB
Group delay time	Constant

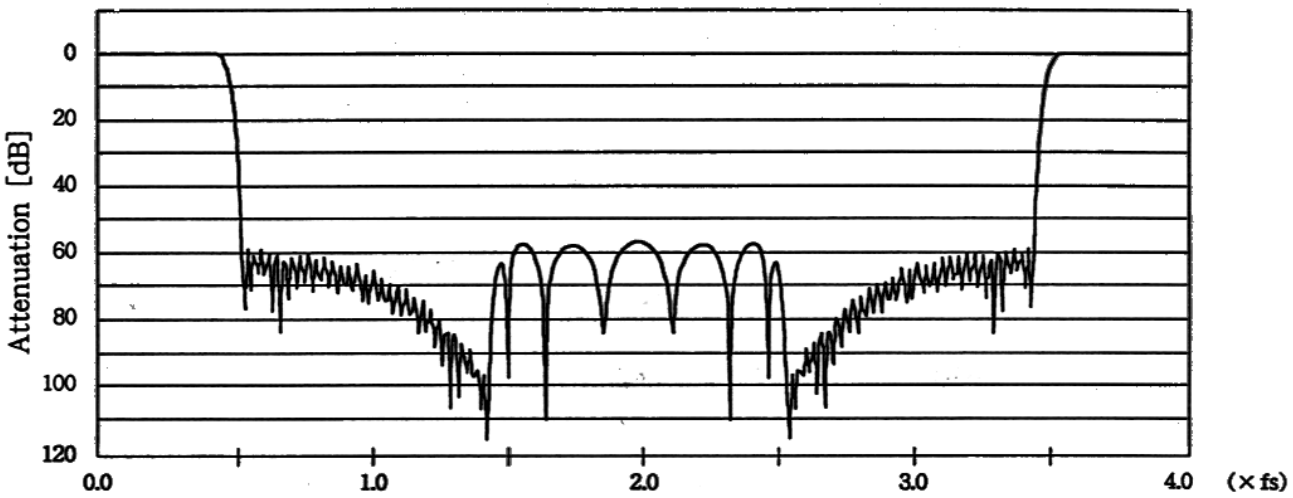


Fig. 7 SM5840B 4fs Frequency Characteristics

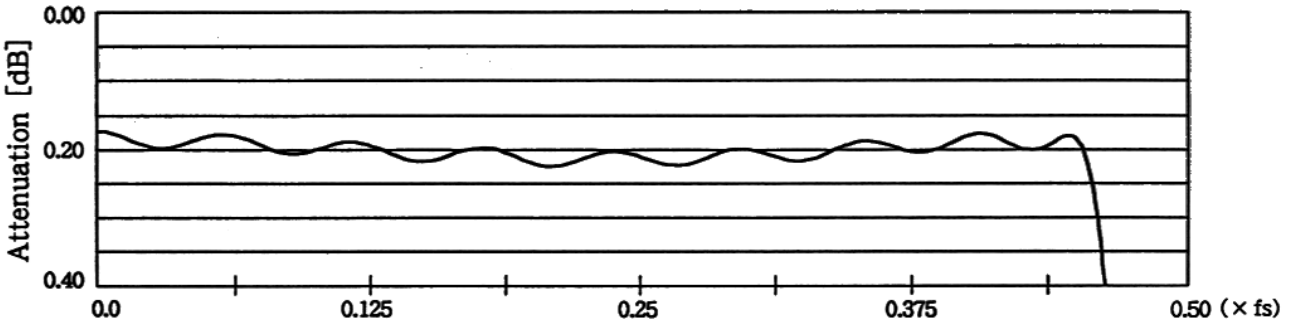


Fig. 8 SM5840B 4fs Passband Characteristics

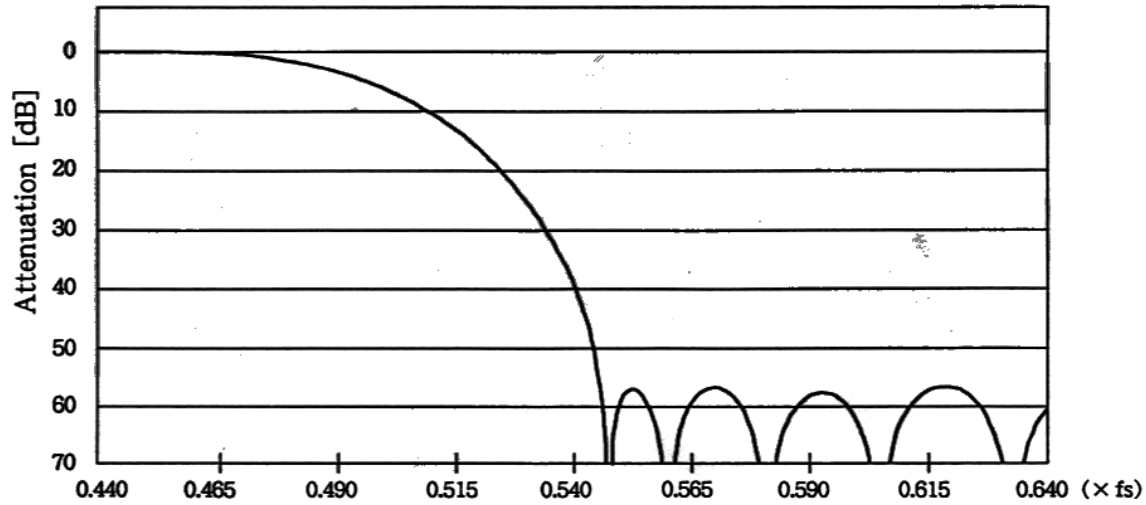


Fig. 9 SM5840B 4fs Transition Characteristics

SM5840B 8-times interpolation filter

Parameter	Value
Passband	0～0.4535fs
Stopband	0.5465～7.4535fs
Passband ripple	0.20 ± 0.03dB
Stopband attenuation	Greater than 55 dB
Group delay time	Constant

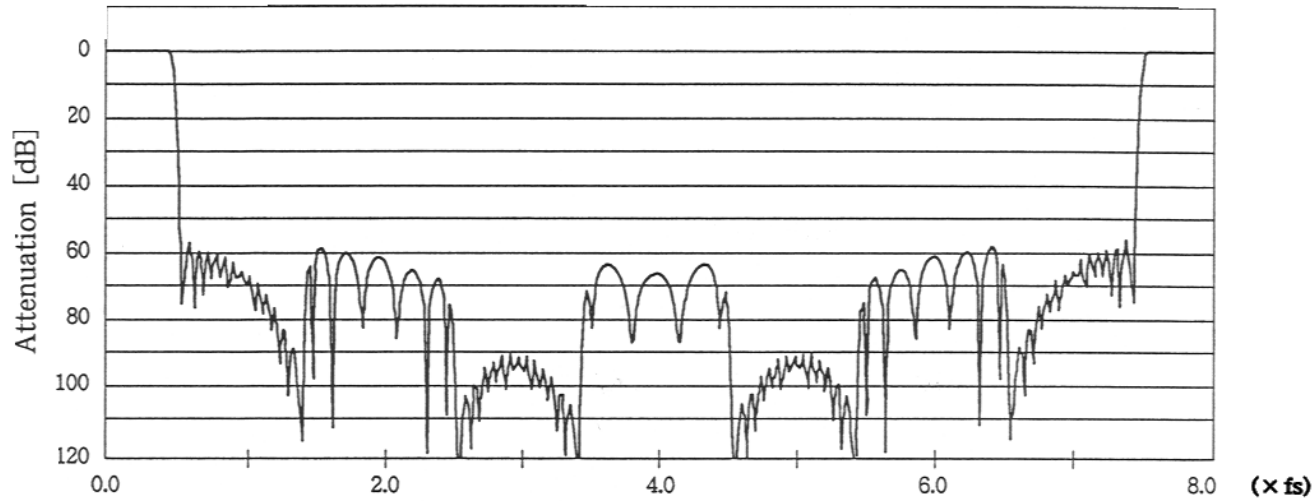


Fig. 10 SM5840B 8fs Frequency Characteristics

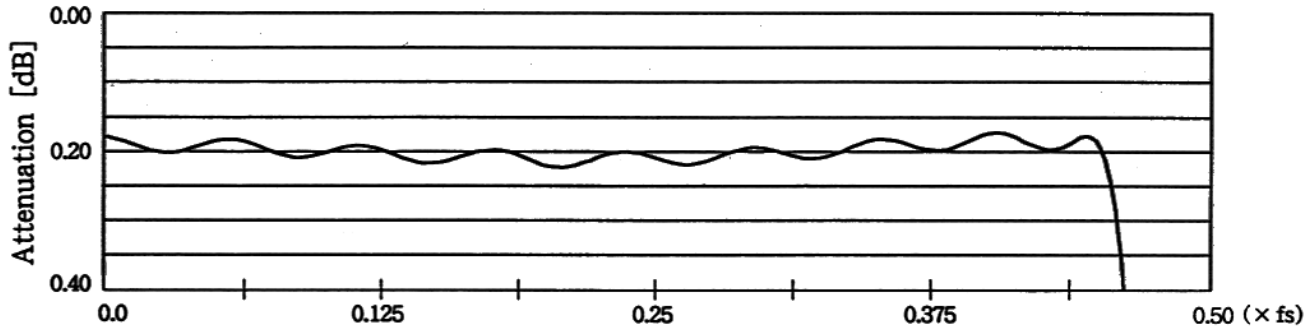


Fig. 11 SM5840B 8fs Passband Characteristics

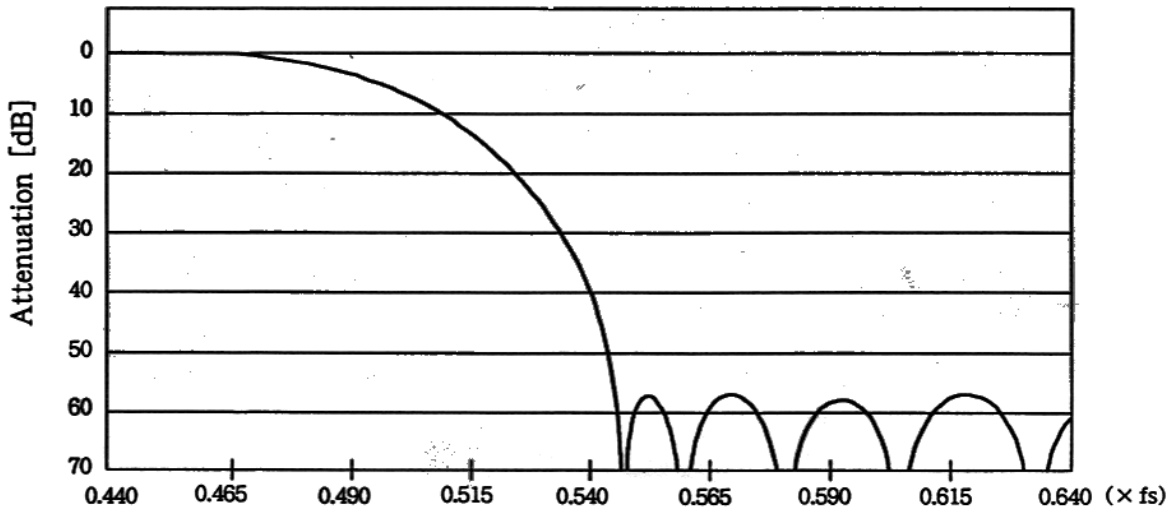


Fig. 12 SM5840B 8fs Transition Characteristics

De-emphasis Filter

Flags		Sample Frequency (fs) 32kHz: FSEL1 = H, FSEL2 = H	44.1kHz: FSEL1 = L, FSEL2 = L	48kHz: FSEL1 = L, FSEL2 = H
Passband (kHz)		0~14.5	0~20.0	0~21.7
Deviation from ideal characteristics	Attenuation	± 0.001dB		
	Phase (θ)	0~1.5°		

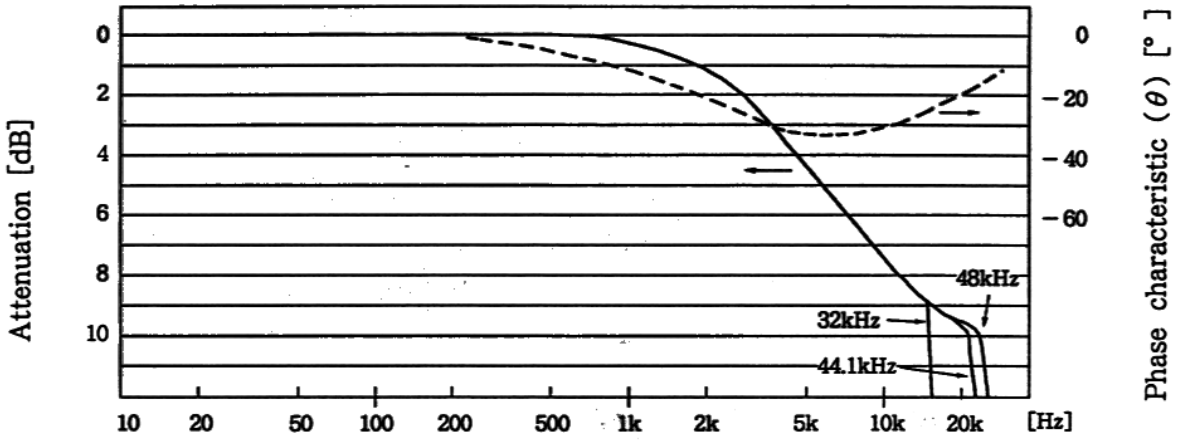


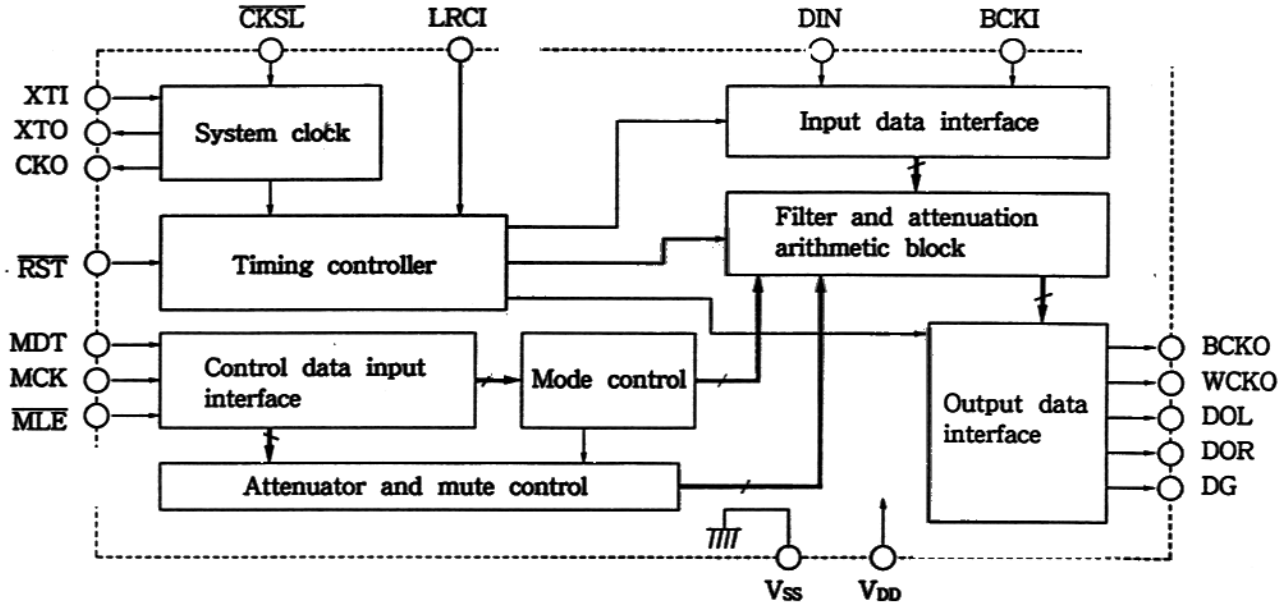
Fig. 13 Passband Characteristics with De-emphasis On

■ PIN DESCRIPTION

Pin Number DIP	Pin Number SOP	Pin Name	i/o	Description	
1	1	$\overline{CKSL}$	ip	Clock **frequency** **The clock frequency is 384fs if this pin is HIGH, and 256fs if it is LOW.**	
2	2	XTI	i	Crystal oscillator connection or external clock input	
3	3	XTO	o	Crystal oscillator connection	
4	4	CKO	o	Oscillator **output clock. The frequency at this pin is the same as the** frequency **on the XTI pin.**	
5	5	Vss	−	Ground	
−	6	NC	−		
−	7	NC	−		
6	8	MDT	ip	Mode set serial data input	These **signals are used to set the** mode **flags and the attenuator** register.
7	9	MCK	ip	Mode set bit clock	
8	10	$\overline{MLE}$	ip	Mode set latch enable	
9	11	$\overline{RST}$	ip	Device reset	
10	12	DG	o	Deglitch output	
11	13	DOR	o	8fs **LR-parallel output mode : right-channel data output** 4fs **LR-alternate output mode : left/right-channel clock output**	
12	14	DOL	o	8fs **LR-parallel output mode : left-channel data putput** 4fs **LR-alternate output mode : left/right-channel data output**	
13	15	WCKO	o	Output word clock	
14	16	V_{DD}	−	Positive supply (5 V standard)	
−	17	NC	−		
−	18	NC	−		
15	19	BCKO	o	Output data bit clock	
16	20	LRCI	ip	Input data word clock. LR input data multiplexed clock.	
17	21	BCKI	ip	Input data bit clock	
18	22	DIN	ip	Input data	

i : Input pin ip : Input pin with internal pull-up resistor o : Output pin

■ BLOCK DIAGRAM



■ Absolute Maximum Ratings

(Vss = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	− 0.3~7.0	V
Input voltage	V_{IN}	− 0.3~V_{DD} + 0.3	V
Storage temperature	T_{STG}	− 40~125	℃
Power dissipation	Pw	250	mW
Soldering	T_{SLD}	255	℃
Soldering time	t_{SLD}	10	sec

■ Recommended Operating Conditions

(Vss = 0V)

Parameter	Symbol	Condition	Unit
Supply voltage	V_{DD}	3.2~5.5	V
Operating temperature	T_{OPR}	− 20~80	℃

〈Pin〉

(＊1)	LRCI, DIN, BCKI, $\overline{CKSL}$, MDT, MCK, $\overline{MLE}$, $\overline{RST}$
(＊2)	CKO, DOL, DOR, BCKO, WCKO, DG

■ DC Characteristics

(Standard supply voltage operation : V_{DD} = 4.5~5.5V, Vss = 0V, Ta = − 20~80℃)

Parameter	Pin	Symbol	Condition	Rating MIN	Rating TYP	Rating MAX	Unit
Supply current	V_{DD}	I_{DD}	(Note. 1)			40	mA
Input voltage	XTI	V_{IH1}		0.7V_{DD}			V
		V_{IL1}				0.3V_{DD}	
	(＊1)	V_{IH2}		2.4			
		V_{IL2}				0.5	
Output voltage	(＊2)	V_{OH}	I_{OH} = − 0.4mA	2.5			V
		V_{OL}	I_{OL} = 1.6mA			0.4	
Input leak current	XTI	I_{LH}	V_{IN} = V_{DD}		10	20	μA
		I_{LL}	V_{IN} = 0V		10	20	
	(＊1)	I_{LH}	V_{IN} = V_{DD}			1.0	
Input current	(＊1)	I_{IL}	V_{IN} = 0V		10	20	μA

(Note. 1) V_{DD} = 5V, f_{SYS} = 256fs = 13MHz ($\overline{CKSL}$ = L), No load

(Low voltage operation : V_{DD} = 3.2~4.5V, Vss = 0V, Ta = − 20~80℃)

Parameter	Pin	Symbol	Condition	Rating MIN	Rating TYP	Rating MAX	Unit
Supply current	V_{DD}	I_{DD}	(Note. 2)			20	mA
Input voltage	XTI	V_{IH1}		0.7V_{DD}			V
		V_{IL1}				0.3V_{DD}	
	(＊1)	V_{IH2}		2.4			
		V_{IL2}				0.5	
Output voltage	(＊2)	V_{OH}	I_{OH} = − 0.2mA	2.5			V
		V_{OL}	I_{OL} = 0.8mA			0.4	
Input leak current	XTI	I_{LH}	V_{IN} = V_{DD}			10	μA
		I_{LL}	V_{IN} = 0V			10	
	(＊1)	I_{LH}	V_{IN} = V_{DD}			1.0	
Input current	(＊1)	I_{IL}	V_{IN} = 0V			10	μA

(Note. 2) V_{DD} = 3.4V, f_{SYS} = 256fs = 11.5MHz ($\overline{CKSL}$ = L), No load

■ AC Characteristics

1. XTI Pin

a. Crystal oscillator operation

($\overline{CKSL}$ = H : System clock = 384fs, V_{DD} = 3.2~5.5V, V_{SS} = 0V, Ta = − 20~80℃)

Parameter	Symbol	Power Supply Voltage		Rating			Unit
			V_{DD}	MIN	TYP	MAX	
Oscillator frequency	f_{MAX}	Standard	4.5~5.5V	2.0		20.0	MHz
		Low	3.2~4.5V	2.0		18.5	

($\overline{CKSL}$ = L : System clock = 256fs, V_{DD} = 3.4~5.5V, V_{SS} = 0V, Ta = − 20~80℃)

Parameter	Symbol	Power Supply Voltage		Rating			Unit
			V_{DD}	MIN	TYP	MAX	
Oscillator frequency	f_{MAX}	Standard	4.5~5.5V	1.0		13.0	MHz
		Low	3.4~4.5V	1.0		11.5	

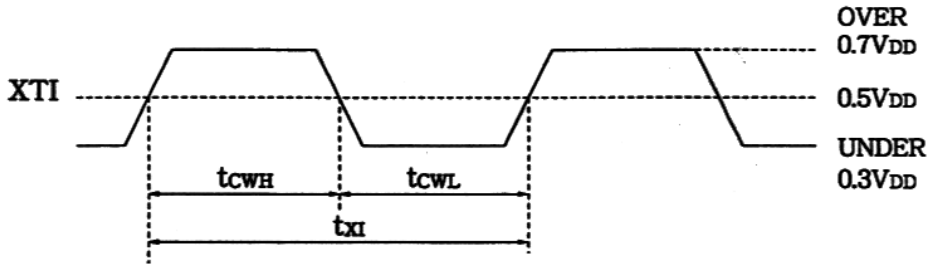
b. External clock input

($\overline{CKSL}$ = H : System clock = 384fs, V_{DD} = 3.2~5.5V, V_{SS} = 0V, Ta = − 20~80℃)

Parameter	Symbol	Power Supply Voltage		Rating			Unit
			V_{DD}	MIN	TYP	MAX	
High-level clock pulsewidth	t_{CWH}	Standard	4.5~5.5V	23		250	ns
		Low	3.2~4.5V	25		250	
Low-level clock pulsewidth	t_{CWL}	Standard	4.5~5.5V	23		250	ns
		Low	3.2~4.5V	25		250	
Clock pulse period	t_{XI}	Standard	4.5~5.5V	50		500	ns
		Low	3.2~4.5V	54		500	

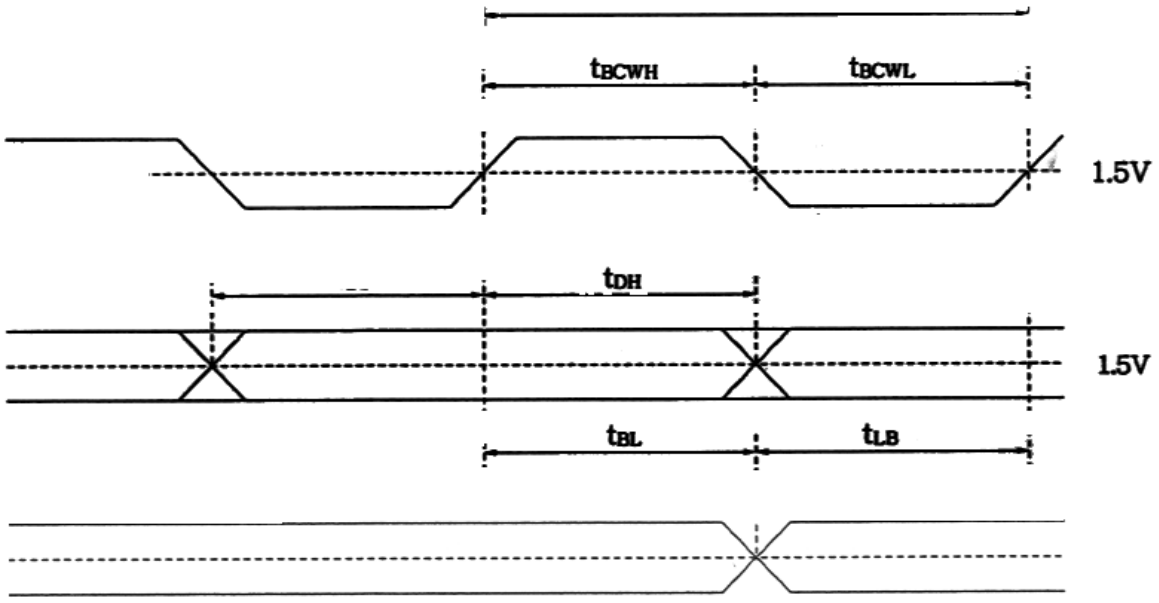
($\overline{CKSL}$ = L : System clock = 256fs, V_{DD} = 3.4~5.5V, V_{SS} = 0V, Ta = − 20~80℃)

Parameter	Symbol	Power Supply Voltage		Rating			Unit
			V_{DD}	MIN	TYP	MAX	
High-level clock pulsewidth	t_{CWH}	Standard	4.5~5.5V	35		500	ns
		Low	3.4~4.5V	38		500	
Low-level clock pulsewidth	t_{CWL}	Standard	4.5~5.5V	35		500	ns
		Low	3.4~4.5V	38		500	
Clock pulse period	t_{XI}	Standard	4.5~5.5V	76		1000	ns
		Low	3.4~4.5V	86		1000	



2. Audio data input timing
BCKI, DIN, LRCI Pin
(V_{DD} = 3.2~5.5V, V_{SS} = 0V, Ta = − 20~80℃)

Parameter	Symbol	Rating			Unit
		MIN	TYP	MAX	
High-level BCKI pulsewidth	t_{BCWH}	50			ns
Low-level BCKI pulsewidth	t_{BCWL}	50			ns
BCKI period	t_{BCY}	100			ns
DIN setup time	t_{DS}	50			ns
DIN hold time	t_{DH}	50			ns
BCKI rising edge to LRCI edge	t_{BL}	50			ns
LRCI edge to BCKI rising edge	t_{LB}	50			ns



b. MDT, MCK, $\overline{MLE}$ Pin

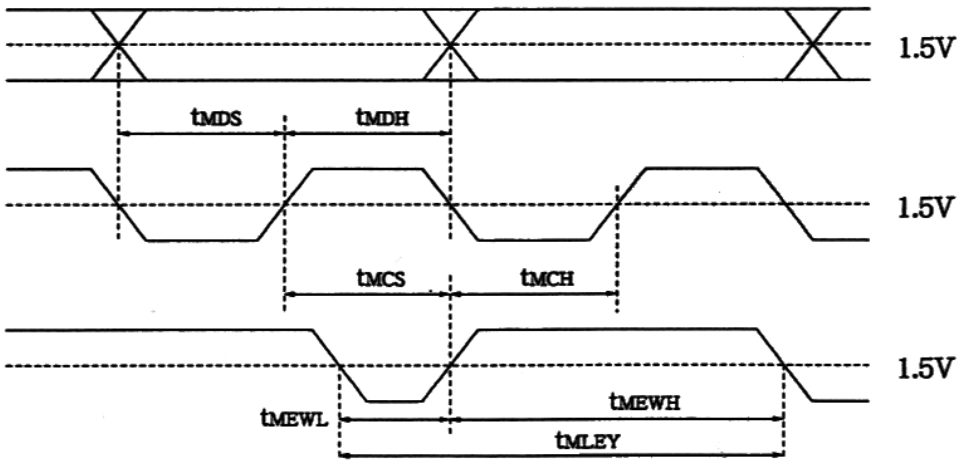
(Standard supply voltage operation : V_{DD} = 4.5~5.5V, V_{SS} = 0V, Ta = − 20~80℃)

Prameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
MDT setup time		tMDS	20			ns
MDT hold time		tMDH	20			ns
$\overline{MLE}$	Setup time	tMCS	40			ns
	Hold time	tMCH	20			ns
	Low-level time	tMEWL	20			ns
	High-level time	tMEWH	20			ns
	Pulse interval	tMLEY	6			TSYS

(Low voltage operation : V_{DD} = 3.2~4.5V, V_{SS} = 0V, Ta = − 20~80℃)

Prameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
MDT setup time		tMDS	40			ns
MDT hold time		tMDH	40			ns
$\overline{MLE}$	Setup time	tMCS	60			ns
	Hold time	tMCH	40			ns
	Low-level time	tMEWL	40			ns
	High-level time	tMEWH	40			ns
	Pulse interval	tMLEY	6			TSYS

(* 1) TSYS is the system clock period : 1/384fs for $\overline{CKSL}$ = H, 1/256fs for $\overline{CKSL}$ = L.



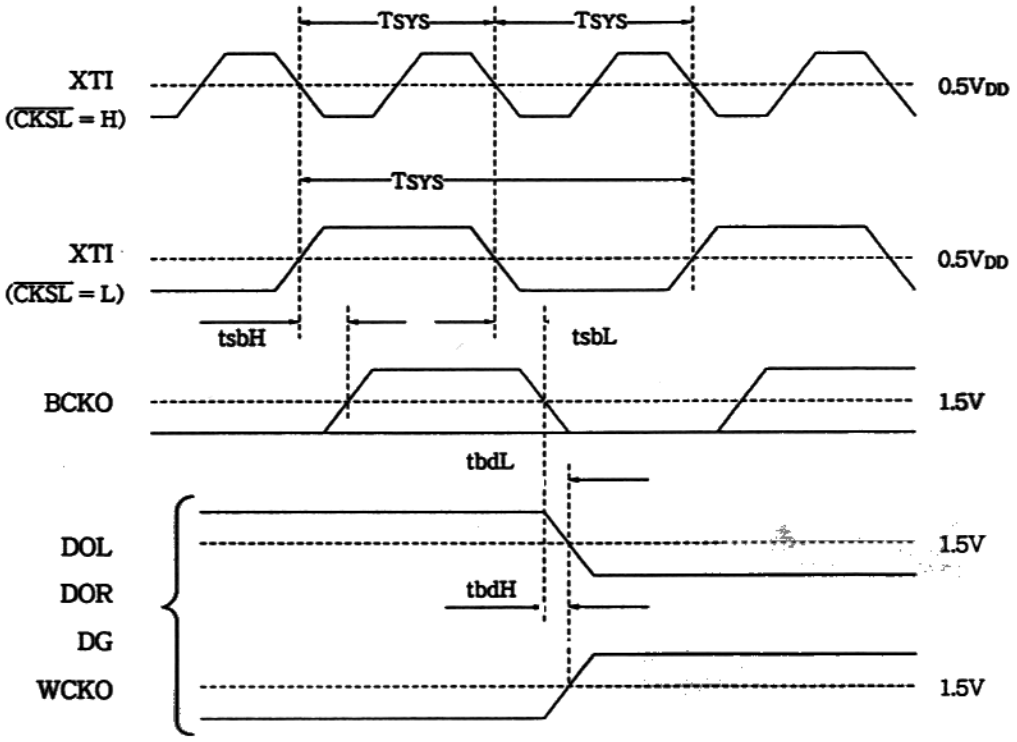
3. Output timing

(Standard supply operation : V_{DD} = 4.5~5.5V, V_{SS} = 0V, Ta = − 20~80℃)

Parameter	Timing	Symbol	Rating MIN	Rating TYP	Rating MAX	Unit	Load
XTO delay from XTI	XTI ↓→XTO ↑	t_{XTO}	3		20	ns	15pF
CKO delay from XTI	XTI ↓→CKO ↓	t_{CKO}	7		30	ns	
BCKO delay from XTI ($\overline{CKSL}$ = H)	XTI ↓→BCKO ↑	tsbH	10		60	ns	
	XTI ↓→BCKO ↓	tsbL	10		60		
BCKO delay from XTI ($\overline{CKSL}$ = L)	XTI ↑→BCKO ↑	tsbH	10		60	ns	
	XTI ↓→BCKO ↓	tsbL	10		60		
DOL, DOR, WCKO, DG delay from BCKO	BCKO ↓→OUT ↑	tbdH	0		20	ns	
	BCKO ↓→OUT ↓	tbdL	0		20		

(Low voltage operation : V_{DD} = 3.2~4.5V, V_{SS} = 0V, Ta = − 20~80℃)

Parameter	Timing	Symbol	Rating MIN	Rating TYP	Rating MAX	Unit	Load
XTO delay from XTI	XTI ↓→XTO ↑	t_{XTO}	3		30	ns	15pF
CKO delay from XTI	XTI ↓→CKO ↓	t_{CKO}	7		45	ns	
BCKO delay from XTI ($\overline{CKSL}$ = H)	XTI ↓→BCKO ↑	tsbH	10		100	ns	
	XTI ↓→BCKO ↓	tsbL	10		100		
BCKO delay from XTI ($\overline{CKSL}$ = L)	XTI ↑→BCKO ↑	tsbH	10		100	ns	
	XTI ↓→BCKO ↓	tsbL	10		100		
DOL, DOR, WCKO, DG delay from BCKO	BCKO ↓→OUT ↑	tbdH	0		30	ns	
	BCKO ↓→OUT ↓	tbdL	0		30		



■ FUNCTIONAL DESCRIPTION

The configuration of the SM5840 arithmetic block is shown in figure below.

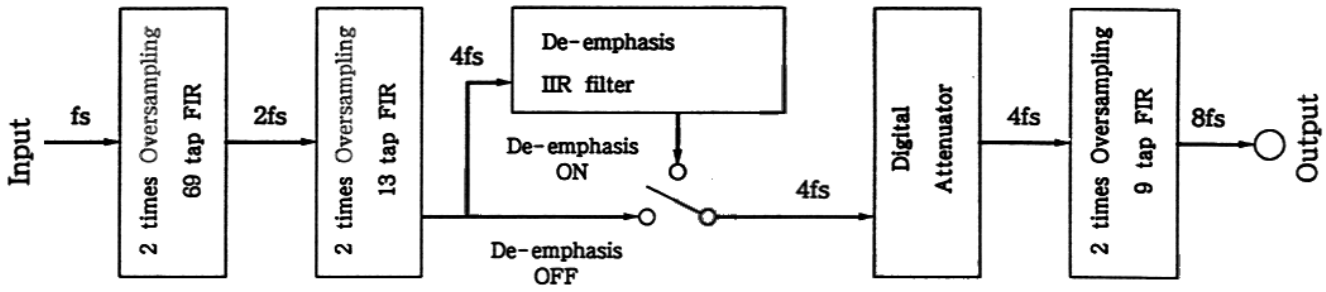


Fig. 14 Arithmetic Block Configuration

1. Oversampling

The SM5840 performs oversampling using a multi-stage FIR interpolation filter. Each filter stage interpolates the signal by a factor of two. The overall interpolation factor of the device is selectable to be either four or eight times the input sample rate. Alias and noise components are suppressed by the interpolation filter to below -55 dB in the stopband. Note that in 4-times oversampling the last filter is bypassed.

2. Digital De-emphasis

The de-emphasis filter is in cascade with the oversampling filters. It is implemented as an IIR filter, and faithfully reproduces the standard de-emphasis gain and phase characteristics. The de-emphasis filter is enabled by setting the DEEM flag and disabled by clearing it. Device reset resets the DEEM flag and selects the 44.1 kHz coefficients. The de-emphasis filter coefficients are selected by the FSEL1 and FSEL2 flags to match the currently selected operating sample rate, as shown below.

Flag	De-emphasis Filter Coefficients		
	fs = 32kHz	44.1kHz	48kHz
FSEL1	H	L	L
FSEL2	H	L	H

3. Digital Attenuator Setting

The attenuation applied to both audio channels is determined by an internal attenuation coefficient DATT. The attenuation is given by "Attenuation = 20×LOG10(1 - DATT/127) [dB]". When DATT = 0, no attenuation is applied. When DATT = 127, the attenuation is infinite and the output is muted. DATT is initialised to 0 by a device reset. The attenuation register is written using the MDT, MCK, and $\overline{\text{MLE}}$ pins, as in the case of the mode flag input. See figure below.

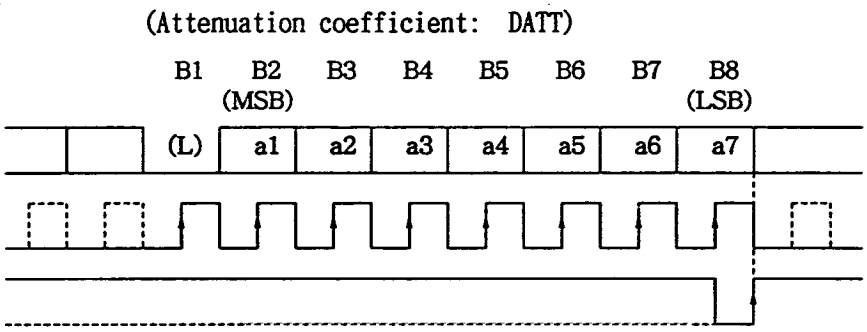


Fig. 15 Setting Attenuation Data

The first bit must be LOW to indicate attenuation data input. The remaining 7 bits define the new value of the attenuation register. The attenuation can be changed by writing a new value into the attenuation register. The attenuation coefficient ramps toward the new value and stops when this value is reached. This is shown in figure below. A new value can be written to the attenuation register before the attenuation coefficients as reached the previously written value. The resulting transition is shown between settings 4 and 5 in the below figure.

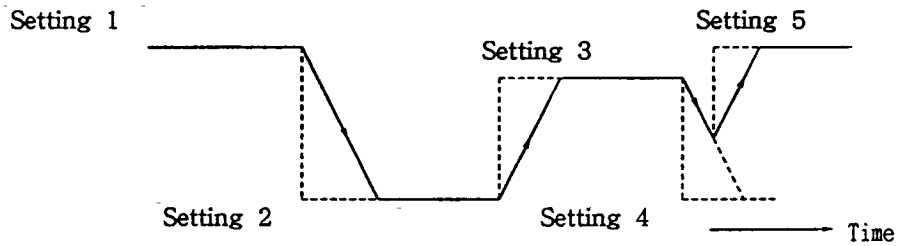


Fig. 16 Attenuation Level Transitions Setting

4. Soft Mute

The output of the SM5840 can be muted by setting the MUTE flag. When set, the attenuation coefficient ramps to a value of 127, smoothly increasing attenuation to infinity. When the MUTE flag is reset, the attenuation coefficient ramps back to the value in the attenuation register. The final attenuation will be either the attenuation before mute was applied, or a new value if the attenuation register was written while MUTE was set. The time taken to increase attenuation from zero to infinity is approximately 1024/fs. This corresponds to 23.2 ms for a 44.1 kHz input sample rate.

5. System Clock

The system clock can be selected to be either 256 or 384 times the input sample rate. The clock signal can be supplied by the internal oscillator circuit by connecting a crystal between pins XTI and XTO, or an external clock signal can be input on pin XTI. The system clock is output on CKO for use by other devices. Note that for a 384fs system clock, the output bit clock is 192fs, while it is 256fs if a 256fs system clock is selected. Clock selection is summarized in Tb.1.

Tb.1 System Clock Selection

CKSL		H	L
Input clock frequency	$f_{XI} = 1/t_{XI}$	384fs	256fs
CLOCK INPUT		External clock or X'tal osillatar	
Internal system clock period	T_{SYS}	$2 \times t_{XI}$	t_{XI}

t_{XI} is the period of the clock on pin XTI

6. Mode Flags

The mode flags control the operation of the SM5840. They are divided into two groups of six flags, with each group of flags input serially on the MDT pin as an 8-bit word. Mode flag input is indicated if the first bit of this word is HIGH. The second bit selects which group of six flags is to be written, and the remaining 6 bits are the values of the flags. Each bit is clocked into the input shift register by the rising edge of MCK. The contents of the shift register are latched into the internal mode register on the rising edge of MLE. Fig. 17 and Fig. 18 show the mode flag input timing. The dotted lines in the figures show allow able signal levels of MLE and MCK. Tb. 2 summarises the effects of all mode flags.

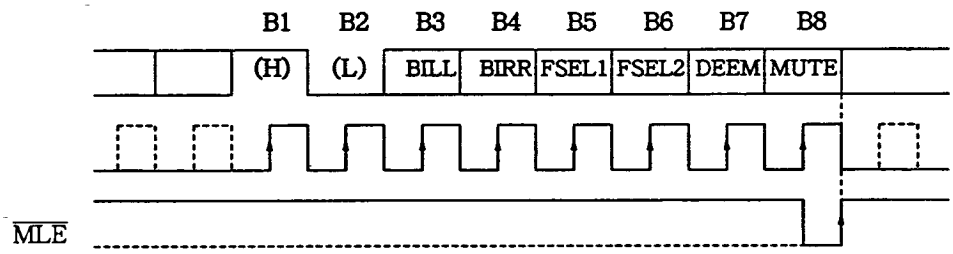


Fig. 17 Mode flag Timing 1

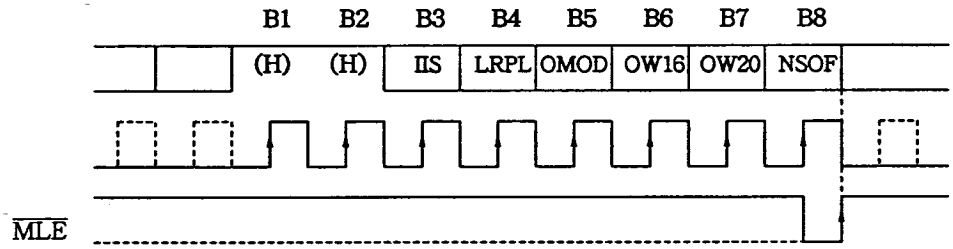


Fig. 18 Mode flag Timing 2

Tb. 2 Mode flag summary

B1	B2	bit	Mode Flag	Mode select: Selected Item	LH	Select				Mode on Reset	Note
H	L	3	BILL	Output mode selection				BIRR		Stereo	Fig 17
								L	H		
		4	BIRR			BILL	L	Stereo	RR		
							H	LL	Not used		
		5	FSEL1	De-emphasis filter sampling frequency				FSEL2		44.1kHz	
								L	H		
		6	FSEL2			FSEL1	L	44.1	48.0		
							H	Not used	32.0		
		7	DEEM	De-emphasis	L	De-emphasis off				○	
					H	De-emphasis on					
		8	MUTE	Mute	L	Mute off				○	
					H	Mute on					
H	H	3	IIS	Serial input format	L	Normal serial input				○	Fig 18
					H	IIS					
		4	LRPL	LRCI polarity	L	Lch/Rch = High/Low				○	
					H	Lch/Rch = Low/High					
		5	OMOD	Output mode	L	8fs LR-parallel				○	
					H	4fs LR-alternate					
		6	OW16	Output word length select				OW16		18 bits	
								L	H		
		7	OW20			OW20	L	18	16		
							H	20	Not used		
		8	NSOF	Noise shaper	L	Noise shaper on				○	
					H	Noise shaper off					

7. Audio Data Input

The bit-serial audio input data is in 16-bit, 2's complement, MSB-first format. If the IIS mode flag is set, IIS bus timing is selected, otherwise standard serial data timing is used. Input timing is shown in Fig. 19 and Fig. 20. The data is input on the DIN pin. Each bit is shifted into the input data shift register on the rising edge of the BCKI bit clock. The contents of the shift register are latched into the left- and right-channel input registers on alternate transitions of the word clock, LRCI. If the LRPL flag is set, data is latched into the left channel on the rising edge of LRCI, and into the right channel on the falling edge of LRCI. The reverse takes place if the LRPL flag is reset. LRPL is reset by a device reset. The timing of the input stage is independent of the timing of the arithmetic circuitry. Hence, the phase relationship between the BCKI and LRCI clocks and the system clock do not affect functional operation. But when the XTI or LRCI clock disturbs, this device must be reset.

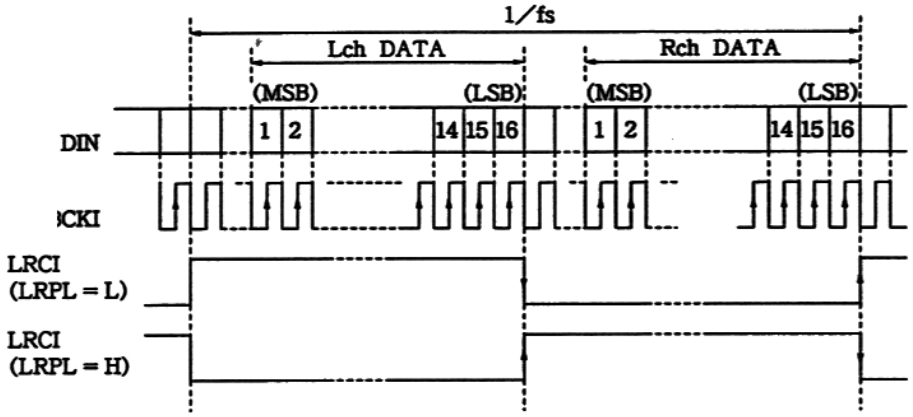


Fig. 19 Input Timing, Standard Format (IIS flag = L)

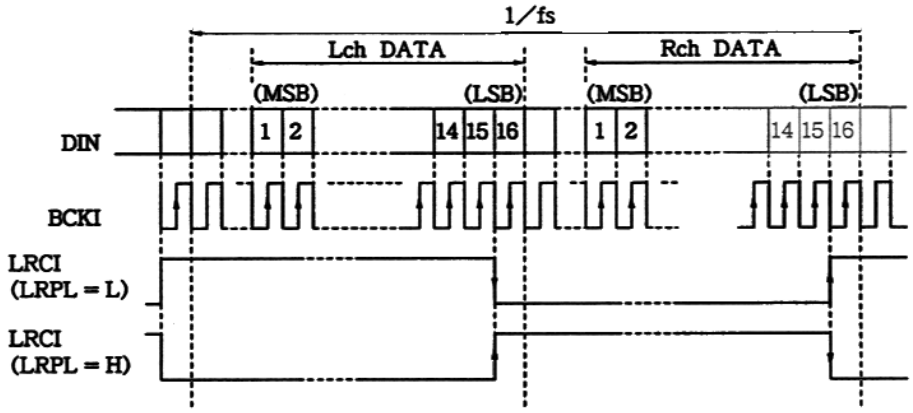


Fig. 20 Input Timing, IIS Format (IIS flag = H)

8. Data Output

The audio output data is in bit-serial, 2's complement, MSB-first format. The output word length is selected by the OW16 and OW20 flags, as shown below.

(1) The output word length is initialized to 18 bits by a device reset. Data can be output in one of two formats. 8fs LR-parallel format is selected if OMOD is reset, and 4fs LR-alternate format is selected if OMOD is set. In the 8fs LR-parallel format, left- and right-channel data is output on both the DOL and DOR output pins. In the 4fs LR-alternate format, left- and right-channel data is output alternately on the DOL output only. The 8fs LR-parallel format is selected by a system reset. The deglitch output signal goes LOW before the start of each word, and returns high 9 bit periods later. It is provided for use by the DAC output sample-and-hold circuits to latch the analog output signal. Figures C to F show the timing for the four combinations of output format and clock frequency. In all of these, clock pulses and data for bits 17 and 18, shown as dotted lines, are present in 18-bit output mode. Clock pulses and data for bits 17 to 20 are present in 20-bit output mode. The output bit clock frequency is 256fs if CKSL is LOW, and 192fs if CKSL is HIGH.

(2) DC Offset (SM5840B only)

In the SM5840B, a DC offset is added to the signal data before it is output. This reduces zero-crossing distortion for small input signals. The amount of DC offset is approximately 0.8 percent, and varies according to the output word length.

(3) Output Mode

Output mode is selected by the BILL and BIRR flags, as follows.

〔BILL = 0, BIRR = 0 Normal stereo mode〕 The left- and right-channel output signals correspond to the left- and right-channel input signals.

〔BILL = 1, BIRR = 0 Left-channel mono mode (LL)〕 Both left- and right-channels output data corresponds to the left-channel input signal.

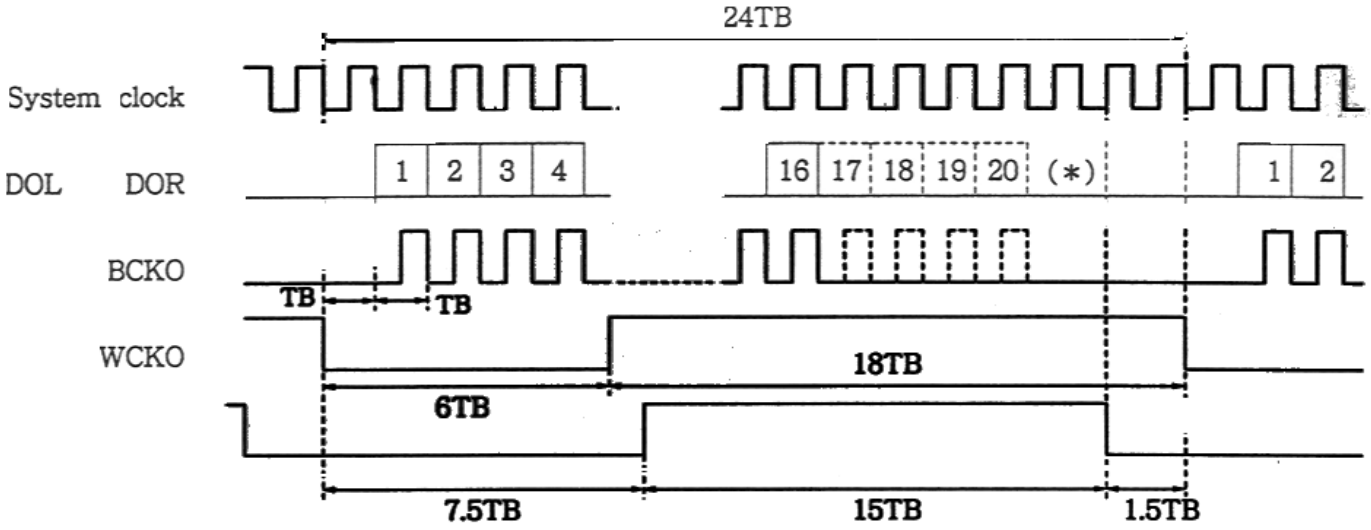
〔BILL = 0, BIRR =1 Right-channel mono mode (RR)〕 Both left- and right-channels output the data corresponding to the right-channel input signal.

The mono modes are designed for use in bilingual playback systems, where one input channel is sent to both output channels. Normal stereo mode is selected by a device reset.

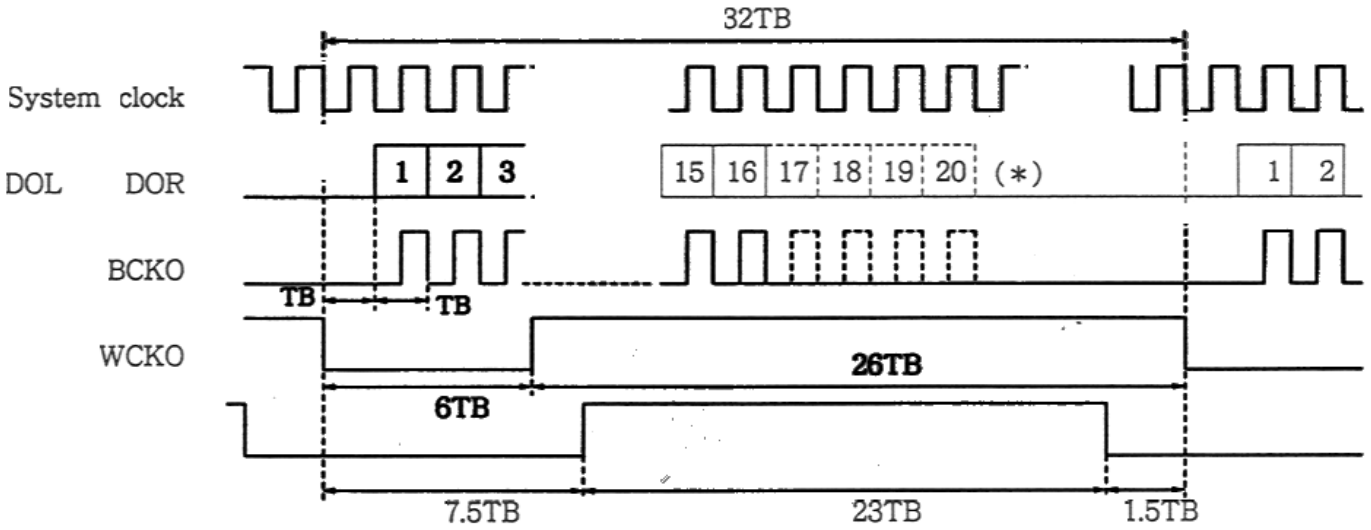
Tb. 3 Output timing

Parameter	Symbol	System clock	Output Mode	
			8fs LR-parallel output	4fs LR-alternate output
Output bit clock rate	TB	$\overline{CKSL}$ = H	1/192fs	1/192fs
		$\overline{CKSL}$ = L	1/256fs	1/256fs
Word length	TDW	$\overline{CKSL}$ = H	24Tsys (*1)	24Tsys
		$\overline{CKSL}$ = L	32Tsys	32Tsys

(*1) Tsys is system clock frequency.

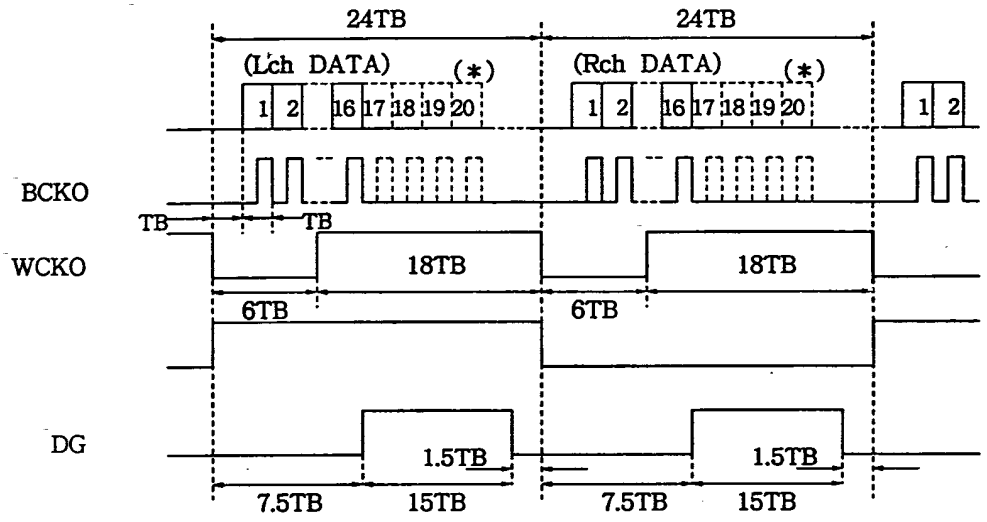


Flag. 8fs Output Timing (OMOD flag = L, $\overline{\text{CKSL}}$ = H)

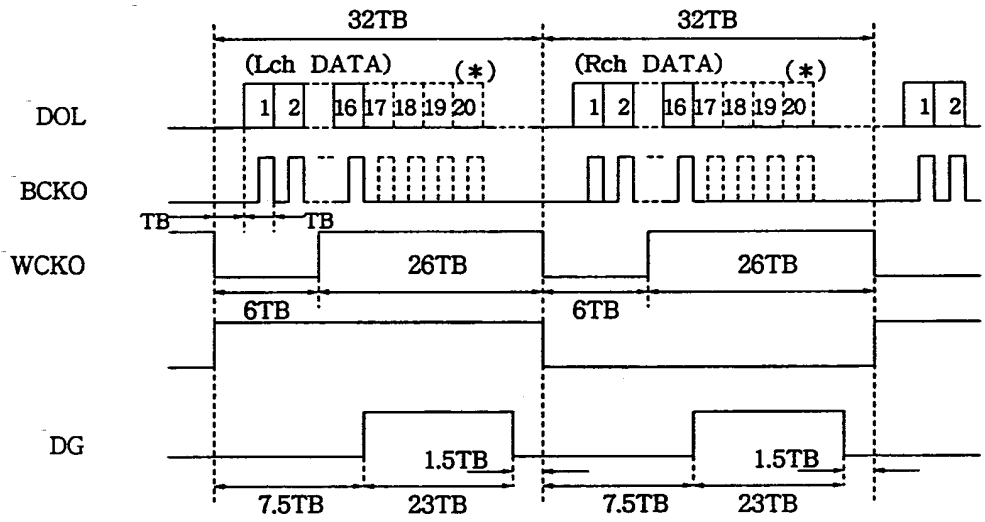


Flag. 8fs Output Timing (OMOD flag **L,** $\overline{\text{CKSL}}$ L)

(*) bit output mode the dotted lines.



Flag. 23 4fs Output Timing (OMOD flag = H, $\overline{CKSL}$ = H)



Flag. 24 4fs Output Timing (OMOD flag = H, $\overline{CKSL}$ = L)

(*) 18 or 20 bit output mode at the dotted lines.

9. DEVICE RESET

The SM5840 should be reset following power-on, switching $\overline{CKSL}$ and when input clocks are disturbed by applying a LOW-level pulse to the $\overline{RST}$ pin. A power-on reset can be effected either by a signal from the controlling micro processor, or by connecting a capacitor of approximately 300 pF between $\overline{RST}$ and VSS. The following events take place on the rising edge of $\overline{RST}$. All mode flags are reset to logic-0. The corresponding modes are shown in Tb. 2. The attenuator register is set to zero that is, no attenuation is applied to the signal. The timing circuitry is set so that arithmetic and output timing counters will be reset to zero on the next start edge of LRCI.

※The value of capacitance for power-on reset must be determined by depending on the time from the power on to the stability of input clocks.

■ TIMING CHART

1. Input timing (DIN, BCKI, LRCI)

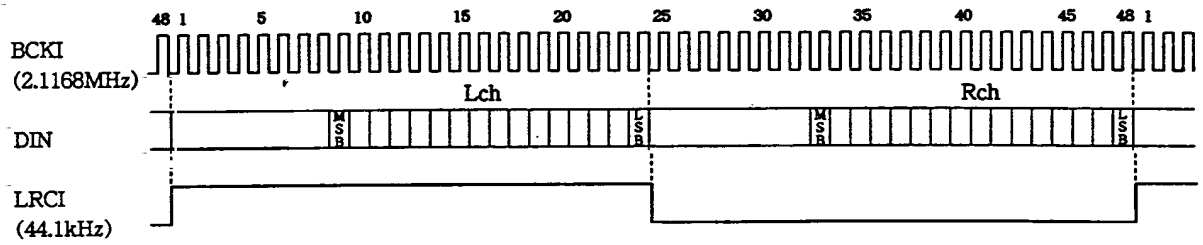


Fig. A Example 1 (IIS flag = L, LRPL flag = L)

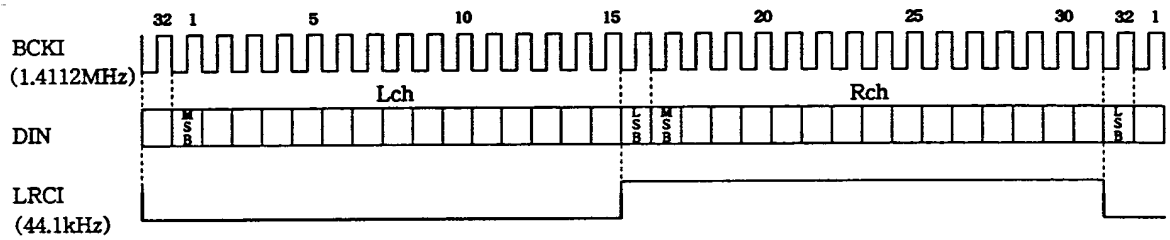


Fig. B Example 2 (IIS flag = H, LRPL flag = H)

2. Output timing (DOL, DOR, BCKO, WCKO, DG) (*) The number of bits in the DOL, DOR and BCKO data and clock outputs depends on the output word length selected by the OW16 and OW20 flags.

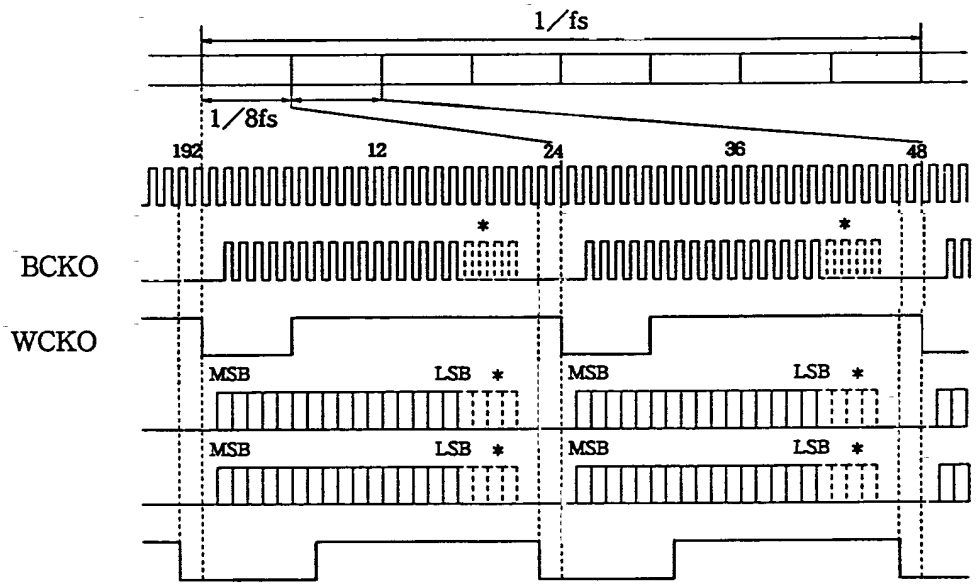


Fig. C Example 1 ($\overline{CKSL}$ = H, OMOD flag = L)

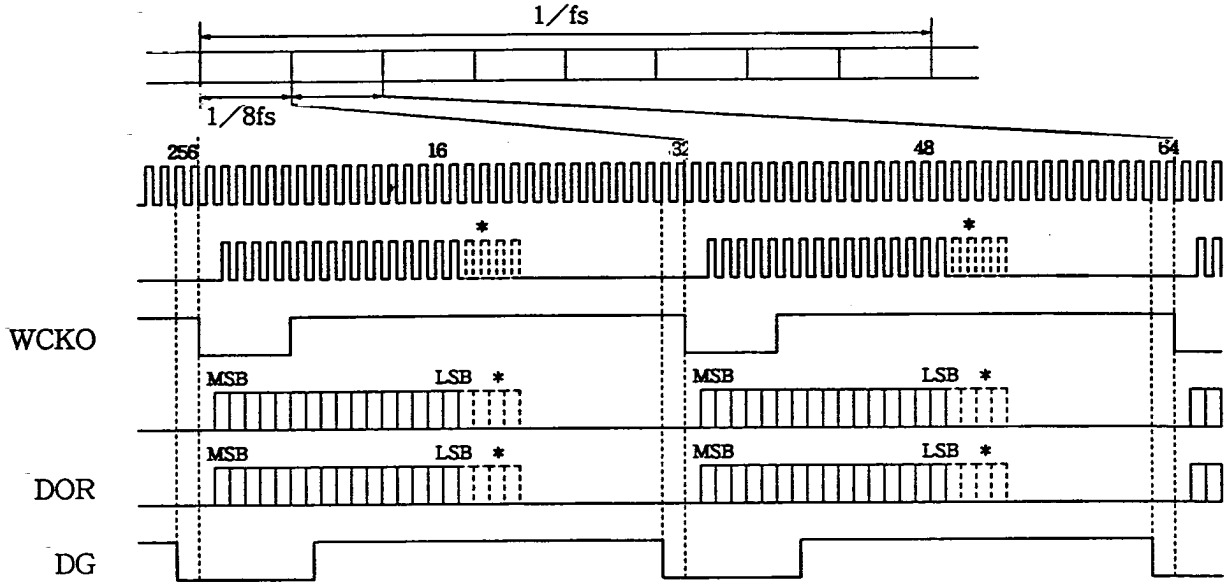


Fig. D Example 2 ($\overline{CKSL}$ = L, OMOD flag = L)

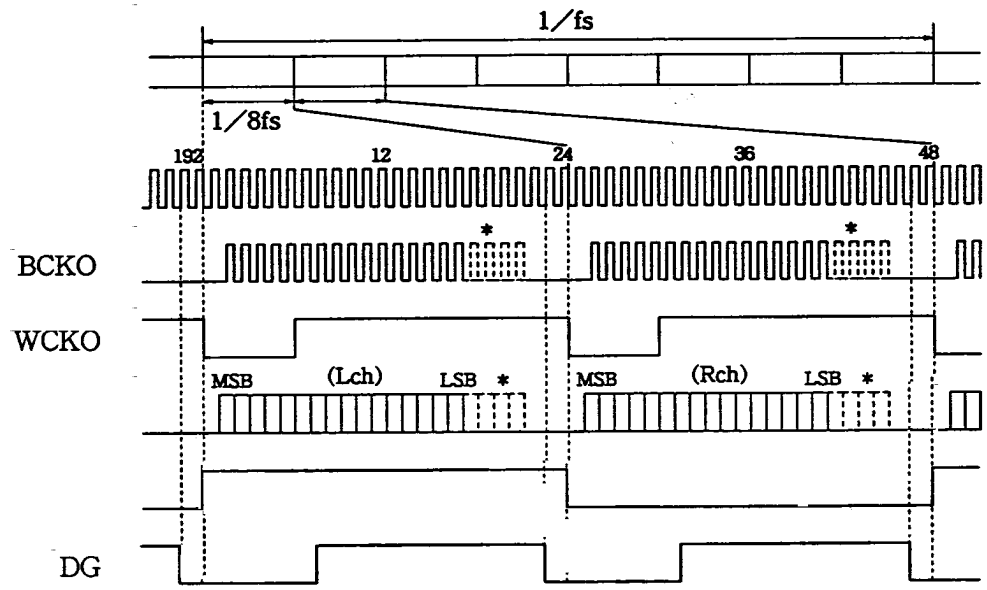


Fig. E Example 3 ($\overline{CKSL}$ H, OMOD flag = H)

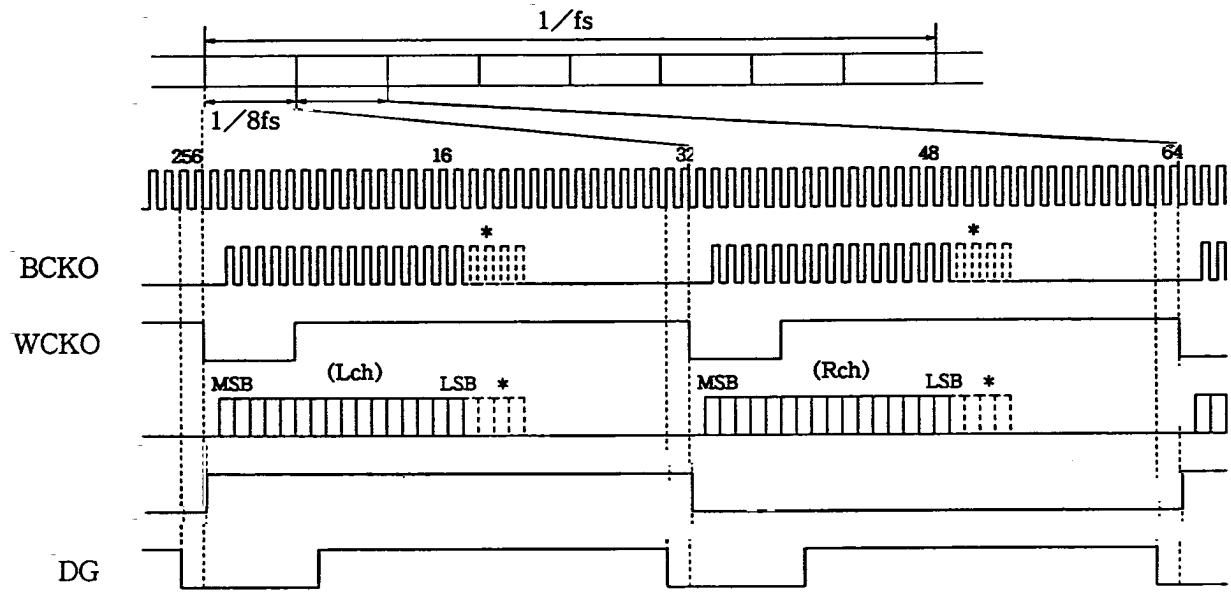
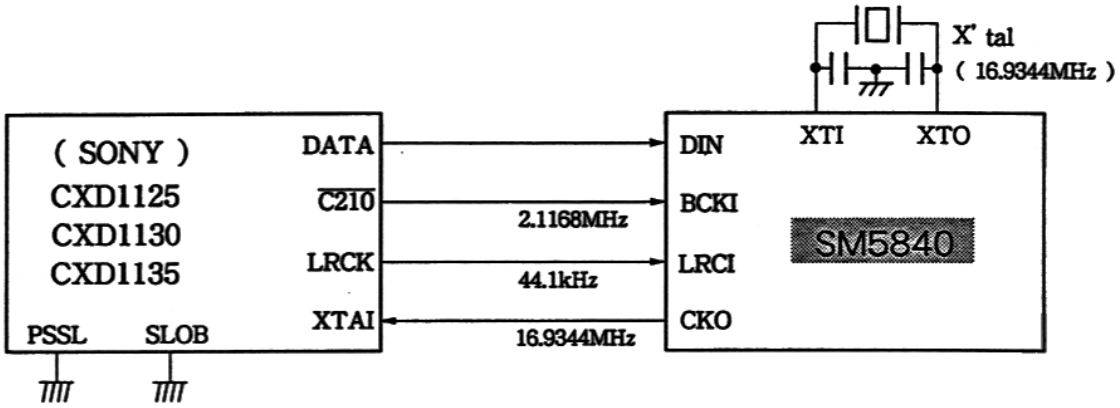
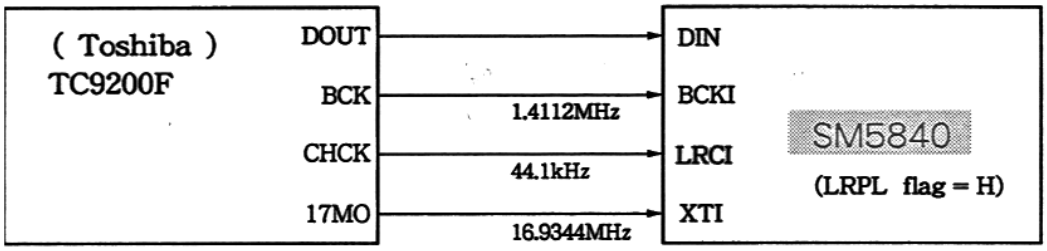


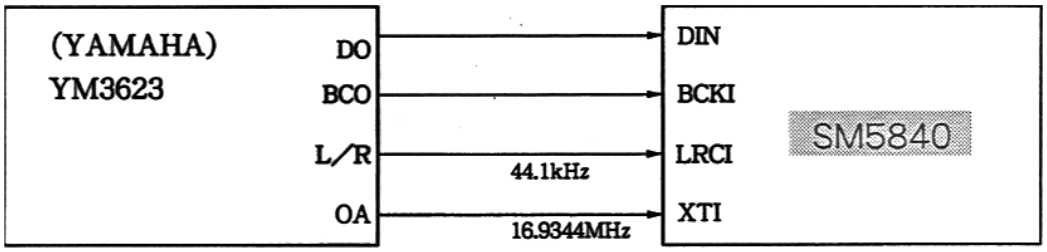
Fig. F Example 4 ($\overline{CKSL}$ = L, OMOD falg = H)

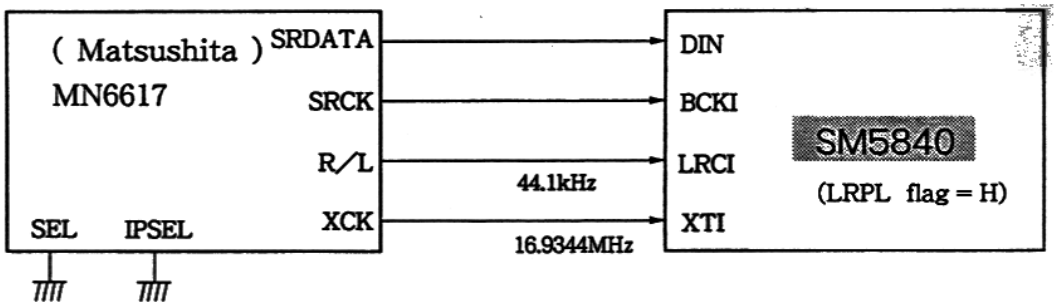
■ APPLICATION CIRCUITS (These circuits show signal interconnection only. Timing relationships should also be taken into consideration when designing a system.)

1. Input interface



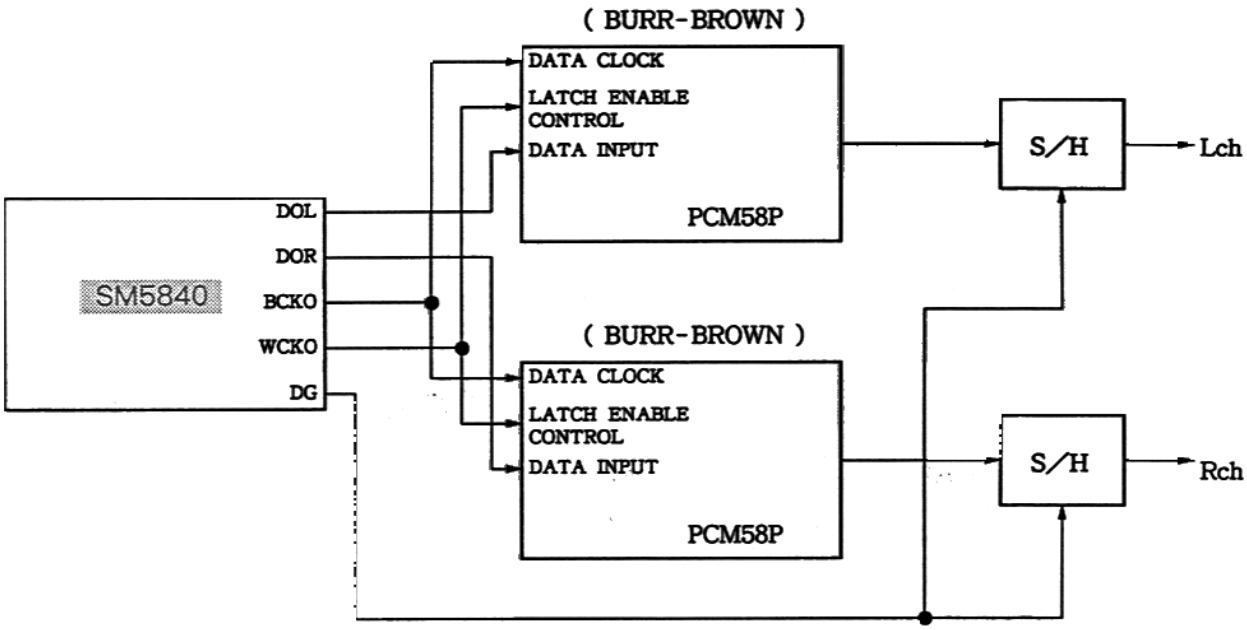






2. Output Interface

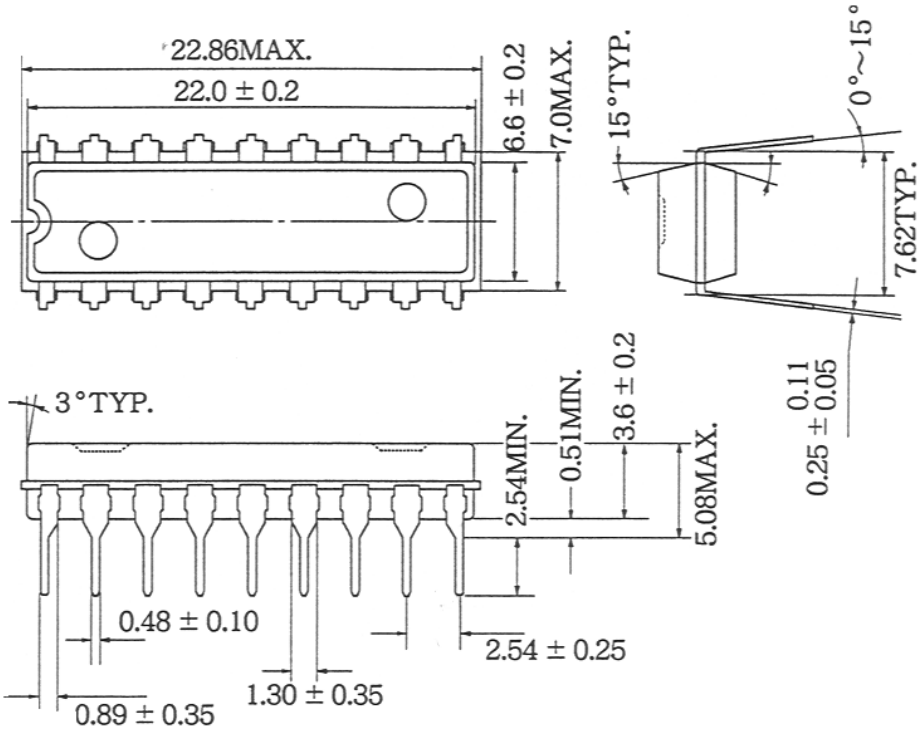
This circuit shows the SM5840 used in 18-bit 8fs LR-parallel output mode with two 18-bit DACs.



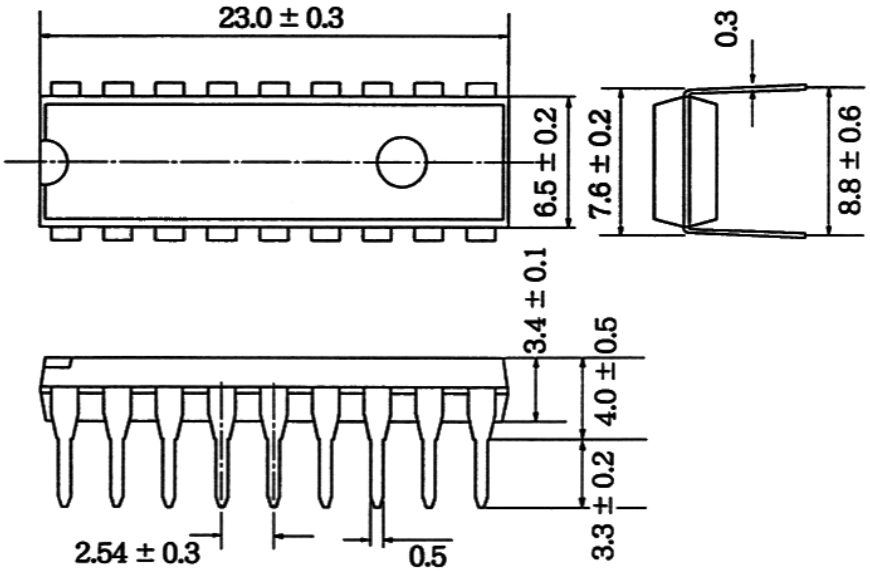
■PACKAGE DIMENSIONS

(Unit : mm)

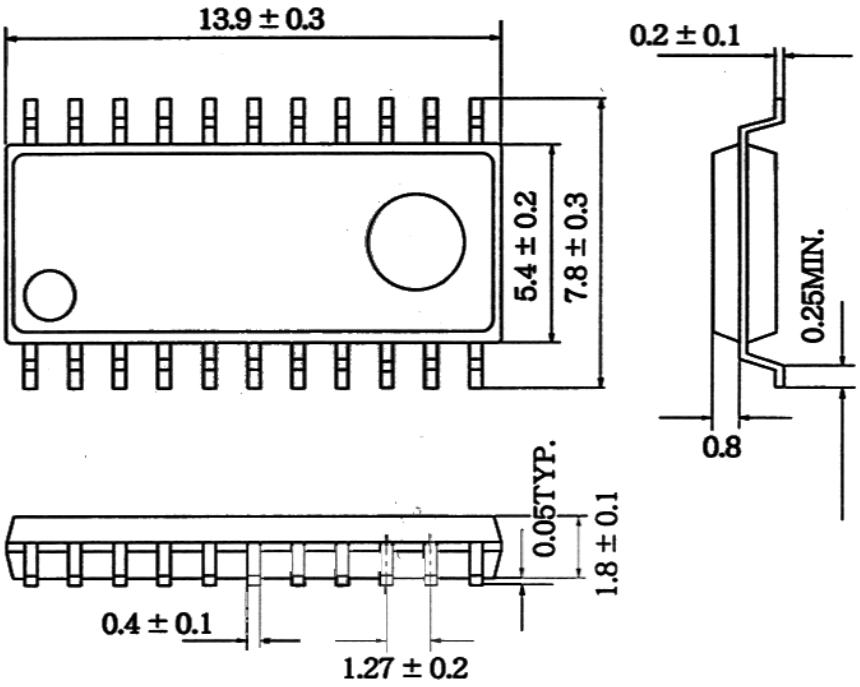
• 18 pin DIP 〈Type A〉



18 pin DIP 〈Type B〉



• 22 pin SOP



※ NOTE : 1. All specifications of this device subject to change without notice.
2. This data sheet does not provide a guarantee in relation to the implementation of industrial proprietary or any other rights.
3. If any questions about COCOM regulations, please contact us.

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