

## CMOS 4-BIT D-TYPE REGISTER

### FEATURES

- ◆ 3-State Outputs with Gated Control Lines
- ◆ Fully Independent Clock
- ◆ Asynchronous Reset
- ◆ Fully Static Operation - DC to 12MHz @ 10Vdc

### DESCRIPTION

The 4076B 4-bit Register consists of four D-Type flip-flops operating synchronously from a common Clock. OR-gated Output Disable inputs force the outputs into a high-impedance state for use in bus-organized systems. OR-gated Data Disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus, they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous Master Reset is provided to clear all four flip-flops simultaneously independent of the Clock or Disable inputs.

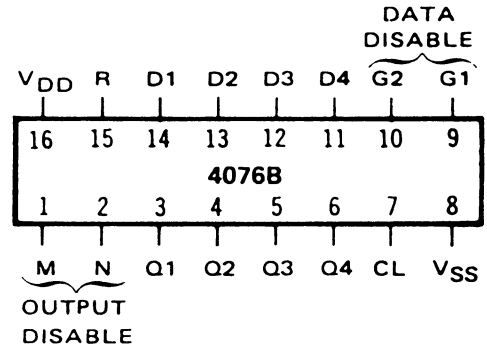
### TRUTH TABLE

Reset	Clock	Data Input Disable		Data D	Next State Output Q	
		G1	G2			
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0		1	X	X	Q	NC
0		X	1	X	Q	NC
0		0	0	1	1	
0		0	0	0	0	
0	1	X	X	X	Q	NC
0		X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 ≡ High Level                      X = Don't Care  
 0 ≡ Low Level                      NC = No Change

### CONNECTION DIAGRAM (all packages)



Add suffix for package:

C 16-pin Cerdip

E 16-pin Epoxy

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

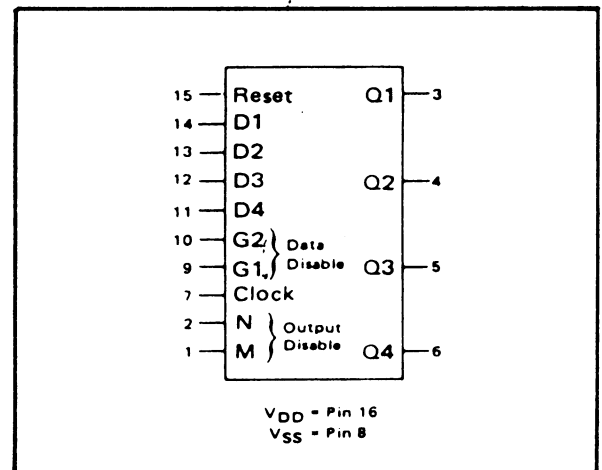
DC Supply Voltage  $V_{DD} - V_{SS}$  3 to 15 Vdc

Operating Temperature  $T_A$

C -55 to +125 °C

E -40 to +85 °C

### BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS<sup>1</sup>

PARAMETER	V <sub>DD</sub> (Vdc)	CONDITIONS	T <sub>LOW</sub> <sup>2</sup>		+25°C			T <sub>HIGH</sub> <sup>2</sup>		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I <sub>DD</sub>	V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub> All valid input combinations	—	5	—	0.05	5	—	150	μA <sub>dc</sub>
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	
3-STATE OUTPUT LEAKAGE CURRENT	I <sub>ZL</sub>		—	±0.1	—	±10 <sup>-4</sup>	±0.1	—	±1.0	μA <sub>dc</sub>

NOTES: <sup>1</sup> Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

<sup>2</sup> T<sub>LOW</sub> = -55°C for C

= -40°C for E

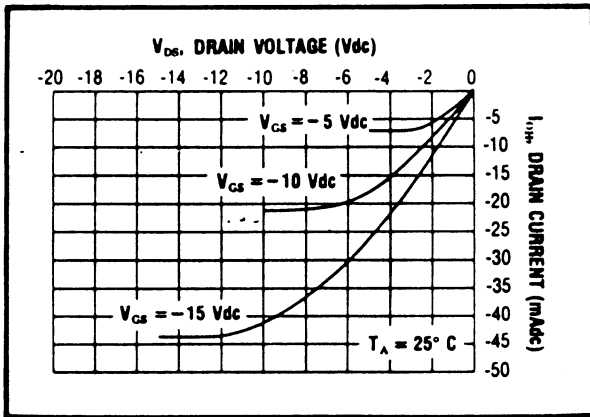
T<sub>HIGH</sub> = +125°C for C

= + 85°C for E

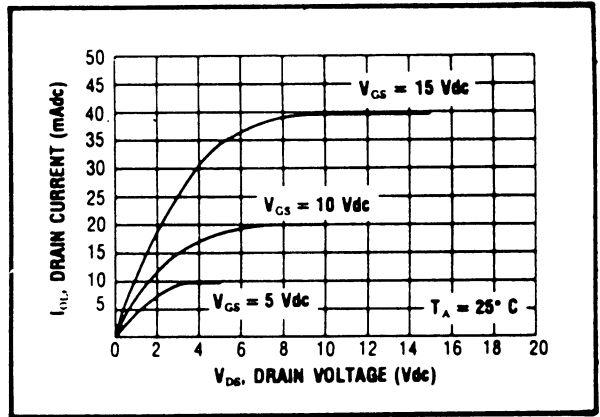
DYNAMIC CHARACTERISTICS (C<sub>L</sub> = 50pF, T<sub>A</sub> = 25°C)

PARAMETER	V <sub>DD</sub> (Vdc)	Min.	Typ.	Max.	Units	
<b>CLOCKED OPERATION</b>						
PROPAGATION DELAY TIME Clock to Q	t <sub>PLH, tPHL</sub>	5	—	150	300	ns
		10	—	70	140	
		15	—	45	90	
Output Disable to Q	t <sub>PHZ, tPLZ</sub>	5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
	t <sub>PZH, tPZL</sub>	5	—	80	160	ns
		10	—	35	70	
		15	—	25	50	
OUTPUT TRANSITION TIME	t <sub>TLH, tTHL</sub>	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM CLOCK PULSE WIDTH	PW <sub>CL</sub>	5	—	80	160	ns
		10	—	40	80	
		15	—	30	60	
MAXIMUM CLOCK FREQUENCY	f <sub>CL</sub>	5	3.0	6.0	—	MHz
		10	6.0	12	—	
		15	8.0	16	—	
MAXIMUM CLOCK RISE & FALL TIME <sup>1</sup>	t <sub>rCL, t<sub>fCL</sub></sub>	5	15	—	—	μs
		10	15	—	—	
		15	15	—	—	
MINIMUM SETUP TIME Data Inputs	t <sub>setup</sub>	5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
Data Disable Inputs	t <sub>setup</sub>	5	—	100	200	ns
		10	—	60	120	
		15	—	45	90	
MINIMUM HOLD TIME All Inputs	t <sub>hold</sub>	5	—	75	150	ns
		10	—	35	70	
		15	—	30	60	
<b>RESET OPERATION</b>						
PROPAGATION DELAY TIME	t <sub>PHL</sub>	5	—	200	400	ns
		10	—	100	200	
		15	—	75	150	
MINIMUM RESET PULSE WIDTH	PW <sub>R</sub>	5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
RESET REMOVAL TIME	t <sub>rem</sub>	5	—	100	200	ns
		10	—	60	120	
		15	—	45	90	

<sup>1</sup> When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

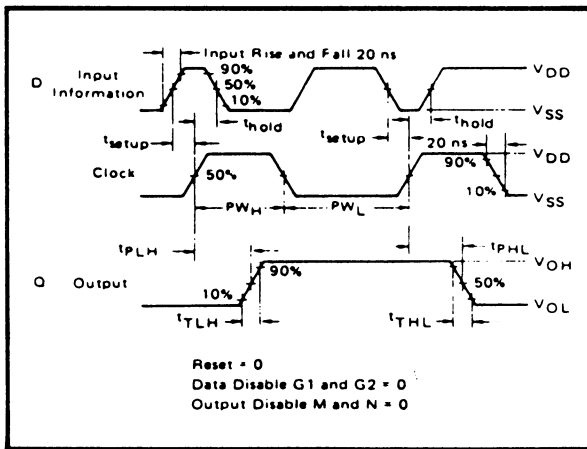


Typical P-Channel Source Current Characteristics

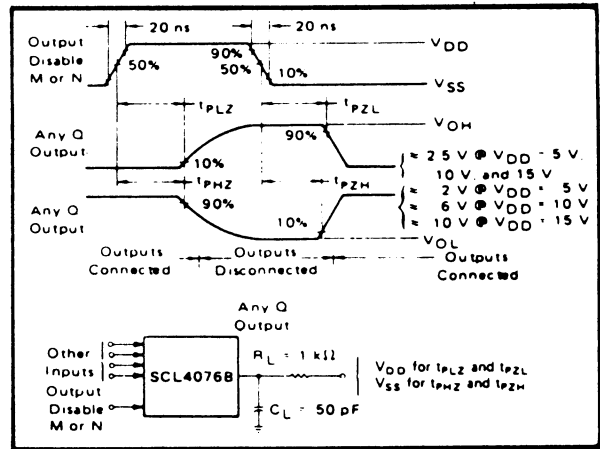


Typical N-Channel Sink Current Characteristics

**TIMING DIAGRAM**



**THREE-STATE PROPAGATION DELAY WAVESHAVE AND CIRCUIT**



**LOGIC DIAGRAM**

