GD4021B

8-BIT SHIFT REGISTER

DESCRIPTION — The 4021B is an Edge-Triggered 8-Bit Shift Register (Parallel-to-Serial Converter) with a synchronous Serial Data Input (D_S), a Clock Input (CP), an asynchronous active HIGH Parallel Load Input (PL), eight asynchronous Parallel Data Inputs (P_0–P_7) and Buffered Parallel Outputs from the last three stages (Q_5–Q_7).

Information on the Parallel Data Inputs (P_0–P_7) is asynchronously loaded into the register while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Serial Data (D_S) inputs. Data present in the register is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL).

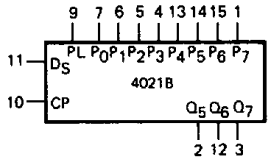
When the Parallel Load Input is LOW, data on the Serial Data Input (D_S) is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

- **TYPICAL SHIFT FREQUENCY OF 18.1 MHz AT V_{DD} = 10 V**
- **PARALLEL-TO-SERIAL DATA TRANSFER**
- **BUFFERED OUTPUTS AVAILABLE LAST THREE STAGES**
- **CLOCK INPUT IS L → H EDGE-TRIGGERED**

PIN NAMES

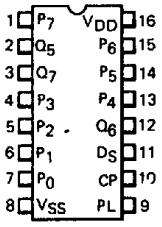
PL	Parallel Load Input
P_0-P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5-Q_7	Buffered Parallel Outputs from the Last Three Stages

LOGIC SYMBOL



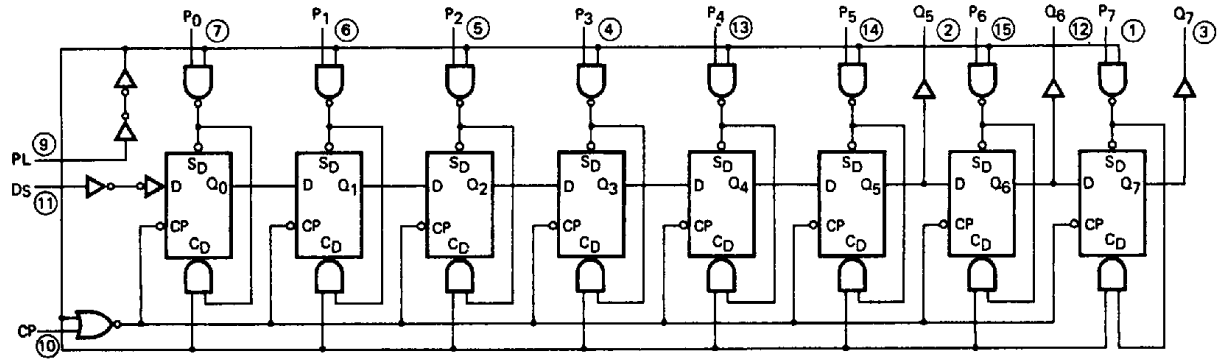
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

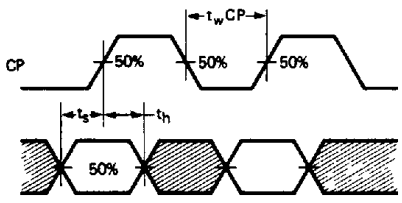
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

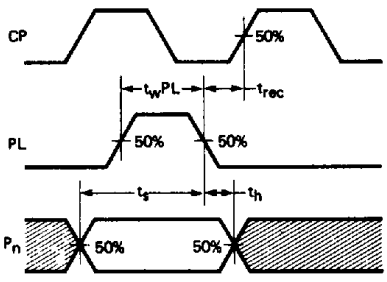
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		134			59			40		ns	
t_{PHL}			184			74			49		ns	
t_{PLH}	Propagation Delay, PL to Q_n		188			78			54		ns	
t_{PHL}			274			105			72		ns	
t_{TLH}	Output Transition Time		58			31			22		ns	
t_{THL}			69			27			22		ns	C_L = 50 pF,
t_wCP	CP Minimum Pulse Width		61			21			14		ns	R_L = 200 kΩ
t_wPL	PL Minumum Pulse Width		67			24			16		ns	Input Transition
t_{rec}	PL Recovery Time		71			28			21		ns	Times ≤ 20 ns
t_s	Set-Up Time D_S to CP		51			16			12		ns	
t_h	Hold Time D_S to CP		49			15			11		ns	
t_s	Set-Up Time P_n to PL		78			28			18		ns	
t_h	Hold Time, P_n to PL		72			26			16		ns	
f_{MAX}	Shift Frequency (Note 3)		7.8			18.1			21		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D_S TO CP



MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.