Electronic tuning PLL frequency synthesizer

BH2615S

The BH2615S is a PLL frequency synthesizer, featuring low radiation and low power consumption.
It includes high sensitive RF amplifier and supports IF count function.

●Features

1) Low voltage operation (2.7V~)
2) High speed prescaler capable of direct dividing VCO (130MHz) frequency.
3) Low radiation (Xtal OSC 75kHz)
4) Low supply current (PLL ON:5mA, PLL OFF:300μA, Typ. V_{DD}=3.0V).
5) Reference frequency : 25, 12.5, 6.25, 3.125, 5, 3, 1kHz
6) On chip IF frequency counter.
7) Unlock detector
8) Output port : 7 ports (open drain output)
9) Data input : serial input (CE. CK. DA)

●Absolute maximum ratings (Ta = 25°C)

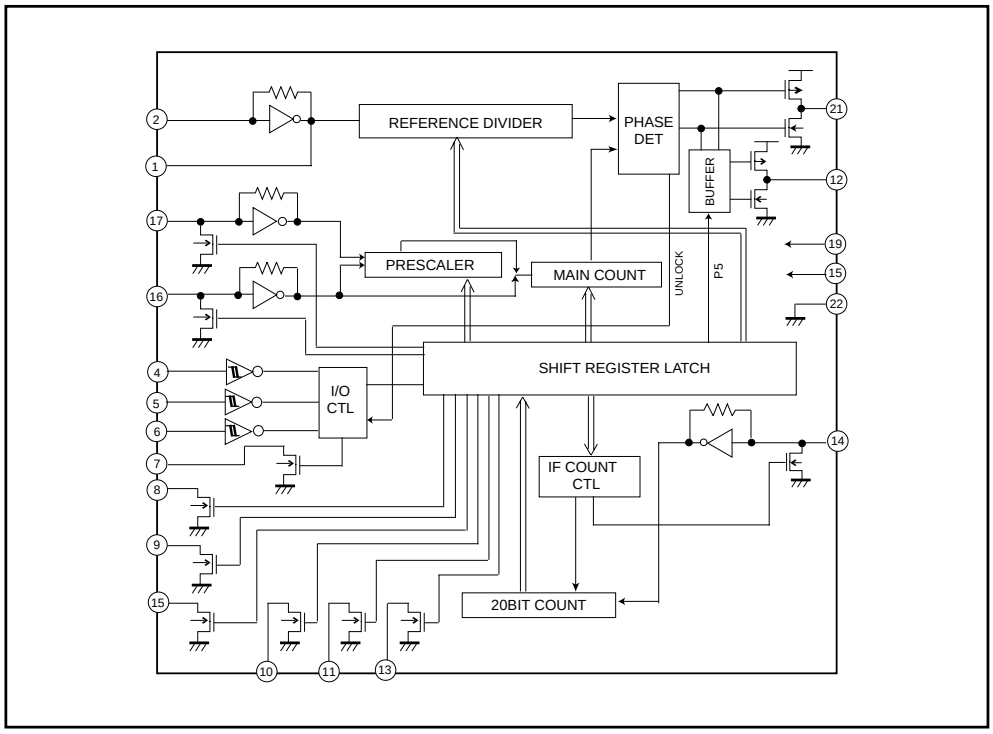
Parameter	Symbol	Limits	Unit	Condition
Maximum supply voltage	V_{DD}	−0.3~+7.0	V	V_{DD1},V_{DD2}
Maximum input voltage 1	V_{IN1}	−0.3~+7.0	V	CE,CK,DA
Maximum input voltage 2	V_{IN2}	−0.3~V_{DD}+0.3	V	XIN,FM_{IN},AM_{IN},IF_{IN}
Maximum output voltage 1	V_{OUT1}	−0.3~10.0	V	P_0,P_1,P_2,P_3,P_4,P_5,CD
Maximum output voltage 2	V_{OUT2}	−0.3~V_{DD}+0.3	V	PD_1,PD_2,P_5,XOUT
Maximum output current	I_{OUT}	0~3.0	mA	P_0,P_1,P_2,P_3,P_4,P_5,CD
Allowable power dissipation	P_D	600 ∗	mW	
Operating temperature	Topr	−10~+75	°C	
Storage temperature	Tstg	−55~+125	°C	

∗ Derating is done at 6.0mW °C for operating above Ta=25°C.

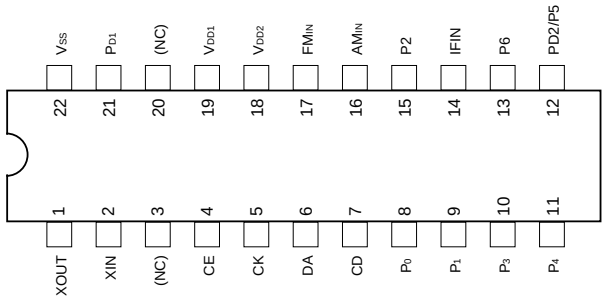
●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD1}=V_{DD2}	2.7	–	3.6	V

●**Block diagram**



●**Pin assigment**



●**Pin descriptions**

Pin No.	Pin Name	Symbol	Functions	I / O
1	Xtal OSC	XOUT	Crystal resonator (75kHz) is connected.	OUT
2		XIN		IN
3	Non contact	NC		
4	Chip enable	CE	"H" level are input during DA and CK. Data is synchronized this clock. Serial data transfered from controller.	IN
5	Clock	CK		
6	Serial data	DA		
7	Count data	CD	IF count data , unlock data output.	Nch open drain
8	Output port	P_0	Controlled by input serial data.	
9		P_1		
10		P_3		
11		P_4		
12		P_5 / P_{D2}	∗Selected input controlled data.	3-State
13		P_6		Nch open drain
14	IF input	IF_{IN}	IF frequency input.	IN
15	Output port	P_2	Controlled by input serial data.	Nch open drain
16	AM input	AM_{IN}	Input AM local OSC.	IN
17	FM input	FM_{IN}	Input FM local OSC.	IN
18	Power supply2	V_{DD2}	Supply voltage 2.7~3.6V	
19	Power supply1	V_{DD1}	Supply voltage 2.7~3.6V	
20	Non contact	NC		
21	Charge pump	P_{D1}	If local OSC freq, divided by N is higher than reference freq, "H". lower, "L" and same, (Floating).	3-State
22	GROUND	V_{SS}		

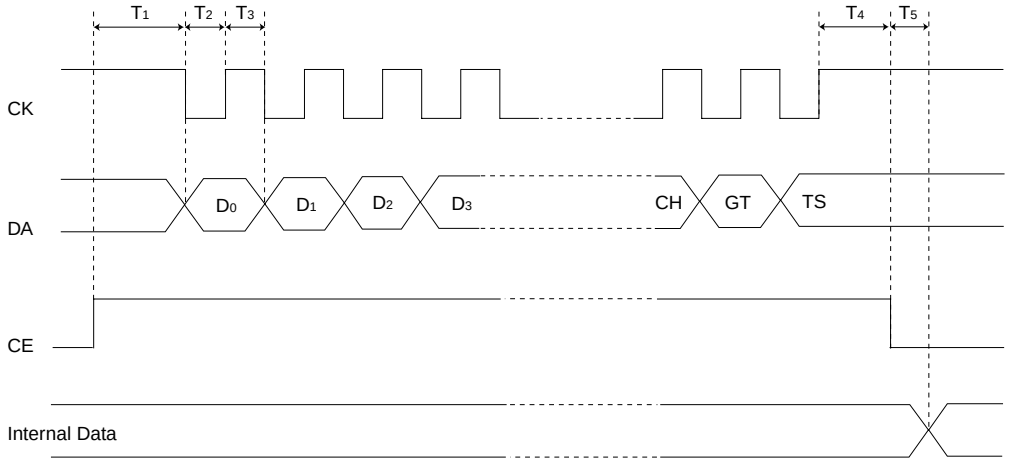
●**Electrical characteristics** (Unless otherwise specified, Ta = 25°C, V_{DD1} = V_{DD2} = 3.0V, V_{SS} = 0.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Supply current 1	I_{DD1}	–	2.8	5.0	mA	FM_{IN}=130MHz, 50mVrms, V_{DD1}+V_{DD2} Current	
Supply current 2	I_{DD2}	–	0.7	1.5	mA	AM_{IN}=1.0MHz, 50mVrms, V_{DD1}+V_{DD2} Current	
Supply current 3	I_{DD3}	–	0.3	1.0	mA	PLL=OFF	
Input "H" level voltage	V_{IH}	0.8V_{DD1}	–	–	–	CE,CK,DA Pins	
Input "L" level voltage	V_{IL}	–	–	0.2V_{DD1}	–	CE,CK,DA Pins	
Input "H" level current 1	I_{IH1}	–	–	1.0	µA	CE,CK,DA Pins,	V_{IN}=V_{DD1}
Input "H" level current 2	I_{IH2}	–	0.3	0.7	µA	XIN Pin,	V_{IN}=V_{DD1}
Input "H" level current 3	I_{IH3}	5	10	15	µA	FM_{IN},AM_{IN} Pins,	V_{IN}=V_{DD2}
Input "H" level current 4	I_{IH4}	3	6	12	µA	IF_{IN} Pin,	V_{IN}=V_{DD1}
Input "L" level current 1	I_{IL1}	–1.0	–	–	µA	CE,CK,DA Pins,	V_{IN}=V_{SS}
Input "L" level current 2	I_{IL2}	–0.7	–0.3	–	µA	XIN Pin,	V_{IN}=V_{SS}
Input "L" level current 3	I_{IL3}	–5	–10	–15	µA	FM_{IN},AM_{IN},IF_{IN} Pins,	V_{IN}=V_{SS}
Output "L" level voltage 1	V_{OL1}	–	0.2	0.5	V	P_0,P_1,P_2,P_3,P_4,P_6,CD,	I_O=1.0mA
Output "OFF" leak current 1	I_{OFF1}	–	–	1.0	µA	P_0,P_1,P_2,P_3,P_4,P_6,CD,	V_O=10V
Output "L" level voltage 2	V_{OL2}	–	0.1	0.5	V	FM_{IN},AM_{IN},IF_{IN},	I_{OUT}=0.1mA
Output "H" level voltage	V_{OH}	V_{DD1} –1.0	V_{DD1} –0.3	–	V	P_{D1},P_{D2},P_5,	I_{OUT}=–1.0mA
Output "L" level voltage	V_{OL}	–	0.2	1.0	V	P_{D1},P_{D2},P_5,	I_{OUT}=1.0mA
Output "OFF" leak current 2	I_{OFF2}	–	–	100	nA	P_{D1},P_{D2},	V_{OUT}=V_{DD1}
Output "OFF" leak current 3	I_{OFF3}	–100	–	–	nA	P_{D1},P_{D2},	V_{OUT}=V_{SS}
On chip feedback resistance 1	R_{F1}	3.8	10	16	MΩ	XIN	
On chip feedback resistance 2	R_{F2}	300	500	1000	kΩ	FM_{IN},AM_{IN},IF_{IN}	
Input frequency input level 1	F_{IN1}	10 100	75	160 900	kHz mVrms	XIN,Sine Wave, C–Coupling	
Input frequency input level 2	F_{IN2}	20 20	–	130 900	MHz mVrms	FM_{IN},Sine Wave, C–Coupling	
Input frequency input level 3	F_{IN3}	0.4 20	–	5.0 900	MHz mVrms	AM_{IN},Sine Wave, C–Coupling	
Input frequency input level 4	F_{IN4}	5.0 40	–	30 900	MHz mVrms	AM_{IN},Sine Wave, C–Coupling	
Input frequency input level 5	F_{IN5}	0.4 20	–	16 900	MHz mVrms	IF_{IN},Sine Wave, C–Coupling	
Minimum pulse width	TW	–	1.0	–	µs	CK,DA	
Input rase time	TR	–	–	500	ns	CE,CK,DA	
Input fall time	TF	–	–	500	ns	CE,CK,DA	

◎ Not designed for radiation resistance.

●Circuit operation

Input data format



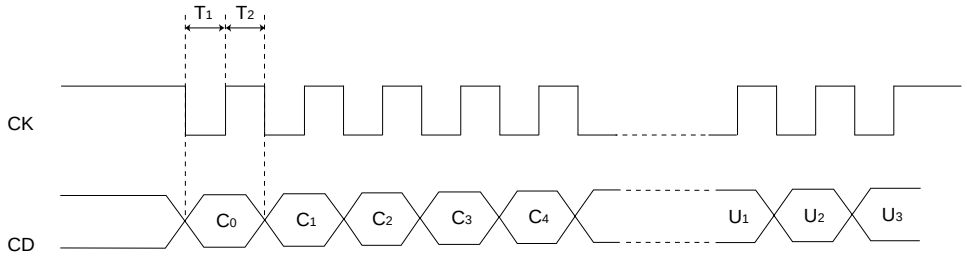
$T_1 \geq 15\mu sec.$ $T_2, T_3 > 1\mu sec.$ $T_4 > 0\mu sec.$ $T_5 < 15\mu sec.$

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

← Input from D_0

P_0	P_1	P_2	P_3	P_4	P_5	P_6	CT	R_0	R_1	R_2	S	PS	CH	GT	TS

Output data format CE="L0" level



Output : pulled up $T_1, T_2 > 1\mu sec.$

C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

C_{16}	C_{17}	C_{18}	C_{19}	U_0	U_1	U_2	U_3

← Output from C_0 ∗ Output data enable , only CT=1 or GT=1.

Structure of control data

1) Division ratio data : D_0~D_{15}

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Example :

Division = 1100 (D) = 1100 ÷ 2 = 550 (D) = 226 (H) S=0,PS=0 Division is twice the set point

0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0

Division = 1107 (D) = 453 (H) S=1,PS=1

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0

Division = 926 (D) = 39E (H) S=1,PS=0

×	×	×	×	0	1	1	1	1	0	0	1	1	1	0	0

2) CT : IF counter on OFF

1 : START

0 : Counter is reset, IF_{IN} pulldown.

3) Output port control data : P_0, P_1, P_2, P_3, P_4, P_5, P_6

1 : Nch open drain output ON (P_5=L0)

0 : Nch open drain output OFF (P_5=HI)

4) R_0, R_1, R_2, Reference frequency data.

Data			
R_0	R_1	R_2	Reference frequency
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	6.25kHz
0	1	1	5kHz
1	0	0	3.125kHz
1	0	1	3kHz
1	1	0	1kHz
1	1	1	* PLL OFF

*FM_{IN}=Pull down, AM_{IN}=Pull down, PD=Floating

5) S : FM_{IN}, AM_{IN} select data

0 : FM_{IN} 1 : AM_{IN}

6) PS : Pre scaler ON with S=1

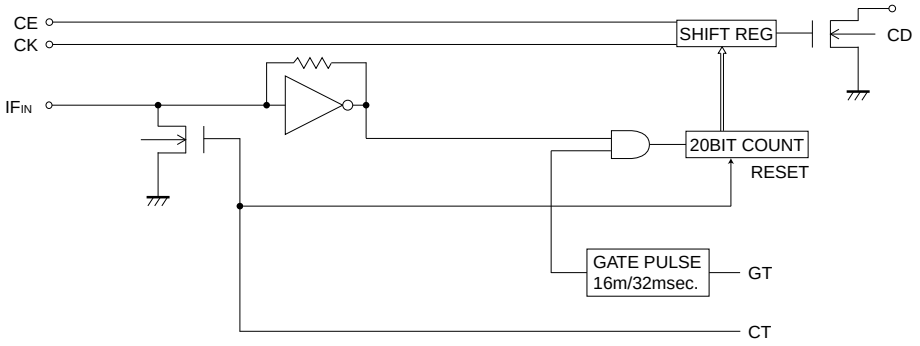
7) GT : IF count or unlock ON / OFF

CT	GT	IF counter	Unlock detector	Output data
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON Gate time=16msec.	ON	
1	1	ON Gate time=32msec.	ON	

8) TS : Test data input “0”.

IF counter

1) Composition



2) Operation of IF detection circuit

CT=1, IF counter start. CT = 0, IF count circuit reset.

GT=0, gate time=16msec. GT=1, gate time=32msec.

3) Output data

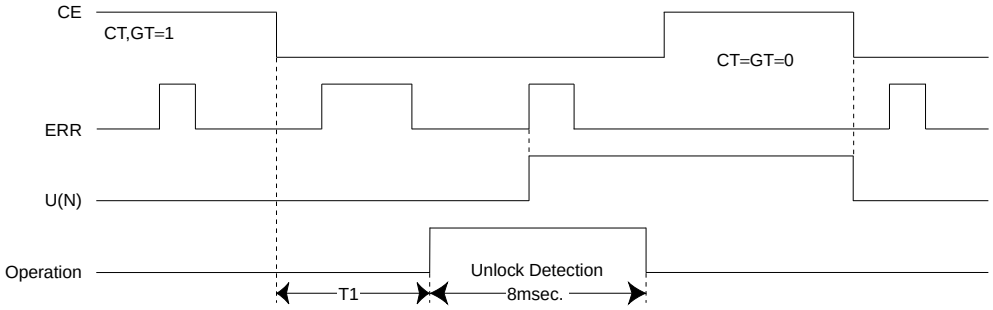
C_0 : LSB C_{19} : MSB

Operation of unlock detector

GT=1 or CT=1, unlock detector start during 8msec.

CT=1, unlock detector start before gate pulse of IF counter.

CT=0 GT=0, IF counter and unlock detector.



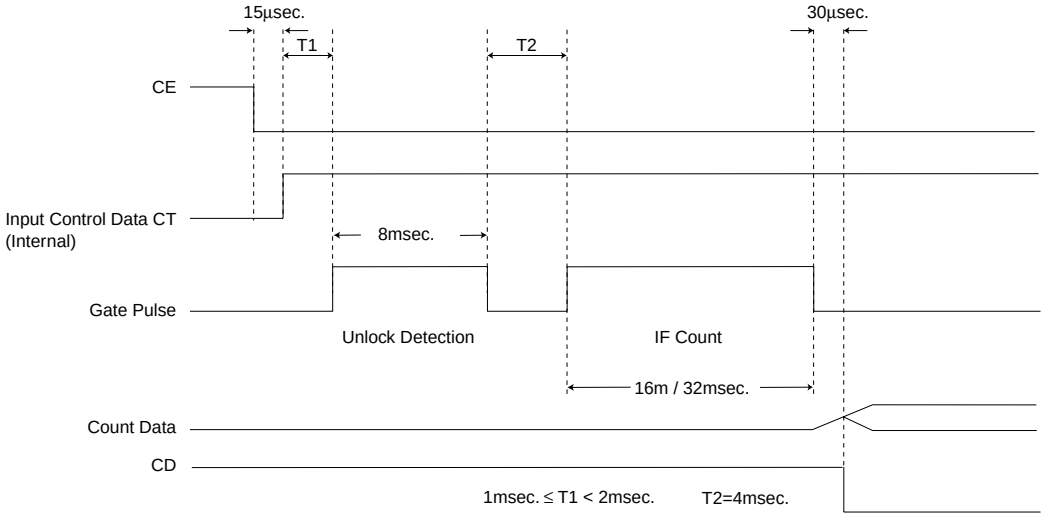
Structure output

1msec. ≤ T1 < 2msec.

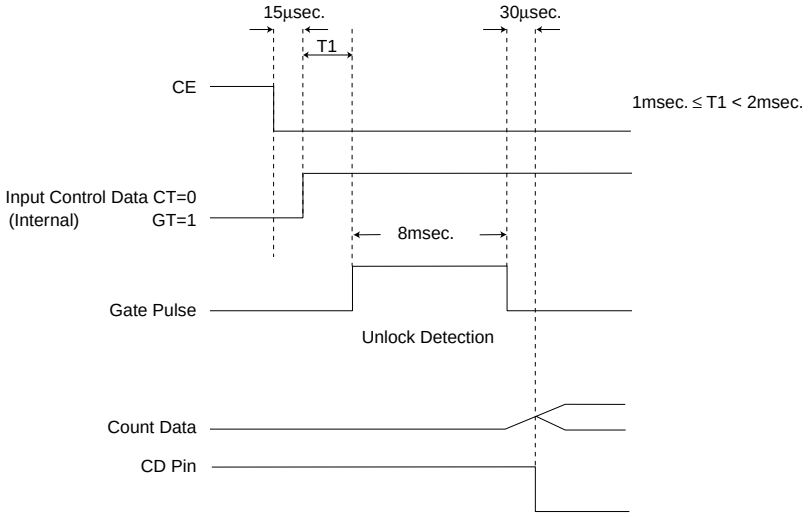
U0	U1	U2	U3					
0	0	0	0			ERR	<	7µsec.
1	0	0	0	7µsec.	<	ERR	<	13µsec.
1	1	0	0	13µsec.	<	ERR	<	26µsec.
1	1	1	0	26µsec.	<	ERR	<	54µsec.
1	1	1	1	54µsec.	<	ERR		

Operation of IF counter and unlock detector.

1) CT=1 : IF count and unlock detector.



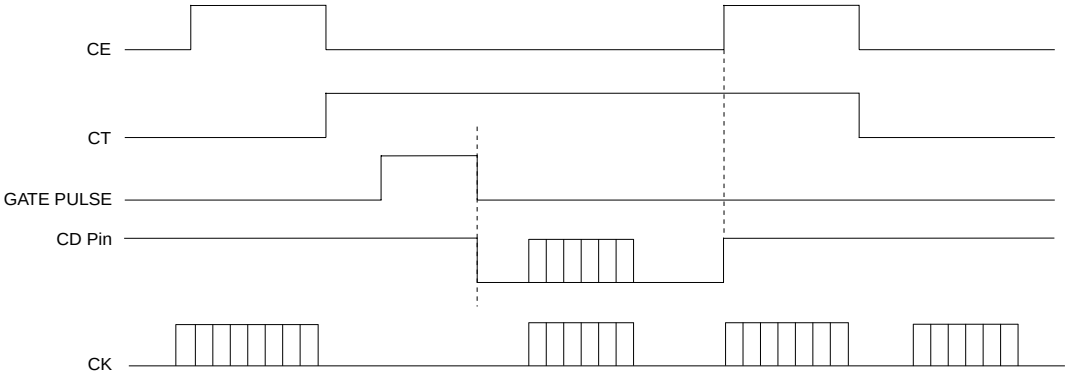
2) CT=0 GT=1 : unlock detection only.



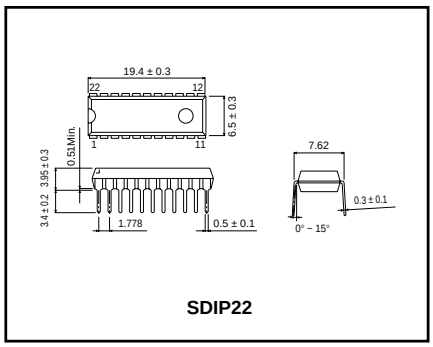
Structure CD Pin

CD Pin becomes “L0” after finishing IF count or unlock detection operation.

Output data synchronized CK.



●**External dimensions** (Units : mm)



SDIP22