To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

RENESAS
Renesas Technology Corp.

M62352P,FP,GP

8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62352 is an integrated circuit semiconductor of CMOS structure with 12 channels of built-in D-A converters with output buffer operational amplifiers.
The 3-wire serial interface method is used for the transfer format mum wiring.
It is able to cascading serial use with Do terminal.
The output buffer operational amplifier operates in the whole voltage range from power supply to ground for both input/output.

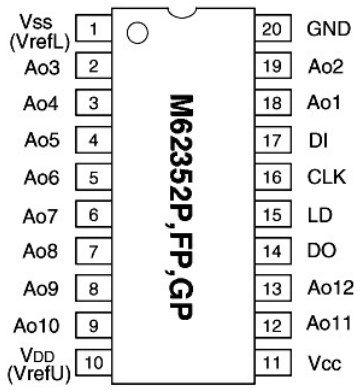
FEATURES

- 12bit serial data input(3-wire serial data transfer method)
- Highly stable output buffer operational amplifier allow operation in the all voltage range from power supply to ground.

APPLICATION

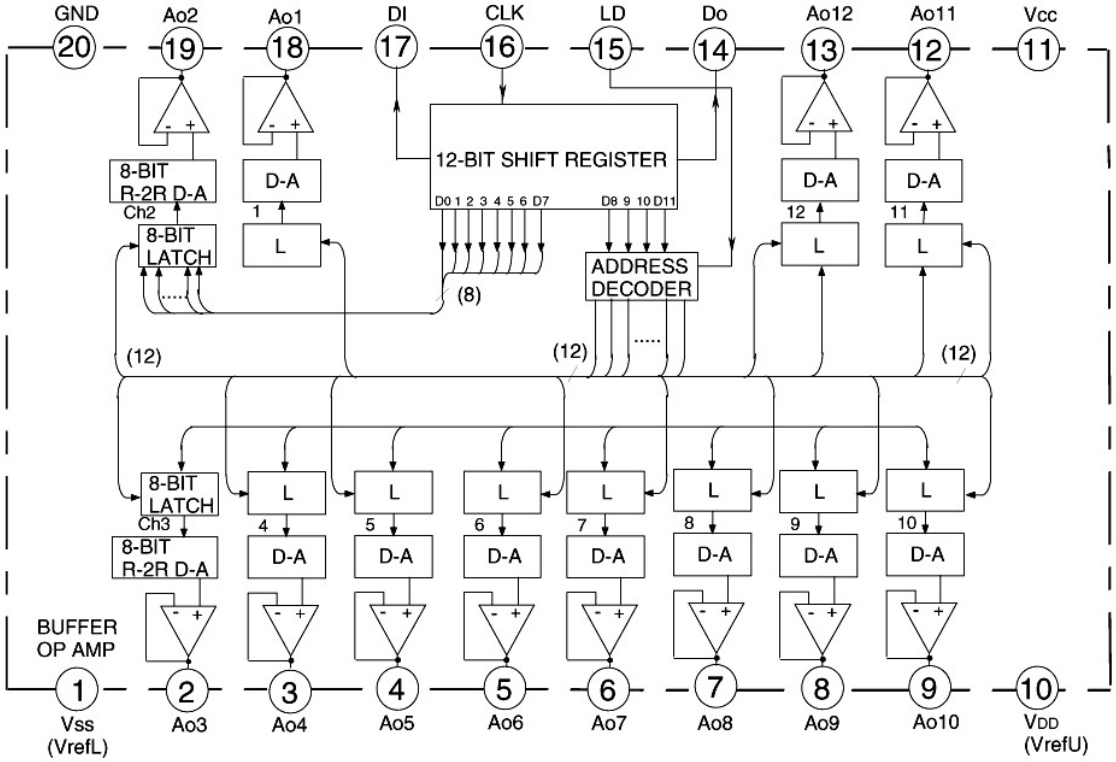
Adjustment/control of industrial or home-use electronic equipment,such as VTR camera,VTR set,TV,and CRT display.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B(P)
20P2N-A(FP)
20P2E-A(GP)

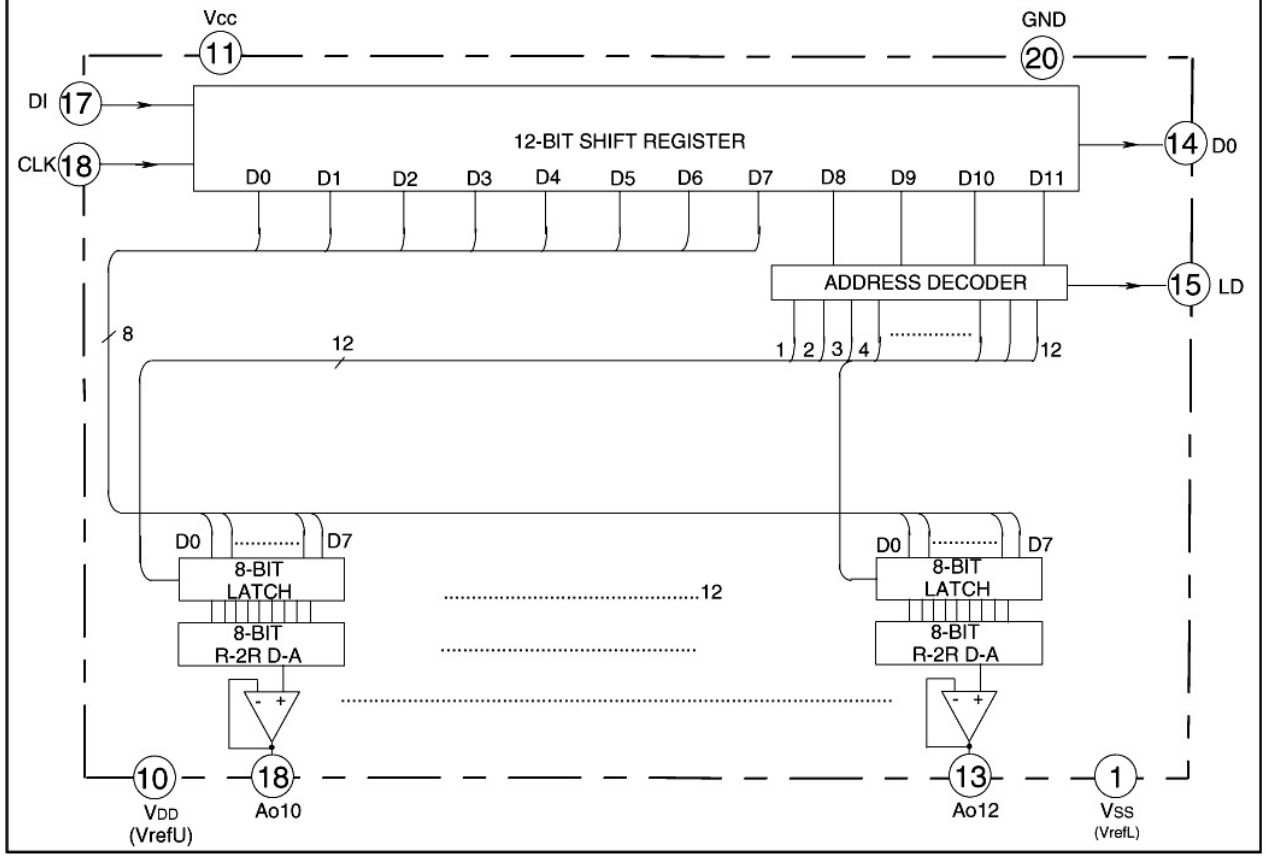
BLOCK DIAGRAM



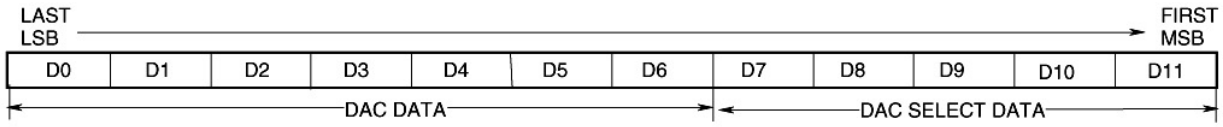
EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑰	DI	Serial data input terminal
⑭	DO	Serial data output terminal
⑯	CLK	Serial clock input terminal
⑮	LD	LD terminal input high level than latch circuit data load
⑱	Ao1	8-bit D-A converter output terminal
⑲	Ao2	
②	Ao3	
③	Ao4	
④	Ao5	
⑤	Ao6	
⑥	Ao7	
⑦	Ao8	
⑧	Ao9	
⑨	Ao10	
⑫	Ao11	
⑬	Ao12	
⑪	Vcc	Power supply terminal
⑳	GND	Digital and analog common GND
⑩	V_{DD}	D-A converter upper reference voltage input terminal
①	Vss	D-A converter lower reference voltage input terminal

BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



DIGITAL DATA FORMAT

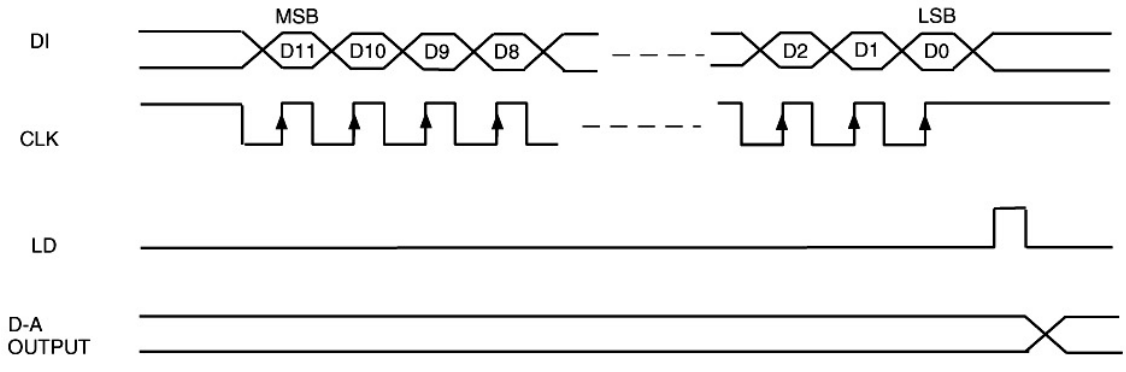


D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	(VrefU-VrefL)/256X1+VrefL
1	0	0	0	0	0	0	0	(VrefU-VrefL)/256X2+VrefL
0	1	0	0	0	0	0	0	(VrefU-VrefL)/256X3+VrefL
1	1	0	0	0	0	0	0	(VrefU-VrefL)/256X4+VrefL
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(VrefU-VrefL)/256X255+VrefL
1	1	1	1	1	1	1	1	VrefU

D8	D9	D10	D11	DAC selection
0	0	0	0	Don t care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2
0	0	1	1	Ao3
0	1	0	0	Ao4
0	1	0	1	Ao5
0	1	1	0	Ao6
0	1	1	1	Ao7
1	0	0	0	Ao8
1	0	0	1	Ao9
1	0	1	0	Ao10
1	0	1	1	Ao11
1	1	0	0	Ao12
1	1	0	1	Don t care
1	1	1	0	Don t care
1	1	1	1	Don t care

*VrefU=V_{DD}
VrefL=Vss

TIMING CHART (MODEL)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~7.0	V
V_{DD}	D-A converter upper reference voltage		-0.3~7.0	V
V_{IN}	Input voltage		-0.3~Vcc+0.3	V
Vo	Output voltage		-0.3~Vcc+0.3	V
Pd	Power dissipation		350(P)/350(FP)/150(GP)	mV
T_{opr}	Operating temperature		-20~+85	°C
T_{stg}	Storage temperature		-55~+125	°C

ELECTRICAL CHARACTERISTICS

Digital part(Vcc,VrefU=+5V±10%,Vcc≥VrefU,GND,VrefL=0V,Ta=-20°C~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		4.5	5.0	5.5	V
Icc	Circuit current	CLK=1MHz operation I_{OA}=0μA		1.6	3.2	mA
I_{ILK}	Input leak current	V_{IN}=0~Vcc	-10		10	μA
V_{IL}	Input low voltage				0.2Vcc	V
V_{IH}	Input high voltage		0.8Vcc			V
V_{OL}	Output low voltage	I_{OL}=2.5mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-400μA		Vcc-0.4		V

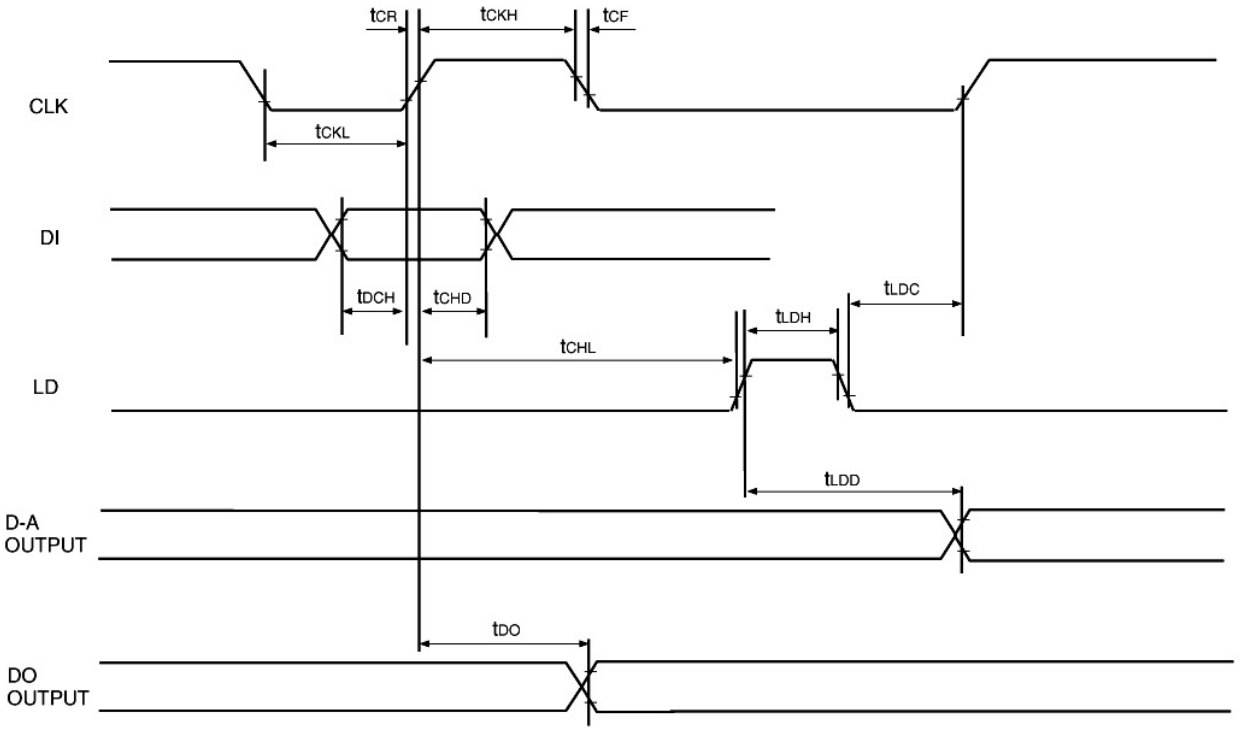
Analog part(Vcc,VrefU=+5V±10%,Vcc≥VrefU,Ta=-20°C~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{DD}	Current dissipation	VrefU=5V,VrefL=0V Data condition;at maximum current		1.4	2.5	mA
V_{DD}	D-A converter upper reference voltage range	The output dose not necessarily be the value within the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range(V_{AO})	3.5		Vcc	V
V_{SS}	D-A converter lower reference voltage range		GND		Vcc-3.5	V
V_{AO}	Buffer amplifier output voltage range	I_{OA}=±100μA	0.1		Vcc-0.1	V
		I_{OA}=±500μA	0.2		Vcc-0.2	
I_{AO}	Buffer amplifier output drive range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	-1		1	mA
S_{DL}	Differential nonlinearity error	VrefU=4.79V VrefL=0.95V Vcc=5.5V(15mV/LSB) Without load(I_{OA}=±0)	-1.0		1.0	LSB
S_L	Nonlinearity error		-1.5		1.5	LSB
S_{ZERO}	Zero code error		-2		2	LSB
S_{FULL}	Full scale error		-2		2	LSB
Co	Output capacitive load				0.1	μF
Ro	Buffer amplifier output impedance			5		Ω

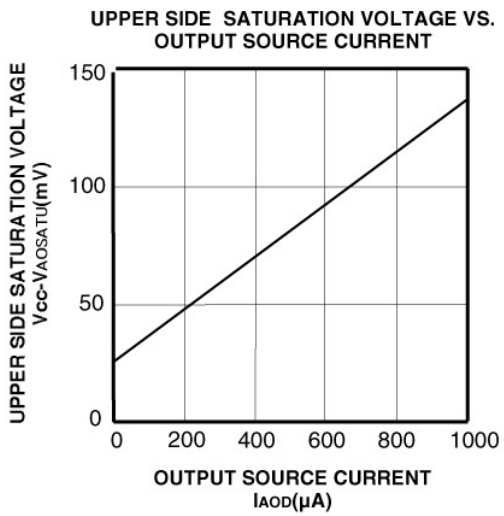
AC CHARACTERISTICS(Vcc,VrefU=+5V±10%,Vcc≥VrefU,GND,VrefL=0V,Ta=-20~+85°C, unless otherwise noted)

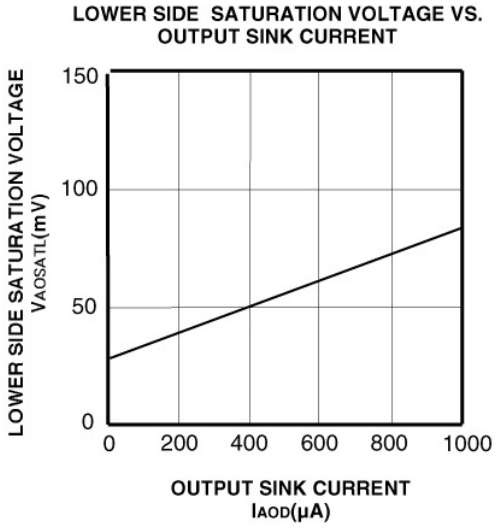
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CLK}	Clock "L"pulse width		200			ns
t_{CKH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data setup time		30			ns
t_{CHD}	Data hold time		60			ns
t_{CHL}	LD setup time		200			ns
t_{LDC}	LD hold time		100			ns
t_{LDH}	LD "H" pulse width		100			ns
t_{DO}	Data output delay time	C_L≤100pF	70		350	ns
t_{LDD}	D-A output setting time	C_L≤100pF V_{AQ}:0.5→ 4.5V The time until the output becomes the final value of 1/2 LSB			300	µs

TIMING CHART



TYPICAL CHARACTERISTICS





SATURATION VOLTAGE VS.OUTPUT CURRENT