Micro Linear

ML2008*, ML2009**

µP Compatible Logarithmic Gain/Attenuator

GENERAL DESCRIPTION

The ML2008 and ML2009 are digitally controlled logarithmic gain/attenuators with a range of –24 to +24dB in 0.1dB steps.

Easy interface to microprocessors is provided by an input latch and control signals consisting of chip select and write.

The interface for gain setting of the ML2008 is by an 8-bit data word, while the ML2009 is designed to interface to a 16-bit data bus with a single write operation by hard-wiring the gain/attenuation pin or LSB pin. The ML2008 can be power downed by the microprocessor utilizing a bit in the second write operation.

Absolute gain accuracy is 0.05dB max over supply tolerance of ±10% and temperature range.

These CMOS logarithmic gain/attenuators are designed for a wide variety of applications in telecom, audio, sonar or general purpose function generation.

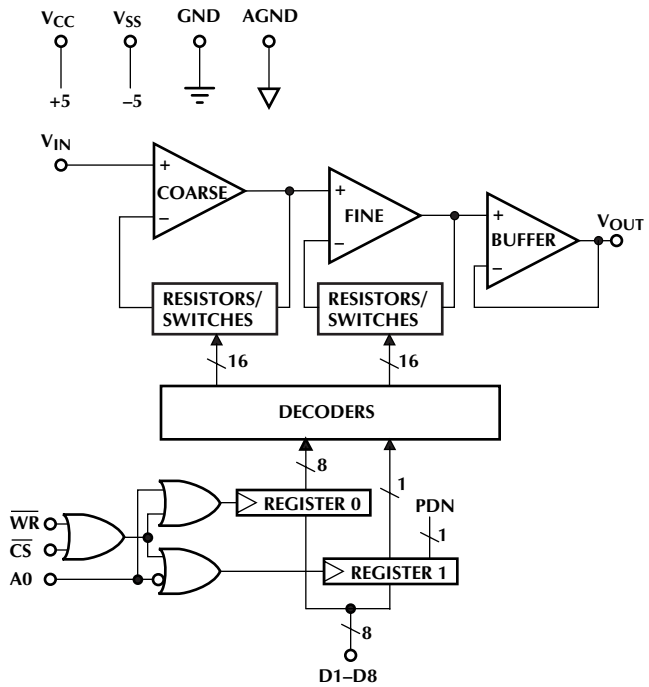
FEATURES

- Low noise 0dBrnc max with +24dB gain
- Low harmonic distortion –60dB max
- Gain range –24 to +24dB
- Resolution 0.1dB steps
- Flat frequency response ±0.05dB from 0.3-4kHz
±0.10dB from 0.1-20kHz
- Low supply current 4mA max from ±5V supplies
- TTL/CMOS compatible digital interface
- ML2008 is designed to interface to an 8-bit data bus; ML2009 to 16-bit data bus

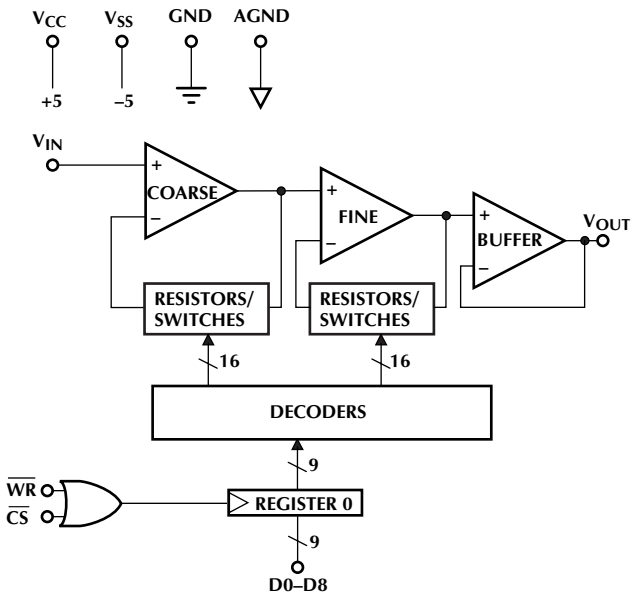
* This Part Is End Of Life As Of August 1, 2000
** This Part Is Obsolete

BLOCK DIAGRAM

ML2008

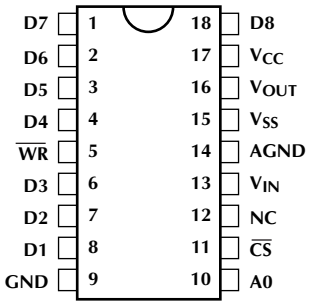


ML2009*



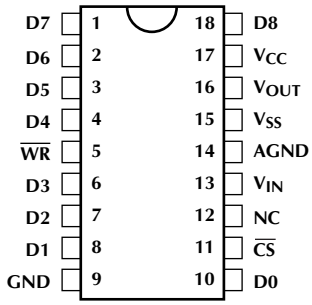
PIN CONFIGURATION

ML2008
18-Pin DIP (P18)



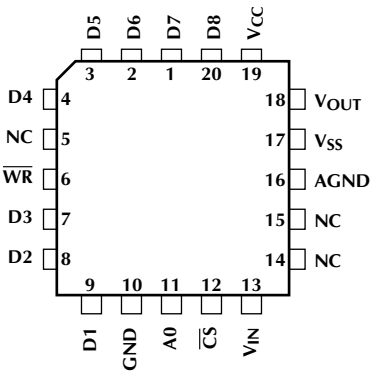
TOP VIEW

ML2009*
18-Pin DIP (P18)



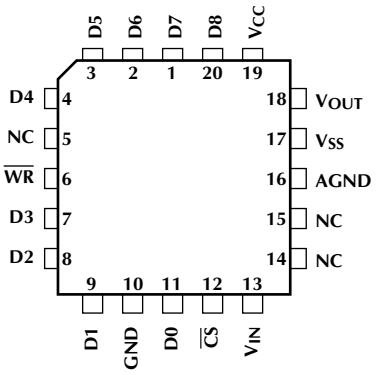
TOP VIEW

20-Pin PLCC (Q20)



TOP VIEW

20-Pin PLCC (Q20)



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{SS}	Negative supply. –5Volts ±10%
V_{CC}	Positive supply. 5Volts ±10%
GND	Digital ground. 0Volts. All digital inputs are referenced to this ground.
AGND	Analog ground. 0Volts. Analog input and output are referenced to this ground.
V_{IN}	Analog input
V_{OUT}	Analog output
D8	Data bit, ATTEN/$\overline{GAIN}$
D7	Data bit, C3
D6	Data bit, C2
D5	Data bit, C1
D4	Data bit, C0

NAME	FUNCTION
D3	Data bit, F3
D2	Data bit, P_{DN}, F2 ML2008; F2 ML2009
D1	Data bit, F0, F1 ML2008; F1 ML2009
D0	Data bit, F0 ML2009 only
$\overline{WR}$	Write enable. This input latches the data bits into the registers on rising edges of $\overline{WR}$.
$\overline{CS}$	Chip select. This input selects the device by only allowing the $\overline{WR}$ signal to latch in data when $\overline{CS}$ is low.
A0 (ML2008 only)	Address select. This input determines which data word is being written into the registers.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... –6.5V
- AGND with Respect to GND ..... V_{CC} to V_{SS}
- Analog Inputs and Outputs ..... V_{SS} –0.3V to V_{CC} +0.3V
- Digital Inputs and Outputs... GND –0.3V to V_{CC} +0.3V
- Input Current Per Pin ..... ±25mA
- Power Dissipation 750mW
- Storage Temperature Range ..... –65°C to +150°C
- Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2008CX, ML2009CX ..... 0°C to +70°C
- ML2008IX, ML2009IX ..... –40°C to +85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... –4V to –6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±10%, V_{SS} = –5V ±10%, Data Word: D8 (ATTEN/$\overline{GAIN}$) = 1, Other Bits = 0, (0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, dBm measurements use 600Ω as reference load, digital timing measured at 1.4V.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Analog							
AG	Absolute Gain Accuracy	4	V_{IN} = 8dBm, 1kHz	–0.05		+0.05	dB
RG	Relative Gain Accuracy	4	100000001 000000000 000000001 All other gain settings All values referenced to 100000000 gain when D8 (ATTEN/$\overline{GAIN}$) = 1, V_{IN} = 8dBm when D8 (ATTEN/$\overline{GAIN}$) = 0, V_{IN} = (8dBm – Ideal Gain) in dB	–0.05 –0.05 –0.05 –0.1		+0.05 +0.05 +0.05 +0.1	dB dB dB dB
FR	Frequency Response	4	300-4000Hz 100-20,000Hz Relative to 1kHz	–0.05 –0.1		+0.05 +0.1	dB dB
V_{OS}	Output Offset Voltage	4	V_{IN} = 0, +24dB gain			±100	mV
I_{CN}	Idle Channel Noise	4 5	V_{IN} = 0, +24dB, C msg weighted V_{IN} = 0, +24dB, 1kHz		–6 450	0 900	dBrnc nv/√Hz
HD	Harmonic Distortion	4	V_{IN} = 8dBm, 1kHz Measure 2nd, 3rd, harmonic relative to fundamental			–60	dB
SD	Signal to Distortion	4	V_{IN} = 8dBm, 1kHz C msg weighted	+60			dB
PSRR	Power Supply Rejection	4	200mV_{P-P}, 1kHz sine, V_{IN} = 0 on V_{CC} on V_{SS}		 –60 –60	 –40 –40	 dB dB
Z_{IN}	Input Impedance, V_{IN}	4		1			Meg
V_{INR}	Input Voltage Range	4		±3.0			V
V_{OSW}	Output Voltage Swing	4		±3.0			V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Digital and DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
I_{IN}	Input Current, Low	4	V_{IH} = GND			–10	µA
I_{IN}	Input Current, High	4	$V_{IH} = V_{CC}$			10	µA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, V_{IN} = 0			4	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$, V_{IN} = 0			–4	mA
I_{CCP}	V_{CC} Supply Current, ML2008 Powerdown Mode Only	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			0.5	mA
I_{SSP}	V_{SS} Supply Current, ML2008 Powerdown Mode Only	4	No output load, V_{IL} = GND, $V_{IH} = V_{CC}$			–0.1	mA
AC Characteristics							
t_{SET}	V_{OUT} Settling Time	4	V_{IN} = 0.185V. Change gain from –24 to +24dB. Measure from $\overline{WR}$ rising edge to when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{STEP}	V_{OUT} Step Response	4	Gain = +24dB. V_{IN} = –3V to +3V step. Measure from V_{IN} = –3V to when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{DS}	Data Setup Time	4		50			ns
t_{DH}	Data Hold Time	4		50			ns
t_{AS}	A0 Setup Time	4		0			ns
t_{AH}	A0 Hold Time	4		0			ns
t_{CSS}	$\overline{CS}$* Setup Time	4		0			ns
t_{CSH}	$\overline{CS}$* Hold Time	4		0			ns
t_{PW}	$\overline{WR}$* Pulse Width	4		50			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

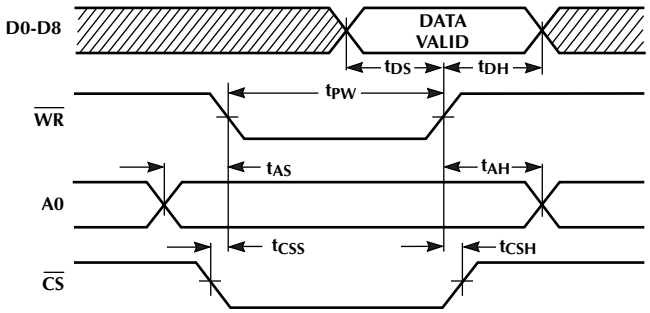
Note 2: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

TIMING DIAGRAM



TYPICAL PERFORMANCE CURVES

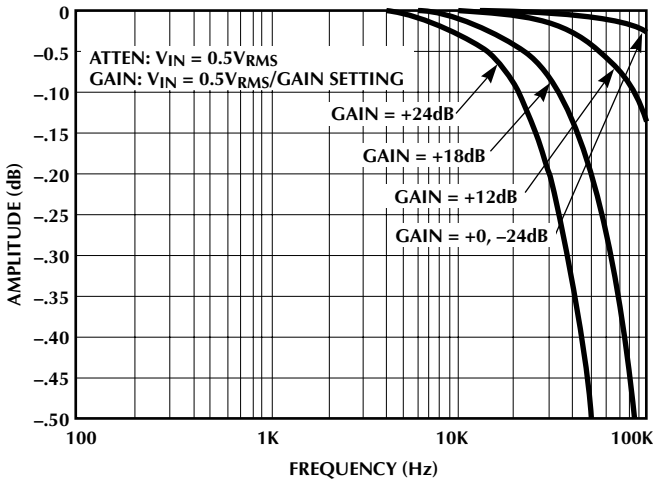


Figure 2. Amplitude vs Frequency (V_{IN}/V_{OUT} = 0.5V_{RMS})

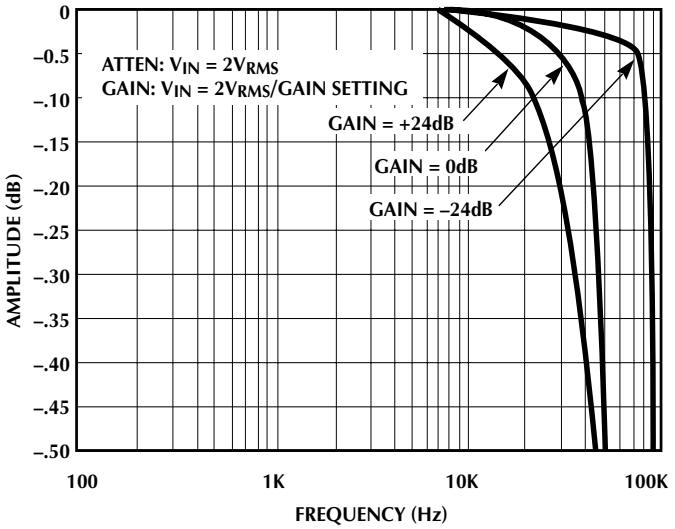


Figure 3. Amplitude vs Frequency (V_{IN}/V_{OUT} = 2V_{RMS})

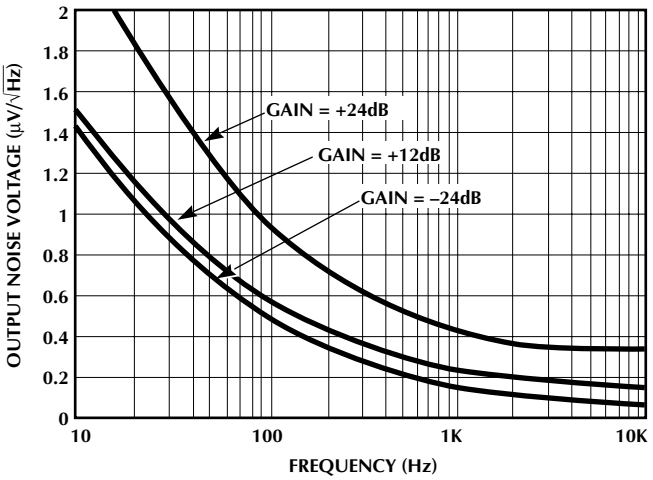


Figure 4. Output Noise Voltage vs Frequency

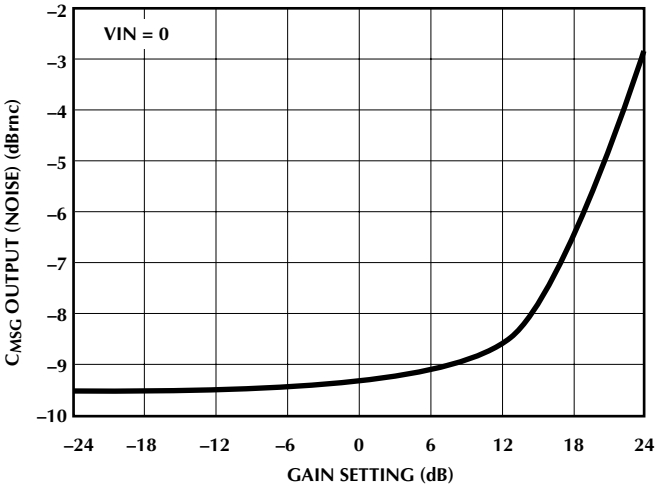


Figure 5. C_{MSG} Output Noise vs Gain Setting

TYPICAL PERFORMANCE CURVES (Continued)

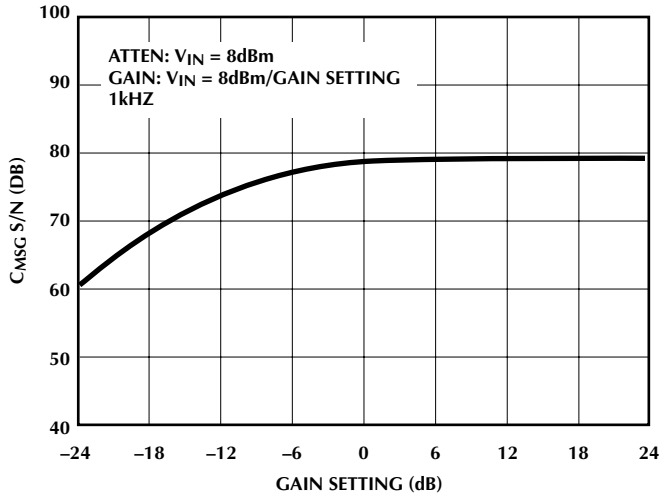


Figure 6. C_{MSG} S/N vs Gain Setting

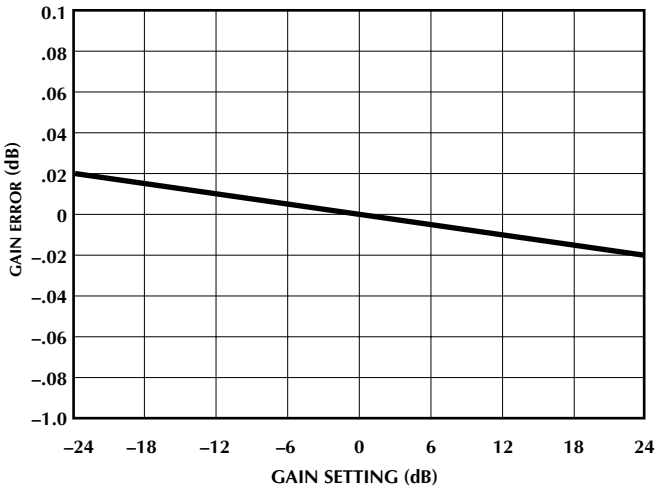


Figure 7. Gain Error vs Gain Setting

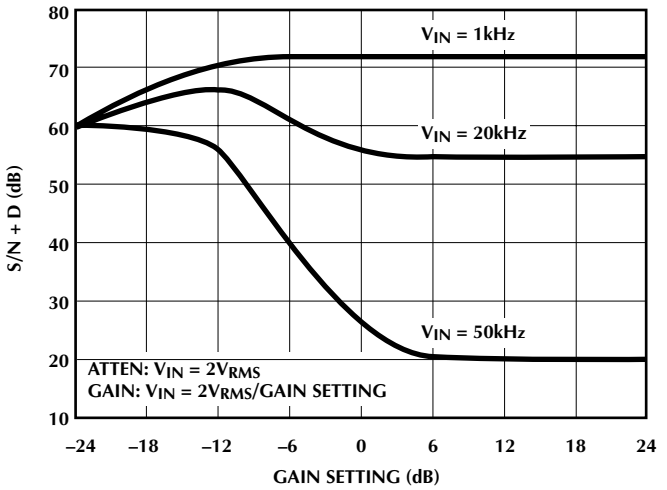


Figure 8. S/N +D vs Gain Setting (V_{IN}/V_{OUT} = 2V_{RMS})

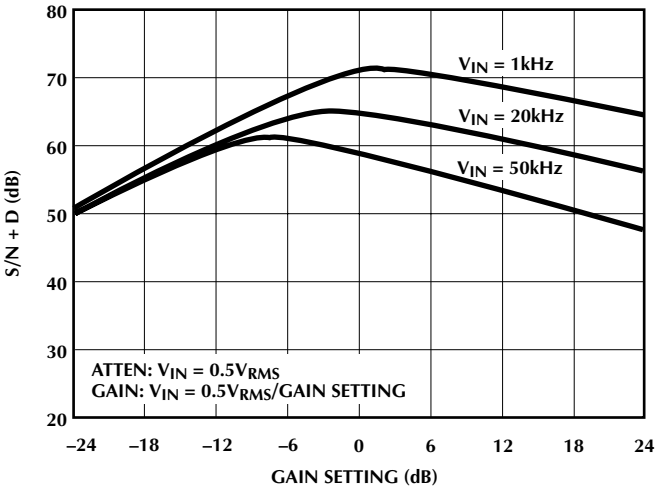


Figure 9. S/N +D vs Gain Setting (V_{IN}/V_{OUT} = 0.5V_{RMS})

1.0 FUNCTIONAL DESCRIPTION

The ML2008, ML2009 consists of a coarse gain stage, a fine gain stage, an output buffer, and a µP compatible parallel digital interface.

1.1 Gain Stages

The analog input, V_{IN}, goes directly into the op amp input in the coarse gain stage. The coarse gain stage has a gain range of 0 to 22.5dB in 1.5dB steps.

The fine gain stage is cascaded onto the coarse section. The fine gain stage has a gain range of 0 to 1.5dB in 0.1dB steps.

Both stages can be programmed for either gain or attenuation, thus doubling the effective gain range.

The logarithmic steps in each gains stage are generated by placing the input signal across a resistor string of 16 series resistors. Analog switches allow the voltage to be tapped from the resistor string at 16 points. The resistors are sized such that each output voltage is at the proper logarithmic ratio relative to the input signal at the top of the string. Attenuation is implemented by using the resistor string as a simple voltage divider, and gain is implemented by using the resistor string as a feedback resistor around an internal op amp.

1.2 Gain Settings

Since the coarse and fine gain stages are cascaded, their gains can be summed logarithmically. Thus, any gain from –24dB to +24dB in 0.1dB steps can be obtained by combining the coarse and fine gain setting to yield the

desired gain setting. The relationship between the register 0 and 1 bits and the corresponding analog gain values is shown in Tables 1 and 2. Note that C3-C0 select the coarse gain, F3-F0 select the fine gain, and ATTEN/$\overline{\text{GAIN}}$ selects either gain or attenuation.

1.3 Output Buffer

The final analog stage is the output buffer. This amplifier has internal gain of 1 and is designed to drive 600Ω, 100pF loads. Thus, it is suitable for driving a telephone hybrid circuit directly without any external amplifier.

1.4 Power Supplies

The digital section is powered between V_{CC} and GND, or 5V. The analog section is powered between V_{CC} and V_{SS} and uses AGND as the reference point, or ±5V.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100µV. However, AGND and GND should be tied together physically near the device and ideally close to the common power supply ground connection.

Typically, the power supply rejection of V_{CC} and V_{SS} to the analog output is greater than –60dB at 1KHz. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

Table 1. Fine Gain Settings (C3 – C0 = 0)

F3	F2	F1	F0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	0.0	0.0
0	0	0	1	–0.1	0.1
0	0	1	0	–0.2	0.2
0	0	1	1	–0.3	0.3
0	1	0	0	–0.4	0.4
0	1	0	1	–0.5	0.5
0	1	1	0	–0.6	0.6
0	1	1	1	–0.7	0.7
1	0	0	0	–0.8	0.8
1	0	0	1	–0.9	0.9
1	0	1	0	–1.0	1.0
1	0	1	1	–1.1	1.1
1	1	0	0	–1.2	1.2
1	1	0	1	–1.3	1.3
1	1	1	0	–1.4	1.4
1	1	1	1	–1.5	1.5

Table 2. Coarse Gain Settings (F3 – F0 = 0)

C3	C2	C1	C0	Ideal Gain (dB) ATTEN/GAIN = 1	Ideal Gain (dB) ATTEN/GAIN = 0
0	0	0	0	0.0	0.0
0	0	0	1	–1.5	1.5
0	0	1	0	–3.0	3.0
0	0	1	1	–4.5	4.5
0	1	0	0	–6.0	6.0
0	1	0	1	–7.5	7.5
0	1	1	0	–9.0	9.0
0	1	1	1	–10.5	10.5
1	0	0	0	–12.0	12.0
1	0	0	1	–13.5	13.5
1	0	1	0	–15.0	15.0
1	0	1	1	–16.5	16.5
1	1	0	0	–18.0	18.0
1	1	0	1	–19.5	19.5
1	1	1	0	–21.0	21.0
1	1	1	1	–22.5	22.5

2.0 DIGITAL INTERFACE

The architecture of the digital section is shown in the preceding black diagram.

The structure of the data registers or latches is shown in Figures 10 and 11 for the ML2008 and ML2009, respectively. The registers control the attenuation/gain setting bits and with the ML2008 the power down bit.

Tables 1 and 2 describe how the data word programs the gain.

The difference between the ML2008 and ML2009 is in the register structure. The ML2008 is an 8-bit data bus version. This device has one 8-bit register and one 2-bit register to store the 9 gain setting bits and 1 powerdown bit. Two write operations are necessary to program the full 10 data bits from eight external data pins. The address pin A0 controls which register is being written into. The powerdown bit, PDN, causes the device to be placed in powerdown. When PDN = 1, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, V_{OUT}, to a high impedance state. While the device is in powerdown, the digital section is still functional and the current data word remains stored in the registers. When PDN = 0, device is in normal operation.

The ML2009 is a 9-bit data bus version. This device has one 9-bit register to store the 9 gain setting bits. The full 9 data bits can be programmed with one write operation from nine external data pins.

The internal registers or latches are edge triggered. The data is transferred from the external pins to the register output on the rising edge of $\overline{\text{WR}}$. The address pin, A0, controls which register the data will be written into as shown in Figures 1 and 2. The $\overline{\text{CS}}$ control signal selects the device by allowing the $\overline{\text{WR}}$ signal to latch in the data only when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, $\overline{\text{WR}}$ is inhibited from latching in new data into the registers.

	D8	D7	D6	D5	D4	D3	D2	D1	BIT
A0 = 0	ATTEN/$\overline{GAIN}$	C3	C2	C1	C0	F3	F2	F1	REG 0
A0 = 1							P_{DN}	F0	REG 1

Figure 10. ML2008 Register Structure

D8	D7	D6	D5	D4	D3	D2	D1	D0	BIT
ATTEN/$\overline{GAIN}$	C3	C2	C1	C0	F3	F2	F1	F0	REG 0

Figure 11. ML2009 Register Structure

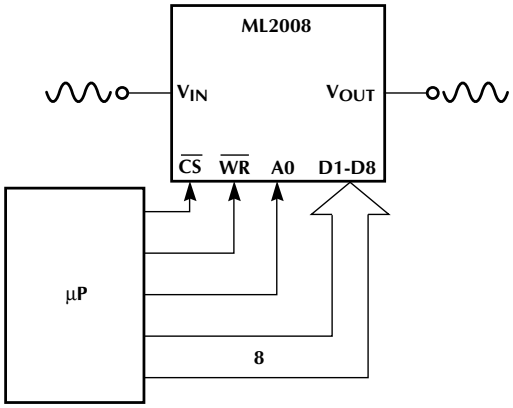


Figure 12. Typical 8-Bit µP Interface, Double Write

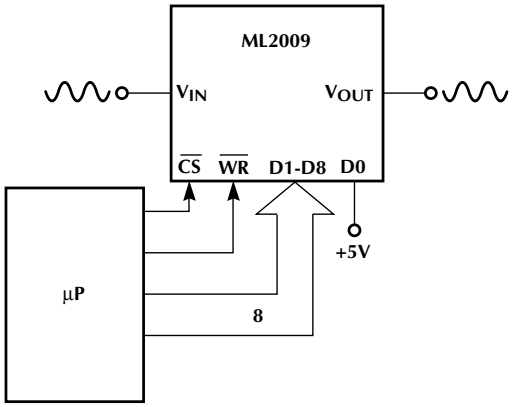


Figure 13. Typical 8-Bit µP Interface, Single Write

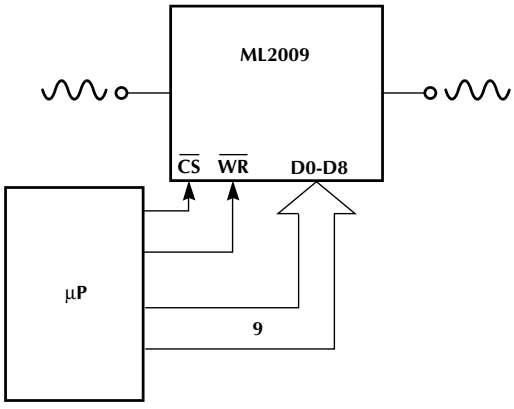


Figure 14. Typical 16-Bit µP Interface

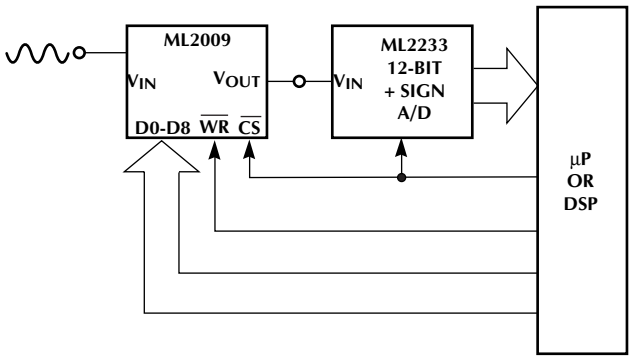


Figure 15. AGC for DSP or Modem Front End

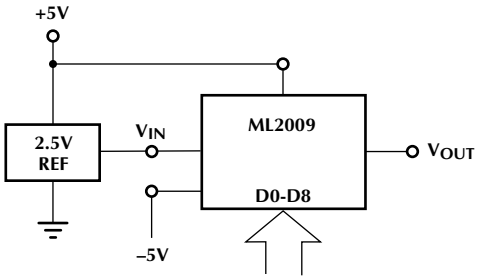


Figure 16. Operation as Logarithmic D/A Converter

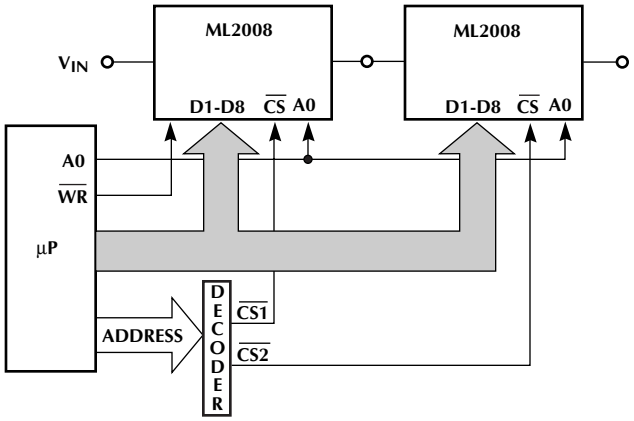
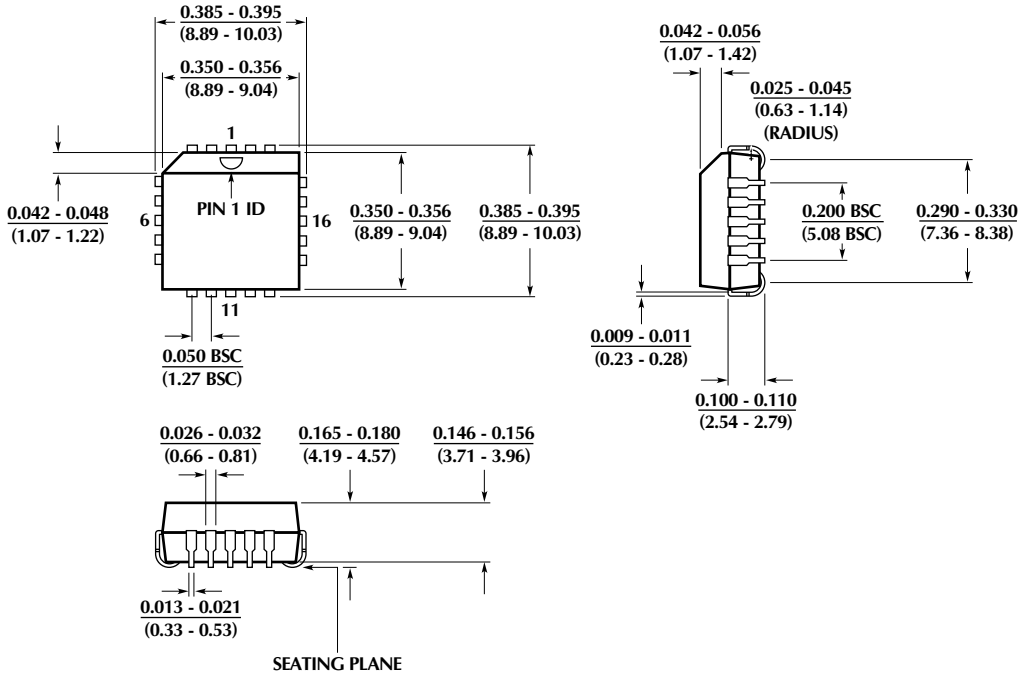


Figure 17. Controlling Multiple Gain/Attenuators

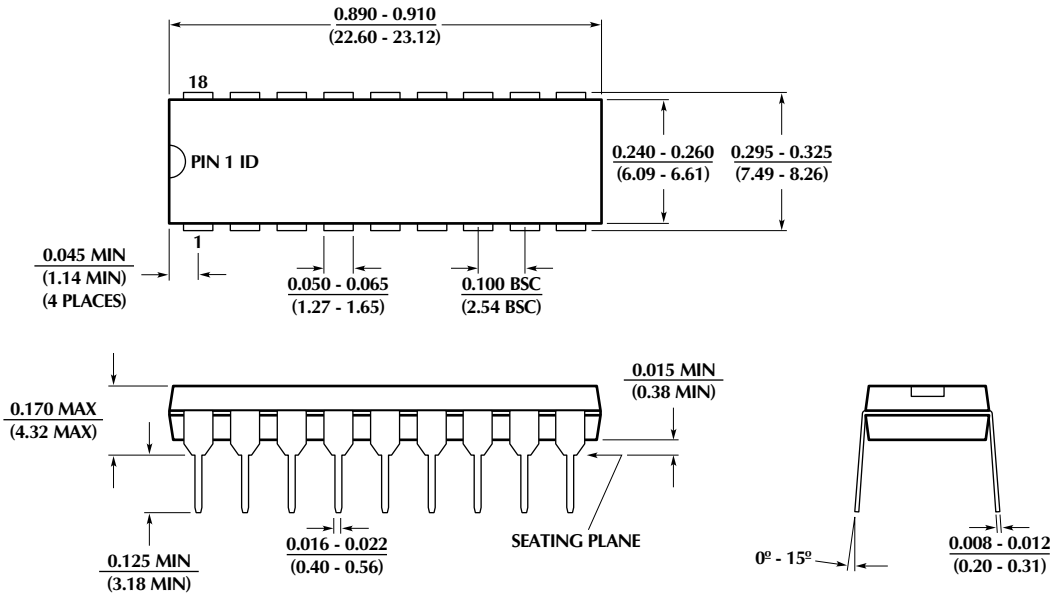
PHYSICAL DIMENSIONS inches (millimeters)

Package: Q20
20-Pin PLCC



PHYSICAL DIMENSIONS inches (millimeters)

Package: P18
18-Pin PDIP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2008IP	–40°C to 85°C	Molded PDIP (P18) (EOL)
ML2008IQ	–40°C to 85°C	Molded PLCC (Q20) (EOL)
ML2008CP	0°C to +70°C	Molded PDIP (P18) (EOL)
ML2008CQ	0°C to +70°C	Molded PLCC (Q20) (EOL)
ML2009IP	–40°C to 85°C	Molded PDIP (P18) (OBS)
ML2009IQ	–40°C to 85°C	Molded PLCC (Q20) (OBS)
ML2009CP	0°C to +70°C	Molded PDIP (P18) (OBS)
ML2009CQ	0°C to +70°C	Molded PLCC (Q20) (OBS)

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