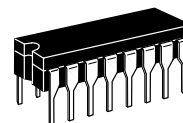


MC14504B

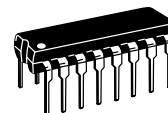
Hex Level Shifter for TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC} . The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

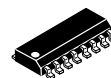
- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



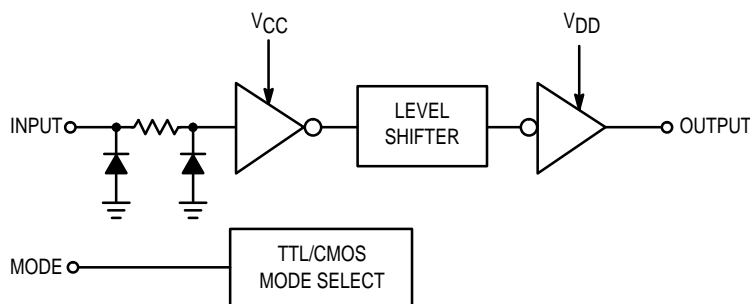
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.

LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

PIN ASSIGNMENT

V_{CC}	1	16	V_{DD}
A_{out}	2	15	F_{out}
A_{in}	3	14	F_{in}
B_{out}	4	13	MODE
B_{in}	5	12	E_{out}
C_{out}	6	11	E_{in}
C_{in}	7	10	D_{out}
V_{SS}	8	9	D_{in}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin, only. Extra precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18\text{ V}$ and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	- 0.5 to 18.0	V
V _{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in}	Input Voltage (DC or Transient)	- 0.5 to + 18.0	V
V _{out}	Output Voltage (DC or Transient)	- 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package*	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{CC} Vdc	V _{DD} Vdc	- 55°C		25°C			125°C		Unit	
				Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = 0 V	V _{OL}	—	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		—	10	—	0.05	—	0	0.05	—	0.05		
		—	15	—	0.05	—	0	0.05	—	0.05		
V _{in} = V _{CC}	V _{OH}	—	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		—	10	9.95	—	9.95	10	—	9.95	—		
		—	15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _{OL} = 1.0 Vdc) TTL-CMOS (V _{OL} = 1.5 Vdc) TTL-CMOS (V _{OL} = 1.0 Vdc) CMOS-CMOS (V _{OL} = 1.5 Vdc) CMOS-CMOS (V _{OL} = 1.5 Vdc) CMOS-CMOS	V _{IL}	5.0	10	—	0.8	—	1.3	0.8	—	0.8	Vdc	
		5.0	15	—	0.8	—	1.3	0.8	—	0.8		
		5.0	10	—	1.5	—	2.25	1.5	—	1.4		
		5.0	15	—	1.5	—	2.25	1.5	—	1.5		
		10	15	—	3.0	—	4.5	3.0	—	2.9		
		—	—	—	—	—	—	—	—	—		—
Input Voltage (V _{OH} = 9.0 Vdc) TTL-CMOS (V _{OH} = 13.5 Vdc) TTL-CMOS (V _{OH} = 9.0 Vdc) CMOS-CMOS (V _{OH} = 13.5 Vdc) CMOS-CMOS (V _{OH} = 13.5 Vdc) CMOS-CMOS	V _{IH}	5.0	10	2.0	—	2.0	1.5	—	2.0	—	Vdc	
		5.0	15	2.0	—	2.0	1.5	—	2.0	—		
		5.0	10	3.6	—	3.5	2.75	—	3.5	—		
		5.0	15	3.6	—	3.5	2.75	—	3.5	—		
		10	15	7.1	—	7.0	5.5	—	7.0	—		
		—	—	—	—	—	—	—	—	—		—
Output Drive Current (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	—	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc	
		—	5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		—	10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	—	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			—	10	1.6	—	1.3	2.25	—	0.9	—	
			—	15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	—	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) CMOS-CMOS Mode	I _{DD} or I _{CC}	—	5.0	—	0.05	—	0.0005	0.05	—	1.5	μAdc	
		—	10	—	0.10	—	0.0010	0.10	—	3.0		
		—	15	—	0.20	—	0.0015	0.20	—	6.0		
Quiescent Current (Per Package) TTL-CMOS Mode	I _{DD}	5.0	5.0	—	0.5	—	0.0005	0.5	—	3.8	μAdc	
		5.0	10	—	1.0	—	0.0010	1.0	—	7.5		
		5.0	15	—	2.0	—	0.0015	2.0	—	15		
Quiescent Current (Per Package) TTL-CMOS Mode	I _{CC}	5.0	5.0	—	5.0	—	2.5	5.0	—	6.0	mAdc	
		5.0	10	—	5.0	—	2.5	5.0	—	6.0		
		5.0	15	—	5.0	—	2.5	5.0	—	6.0		

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits			Unit
					Min	Typ #	Max	
Propagation Delay, High to Low	t_{PHL}	TTL – CMOS $V_{DD} > V_{CC}$	5.0	10	—	140	280	ns
			5.0	15	—	140	280	
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0	10	—	120	240	
			5.0	15	—	120	240	
			10	15	—	70	140	
		CMOS – CMOS $V_{CC} > V_{DD}$	10	5.0	—	185	370	
15	5.0		—	185	370			
15	10		—	175	350			
Propagation Delay, Low to High	t_{PLH}	TTL – CMOS $V_{DD} > V_{CC}$	5.0	10	—	170	340	ns
			5.0	15	—	160	320	
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0	10	—	170	340	
			5.0	15	—	170	340	
			10	15	—	100	200	
		CMOS – CMOS $V_{CC} > V_{DD}$	10	5.0	—	275	550	
15	5.0		—	275	550			
15	10		—	145	290			
Output Rise and Fall Time	t_{TLH} , t_{THL}	ALL	—	5.0	—	100	200	ns
			—	10	—	50	100	
			—	15	—	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

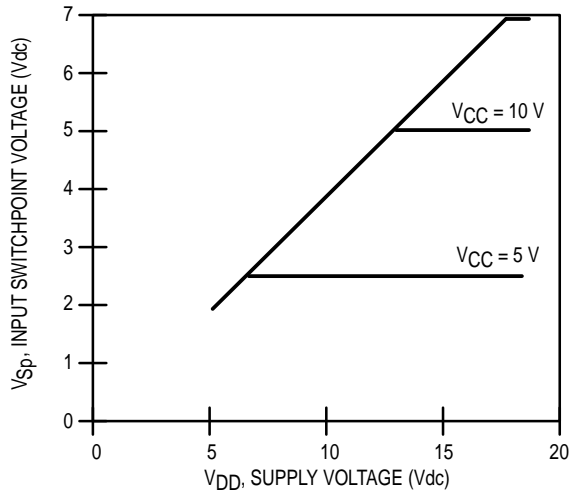


Figure 1. Input Switchpoint CMOS to CMOS Mode

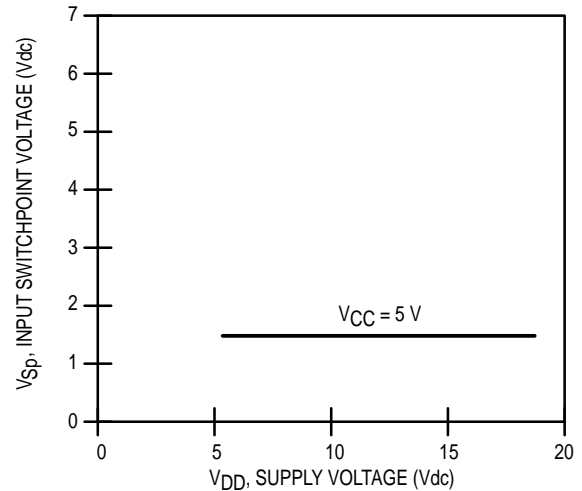


Figure 2. Input Switchpoint TTL to CMOS Mode

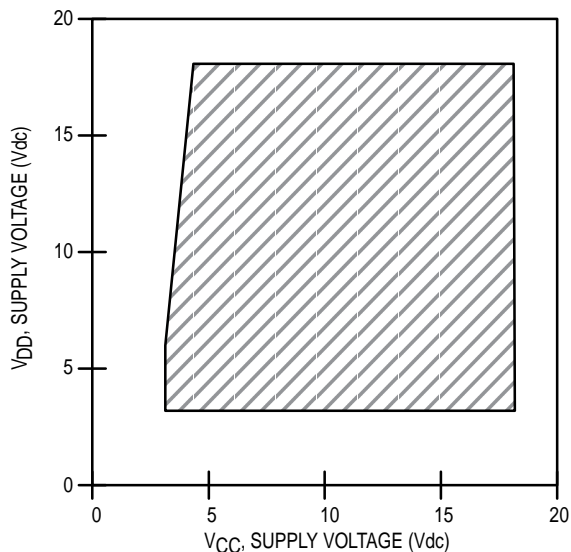


Figure 3. Operating Boundary CMOS to CMOS Mode

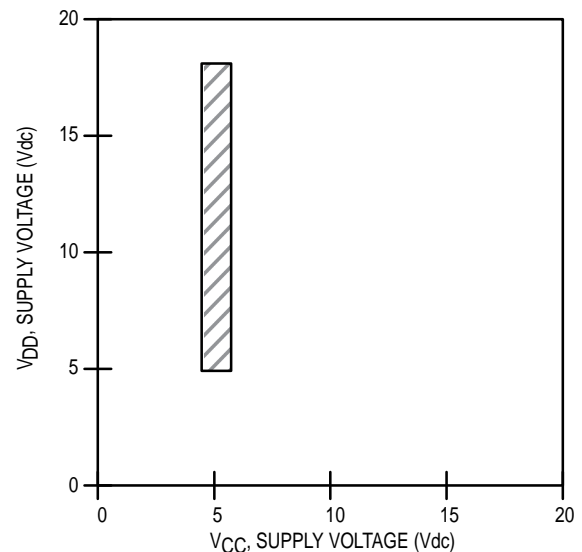
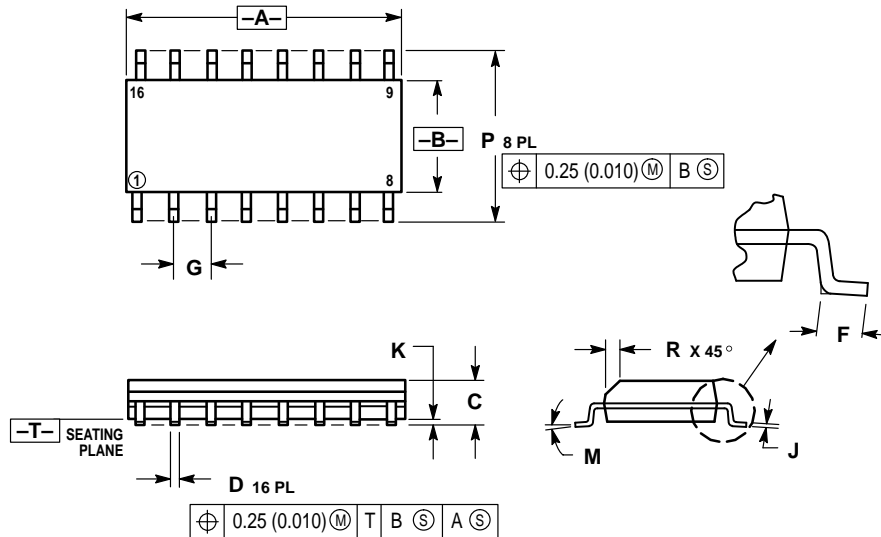


Figure 4. Operating Boundary TTL to CMOS Mode

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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