Micro Linear

ML2252*, ML2259**

µP Compatible 8-Bit A/D Converters with 2- or 8-Channel Multiplexer

GENERAL DESCRIPTION

The ML2252 and ML2259 combine an 8-bit A/D converter, 2- or 8-channel analog multiplexer, and a microprocessor compatible 8-bit parallel interface and control logic in a single monolithic CMOS device.

Easy interface to microprocessors is provided by the latched and decoded multiplexer address inputs and a double buffered three-state data bus. These analog-to-digital converters allow the microprocessor to operate completely asynchronous to the converter clock.

The built in sample and hold function provides the ability to digitize a 5V, 50kHz sinewave to 8-bit accuracy. The differential comparator design provides low power supply sensitivity to DC and AC variations. The voltage reference can be externally set to any value between ground and V_{CC}, thus allowing a full conversion over a relatively small span. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

The device is suitable for a wide range of applications from process and machine control to consumer, automotive, and telecommunication applications.

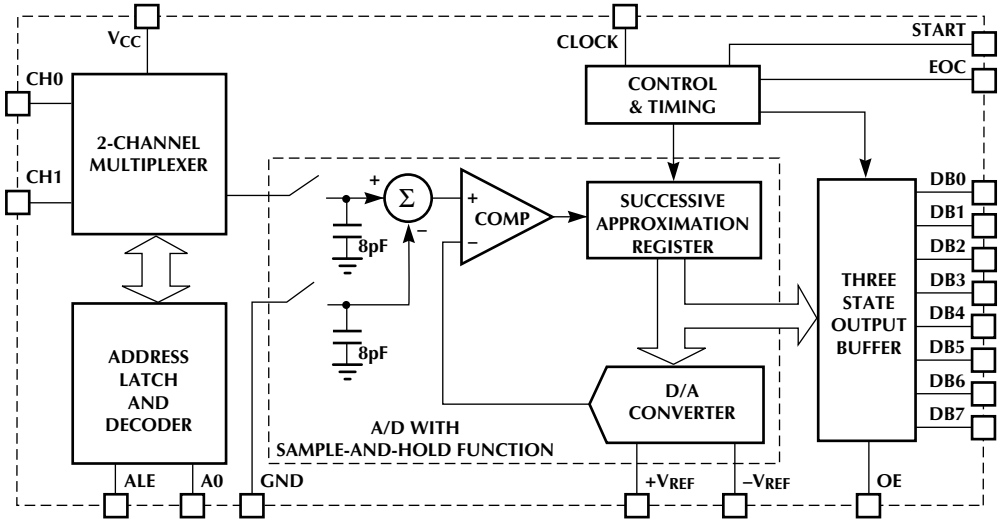
FEATURES

- Conversion time (f_{CLK} = 1.46MHz); 6.6µs
- Total unadjusted error; ±1/2LSB or ±1LSB
- No missing codes
- Sample and hold; 390ns acquisition
- Capable of digitizing a 5V, 50kHz sinewave
- 2- or 8-channel input multiplexer
- 0V to 5V analog input range with single 5V power supply
- Operates ratiometrically or with up to 5V voltage reference
- No zero or full scale adjust required
- Analog input protection; 25mA per input min
- Continuous conversion mode
- Low power dissipation; 15mW max
- TTL and CMOS compatible digital inputs and outputs

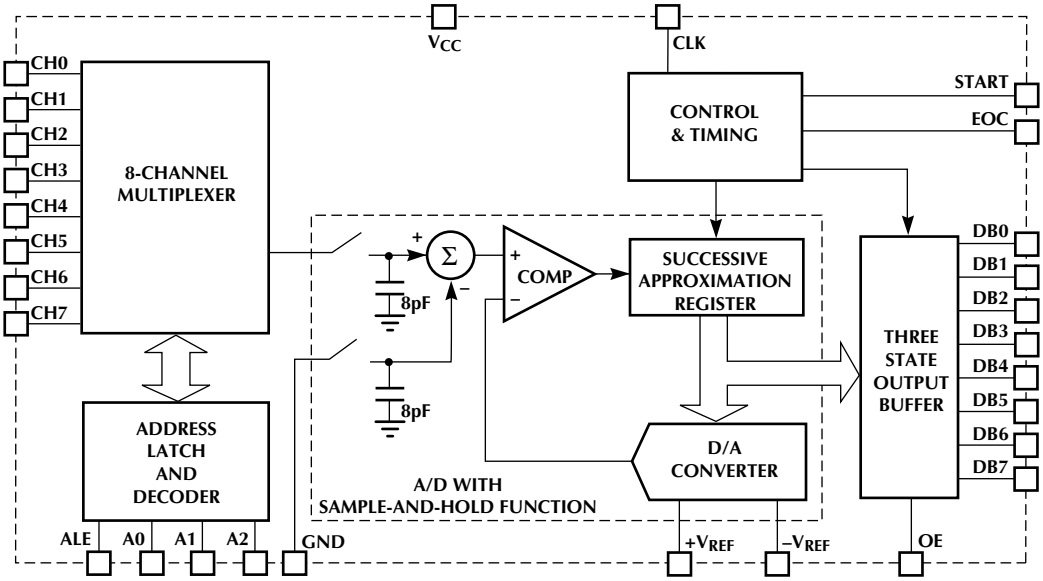
ML2252 BLOCK DIAGRAM

* This Part Is Obsolete

** This Part Is End of Life As Of August 1, 2000

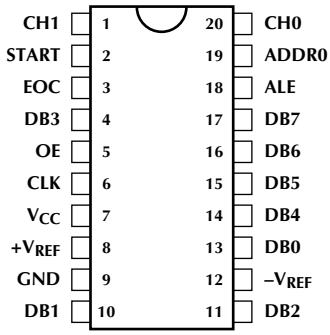


ML2259 BLOCK DIAGRAM



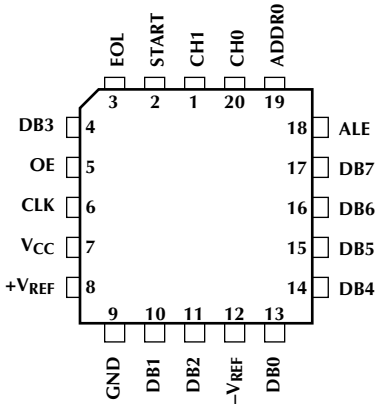
PIN CONFIGURATION

ML2252
20-Pin DIP (P20)



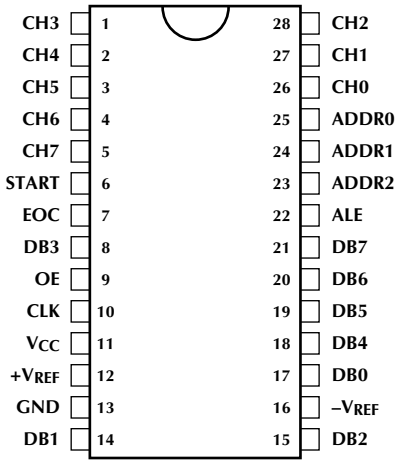
TOP VIEW

ML2252
20-Pin PLCC (Q20)



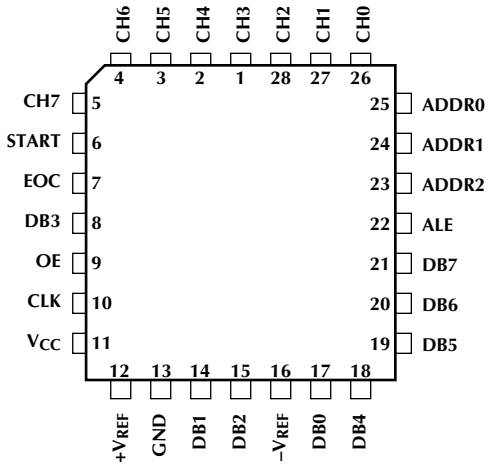
TOP VIEW

ML2259
28-Pin DIP(P28W)



TOP VIEW

ML2259
28-Pin PLCC (Q28)



TOP VIEW

PIN DESCRIPTION

Pin Number ML2252	Pin Number ML2259	Name	Function
	1	CH3	Analog input 3.
	2	CH4	Analog input 4.
	3	CH5	Analog input 5.
	4	CH6	Analog input 6.
	5	CH7	Analog input 7.
2	6	START	Start of conversion. Active high digital input pulse initiates conversion.
3	7	EOC	End of conversion. This output goes low after a START pulse occurs, stays low for the entire A/D conversion, and goes high after conversion is completed. Data on DB0–DB7 is valid on rising edge of EOC and stays valid until next EOC rising edge.
4	8	DB3	Data output 3.
5	9	OE	Output enable input. When OE = 0, DB0–DB7 are in high impedance state; OE = 1, DB0–DB7 are active outputs.
6	10	CLK	Clock. Clock input provides timing for A/D converter, S/H, and digital interface.
7	11	V_{CC}	Positive supply. 5V ±10%.
8	12	$+V_{REF}$	Positive reference voltage.
9	13	GND	Ground. 0V, all analog and digital inputs or outputs are referenced to this point.
10	14	DB1	Data output 1.
11	15	DB2	Data output 2.
12	16	$-V_{REF}$	Negative reference voltage.
13	17	DB0	Data output 0.
14	18	DB4	Data output 4.
15	19	DB5	Data output 5.
16	20	DB6	Data output 6.
17	21	DB7	Data output 7.
18	22	ALE	Address latch enable. Input to latch in the digital address (ADDR2-0) on the rising edge of the multiplexer.
	23	ADDR2	Address input 2 to multiplexer. Digital input for selecting analog input.
	24	ADDR1	Address input 1 to multiplexer. Digital input for selecting analog input.
19	25	ADDR0	Address input 0 to multiplexer. Digital input for selecting analog input.
20	26	CH0	Analog input 0.
1	27	CH1	Analog input 1.
	28	CH2	Analog input 2.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage, V_{CC} 6.5V
Logic Inputs ..... –0.3V to V_{CC} 0.3V
Analog Inputs ..... –0.3V to V_{CC} 0.3V
Input Current per Pin ..... ±25mA
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C

Thermal Resistance (θ_{JA})
20-Pin PDIP ..... 67°C/W
20-Pin PLCC ..... 78°C/W
28 Pin PDIP ..... 48°C/W
28-Pin PLCC ..... 68°C/W

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 4.5V to 6.3V
Temperature Range ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = +V_{REF} = 5V ±10%, –V_{REF} = GND, f_{CLK} = 1.46MHz, T_A = Operating temperature range (Note 1)

PARAMETER	CONDITIONS	ML2252B, ML2259B			ML2252C, ML2259C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Converter and Multiplexer Characteristics								
Total Unadjusted Error	V_{REF} = V_{CC}, (Note 2)			±1/2			±1	LSB
+V_{REF} Voltage Range		–V_{REF}		V_{CC} + 0.1	–V_{REF}		V_{CC} + 0.1	V
–V_{REF} Voltage Range		GND – 0.1		+V_{REF}	GND – 0.1		+V_{REF}	V
Reference Input Resistance		14	20	35	14	20	28	k ý
Analog Input Range	(Note 3)	GND – 0.1		V_{CC} + 0.1	GND – 0.1		V_{CC} + 0.1	V
Power Supply Sensitivity	DC, V_{CC} = 5V ±10%		±1/32	±1/4		±1/32	±1/4	LSB
	100mVp-p, 100kHz Sine on V_{CC}, V_{IN} = 0		±1/16			±1/16		LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = V_{CC}, (Note 4) Off Channel = 0V	–1			–1			µA
	On Channel = 0V, (Note 4) Off Channel = V_{CC}			1			1	µA
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 0V, (Note 4) Off Channel = V_{CC}	–1			–1			µA
	On Channel = V_{CC}, (Note 4) Off Channel = 0V			1			1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital and DC						
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = V_{CC}			1	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	–1			µA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = –2mA	4.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 2mA			0.4	V
I_{OUT}	Three-State Output Current	V_{OUT} = 0V	–1			µA
		V_{OUT} = V_{CC}			1	µA
I_{CC}	Supply Current			1.5	3	mA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC and Dynamic Performance Characteristics (Note 5)						
t_{ACQ}	Sample and Hold Acquisition			1/2		$1/f_{CLK}$
f_{CLK}	Clock Frequency		10		1460	kHz
t_C	Conversion Time			8.5	8.5 + 250ns	$1/f_{CLK}$
SNR	Signal to Noise Ratio	V_{IN} = 51kHz, 5V sine. f_{CLK} = 1.46MHz ($f_{SAMPLING}$ > 150kHz). Noise is sum of all nonfundamental components up to 1/2 of $f_{SAMPLING}$		47		dB
THD	Total Harmonic Distortion	V_{IN} = 51kHz, 5V sine. f_{CLK} = 1.46MHz ($f_{SAMPLING}$ > 150kHz). THD is sum 2, 3, 4, 5 harmonics relative to fundamental		–60		dB
IMD	Intermodulation Distortion	$V_{IN} = f_A + f_B$. f_A = 49kHz, 2.5V sine. f_B = 47.8kHz, 2.5V sine, f_{CLK} = 1.46MHz ($f_{SAMPLING}$ > 150kHz). IMD is ($f_A + f_B$), ($f_A - f_B$), ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), ($f_A - 2f_B$) relative to fundamental		–60		dB
FR	Frequency Response	V_{IN} = 0 to 50kHz. 5V sine relative to 1kHz		0.1		dB
t_{DC}	Clock Duty Cycle	(Note 6)	40		60	%
t_{EOC}	End of Conversion Delay			1/2	1/2 + 250ns	$1/f_{CLK}$
t_{WS}	Start Pulse Width		50			ns
t_{SS}	Start Pulse Setup Time	Synchronous only, (Note 7)	40			ns
t_{WALE}	Address Latch Enable Pulse Width		50			ns
t_S	Address Setup		0			ns
t_H	Address Hold		50			ns
$t_{H1, H0}$	Output Enable for DB0–DB7	Figure 1, C_L = 50pF			100	ns
		Figure 1, C_L = 10pF			50	ns
$t_{1H, 0H}$	Output Disable for DB0–DB7	Figure 1, C_L = 50pF			100	ns
		Figure 1, C_L = 10pF			50	ns
C_{IN}	Capacitance of Logic Input			5		pF
C_{OUT}	Capacitance of Logic Outputs			10		pF

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Total unadjusted error includes offset, full scale, linearity, multiplexer and sample and hold errors.

Note 3: For $-V_{REF} \bullet V_{IN}$ (+) the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allow 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

Note 4: Leakage current is measured with the clock not switching.

Note 5: C_L = 50pF, timing measured at 50% point.

Note 6: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 40ns. The maximum time the clock can be high or low is 60µs.

Note 7: The conversion start setup time requirement only needs to be satisfied if a conversion must be synchronized to a given clock rising edge. If the setup time is not met, start conversion will have an uncertainty of one clock pulse.

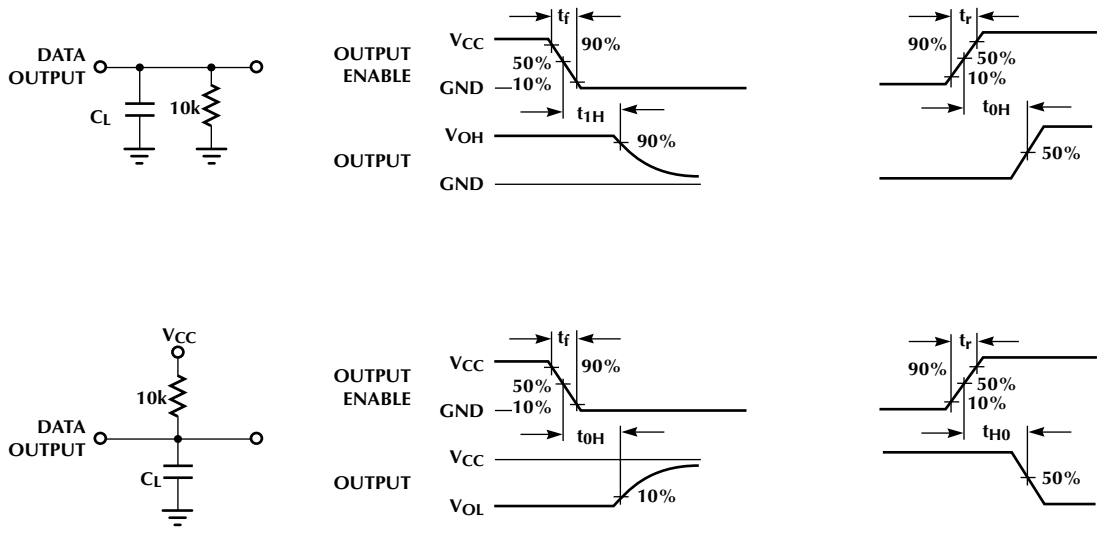


Figure 1. High Impedance Test Circuits and Waveforms

TYPICAL PERFORMANCE CURVES

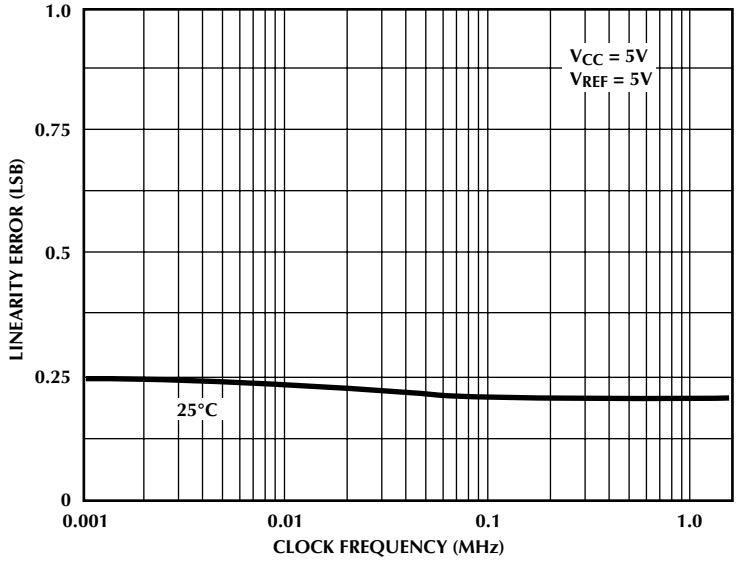


Figure 2. Linearity Error vs f_{CLK}

TYPICAL PERFORMANCE CURVES (Continued)

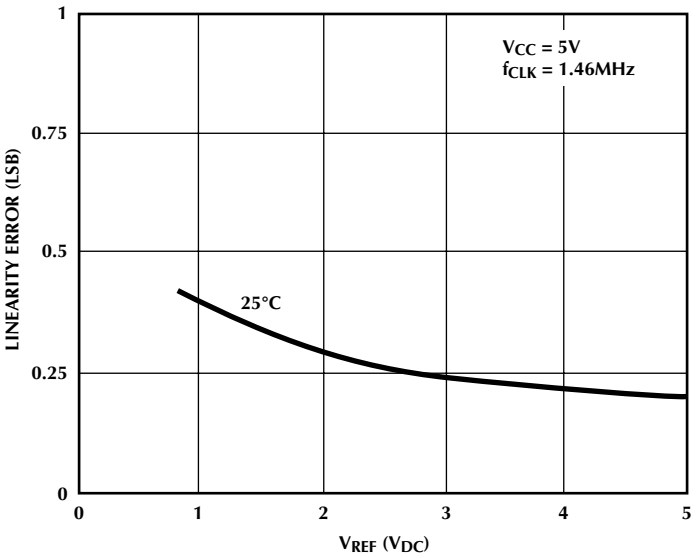


Figure 3. Linearity Error vs V_{REF} Voltage

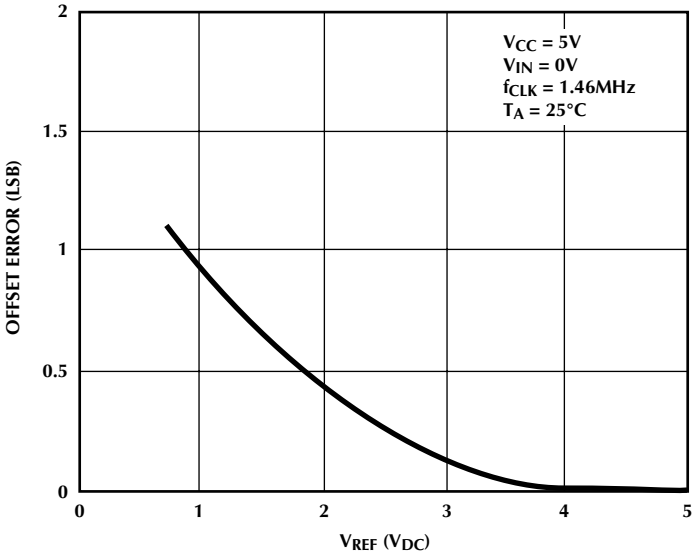


Figure 4. Unadjusted Offset Error vs V_{REF} Voltage

1.0 FUNCTIONAL DESCRIPTION

1.1 MULTIPLEXER ADDRESSING

The ML2252 and ML2259 contain a single ended analog multiplexer. A particular input channel is selected by using the address decoder. The relationship between the address inputs, ADDR0–ADDR2, and the analog input selected is shown in Table 1. The address inputs are latched into the decoder on the rising edge of the address latch signal ALE.

ML2252

SELECTED ANALOG CHANNEL	ADDRESS INPUT
CH0	0
CH1	1

ML2259

SELECTED ANALOG CHANNEL	ADDRESS INPUT		
	ADDR2	ADDR1	ADDR0
CH0	0	0	0
CH1	0	0	1
CH2	0	1	0
CH3	0	1	1
CH4	1	0	0
CH5	1	0	1
CH6	1	1	0
CH7	1	1	1

Table 1. Multiplexer Address Decoding

1.2 A/D CONVERTER

The A/D converter uses successive approximation to perform the conversion. The converter is composed of the successive approximation register, the DAC and the comparator.

The DAC generates the precise levels that determine the linearity and accuracy of the conversion. The DAC is composed of a capacitor upper array and a resistor lower array. The capacitor upper array generates the 4 MSB decision levels while the series resistor lower array generates the 4 LSB decision levels. A switch decoder tree is used to decode the proper level from both arrays.

The capacitor/resistor array offers fast conversion, superior linearity and accuracy since matching is only required between $2^4 = 16$ elements (as opposed to $2^8 = 256$ elements in conventional designs). And since the levels are based on the ratio of capacitors to capacitors and resistors to resistors, the accuracy and long term stability of the converter is improved. This also guarantees monotonicity and no missing codes, as well as eliminating any linearity temperature or power supply dependence.

The successive approximation register is a digital block used to store the bit decisions from the conversion.

The comparator design is unique in that it is fully differential and auto zeroed. The fully differential architecture provides excellent noise immunity, excellent power supply rejection, and wide common mode range. The comparator is auto zeroed at the start of each conversion in order to remove any DC offset and full scale gain error, thus improving accuracy and linearity.

Another advantage of the capacitor array approach used in the ML2252 and ML2259 is the inherent sample-and-hold function. This true S/H allows an accurate conversion to be done on the input even if the analog signal is not stable. Linearity and accuracy are maintained for analog signals up to 1/2 the sampling frequency. As a result, input signals up to 50kHz can be converted without degradation in linearity or accuracy.

The sequence of events during a conversion is shown in figure 5. The rising edge of a START pulse resets the internal registers and initiates a conversion on the next rising edge of CLK providing that (t_{SS}) start pulse setup time is satisfied. If this setup time is not met, start conversion will have an uncertainty of one clock pulse. The input is then sampled for the next half CLK period until EOC goes low. EOC goes low on the falling edge of the next CLK pulse indicating that the conversion is now beginning. The actual conversion now takes place for the next eight CLK pulses, one bit for each CLK pulse. After the conversion is done, the data is updated on DB0–DB7 and EOC goes high on the rising edge of the 9th CLK pulse, indicating that the conversion has been completed and data is valid on DB0–DB7. The data will stay valid on DB0–DB7 until the next conversion updates the data word on the next rising edge of EOC.

A conversion can be interrupted and restarted at any time by a new START pulse.

1.3 ANALOG INPUTS AND SAMPLE/HOLD

The ML2252 and ML2259 have a true sample-and-hold circuit which samples both the selected input and ground simultaneously. These analog to digital converters can reject AC common mode signals from DC–50kHz as well as maintain linearity for signals from DC–50kHz.

The plot in Figure 6 shows a 2048 point FFT of the ML2259 converting a 50kHz, 0 to 5V, low distortion sine wave input. The ML2252 and ML2259 sample and digitize, at their specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 50kHz.

The signal at the analog input is sampled during the interval when the sampling switch is open prior to conversion start. The sampling window (S/H acquisition time) is one half CLK period long and occurs one half CLK period after START goes low. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. One half CLK period later, the sampling switch opens, the signal present at analog input is stored and conversion starts. Since any error on the analog input at the end of the S/H acquisition time will cause additional conversion error, care should be taken to insure adequate settling and charging time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

Each analog input has dual diodes to the supply rails, and a minimum of ±25mA (±100mA typically) can be injected into each analog input without causing latchup.

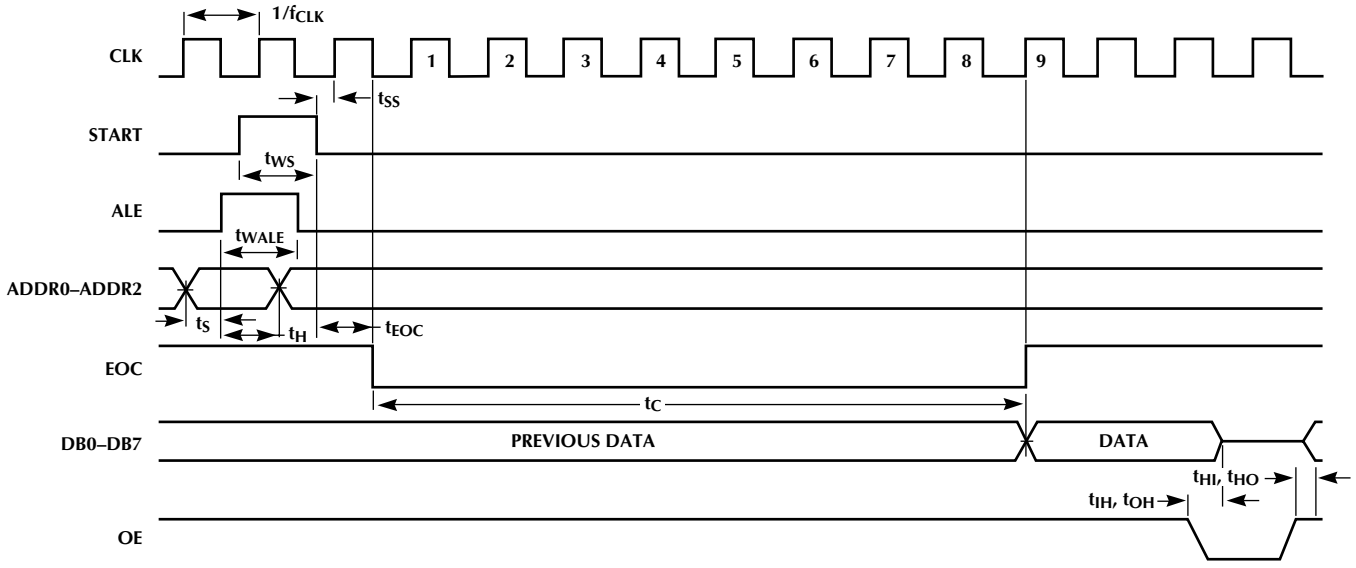


Figure 5. Timing Diagram

1.4 REFERENCE

The voltage applied to the $+V_{REF}$ and $-V_{REF}$ inputs defines the voltage span of the analog input (the difference between V_{INMAX} and V_{INMIN}) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the reference input resistance, typically 20k.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $+V_{REF}$ pin can be tied to V_{CC} and $-V_{REF}$ tied to GND. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference pins can be biased with a time and temperature stable voltage source.

$+V_{REF}$ and $-V_{REF}$ can be at any voltage between V_{CC} and GND. In addition, the difference between $+V_{REF}$ and $-V_{REF}$ can be set to small values for conversions over smaller voltage ranges. Particular care must be taken with regard to noise pickup, circuit layout ond system error voltage sources when operating with a reduced span due to the increased sensitivity converter.

1.5 POWER SUPPLY AND REFERENCE DECOUPLING

A 10µF electrolytic capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible. In addition, with clock frequencies above 1MHz, a 0.1µF ceramic disc capacitor should be used to bypass V_{CC} to GND.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1µF ceramic disc capacitors at the reference input pins (pins 12, 16).

1.6 DYNAMIC PERFORMANCE

Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92dB.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2252 and ML2259 are defined as

$$20\log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

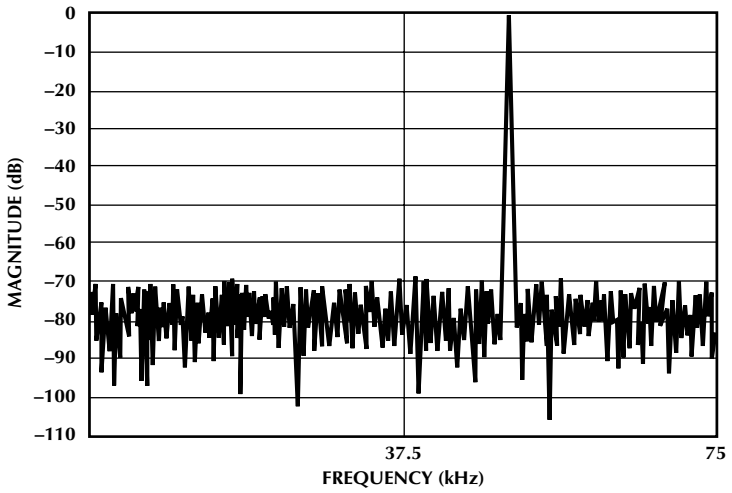


Figure 6. Output Spectrum

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3,... . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$) and ($f_A - 2f_B$) only.

1.7 DIGITAL INTERFACE

The analog inputs are selected by the digital addresses, ADDR0–ADDR2, and latched on the rising edge of ALE. This is described in the Multiplexer Addressing section.

A conversion is initiated by the rising edge of a START pulse. As long as this pulse is high, the internal logic is reset.

The sampling interval starts with the following CLK rising edge after a START falling edge and ends on the falling edge of CLK. The conversion starts and EOC goes low. The sampling clock is at least one half CLK period wide. Each bit conversion in the successive approximation process takes 1 CLK period. On the rising edge of the ninth CLK pulse, the digital output of the conversion is updated on the outputs DB0–DB7 and EOC goes high indicating the conversion is done and data on DB0–DB7 is valid.

One feature of the ML2252 and ML2259 is that the data is double buffered. This means that the outputs DB0–DB7 will stay valid until updated at the end of the next conversion and will not become invalid when the next conversion starts. This facilitates interfacing with external logic of µP.

The signal OE drives the data bus, DB0–DB7, into the high impedance state when held low. This allows the ML2252 and ML2259 to be tied directly to a µP system bus without any latches or buffers.

1.7.1 Restart During Conversion

If the A/D is restarted (start goes low and returns high) during a convesion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed. EOC will remain low and the output data latch is not updated.

1.7.2 Continuous Conversions

In the free-running, continuous conversion mode, the start input is tied to the (figure 7) EOC output. An initialization pulse, following power-up, of mementarily forcing a logic high level is required to guarantee operation.

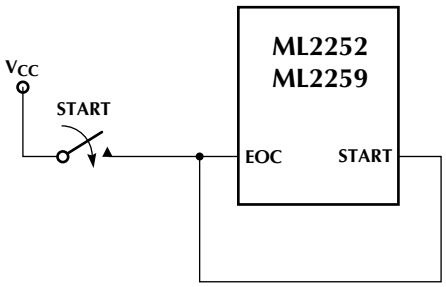


Figure 7. Continuous Conversion Mode

2.0 TYPICAL APPLICATIONS

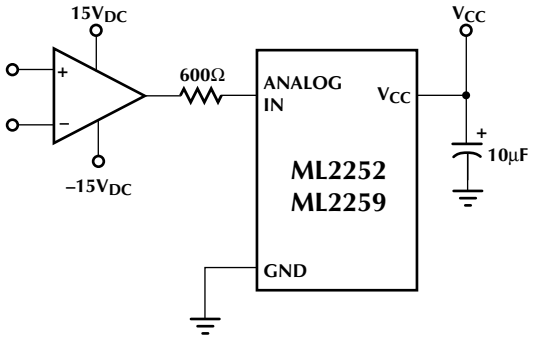


Figure 8. Protecting the Input

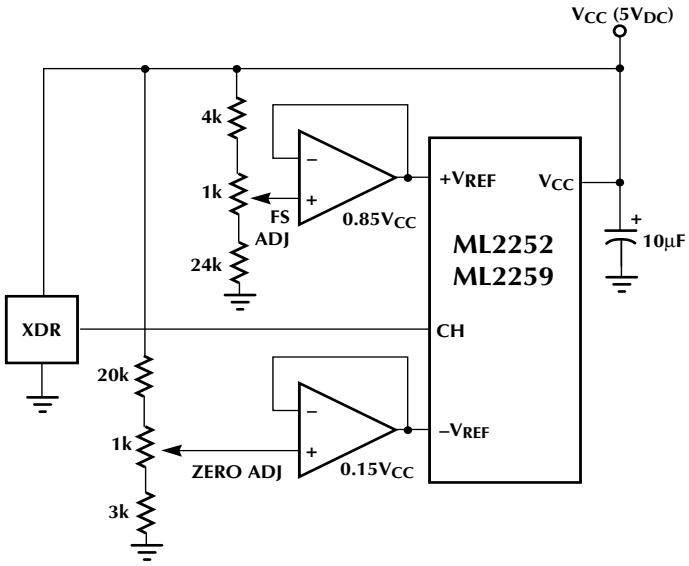
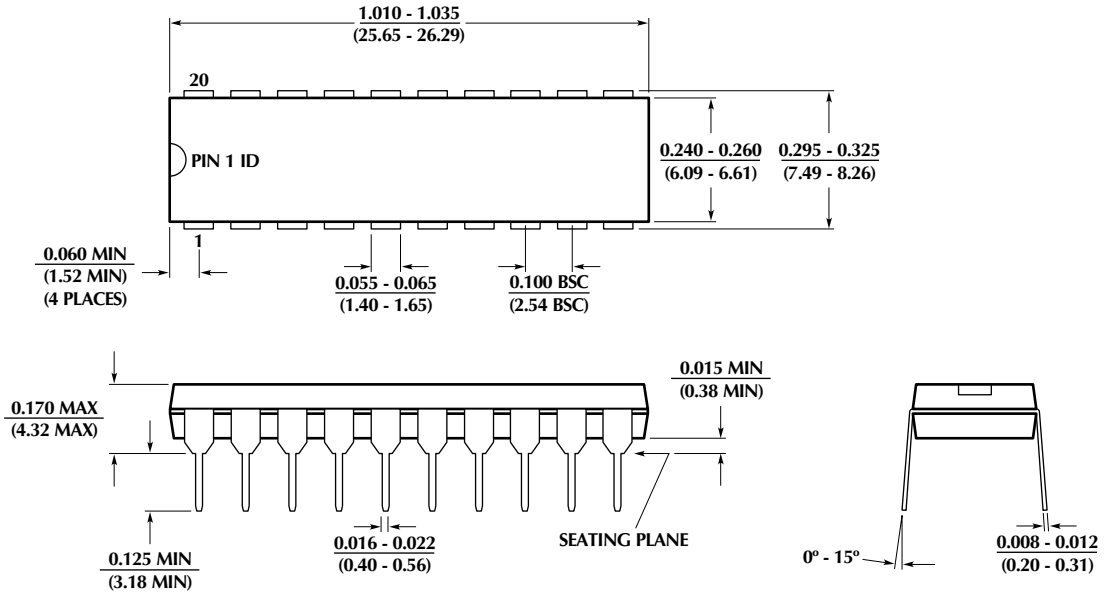


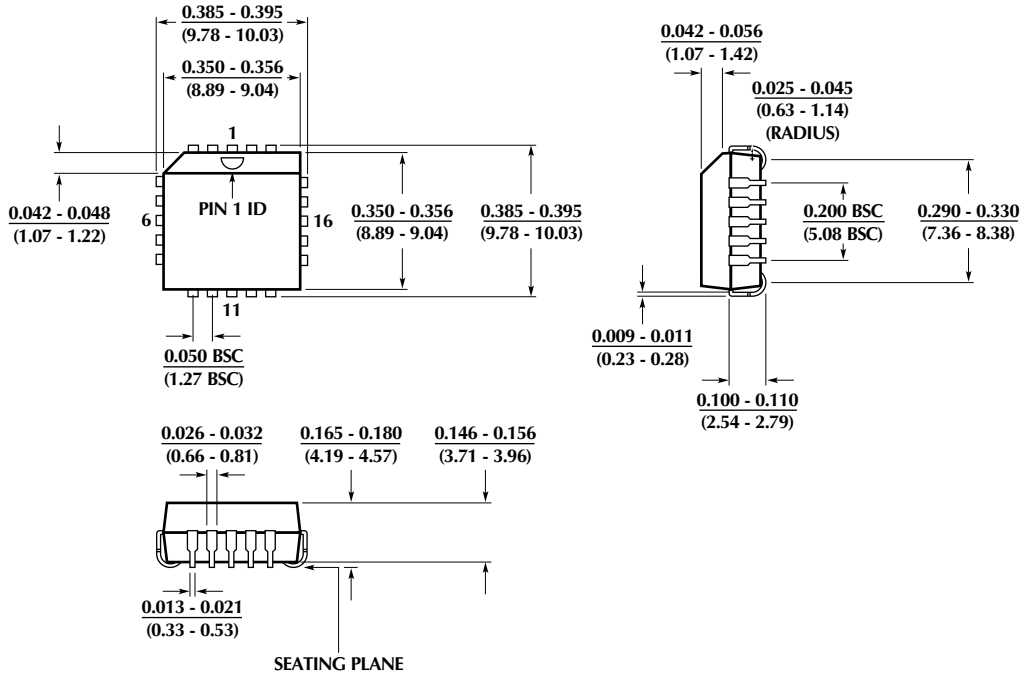
Figure 9. Operating with Ratiometric Transducers 15% of V_{CC} - V_{XDR} - 85% of V_{CC}

PHYSICAL DIMENSIONS inches (millimeters)

Package: P20
20-Pin PDIP

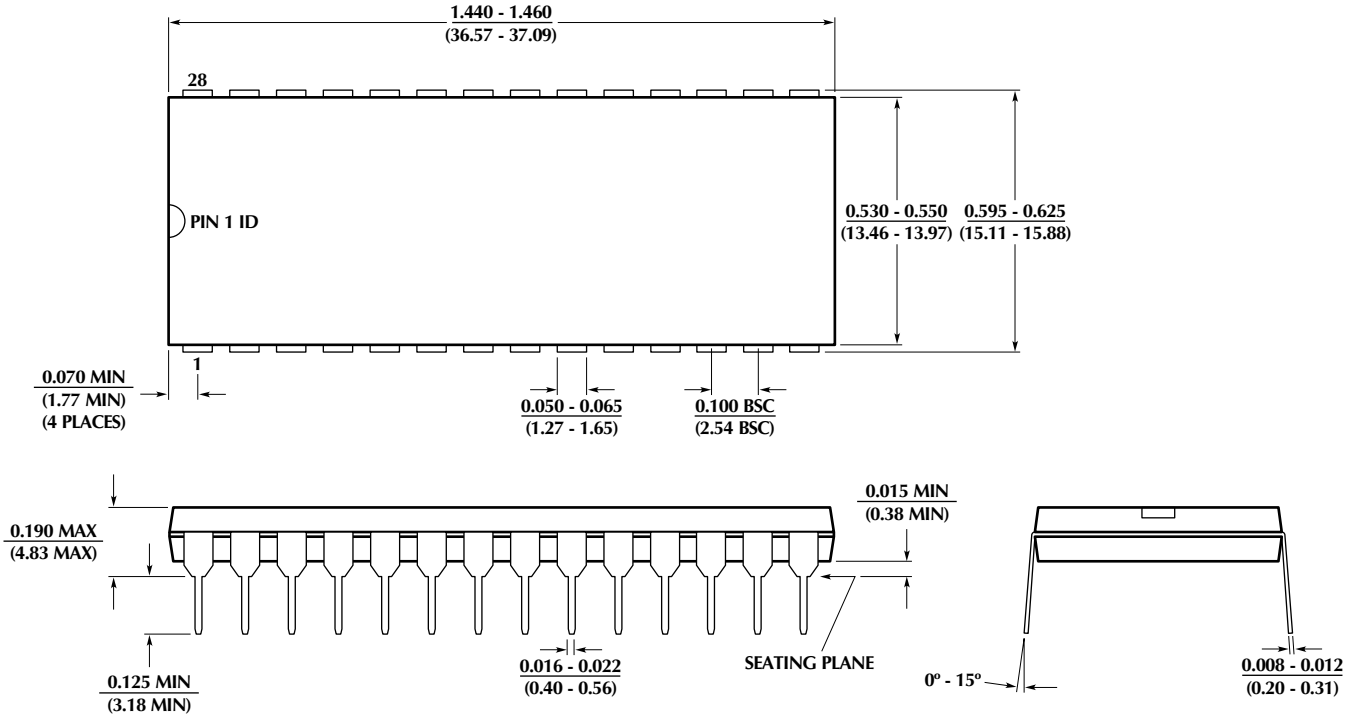


Package: Q20
20-Pin PLCC

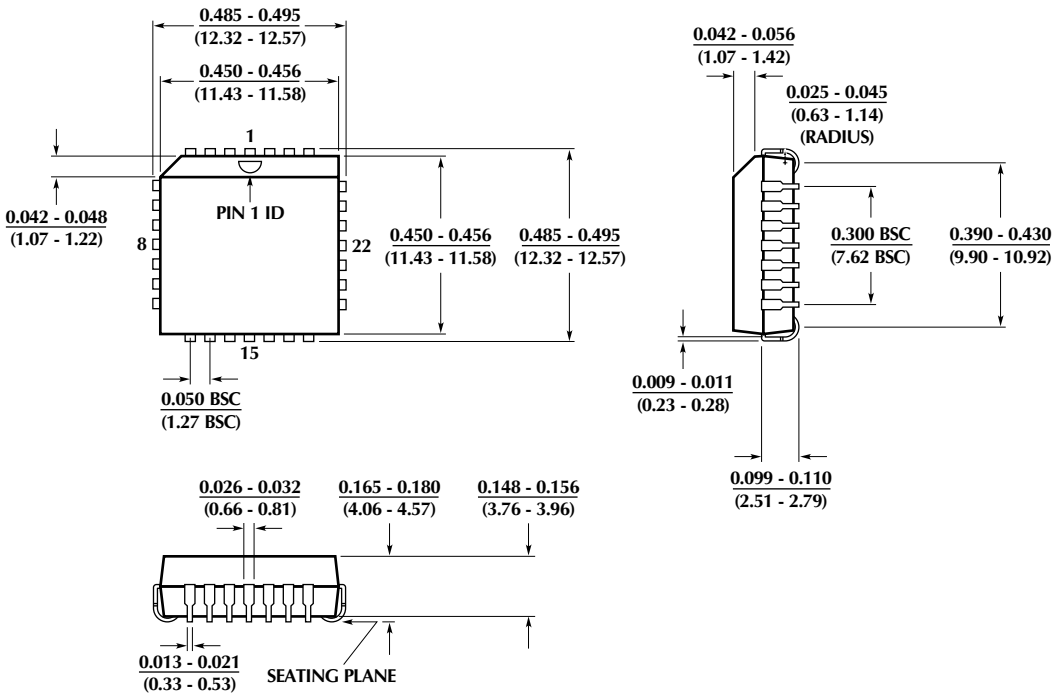


PHYSICAL DIMENSIONS inches (millimeters) (Continued)

Package: P28W
28-Pin Wide PDIP



Package: Q28
28-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
Two Analog Inputs, 20-Pin Package			
ML2252BCP (OBS)	±1/2 LSB	0°C to 70°C	Molded DIP (P20)
ML2252BCQ (OBS)		0°C to 70°C	Molded PLCC (Q20)
ML2252CCP (OBS)	±1 LSB	0°C to 70°C	Molded DIP (P20)
ML2252CCQ (OBS)		0°C to 70°C	Molded PLCC (Q20)
Eight Analog Inputs, 28-Pin Package			
ML2259BCP (EOL)	±1/2 LSB	0°C to 70°C	Molded DIP (Q28)
ML2259BCQ (OBS)		0°C to 70°C	Molded PLCC (Q28)
ML2259CCP (OBS)	±1 LSB	0°C to 70°C	Molded DIP (P28W)
ML2259CCQ (OBS)		0°C to 70°C	Molded PLCC (Q28)

2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Fax: 408/432-0295