

MC12015 MC12016 MC12017

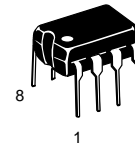
Dual Modulus Prescaler

The MC12015, MC12016 and MC12017 are dual modulus prescalers which will drive divide by 32 and 33, 40 and 41, and 64 and 65, respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc \pm 10% at Pin 7, or by applying an unregulated voltage source from 5.5Vdc to 9.5 Vdc to Pin 8.

- 225 MHz Toggle Frequency
- Low-Power 7.5 mA Maximum at 6.8 V
- Control Input and Output Are Compatible With Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

MECL PLL COMPONENTS DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

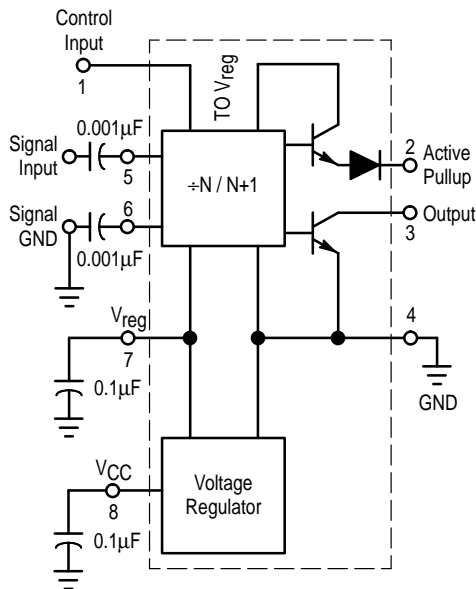


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

SIMPLIFIED BLOCK DIAGRAM



1. V_{reg} at Pin 7 is not guaranteed to be between 4.5 and 5.5V when V_{CC} is being applied to Pin 8
2. Pin 7 is not to be used as a source of regulated output voltage

ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|----------|--|---------|
| MC12015D | $T_A = -40^\circ \text{ to } +85^\circ \text{C}$ | SO-8 |
| MC12016D | | |
| MC12017D | | |
| MC12015P | | Plastic |
| MC12016P | | |
| MC12017P | | |

MC12015 MC12016 MC12017

MAXIMUM RATINGS [tblhead]

| Rating | Symbol | Value | Unit |
|-----------------------------|-----------|-------------|------|
| Regulated Voltage, Pin 7 | V_{reg} | 8.0 | Vdc |
| Power Supply Voltage, Pin 8 | V_{CC} | 10 | Vdc |
| Operating Temperature Range | T_A | -40 to +85 | °C |
| Storage Temperature Range | T_{stg} | -65 to +175 | °C |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.5$ to 9.5 V; $V_{reg} = 4.5$ to 5.5 V; $T_A = -40$ to 85 °C, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------|-----|-----|-----------------|------|
| Toggle Frequency (Sine Wave Input) | f_{max} | 225 | – | – | MHz |
| | f_{min} | – | – | 35 | |
| Supply Current | I_{CC} | – | 6.0 | 7.8 | mA |
| Control Input HIGH (+32, 40 or 64) | V_{IH} | 2.0 | – | – | V |
| Control Input LOW (+33, 41 or 65) | V_{IL} | – | – | 0.8 | V |
| Output Voltage HIGH ($I_{source} = 50\mu A$) [Nofe 1] | V_{OH} | 2.5 | – | – | V |
| Output Voltage LOW ($I_{sink} = 2mA$) [Note 1] | V_{OL} | – | – | 0.5 | V |
| | | | | | |
| Input Voltage Sensitivity | V_{in} | 400 | – | 800 | mVpp |
| | | 200 | – | 800 | |
| PLL Response Time [Notes 2 and 3] | t_{PLL} | – | – | t_{out} to 70 | ns |

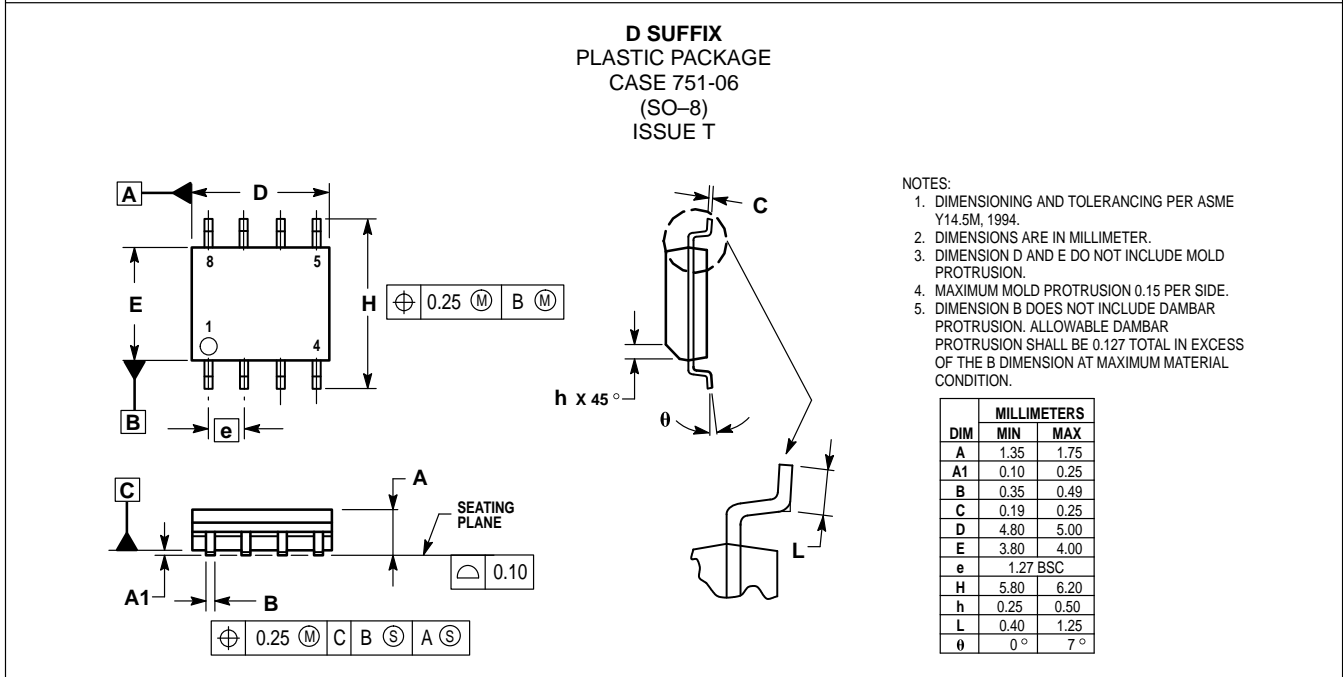
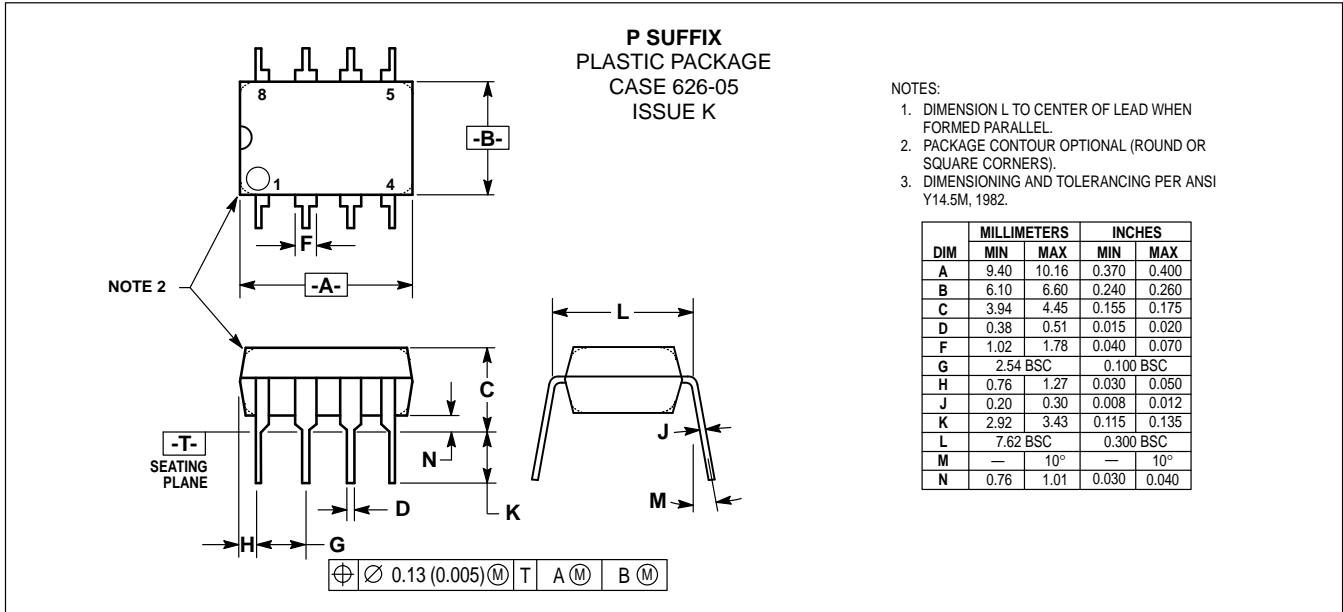
NOTES: 1. Pin 2 connected to Pin 3.


2. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.

3. t_{out} = period of output waveform.

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OUTLINE DIMENSIONS



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