

# **High Frequency Power Supply Controller**

#### GENERAL DESCRIPTION

The ML4810 and ML4811 High Frequency PWM Controllers are optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. The ML4810/11 contain a unique overload protection circuit which helps to limit stress on the output devices and reliably performs a soft-start reset. These controllers are designed to work in either voltage or current mode and provide for input voltage feed forward.

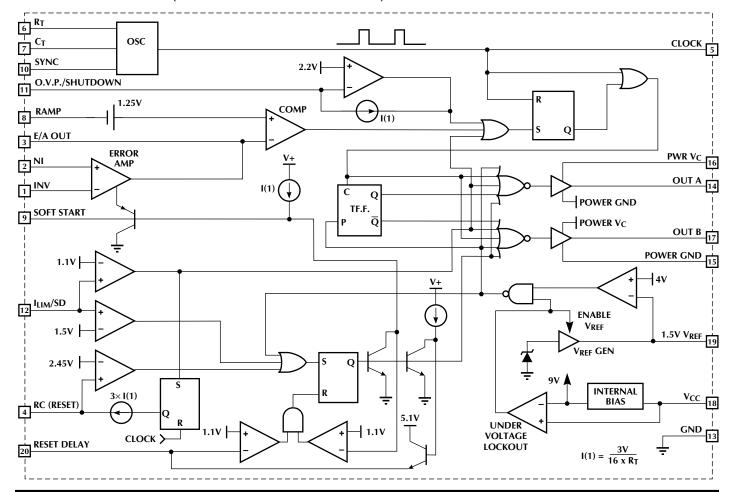
A 1.1V threshold current limit comparator provides a cycle-by-cycle current limit. An integrating circuit "counts" the number of times the 1.1V limit was reached. A soft-start cycle is initiated if the cycle-by-cycle current limit is repeatedly activated. A reset delay function is provided on the ML4811.

These controllers are similar to the UC1825 controller, however these controllers include many features not found on the 1825. These features are set in *Italics*.

#### **FEATURES**

- Integrating Soft Start Reset
- High current (2A peak) dual totem pole outputs
- Practical operation to 1MHz (f<sub>OSC</sub>)
- 5.1V ±2% trimmed bandgap reference
- Under voltage lockout with 7V hysteresis
- Soft Start Reset Delay (ML4811)
- Oscillator synchronization function (ML4811)
- Soft Start latch ensures full soft start cycle
- Outputs pull low for undervoltage lockout
- Accurately controlled oscillator ramp discharge current
- All timing currents "slaved" to R<sub>T</sub> for precise control
  - \* This part is End of Life as of August 1, 2000
  - \*\* This part is Obsolete

#### **BLOCK DIAGRAM** (Pin numbers shown are for ML4811)



# PIN CONFIGURATION

ML4810 16-Pin DIP (P16) **16-Pin SOIC (\$16W)** 16 \_\_\_\_\_ 5.1V REF NI \_\_\_\_\_ 2 15 VCC E/A OUT OUTB RCRESET [ POWER V<sub>C</sub> PWR GND OUTA RAMP \_\_\_\_ GND SOFT START 9 ILIM/S.D. **TOP VIEW** 

20-Pin DIP (P20) 20-Pin SOIC (\$20) 20 RESET DELAY 19 5.1V REF NI 🗌 E/A OUT 3 18 VCC 17 OUTB RCRESET CLOCK 5 16 POWER VC 15 PWR GND R<sub>T</sub> 14 OUTA Ст 🗌 RAMP 8 13 GND

TOP VIEW

12 | I<sub>LIM</sub>/S.D.

OVP

SOFT START

SYNC 10

ML4811

# **PIN DESCRIPTION**

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	INV	Inverting input to error amp.	11	OVP	Exceeding 2.5V terminates the PWM cycle and inhibits the outputs.
2	NI	Non-inverting input to error amp.	4.0		·
3	E/A OUT	Output of error amplifier and input to main comparator.	12	I <sub>LIM</sub> /S.D.	Current limit sense pin. Normally connected to current sense resistor.
		·	13	GND	Analog signal ground.
4	RC <sub>RESET</sub>	Timing elements for Integrating Soft Start reset.	14	OUTA	High current totem pole output. This output is the first one energized after
5	CLOCK	Oscillator output.			power on reset.
6	$R_T$	Timing resistor for oscillator — sets charging current for oscillator timing	15	PWR GND	Return for the high current totem pole outputs.
_		capacitor (pin 6).	16	$V_{C}$	Positive supply for the high current
7	$C_{T}$	Timing capacitor for oscillator.			totem pole outputs.
8	RAMP	Non-inverting input to main comparator. Connected to C <sub>T</sub> for	17	OUTB	High current totem pole output.
		voltage mode operation or to current sense resistor for current mode.	18	$V_{CC}$	Positive supply for the IC.
0	COST STADT		19	5.1V REF	Buffered output for the 5.1V voltage
9	SOFT START	Normally connected to Soft Start capacitor.			reference.
10	CVALC		20	RESET DELAY	Timing capacitor to determine the
10	SYNC	A high going pulse terminates the PWM cycle and discharges C <sub>T</sub> .			amount of delay between fault.

#### **ABSOLUTE MAXIMUM RATINGS**

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (Pins 18, 16)					
Output Current, Source or Sink (Pins 14, 17)					
DC 0.5	Α				
Pulse (0.5μs)	Α				
Analog Inputs					
(Pins INV, NI, SOFT START)0.3V to 7	V				
(Pins 9, 10, 11, 12, 20)0.3V to 6	V				

Clock Output Current (Pins 5)	5mA
Error Amplifier Output Current (Pin 3)	5mA
Junction Temperature	150°C
Storage Temperature Range –65	5°C to 150°C
Lead Temperature (Soldering 10 sec.)	260°C
Thermal Resistance ( $\theta_{JA}$ )	
Plastic DIP	65°C/W
Plastic SOIC	65°C/W

### **OPERATING CONDITIONS**

Temperature Range	
ML4810, ML4811	0°C to 70°C

#### **ELECTRICAL CHARACTERISTICS**

Unless otherwise specified,  $V_{CC} = 15V$ ,  $R_T = 3.65k\Omega$ ,  $C_T = 1000pF$ ,  $T_A = Operating Temperature Range$ . (Note 1)

PARAMETER CONDITIONS MIN TYP MAX UNITS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR	,		'	•	
Initial Accuracy	T <sub>J</sub> = 25°C	360	400	440	kHz
Voltage Stability	10V < V <sub>CC</sub> < 25V		0.2	4	%
Temperature Stability			5		%
Total Variation	line, temperature	340		460	kHz
Clock Out High		3.9	4.5		V
Clock Out Low			2.3	2.9	V
Ramp Peak			2.8		V
Ramp Valley			1.0		V
Ramp Valley to Peak		1.6		2.3	V
Sync Input Threshold		0.8	1.0	1.4	V
Sync Input Current	SYNC = 4V				μА
REFERENCE		,			
Output Voltage	T <sub>J</sub> = 25°C, I <sub>O</sub> = 1mA	5.00	5.10	5.20	V
Line Regulation	10V < V <sub>CC</sub> < 25V		2	20	mV
Load Regulation	1mA < I <sub>O</sub> < 10mA		5	20	mV
Temperature Stability	0°C < T <sub>J</sub> < 150°C		0.2	0.4	%
Total Variation	line, load, temperature	4.95		5.25	V
Output Noise Voltage	10Hz to 10kHz		50		μV
Long Term Stability	T <sub>J</sub> = 125°C, 1000 hrs		5	25	mV
Short Circuit Current	V <sub>REF</sub> = 0V	-15	-50	-100	mA
UNDERVOLTAGE LOCKOUT		·			
Start Threshold		15	16	17	V
UVLO Hysteresis		6.5	7	7.5	V
ERROR AMPLIFIER		•		•	
Input Offset Voltage				±20	mV
Input Bias Current			0.6	3	μΑ
Input Offset Current			0.1	1	μΑ
Open Loop Gain	1 < V <sub>O</sub> < 4V	60	96		dB

# **ELECTRICAL CHARACTERISTICS** (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER (Conti	nued)					_
CMRR		1.5 < V <sub>CM</sub> < 5.5V	65	95		dB
PSRR		10 < V <sub>CC</sub> < 30V	75	90		dB
Output Sink Current		V <sub>PIN 3</sub> = 1V	1	2.5		mA
Output Source Current		$V_{PIN 3} = 4V$	-0.5	-1.3		mA
Output High Voltage		$I_{PIN 3} = -0.5 mA$	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN 3} = 1mA$	0	0.5	1.0	V
Unity Gain Bandwidth			3	5.5		MHz
Slew Rate			6	12		V/µs
PWM COMPARATOR						
Pin 8 Bias Current		V <sub>PIN 8</sub> = 0V		-1	-5	μА
Duty Cycle Range			0		75	%
Pin 3 Zero DC Threshold			1.1	1.25		V
Delay to Output				50	80	ns
SOFT-START						
Charge Current (Pin 9)	ML4811	V <sub>PIN</sub> 9 = 1V, V <sub>PIN</sub> 4, 12 = 0	-35	-55	-75	μΑ
Discharge Current (Pin 9)	ļ	$V_{PIN 9} = 3V, V_{PIN 4} > 2.5$	1	5		mA
		V <sub>PIN 9</sub> = 3V, V <sub>PIN 12</sub> > 1.65, V <sub>PIN 4</sub> < 2	1	5		mA
Charge Current (Pin 20)		V <sub>PIN 20</sub> = 1V	1	5		mA
Discharge Current (Pin 20)		Requires external discharge resistor		0		μА
CURRENT LIMIT/SHUTD	OWN					
Pin 12 Bias Current		0V < V <sub>PIN 12</sub> < 4V			+15	μΑ
Current Limit Threshold	ML4810		1.2	1.3	1.4	V
	ML4811		0.95	1.1	1.3	V
Reset Threshold (Pin 12)	ML4810	V <sub>PIN 4</sub> < 2V	1.60	1.75	1.90	V
	ML4811	V <sub>PIN 4</sub> < 2V	1.4	1.50	1.8	V
Delay to Output				40	70	ns
Pin 4 Charging Current		V <sub>PIN 12</sub> = 2V	120	150	180	μА
Restart Threshold (Pin 4)			2	2.45	3	V
OVP Shutdown Threshold	d (Pin 11)		2.4	2.7	2.8	V
OVP Input Current		V <sub>PIN 11</sub> = 3V	40	50	60	μА
Charge Current (Pin 8)	ML4810	V <sub>PIN 8</sub> = 1V, V <sub>PIN 4</sub> , 9 = 0	-40	-50	-60	μА
OUTPUT						
Output Low Level		I <sub>OUT</sub> = 20mA		0.25	0.4	V
		I <sub>OUT</sub> = 200mA		1.2	2.2	V
Output High Level		I <sub>OUT</sub> = -20mA	13.0	13.5		V
Cutput riight Lovol		I <sub>OUT</sub> = -200mA	12.0	13.0		V
Collector Leakage		V <sub>C</sub> = 30V		100	500	μΑ
Rise/Fall Time		C <sub>L</sub> = 1000pF		30	60	ns
		оц - 1000ф1		1 30	1 00	113
SUPPLY Start Lin Current	NAL 4010	V 9V		2.0	2.5	A
Start Up Current	ML4810	V <sub>CC</sub> = 8V		2.0	3.5	mA
	ML4811	V <sub>CC</sub> = 8V		2.5	4.0	mA mA
I <sub>CC</sub>	ML4810	V <sub>PIN 1, 7, 9</sub> = 0V, V <sub>PIN 2</sub> = 1V, T <sub>A</sub> = 25°C		32	46	mA
	ML4811	$V_{PIN 1, 7, 9} = 0V, V_{PIN 2} = 1V, T_A = 25^{\circ}C$		38	55	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.



#### **FUNCTIONAL DESCRIPTION**

#### **SOFT START AND CURRENT LIMIT**

The ML4810/11 offers a unique system of fault detection and reset. Most PWM controllers use a two threshold method which relies on the buildup of current in the output inductor during a fault. This buildup occurs because:

- Inductor di/dt is a small number when the switch is off under load fault (short circuit) conditions, since VL is small.
- 2. Some energy is delivered to the inductor since the IC must first detect the over-current because there is a finite delay before the output switch can turn off.

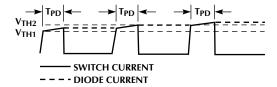


Figure 1. Current Waveforms for Slow Turn-Off System with Load Fault

This scheme was adequate for controllers with longer comparator propagation delays and turn-off delays than is desirable in a high frequency system. For systems with low propagation delays, very little energy will be delivered to the inductor and the current "ratcheting" described above will not occur. This results in the controller never detecting the load fault and continuing to pump full current to the load indefinitely, causing heating in the output rectifiers and inductor.

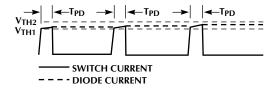


Figure 2. Current Waveforms for High Speed System with Load Fault

A method of circumventing this problem involves "counting" the number of times the controller terminates the PWM cycle due to the cycle by cycle current limit.

When the switch current crosses the 1.1V threshold A1 signals the F1 to terminate the cycle and sets F3, which is reset at the beginning of the PWM cycle. The output of F3 turns on a current source to charge C2. When, after several cycles, C2 has charged to 2.45V, A5 turns on F2 to discharge soft start capacitor C1. Charge is short lived (for instance a disk drive start-up or a board being plugged into a live rack) the control can "ride out" the surge with the switch protected by the cycle by cycle limit. R1 and C1 can be selected to track diode heating, or to ride out various system surge requirements as required.

If the high current demand is caused by a short circuit, the duty cycle will be short and the output diodes will carry the current for the majority of PWM cycle. C2 charges fastest for low duty cycles (since F3 will be on for a longer time) providing for quicker shutdown during short-circuit when the output diodes are being maximally stressed.

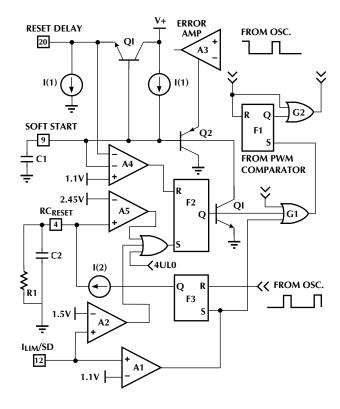


Figure 3. Integrating Soft Start Reset

#### **OSCILLATOR**

The ML4811 oscillator charges the external capacitor ( $C_T$ ) with a current ( $I_{SET}$ ) equal to  $3/R_T$ . When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse. A discharge of the oscillator con be initiated by applying a high level to the Sync pin. A short pulse of a frequency higher than the oscillator's free running frequency can be used to synchronize the ML4811 to an external clock. The pulse can be equal to the desired deadtime ( $T_D$ ) or the deadtime can be determined by  $I_{DIS}$  and  $C_T$ , whichever is greater.

The oscillator period can be described by the following relationship:

$$t_{OSC} = t_{RAMP} + t_{DEADTIME}$$

where:

$$t_{RAMP} = \frac{C \text{ (Ramp Valley to Peak)}}{I_{SFT}}$$

and:

$$t_{DEADTIME} = \frac{C \text{ (Ramp Valley to Peak)}}{I_{O1}}$$

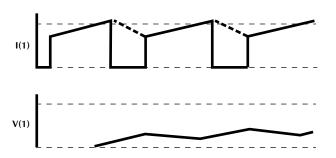


Figure 4. Switching Current and Pin 4 Voltage — Normal

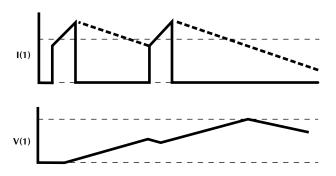


Figure 5. Switching Current and Pin 4 Voltage — Load Fault

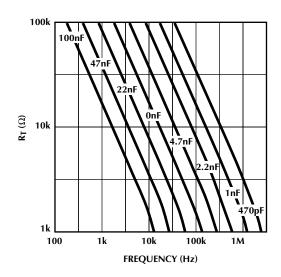
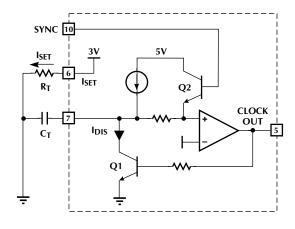


Figure 7. Oscillator Timing Resistance vs Frequency



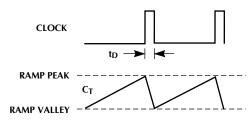
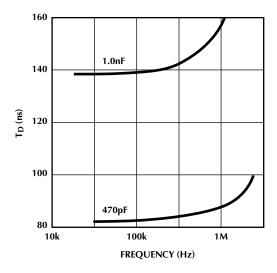


Figure 6. Simplified Oscilator Block Diagram and Timing



**Figure 8. Oscillator Deadtime vs Frequency** 

#### **ERROR AMPLIFIER**

The ML4811 error amplifier is a 5.5 MHz bandwidth  $12 V/\mu sec$  slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

#### **OUTPUT DRIVER STAGE**

The ML4811 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

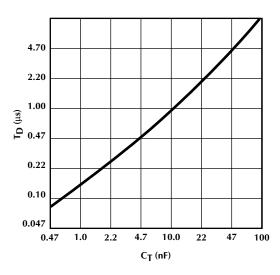


Figure 9. Oscillator Deadtime vs  $C_T$  ( $3k\Omega \le R_T \le 100k\Omega$ )

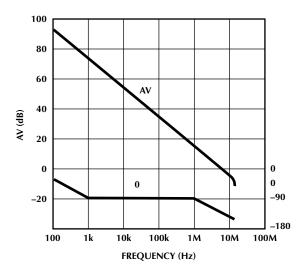


Figure 11. Open Loop Frequency Response

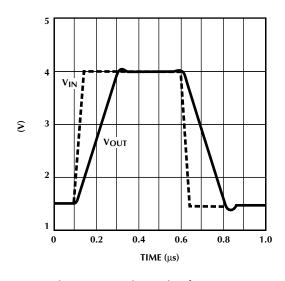
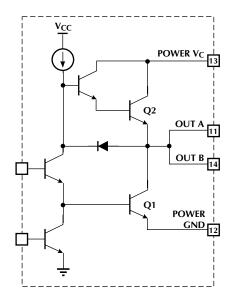
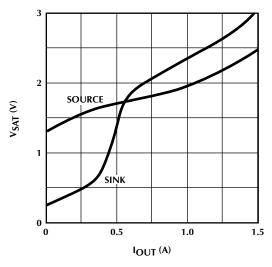


Figure 10. Unity Gain Slew Rate



**Figure 12. Simplified Schematic** 



**Figure 13. Saturation Curves** 

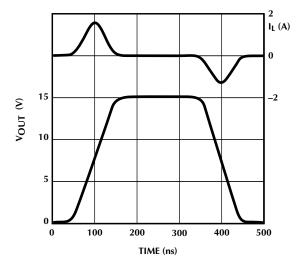


Figure 15. Rise/Fall Time ( $C_L = 10,000pF$ )

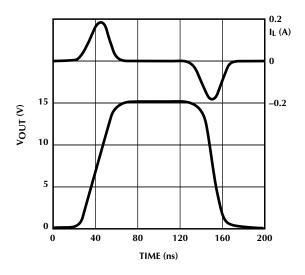


Figure 14. Rise/Fall Time ( $C_L = 1000pF$ )

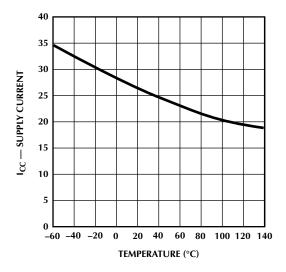
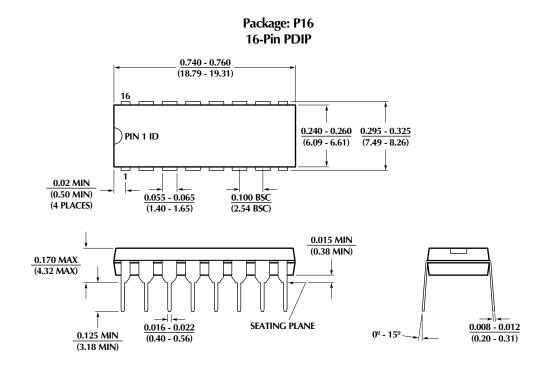
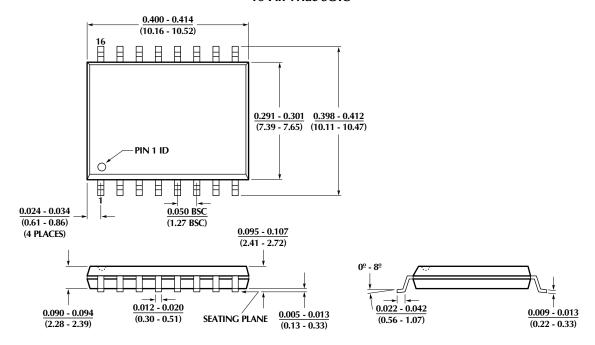


Figure 16. Supply Current vs. Temperature

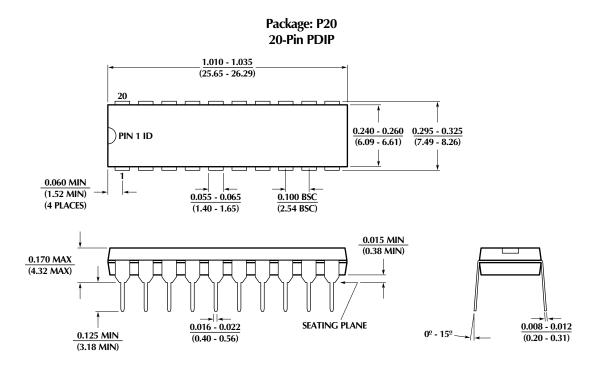
# PHYSICAL DIMENSIONS inches (millimeters)

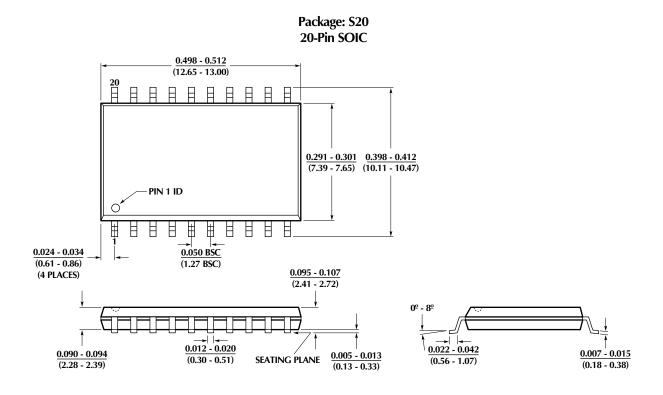


#### Package: S16W 16-Pin Wide SOIC



# PHYSICAL DIMENSIONS inches (millimeters) (Continued)





## **ORDERING INFORMATION**

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4810CP	0°C to 70°C	16-Pin PDIP (P16) (End Of Life)
ML4810CS	0°C to 70°C	16-Pin Wide SOIC (S16W) (Obsolete)
ML4811CP	0°C to 70°C	20-Pin PDIP (P20) (Obsolete)
ML4811CS	0°C to 70°C	20-Pin SOIC (S20)(Obsolete)

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