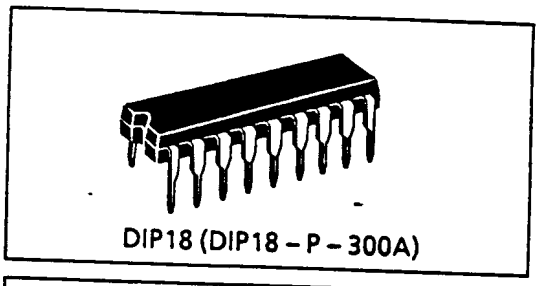
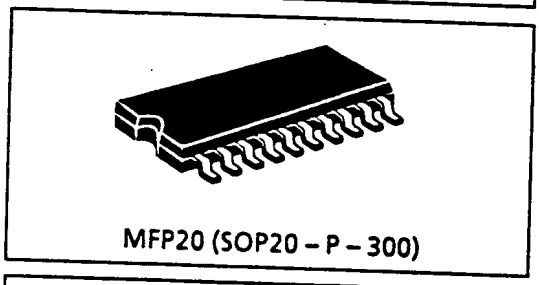
TC35300BP,TC35310F

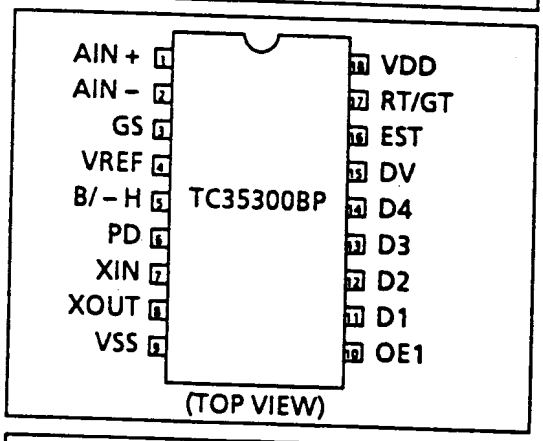
(DTMF RECEIVER)

1. GENERAL DESCRIPTION

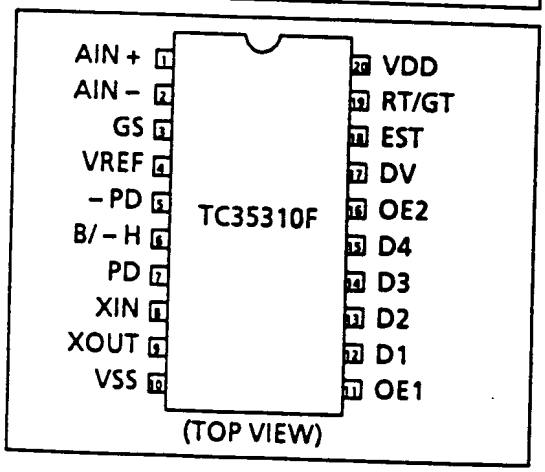
TC35300BP,TC35310F are the LSI designed for detecting Dual Tone Multi Frequency (DTMF) used for Push Button (PB) signal. The DTMF signal is detected from signal transferred through the telephone line, and is outputted after conversion into 4-bit code. The built-in differential amplifier at the input allows easy connection with the balanced circuit. The latch circuit with 3-state output is applied to the data output stage allowing its easy interfacing with other devices.


DIP18 (DIP18 – P – 300A)


MFP20 (SOP20 – P – 300)



(TOP VIEW)



(TOP VIEW)

2. FEATURES

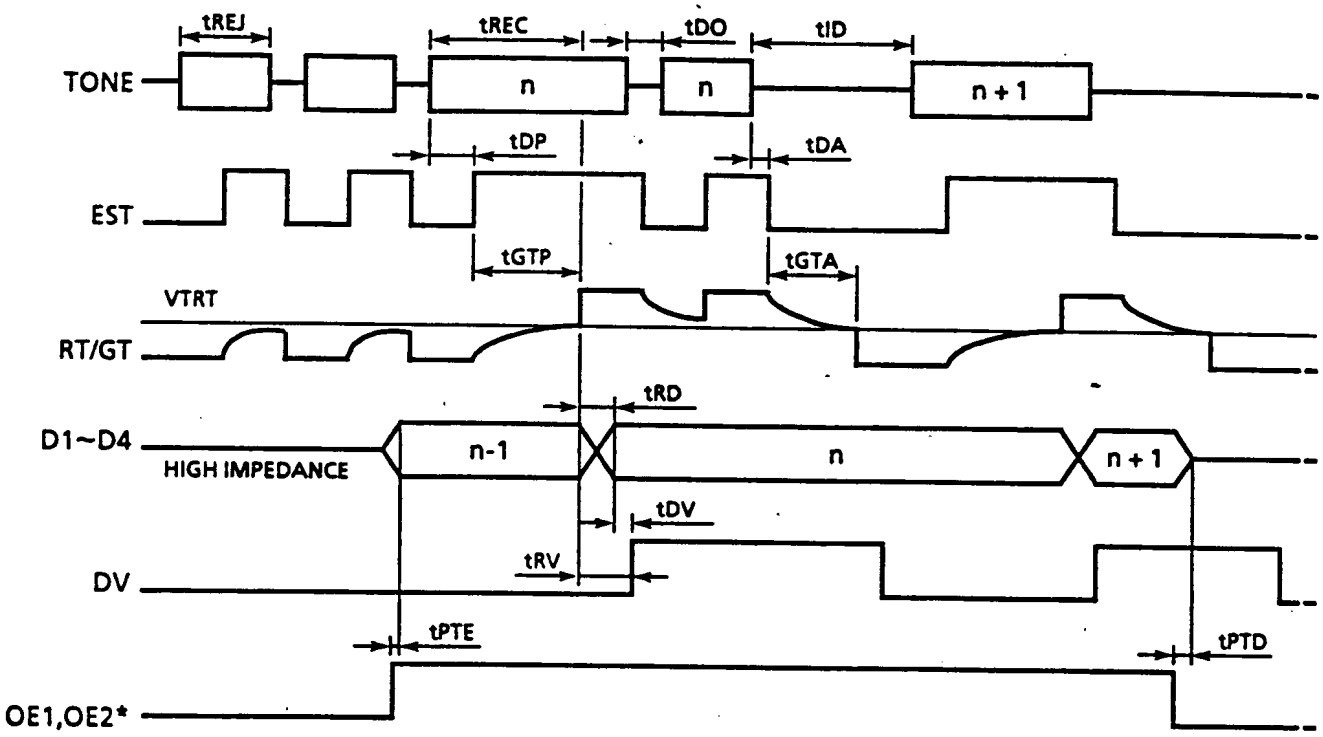
- ☐ Dynamic range over 34dB
- ☐ Power down mode
- ☐ Adjustable reception level
- ☐ 4-bit Hexadecimal code or binary coded 2OF-8 selectable
- ☐ External CR for adjusting acquisition and release time
- ☐ Built in anti-aliasing filter at signal input stage
- ☐ 3-Stage data output
- ☐ 3.5MHz crystal oscillator or ceramic resonator
- ☐ CMOS Low power
- ☐ +5V Single power supply
- ☐ 18-Pin DIP TC35300BP, 20-Pin SOP TC35310F

2.1 APPLICATIONS

- ☐ Automatic answering telephone set
- ☐ PBX
- ☐ Remote control

The products described in this document are strategic products subject to COCOM regulations. They should not be exported without authorization from the appropriate governmental authorities.
TOSHIBA CORPORATION

3. TIMING CHART



*TC35310F only

4. PIN DESCRIPTION

PIN NO. DIP	PIN NO. SOP	NAME	IN/OUT	FUNCTION
1	1	AIN +	IN	Non-inverting input of first stage differential amplifier
2	2	AIN −	IN	Inverting input of first stage differential amplifier
3	3	GS	OUT	Output terminal of first stage differential amplifier (Gain is adjusted through connecting with feedback resistance.)
4	4	VREF	OUT	Output of reference voltage of VDD/2 to be used for biassing first stage differential amplifier
−	5	− PD	IN	At "L", power-down mode is made. Clearing function of D1 to D4 outputs is not provided.
5	6	B/ − H	IN	Format of D1 to D4 outputs is selected. "L" : Hexadecimal Code "H" : 2 of 8 Binary Code (For each output code, refer to the attached table.)
6	7	PD	IN	At "H", power-down mode is made. Clearing function of D1 to D4 outputs is not provided.
7	8	XIN	IN	Connect crystal oscillator of 3.579545MHz. Becomes input terminal when external clock is used.
8	9	XOUT	OUT	Connect crystal oscillator of 3.579545MHz. Make open for using external clock.
9	10	VSS	−	Ground terminal (usually 0V)
10	11	OE1	IN	3-state control terminal of D1 to D4 (Pull-up resistance is built in.) OE1 = "H", OE2 = "H" : Enable OE1 = "L", OE2 = ANY : High impedance
11	12	D1	OUT	Output terminal of receiving data At OE1·OE2 = "L" : High impedance At OE1·OE2 = "H" : Enable (The digital output format is programmed by B/-H.)
12	13	D2	OUT	
13	14	D3	OUT	
14	15	D4	OUT	
−	16	OE2	IN	3-state control terminal of D1 to D4 OE1 = "H", OE2 = "H" : Enable OE1 = ANY, OE2 = "L" : High impedance
15	17	DV	OUT	When a valid tone-pair is detected continuously for specified time, the level becomes high.
16	18	EST	OUT	When a detected tone pair is effective, the level becomes high.
17	19	RT/GT	IN/OUT	Tone acquisition time and release time can be set through connection with resistance and capacitor. (For each time setting, refer to calculating formula shown hereinafter.)
18	20	VDD	−	Power supply terminal (Normally 5V)

5. FUNCTIONAL DESCRIPTION

5.1 DESCRIPTION OF CIRCUIT CONSTRUCTION AND OPERATION

TC35300BP,TC35310F consist of the band pass filter which correspond to the frequency band using DTMF signal, and the logic circuit in which verifies the frequency and duration of the received tone to decode a before passing the corresponding code to the output.

The outline of each operations described in the following.

a) Band Pass Filter and Zero-crossing Detector Circuit

The band pass filter section is composed of the high-accuracy switched capacitor filters and the anti-aliasing filter in the first stage.

Anti-aliasing filter reduces the extraneous high frequency components. The first stage of switched capacitor filters is provided a dial tone rejection filter where sufficiently dissipates the frequency components of 350Hz to 440Hz due to suppress the error detection.

Removing the unnecessary signal components, furthermore, the signal is applied band pass filters each enclosing high or low-group frequency.

Each filter output is followed by zero-crossing detector with hysteresis. When the each signal amplitude at the output exceeds specified level, the signal is transformed into full-rail logic signal.

b) Signal Decision Circuit and Timer Controlling Circuit

The signal judgment circuit decides that the each transformed logic signal detected to be effective or not. When these signals are decided to be effective, EST becomes high, and the corresponding code of DTMF digit is transferred to the matrix circuit. When the detected signal is not a DTMF signal or an absence of signal, then EST becomes low.

The timer controlling circuit is used for measuring the effective signal duration and for protecting against the drop out of valid signal by means of the analogical delay by external RC time-constant driven by EST. (These time are measured by the voltage at RT/GT based at the time of EST change. Therefore, the actual tone reception time and release time are added tDP, tDA in each time. tDP and tDA are the delay time of EST after the signal input.) When the voltage at RT/GT changes from 0V to VTRT the input signal is judged to be effective, and the corresponding 4-bit code with the input signal is latched into D1 to D4. After completion of latch,DV output becomes high. When the voltage at RT/GT fall down from VDD to VTRT, DV output becomes low.

The effective tone pair code received lastly is always latched into D1 to D4 outputs.

5.2 DTMF TO BINARY DECODING (HEXADECIMAL AND 2-OF-8)

As the 4-bit digital outputs of D1 to D4, two kinds of format shown in the following are possible through the setting of B/-H.

When B/-H = "L", the output format becomes that of the hexadecimal code, and when B/-H = "H", becomes the binary coded 2-of-8. In the binary coded 2-of-8, each 2-bit value of D4, D3 and D2, D1 corresponds with m or n of ROW m and COL n. (Refer to the Table.)

FL	FH	DIGIT	B/-H		L (HEXADECIMAL)				H (2-of-8)			
			OE1	*OE2	D4	D3	D2	D1	D4	D3	D2	D1
697	1209	1	H	H	L	L	L	H	L	L	L	L
697	1336	2	H	H	L	L	H	L	L	L	L	H
697	1477	3	H	H	L	L	H	H	L	L	H	L
770	1209	4	H	H	L	H	L	L	L	H	L	L
770	1336	5	H	H	L	H	L	H	L	H	L	H
770	1477	6	H	H	L	H	H	L	L	H	H	L
852	1209	7	H	H	L	H	H	H	H	L	L	L
852	1336	8	H	H	H	L	L	L	H	L	L	H
852	1477	9	H	H	H	L	L	H	H	L	H	L
941	1336	0	H	H	H	L	H	L	H	H	L	H
941	1209	*	H	H	H	L	H	H	H	H	L	L
941	1477	#	H	H	H	H	L	L	H	H	H	L
697	1633	A	H	H	H	H	L	H	L	L	H	H
770	1633	B	H	H	H	H	H	L	L	H	H	H
852	1633	C	H	H	H	H	H	H	H	L	H	H
941	1633	D	H	H	L	L	L	L	H	H	H	H
—	—	ANY	L	H	Z	Z	Z	Z	Z	Z	Z	Z
			H	L								
			L	L								
									ROW m		COL n	

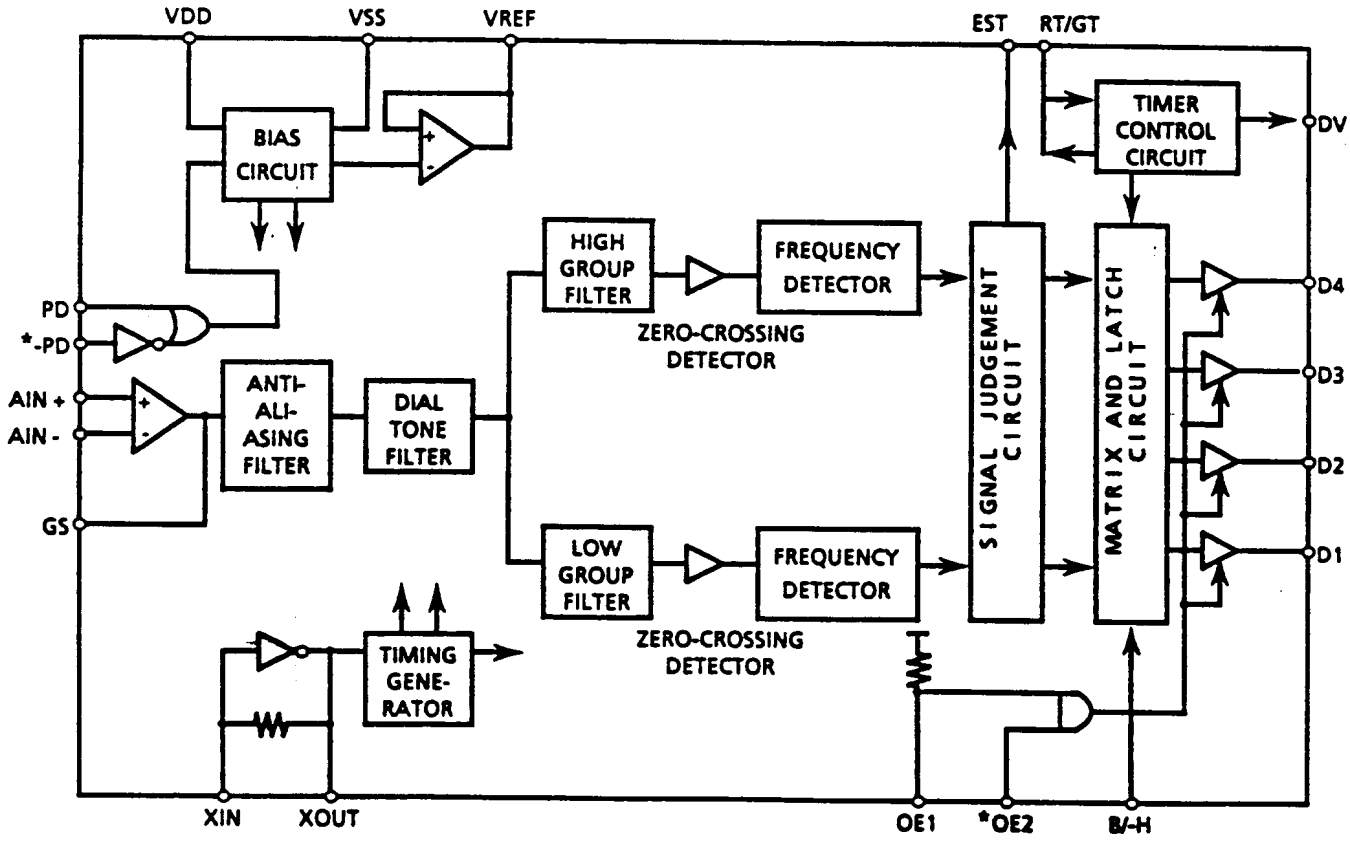
* TC35310F only

"Z" means high impedance.

5.3 DTMF DIALING MATRIX

	COL0	COL1	COL2	COL3
ROW0	1	2	3	A
ROW1	4	5	6	B
ROW2	7	8	9	C
ROW3	*	0	#	D

5.4 TC35300BP, TC35310F INTERNAL BLOCK DIAGRAM



*TC35310F only

5.5 SETTING OF GUARD TIME

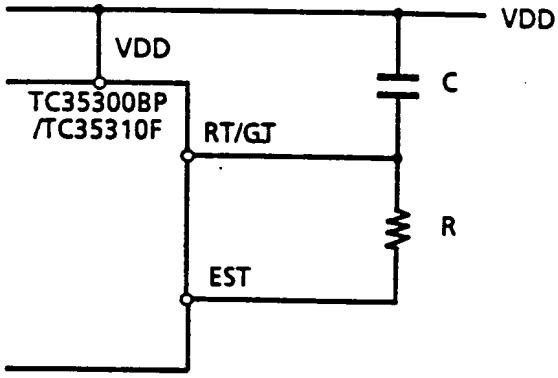
Valid DTMF signal time and the protection time against tone drop out are set through using the time constant of the external resister and capacitor.

Each time is calculated with the formula hereunder. The other methods shown in the following figures b and c can be used according to the application.

$$tREC = tDP + tGTP$$
$$tID = tDA + tGTA$$

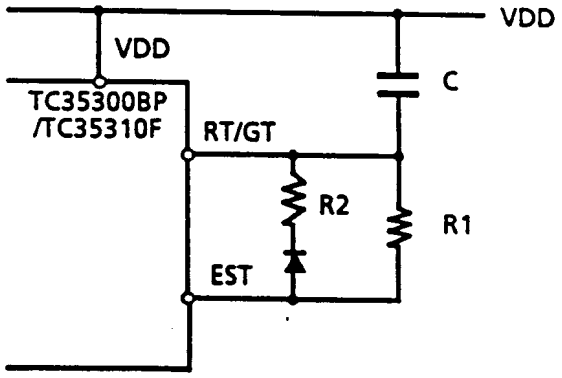
a) Fundamental Circuit

$$tGTP = R \cdot C \cdot \ln[VDD/(VDD-VTRT)]$$
$$tGTA = R \cdot C \cdot \ln(VDD/VTRT)$$



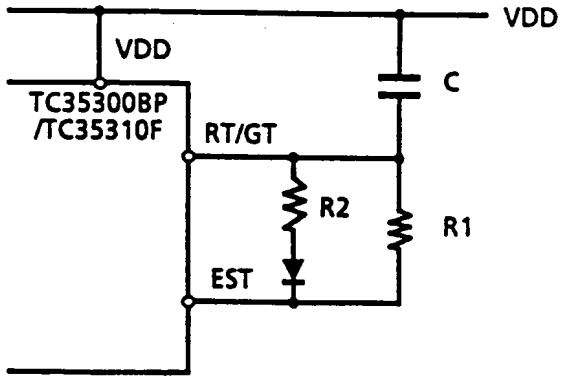
b) $tGTP < tGTA$

$$tGTP = (R1 \cdot R2)/(R1 + R2) \cdot C \cdot \ln[VDD/(VDD-VTRT)]$$
$$tGTA = R1 \cdot C \cdot \ln(VDD/VTRT)$$



c) $tGTP > tGTA$

$$tGTP = R1 \cdot C \cdot \ln[VDD/(VDD-VTRT)]$$
$$tGTA = (R1 \cdot R2)/(R1 + R2) \cdot C \cdot \ln(VDD/VTRT)$$



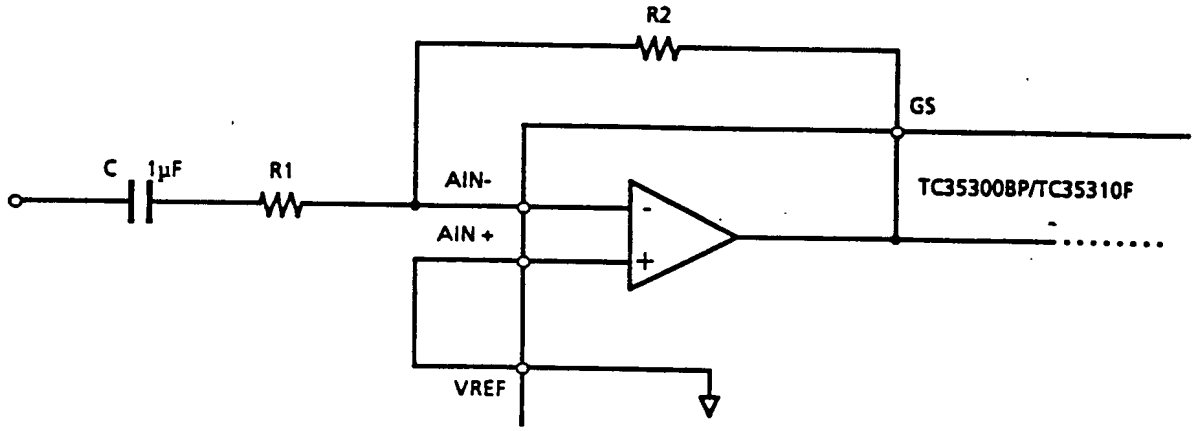
5.6 RECEPTION LEVEL ADJUSTMENT AND DYNAMIC RANGE EXPANSION

The reception level of TC35300BP and TC35310F can be set up freely by gain adjustment at the input stage operational amplifier.

The dynamic range can also be expanded over 34dB by composing the logarithmic input circuit configuration, which enables the END to END application.

a) Standard Input Circuit

o Configuration



VOLTAGE GAIN : $A = 20 \cdot \log (R2/R1)$

INPUT IMPEDANCE : $Z = \sqrt{R1 + 1/(\omega C)}$

o Adjustment of Reception Level

The reception level can be set by the value of R1 and R2 keeping the total dynamic range 34-dB MIN. Where R2 is set to be over 30kΩ.

Minimum Reception Level $Vin(min) = -33 - 20 \cdot \log(R2/R1)$ dBm

Maximum Reception Level $Vin(max) = 1 - 20 \cdot \log(R2/R1)$ dBm

o Example

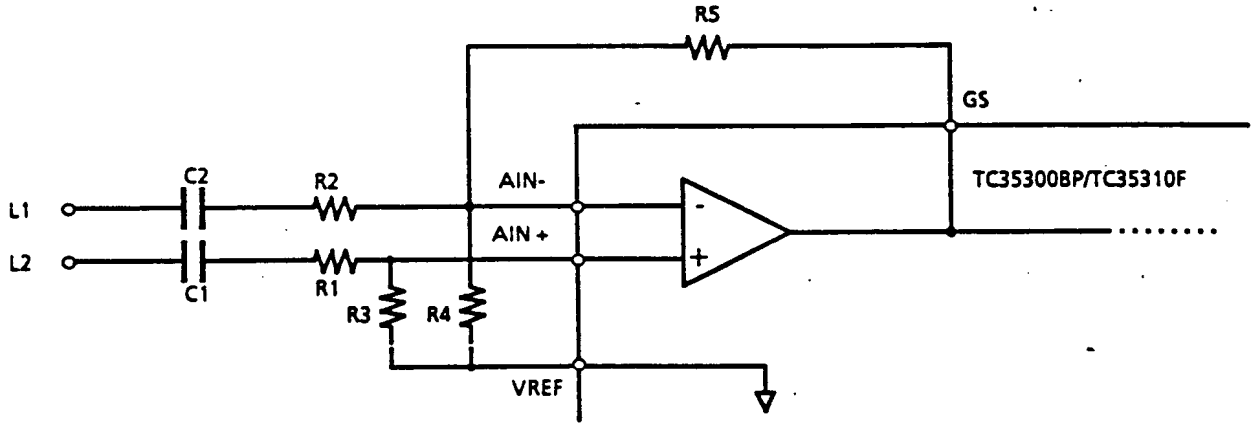
Reception signal level		R1 (kΩ)	R2 (kΩ)
MIN.(dBm)	MAX.(dBm)		
-33	+1	100	100
-36	-2	91	130
-39	-5	75	150
-42	-8	56	160

Note) To prevent unrequired signal reception, the gain setting should be done attentively.

b) Differential Input Circuit

Since the differential amplifier is applied to the signal input portion, TC35300BP,TC35310F can also easily be connected to the balanced circuit in the manner shown below.

o Configuration



VOLTAGE GAIN : $A = 20 \cdot \log (R5/R1)$

INPUT IMPEDANCE : $Z = 2\sqrt{R1 + 1/(\omega C)}$

o Adjustment of Reception Level

The reception level can be set by the value of R1 and R5 keeping the total dynamic range 34-dB MIN. Where R5 is set to be over 30kΩ.

Minimum Reception Level $Vin(min) = -33 - 20 \cdot \log(R5/R1)$ dBm

Maximum Reception Level $Vin(max) = 1 - 20 \cdot \log(R5/R1)$ dBm

o Example

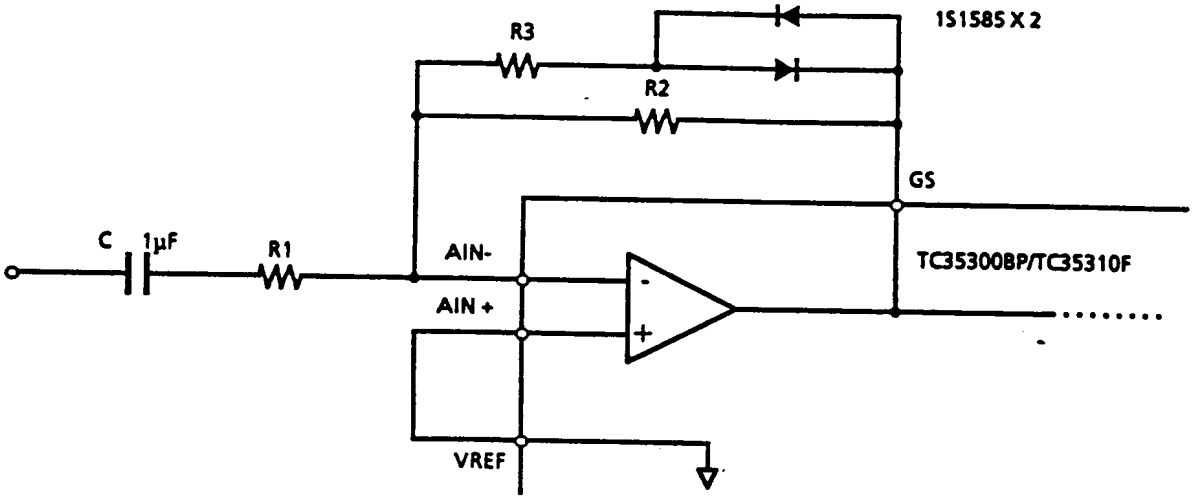
Detection signal level		R1 (kΩ)	R5 (kΩ)
MIN.(dBm)	MAX.(dBm)		
-33	+1	100	100
-36	-2	91	130
-39	-5	75	150
-42	-8	56	160

Note) To prevent unrequired signal reception, the gain setting should be done attentively.

c) Logarithmic Input Circuit - for expanding dynamic range

TC35300BP,TC35310F can expand the dynamic range by composing logarithmic amplifier at the input stage operational amplifier.

o Configuration



INPUT IMPEDANCE : $Z = \sqrt{R1 + 1/(\omega C)}$

o Adjustment of Detection Level

The reception level can be set by the value of R1,R2 and R3. Using a logarithmic input circuit, dynamic range is expanded over 34dB. Where parallel resistance of R2 and R3 is set to be over 30kΩ.

Minimum Reception Level $Vin(min) = -33 - 20 \cdot \log(R2/R1)$ dBm

Maximum Reception Level $Vin(max) = 1 - 20 \cdot \log [1/R1 \cdot (R2 \cdot R3)/(R2 + R3)]$ dBm

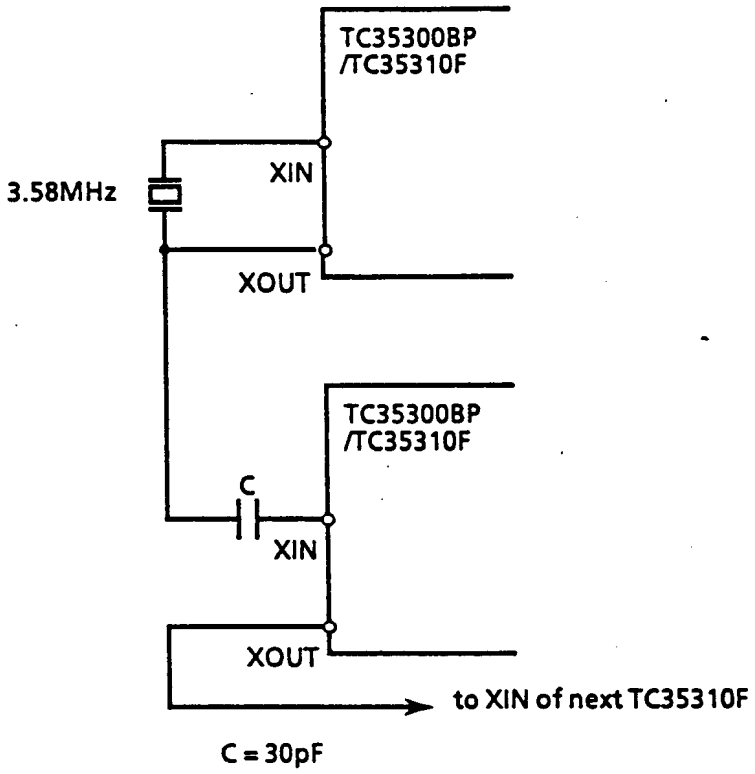
o Example

Detection signal level		R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	Dynamic Range (kΩ)
MIN.(dBm)	MAX.(dBm)				
-39	+1	51	100	100	40
-43	+1	51	160	75	44
-53	+1	30	330	36	54

Note) To prevent unrequired signal reception, the gain setting should be done attentively.

5.7 CRYSTAL OSCILLATOR

TC35300BP,TC35310F oscillator output of the first device in the chain is coupled through a 30pF capacitor to the oscillator input(XIN) of the next device. Subsequent device is connected in a similar fashion.



6. ELECTRICAL CHARACTERISTICS

6.1 MAXIMUM RATINGS

ITEM	SYMBOL	RATING		UNIT
		TC35300BP	TC35310F	
Power Supply Voltage	VDD	VSS-0.5 to VSS + 7.0	VSS-0.5 to VSS + 7.0	V
Input Voltage	VIN	VSS-0.5 to VDD + 0.5	VSS-0.5 to VDD + 0.5	V
Input Current	IIN	-10 to + 10	-10 to + 10	mA
Output Voltage	VOUT	VSS-0.5 to VDD + 0.5	VSS-0.5 to VDD + 0.5	V
Power Dissipation	PD	300	180	mW
Storage Temperature	Tstg	-60 to + 150	-60 to + 150	°C
Operating Temperature	Topr	-40 to + 85	-40 to + 85	°C

6.2 DC ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Voltage	VDD			4.75		5.25	V
Operating Supply Current	IDD (opr)	PD = 0V,-PD = 5.0V			3.0	7.0	mA
Static Supply Current	IDD (Stby)	PD = 5.0V,-PD = 0V			0.01	10.0	uA
High Level Input Voltage	VIH			3.5			V
Low Level Input Voltage	VIL					1.5	V
High Level Output Current	IOH	VOUT = 4.6V (Except for RT/GT)		0.4	0.8		mA
		VOUT = 4.6V (RT/GT)		0.8	1.0		mA
Low Level Output Current	IOL	VOUT = 0.4V (Except for RT/GT)		1.0	2.5		mA
		VOUT = 0.4V (RT/GT)		1.2	3.0		mA
High Level Input Current	IIH	VIN = 5.0V				0.1	uA
Low Level Input Current	IIL	VIN = 0V				0.1	uA
Pull-up Current	ISO	OE1 = 0V	TC35300BP		7.5	15	uA
			TC35310F		50.0		
RT/GT Threshold Voltage	VTRT			2.2	2.35	2.5	v
VREF Output Voltage	VREF			2.4		2.7	v
VREF Output Resistance	RREF	VREF = 2.55V				1	kΩ

Ta = 25°C,VDD = 5V,VSS = 0V

6.3 AC ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Input Signal *1 Level for Reception		Each Tone Composite Signal	+1			dBm
Minimum Input Signal *1 Level for Reception				-40	-33	dBm
Tone Amplitude Ratio				±10		dB
Frequency Deviation Tone Reception			±1.5			%
Frequency Deviation Tone Rejection			±3.5			%
Third Tone Rejection Ratio				-16		dB
Dial Tone Rejection Ratio				+22		dB
Noise Rejection Ratio				-12		dB
EST Output Delay Time	tDP	"L" -> "H"	5	11	14	mS
	tDA	"H" -> "L"	0.5	4.0	8.5	mS
Tone-Reception Signal Duration Time	tREC	Refer to Test Circuit	40			mS
Tone-Rejection Signal Duration Time	tREJ				20	mS
Signal Quiescent Time	tID		40			mS
Signal Hit Protection Time	tDO				20	mS
Data Output Delay Time	tRD	RT->D1 to D4		6	9	uS
DV Output Delay Time	tRV	RT->DV		12		uS
	tDV	D1 to D4-DV		5		uS
Output Enable Time	tPTE	RL = 10kΩ, CL = 50pF		50	60	nS
Output Disable Time	tPTD	RL = 10kΩ, CL = 50pF		300		nS
Clock Frequency	fCLK		3.5759	3.5795	3.5831	MHz
Capacitive Load	CLX	XOUT			30	pF

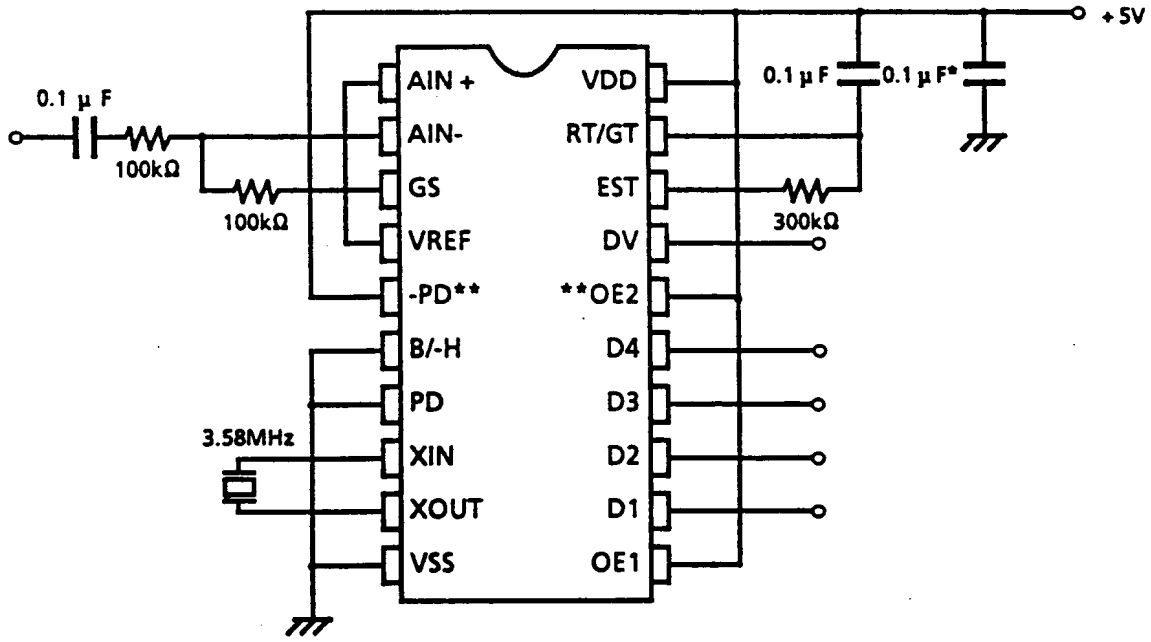
Ta = 25°C, VDD = 5V, VSS = 0V, fCLK = 3.579545MHz

*1 : Input stage amplifier gain = 0dB

6.4 OPERATIONAL AMPLIFIER CHARACTERISTICS (AIN+, AIN- to GS)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	VIO			±25		mV
Input Offset Current	IIO	VSS ≤ VIN ≤ VDD		±100		nA
Power Supply Rejection Ratio	PSRR	1 KHz		60		dB
Common Mode Rejection Ratio	CMRR			60		dB
Open Loop Gain	AO			65		dB
0 dB Band Width	fT			500		kHz
Rated Output Voltage	VO	Load Resistance: 100 kΩ or over		4.5		Vpp
Load Resistance	RL	GS		30		kΩ
Capacitive Load	CL	GS		50		pF

Ta = 25°C, VDD = 5V, VSS = 0V



All resistors are ±1% tolerance.
All capacitors are ±5% tolerance.

* The performances of TC35300BP and TC35310F can be optimized by keeping noise on the supply rails to minimum. The decoupling 0.1uF capacitor should be connected close to the device.

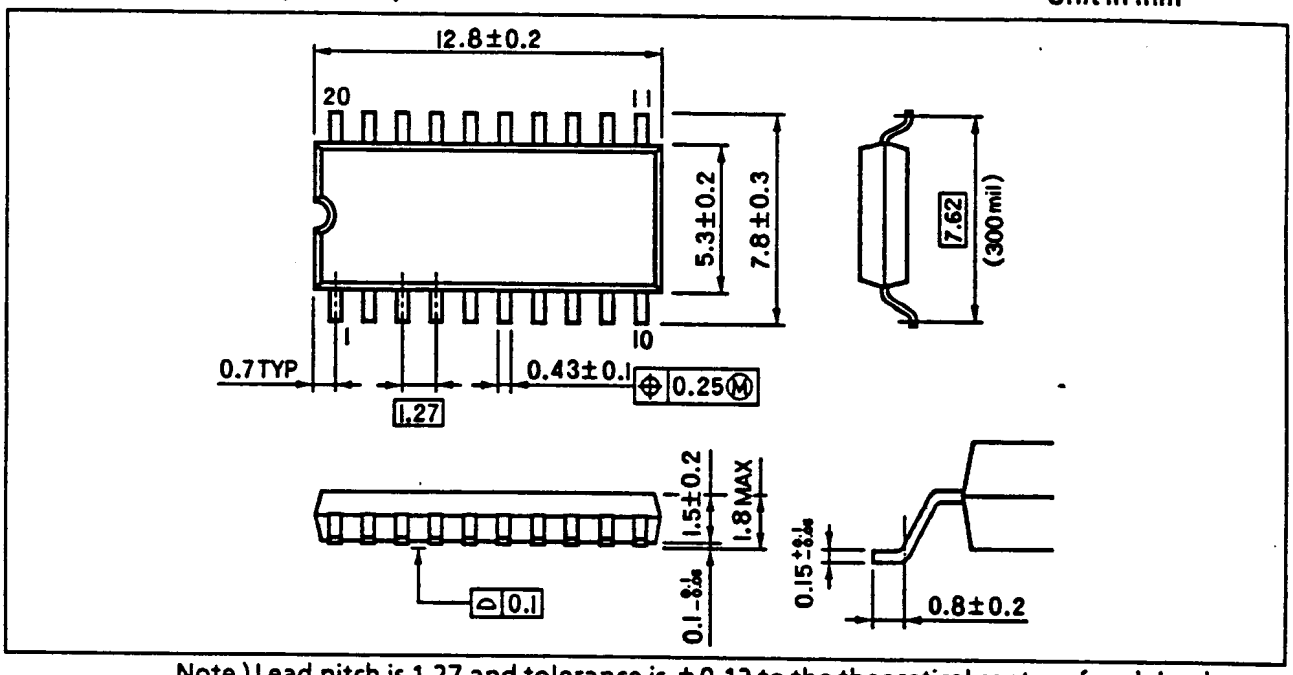
** TC35310F only

TEST CIRCUIT

7. OUTLINE DRAWING OF PACKAGE

MFP 20 PIN (F20GA-P)

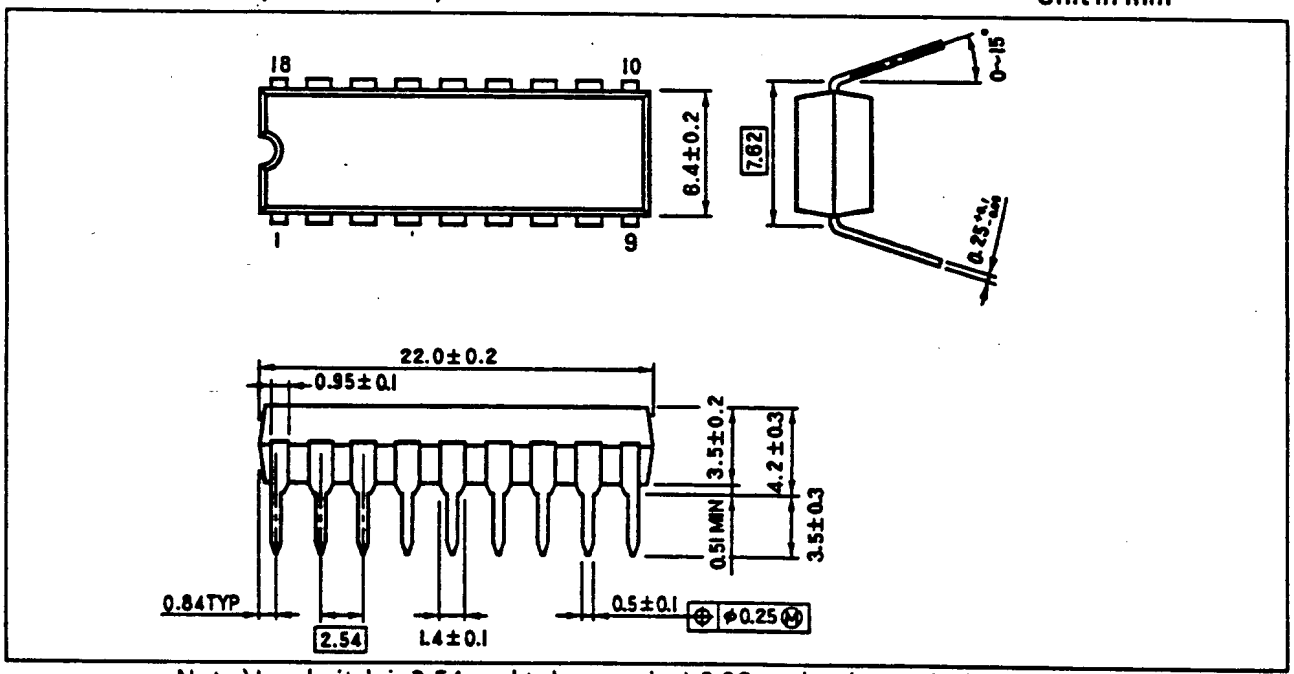
Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 to the theoretical center of each lead that is obtained on the basis of No.1 and No.20 leads.

DIP 18 PIN (DIP18-P-300A)

Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.28 to the theoretical center of each lead that is obtained on the basis of No.1 and No.18 leads.