

## **CML Semiconductor Products**

PRODUCT INFORMATION

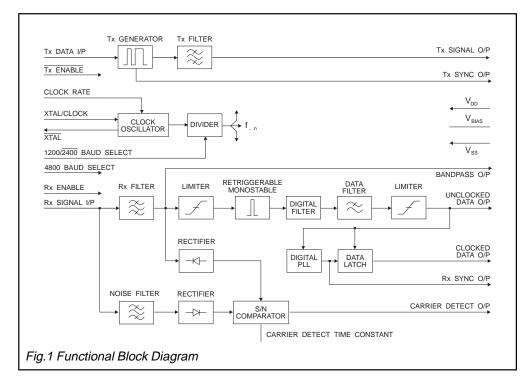
# FX469 1200/2400/4800 Baud FFSK Modem

Publication D/469/6 April 1998

#### **Features**

- Selectable Data Rates1200, 2400 and 4800 Baud
- Full-Duplex FFSK
- Rx and Tx Bandpass Filters
- Clock Recovery and Carrier Detect Facilities
- Rx and Tx Enable Functions

- Pin Selected Xtal/Clock Inputs 1.008MHz or 4.032MHz
- Radio and General Applications
  - Data-Over-Radio
  - PMR and Cellular Signalling
  - Portable Data Terminals
  - Personal/Cordless Telephone



**FX469** 

#### Brief Description

The FX469 is a single-chip CMOS LSI circuit which operates as a full-duplex pin-selectable 1200, 2400 or 4800 baud FFSK Modem. The mark and space frequencies are 1200/1800, 1200/2400 and 2400/4800 Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point.

Employing a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) to provide band-rate, transmit frequencies, and Rx and Tx synchronization, the transmitter and receiver operate entirely independently including individual section powersave functions.

The FX469 includes on chip circuitry for Carrier Detect and Rx Clock recovery, both of which are made available as output pins.

Rx, Tx and Carrier Detect paths each contain a bandpass filter to ensure the provision of optimum signal conditions both in the modem and for the Tx modulation circuitry.

The FX469 demonstrates a high sensitivity and good bit-error-rate under adverse signal conditions; the carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high noise environments.

This low-power device requires few external components and is available in small outline plastic (S.O.I.C) and cerdip DIL packages.

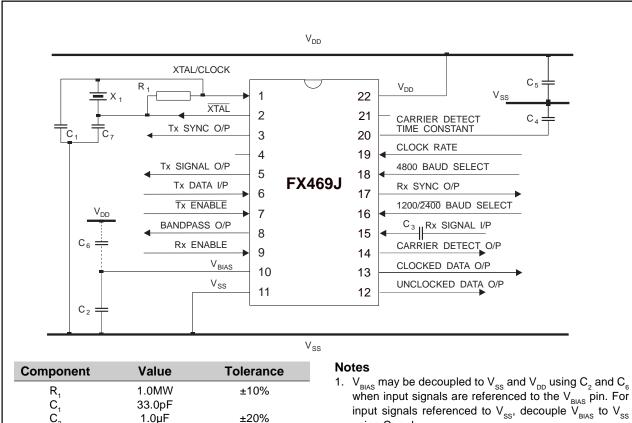
## Pin Number Function

	FX469									
DW	LG/LS	J/P6								
1	1	1	Xtal or externa selection of thi Selection infor clock input ma failure. it is rec	The input to the on-chall clock. Clock frequency will affect mation on the next pay cause device dama tommended that the pateraction fuse).	ncy selection is by the the operational Datage. Operation of an age. To minimise datage.	ne "Clock Rate" input ta Rate of this devic y CML microcircuit mage in the event o	nt pin. The e. Refer to Baud without a Xtal or f a Xtal/drive			
2	2	2	XtalN: Outpu	t of the on-chip inver	ter.					
3	3	3		A squarewave, prof the FFSK signal (So		nchronize the input	of logic data and			
4	5	5	sinewave) FFS	: When the transm SK signal (See Figure nitter disabled, this o	÷ 4).		-step pseudo			
5	7	6	Tx Data I/P : S	Tx Data I/P: Serial logic data to be transmitted is input to this pin.						
6	8	7	put the transm	<b>Tx EnableN :</b> A logic '0' will enable the transmitter (See Figure 4). A logic '1' at this input will put the transmitter into powersave whilst forcing "Tx Sync Out" to a logic '1' and "Tx Signal Out" to a high-impedance state. This pin is internally pulled to $V_{DD}$ .						
7	9	8		<b>P:</b> The output of the require buffering pri		. This output impeda	ance is typically			
8	10	9	Rx Fnable :	The control of the Rx	function. The contro	ol of other outputs is	given below			
	10	J	Rx Enable	= Rx Function	Clock Data O/P	Carrier Detect	Rx Sync Out			
			"1"	= Enabled	Enabled	Enabled	Enabled			
			"0"	= Powersave	"0"	"0"	1" or "0"			
9	11	10	should be decor This bias volta	out of the on-chip and oupled to V <sub>ss</sub> by a cauge is maintained und supply rail (GND).	pacitor ( $C_2$ ). (See F	igure 2.	<sub>DD</sub> /2, this pin			
10	12	11	ss. Negative	зирріў Ган (ЭН <i>D)</i> .						

## Pin Number Function

DW	FX469 LG/LS	J/P6								
11	13	12	Unclocked Data O/P: The recovered asynchronous serial data output from the receiver.							
12	14	13	Clocked Data O/P: The recovered synchronous serial data output from the receiver.  Data is latched out by the recovered clock, available at the "Rx Sync O/P," (See Figure 5).							
13	15	14	Carrier Detect O/P: When an F	Carrier Detect O/P: When an FFSK signal is being received this output is a logic '1.'						
14	16	15	<b>Rx Signal I/P:</b> The FFSK signal input for the receiver. This input should be coupled via a capacitor, $C_3$ .							
15	18	17	<b>Rx Sync O/P:</b> A flywheel squarewave output. This clock will synchronize to incoming Rx FFSK data (See Figure 5).							
16	19	16	1200/2400 Baud Select: A logic '1' on this pin selects the 1200 baud option.  Tone frequencies are: one cycle of 1200Hz represents a logic '1,' one-and-a-half cycles of 1800Hz represents a logic '0.' A logic '0' on this pin selects the 2400 baud option.  Tone frequencies are: one-half cycle of 1200Hz represents a logic '1,' one cycle of 2400Hz represents a logic '0.' This function is also used, in part, to select the 4800 baud option. This pin has an internal 1Mw pullup resistor.  Operational Data Rate Configurations are illustrated in the table below.							
			Operational Data Rate Configu	ırations are illustı	rated in the	table bel	OW.			
								7		
			Operational Data Rate Configu Xtal/Clock Frequency Clock Rate pin	1.008MH			ow. <b>4.032MH</b> 1	<b>z</b> 1		
			Xtal/Clock Frequency Clock Rate pin 1200/2400 Select pin	<b>1.008MH</b> 0 1	0 0	1 1	<b>4.032MH</b> 1 0			
			Xtal/Clock Frequency Clock Rate pin	<b>1.008MH</b>	<b> z</b> 0	1	<b>1.032MH</b> 1	1		
17	20	18	Xtal/Clock Frequency Clock Rate pin 1200/2400 Select pin 4800 Select pin Baud Rate  4800 Baud Select: A logic '1' or Select pin will select the 4800 op Tone frequencies are: one-half or represents a logic '0.' This state of Clock Rate: A logic input to select	1.008MH 0 1 0 1200 1200  1 this pin combine tion (1Mw pulldow cycle of 2400Hz recan only be achie	0 0 0 2400 ed with a loo wn resistor) epresents a ved using a	1 1 0 1200 gic '0' on 1 a logic '1,' a 4.032MH	1.032MH 1 0 0 2400 the 1200/ one cycl Hz Xtal in	1 0 1 <b>4800</b> 2400 Bauce e of 4800H put.	Ηz	
17	20	18	Xtal/Clock Frequency Clock Rate pin 1200/2400 Select pin 4800 Select pin Baud Rate  4800 Baud Select: A logic '1' or Select pin will select the 4800 op Tone frequencies are: one-half or represents a logic '0.' This state of	1.008MH 0 1 0 1200 1200  1 this pin combine tion (1Mw pulldow cycle of 2400Hz recan only be achie	0 0 0 2400 ed with a loo wn resistor) epresents a ved using a	1 1 0 1200 gic '0' on 1 a logic '1,' a 4.032MH	1.032MH 1 0 0 2400 the 1200/ one cycl Hz Xtal in	1 0 1 <b>4800</b> 2400 Bauce e of 4800H put.	Ηz	
17 18	20 21 22	18 19 20	Xtal/Clock Frequency Clock Rate pin 1200/2400 Select pin 4800 Select pin Baud Rate  4800 Baud Select: A logic '1' or Select pin will select the 4800 op Tone frequencies are: one-half or represents a logic '0.' This state of Clock Rate: A logic input to sele Xtal/clock. Logic '1' = 4.032MHz,	1.008MH 0 1 0 1200  1200  1 this pin combine tion (1Mw pulldown pulldown pulldown pulldown pulldown pulldown pullogic an only be achied to the carrier the carrier detects.	0 0 2400 ed with a log wn resistor) epresents a ved using a use of eithe MHz. This in	1 1 0 1200 1200 1200 1200 1200 1200 120	1.032MH 1 0 0 2400 the 1200/ one cycl Hz Xtal in	1 0 1 4800 2400 Bauce of 4800 put.  032MHz al pulldown	Hz n	
			Xtal/Clock Frequency Clock Rate pin 1200/2400 Select pin 4800 Select pin Baud Rate  4800 Baud Select: A logic '1' or Select pin will select the 4800 op Tone frequencies are: one-half or represents a logic '0.' This state of  Clock Rate: A logic input to sele Xtal/clock. Logic '1' = 4.032MHz, resistor (1.008MHz).  Carrier Detect Time Constant: C <sub>4</sub> connected to this pin will affect	1.008MH 0 1 0 1200  1 this pin combined tion (1Mw pulldown pulldown pulldown pulldown pulldown pulldown pulldown pullogic of 2400Hz recan only be achied to the carrier of the carrier detected the carrier detected the carrier detected pullogic of the carrier detect	0 0 0 2400 ed with a log wn resistor) epresents a ved using a ved using a lise of eithe MHz. This in	1 1 0 1200 1200 1200 1200 1200 1200 120	1.032MH 1 0 0 2400 the 1200/ one cycl Hz Xtal in	1 0 1 4800 2400 Bauce of 4800 put.  032MHz al pulldown	Hz n	

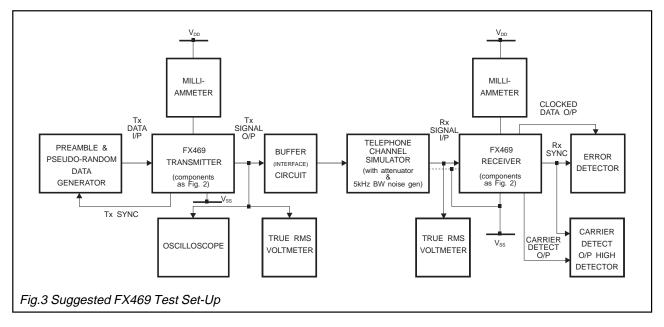
## **Application Information**



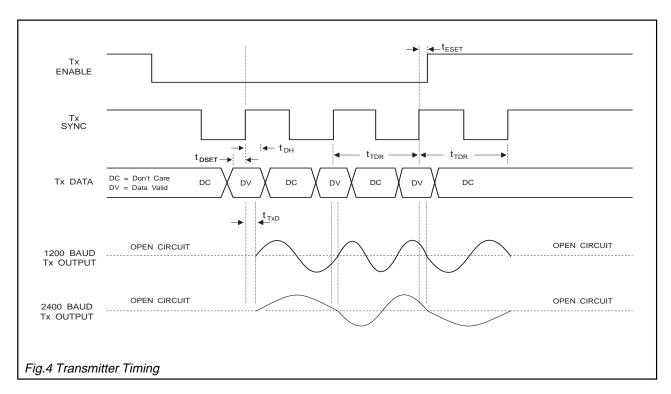
Component	value	lolerance
R,	1.0MW	±10%
C <sub>1</sub>	33.0pF	
$C_2$	1.0µF	±20%
$C_3$	0.1µF	
C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0.1µF	±10%
C <sub>5</sub>	1.0µF	±20%
C <sub>6</sub>	1.0µF	
C,	33.0pF	
$X_1^{'}$	1.008MHz	See
·	or	'Clock-Rate'
	4.032MHz	Pin

Fig.2 External Components

- input signals referenced to  $\rm V_{SS},$  decouple  $\rm V_{BIAS}$  to  $\rm V_{SS}$ using  $C_2$  only.
- 2. Use C<sub>5</sub> when input signals are referenced to V<sub>ss</sub>, to decouple V<sub>DD</sub>.
- 3. The value of  $C_4$  determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. C, may be varied to trade-off response time for noise immunity.
- 4. C<sub>7</sub> reduces Xtal voltage overshoot. Refer to CML Xtal Application Note D/XT/2 December 1991.

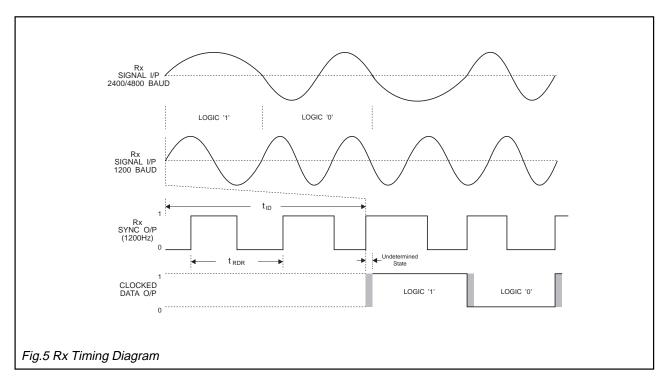


## Application Information .....



Characteristics		Note	Min.	Тур.	Max.	Unit
Tx Delay, Signal to Disable Time	t <sub>eset</sub>	3	2.0	-	800	μs
Data Set-Up Time	t	1	2.0	-	-	μs
Data Hold Time	t <sub>DH</sub>		2.0	-	-	μs
Tx Delay to O/P Time	t <sub>TxD</sub>		-	1.2	-	µs
Tx Data Rate Period	t <sub>TDR</sub>	3	-	833	-	µs
Rx Data Rate Period	t <sub>RDR</sub>	3	800	-	865	µs
Undetermined State	KDK		-	-	2.0	us.
Internal Rx Delay	t <sub>in</sub>		-	1.5	-	ms

- 1. Consider the Xtal/Clock tolerance.
- 2. All Tx timings are related to the Tx Sync Output.
- 3. 1200 baud example.



## **Specification**

#### **Absolute Maximum Ratings**

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

 $\begin{array}{lll} & & -0.3 \text{ to } 7.0 \text{V} \\ & & \text{Input voltage at any pin (ref V}_{\text{SS}} = 0 \text{V}) & -0.3 \text{ to (V}_{\text{DD}} + 0.3 \text{V}) \\ & & \text{Sink/source current (supply pins)} & +/-30 \text{mA} \\ & & & \text{(other pins)} & +/-20 \text{mA} \\ & & \text{Total device dissipation @ T}_{\text{AMB}} \text{ 25°C} & 800 \text{mW Max.} \\ & & \text{Derating} & 10 \text{mW/°C} \end{array}$ 

Operating temperature range: FX469DW/LG/LS/P6 -30°C to +70°C (plastic) FX469J -30°C to +85°C (cerdip)

Storage temperature range: FX469DW/LG/LS/P6 -40°C to +85°C (plastic)
FX469J -55°C to +125°C (cerdip)

#### **Operating Limits**

All device characteristics are measured under the following conditions unless otherwise specified:  $V_{DD} = 5.0V$ ,  $T_{AMB} = 25^{\circ}C$ . Audio Level 0dB ref: = 300mVrms. Xtal/Clock = 4.032MHz. Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth Baud Rate = 1200 baud.

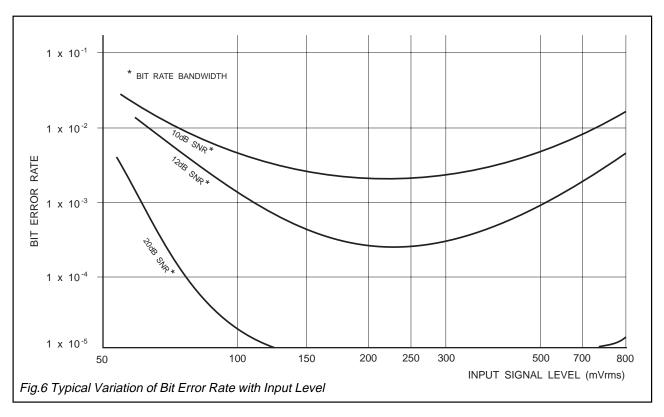
Characteristics	See Note	Min.	Тур.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current Rx Enabled Tx Disabled	I	-	3.6	-	mA
Rx and Tx Enabled		-	4.5	-	mA
Rx and Tx Disabled		-	650	-	μΑ
Logic '1' Level	1	4.0	-	_	·V
Logic '0' Level	1	-	-	1.0	V
Digital Output Impedance		_	4.0	-	kw
Analogue and Digital Input Impedance		100	-	_	kw
Tx Output Impedance		-	0.6	1.0	kw
On-Chip Xtal Oscillator					
R <sub>IN</sub>		10.0	_	_	Mw
R <sub>out</sub>		5.0	_	15.0	kw
Inverter d.c. Voltage Gain		10.0	_	20.0	V/V
Gain Bandwidth Product		4.1	_	-	MHz
Xtal Frequency	2	-	1.008	_	MHz
Xtal Frequency	2	_	4.032	-	MHz
•	_				
Dynamic Values					
Receiver					
Signal Input Dynamic Range SNR = 50dB		100	230	1000	mVrms
Bit Error Rate SNR = 12dB	3 4				
1200 Baud		-	2.5	-	10 <sup>4</sup>
2400 Baud		-	1.5	-	10³
4800 Baud		-	1.5	-	10³
SNR = 20d8	3 4				
1200/2400/4800 Baud		-	<1.0	-	10 <sup>8</sup>
Receiver Synchronization SNR =12dE	<b>3</b> 7				
Probability of Bit 16 Being Correct	,	_	0.995	_	
			0.000		
Carrier Detect	5, 10				
Sensitivity	7, 8	-	-	150	mVrms
Probabilty of C.D. Being High					
After Bit 16 SNR = 12dB	,		0.995		
0dB Noise No Signal	9		0.05		

## Specification .....

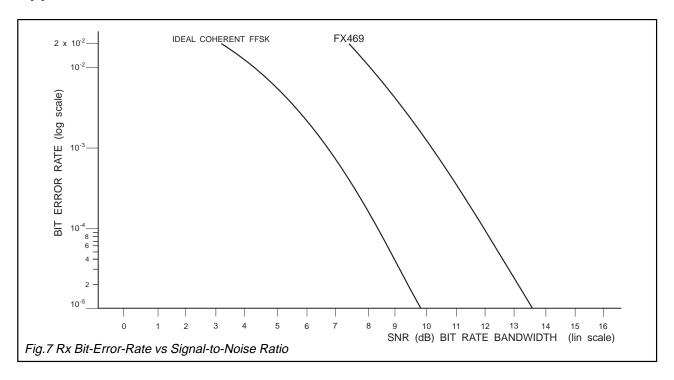
Characteristics	(	See Note	Min.	Тур.	Max.	Unit
Transmitter Output						
Tx Output Level			-	775	-	mVrms
Output Level Variation						
1200/1800Hz or 1200/2	400Hz or 2400/4	4800Hz	0	-	±1.0	dB
Output Distortion			-	3.0	5.0	%
3rd Harmonic Distortion			-	2.0	3.0	%
Logic '1' Carrier Frequency	1200 Baud	6	-	1200	-	Hz
, ,	2400 Baud	6	-	1200	-	Hz
	4800 Baud	6	-	2400	-	Hz
Logic '0' Carrier Frequency	1200 Baud	6	-	1800	-	Hz
	2400 Baud	6	-	2400	-	Hz
	4800 Baud	6	-	4800	-	Hz
Isochronous Distortion						
1200Hz - 1800Hz/1800Hz - 1200Hz			-	25.0	40.0	μs
1200Hz - 2400Hz/2400Hz - 1200Hz			-	20.0	30.0	μs
2400Hz - 4800Hz/4800Hz - 2	2400Hz			-	10.0	20 μs

#### **Notes**

- With reference to V<sub>DD</sub> = 5.0 volts.
   Xtal frequency, type and tolerance depends upon system requirements.
- 3. See Figure 5 (variation of BER with Input Signal Level).
- 4. SNR = Signal-to-Noise Ratio in the Bit-Rate Bandwidth.
- 5. See Figure 2.6. Dependent upon Xtal tolerance.
- 7. 10101010101 ...01 pattern.
- 8. Measured with a 150mVrms input signal (no noise); 1200/2400 baud operation.
- 9. Reference (0dB) level for C.D. probability measurements is 230mVrms.
- 10. For 1200 and 2400 baud operation only; when operating at 4800 baud the Carrier Detect output should be ignored.



## **Application Information**



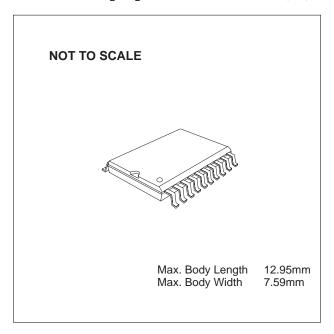
### **Package Outlines**

The FX469 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document. Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

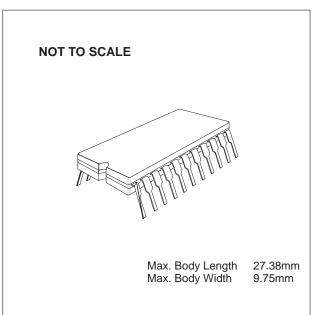
## **Handling Precautions**

The FX469 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX469DW 20-pin plastic S.O.I.C. (D3)



FX469J 22-pin cerdip DIL (J3)



## Package Outlines .....

**FX469LG** 24-pin quad plastic encapsulated

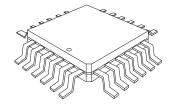
bent and cropped (L1)

**FX469LS** 24-lead plastic leaded chip carrier

(L2)

10.40mm

**NOT TO SCALE** 



Max. Body Length 10.25mm Max. Body Width 10.25mm NOT TO SCALE

Max. Body Length 10.40mm

Max. Body Width

## **Ordering Information**

**FX469DW** 20-pin surface mount S.O.I.C.

**FX469J** 22-pin cerdip DIL

FX469LG 24-pin quad plastic encapsulated

bent and cropped

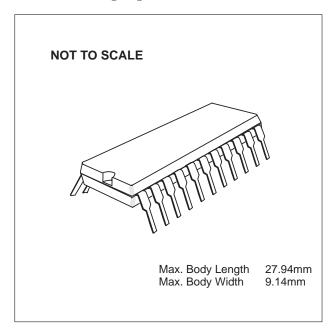
(L1)

**FX469LS** 24-lead plastic leaded chip carrier

(12)

**FX469P6** 22-pin plastic DIL

FX469P6 22-pin plastic DIL



CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.



#### **CML Product Data**

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc (Consumer Microcircuits Limited (UK), MX-COM, Inc. (USA) and CML Microcircuits (Singapore) Pte Ltd) have undergone name changes and, whilst maintaining their separate new names (CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd), now operate under the single title CML Microcircuits.

These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

#### **CML Microcircuits Product Prefix Codes**

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

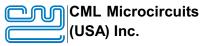
This notification is relevant product information to which it is attached.

Company contact information is as below:



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