SIEMENS

Dual-Tone Multi-Frequency Generator (DTMF)

PSB 8591

| Type	Ordering Code	Package
PSB 8591	Q67000–Y895	P-DIP-20

The DTMF generator PSB 8591 is a monolithic IC using the I^2L technology. It provides all Dual-Tone Multi-Frequency (DTMF) pairs required in tone dialing systems. The eight different audio output frequencies are generated from an on-chip reference oscillator with an external low-cost crystal (2^{22} Hz). The internal temperature compensated voltage reference determines the audio output levels and controls the on-chip shunt regulator which provides the adaptation to different feeding conditions.

In order to meet the CEPT recommendations an external 2-pole RC filter can easy be connected. Typical telephone applications are shown in **figures 15a-15c**. The PSB 8591 can interface directly to a single-contact keyboard. Furthermore, the device can be controlled either from a MPU (binary mode) or via a 2-out-of-8 keyboard. The PSB 8591 works in parallel to the speech circuit. If no key is pressed, the device consumes only low standby current. When data is input via keyboard or MPU interface, a low-active mute signal is generated.

Features

- CEPT compatible output spectrum and output levels
- Directly line powered
- MUTE output
- Chip disable ($\overline{CD}$)
- Current sink disable ($\overline{CSD}$)
- MPU interface with data latch on-chip
- Operation with either single contact or 2-out-of-8 keyboard
- 2 key rollover with contact debouncing
- Dual-tone and single-tone operation
- High frequency accuracy (typ. 0.4%)
- Standard low-cost crystal 4.19 MHz
- Power dissipation limited by internal thermal overload protection
- I^2L technology

Block Diagram
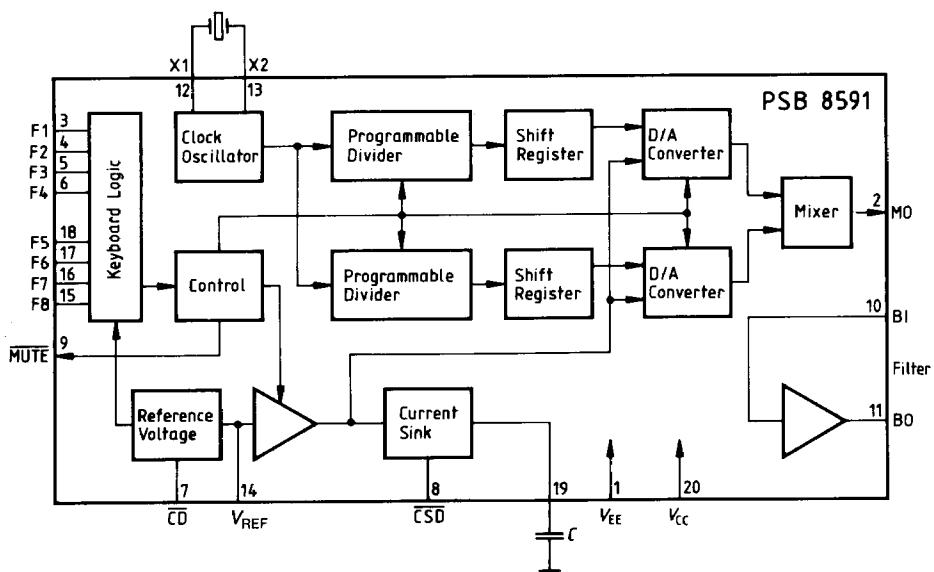
Pin Configuration
(top view)
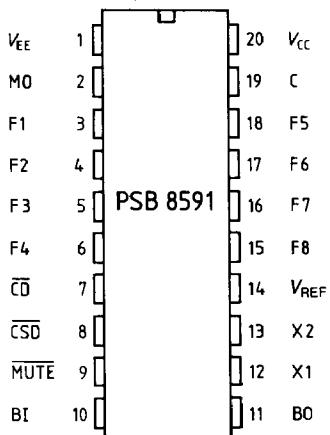
Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{EE}	Negative power line connection
2	MO	**Mixer Output**
3 4 5 6	F1 F2 F3 F4	Keyboard interface
7	$\overline{CD}$	**Chip Disable**
8	$\overline{CSD}$	**Current Sink Disable**
9	$\overline{MUTE}$	**MUTE** output (open collector)
10	BI	Input of output amplifier
11	BO	Output of output amplifier
12 13	X1 X2	Connections for crystal $f = 2^{22}$ Hz
14	V_{REF}	Voltage reference
15	F8	Keyboard interface and mode select
16 17	F7 F6	Keyboard interface and write enable
18	F5	Keyboard interface and supply current enable
19	C	Connection for filtering capacitor for the current sink
20	V_{CC}	Positive power line connection

Connection to the Telephone Line
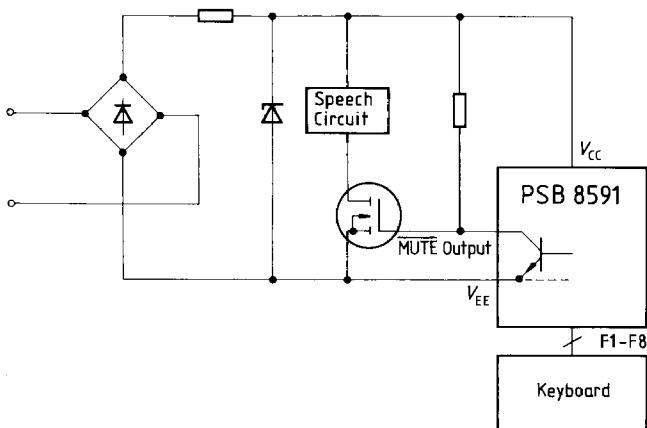
Single Contact Keyboard Interface
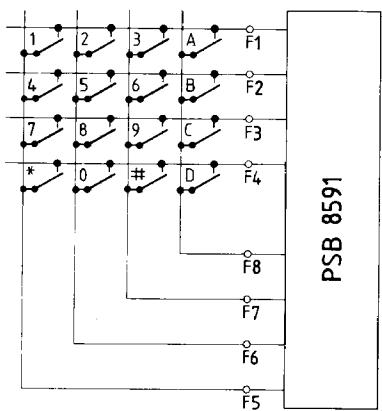
Two key rollover with contact debounce is provided.

Required contact specifications:

open contact: resistance $R_N > 400$ kΩ

closed contact: resistance $R_E \leq 1$ kΩ for $I = 100$ μA

Siemens Aktiengesellschaft   890

Functional Description

1. Line Adaptation

The DTMF generator PSB 8591 has an internal temperature-compensated voltage reference. This reference voltage controls a shunt regulator which sets the DC voltage $V_L = V_{CC} - V_{EE}$ to 5 V. The external filtering capacitor C gives the shunt regulator for frequencies above 300 Hz the behavior of a high impedance current sink. The shunt regulator includes a start-up circuit for the quick charging of the filtering capacitor **(figure 1)**. The shunt regulator can sink line currents up to 120 mA while the power dissipation is limited by internal thermal overload protection. If the chip temperature exceeds a preset value ($T_j \approx 150\,°C$, $P_V \approx 1$ W), the filtering capacitor is discharged, the shunt regulator is switched off and the voltage V_L rises to the breakdown voltage of the external overvoltage protection network **(figure 2)**. If the current sink is disabled (low level at $\overline{CSD}$, pin 8) an external shunt regulator or speech circuit should be used.

2. Tone Generation

The on-chip oscillator generates together with the external clock crystal the master clock frequency $f_{CLK} = 4.194304$ MHz.

Clock f_{CLK} is scaled by a factor of 16 to $f_{CLK\ 1} = 262.144$ kHz. The programmable dividers for the higher (f_5-f_8) and lower (f_1-f_4) audio frequency groups are driven by the clock f_{CLK}. The programmable dividers generate the clock for the 6-bit L/R shift registers. Each shift register controls one D/A converter and the polarity of its output waveform. The output sinewave is synthesized as a stairstep function with 11 voltage levels. The output waveform has 22 time segments **(figure 3)**. The time segments t_1 to t_6, t_8 to t_{17} and t_{19} to t_{22} are equal. The time segments t_7 and t_{18} are equal but slightly different from the others in order to meet the required output frequencies as closely as possible. The output waveforms are symmetrical; therefore, no even harmonics exist. The stairstep function with 11 voltage levels is calculated such that, theoretically, the lowest order harmonics are the 21st and 23rd. Because of the different length of time segments t_7 and t_{18} and the tolerances of the D/A converter, lower odd harmonics exist.

Figure 3
Synthesized Output Waveforms
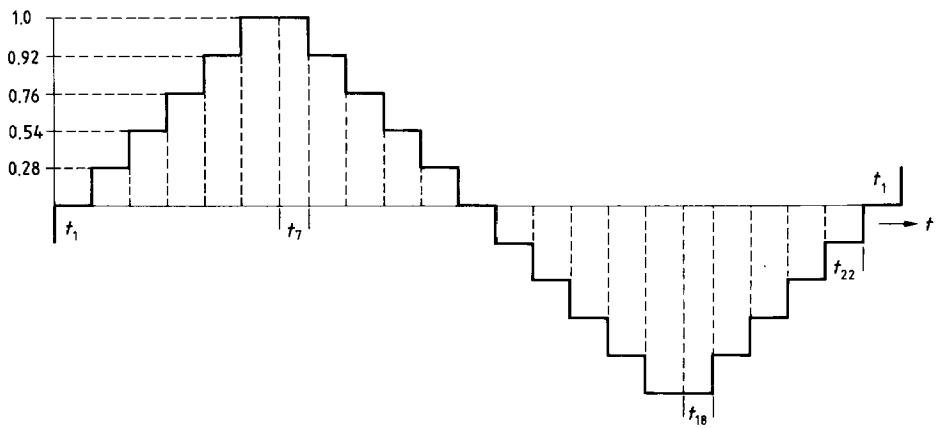
3. Output Levels

Each D/A converter generates a five-level stairstep function. The mixer alternately reverses the polarity of the five-level stairstep function which leads to the symmetrical 11-level stairstep function **(figure 3)**. Furthermore, the mixer adds the stairstep function of the lower and of the higher frequency group.

The nominal amplitudes of the stairstep function at the mixer output are:

Lower frequency group $\quad\quad i_{ML} = 42.5 \; \mu A$
Higher frequency group $\quad\quad i_{MH} = 53.5 \; \mu A$

Figure 4 shows the AC schematic of the output section of the PSB 8591. The feedback loop of the output amplifier is externally arranged. The resistors R_1 to R_3 determine the output level (V_{OL} and V_{OH}) and the output impedance Z_O, as shown below.

$$Z_O = \frac{R_1 \, (r_2 + r_3)}{R_1 + r_3 \; \left(1 + \dfrac{R_3 + R_1}{R_2 + r_1}\right)}$$

$$V_{OL, H} = i_{ML, H} \times \frac{(R_3 + R_1) \, R_L \times r_1}{R_1 \, (R_2 + r_1)} \times \frac{Z_O}{Z_O + R_L}$$

The ratio of the resistors R_3/R_2 is restricted to the range $R_3/R_2 < 1.2$, otherwise the output amplitudes are clipped. Normally, the resistors R_2 and R_3 are equal. **Figure 8** shows the sum level P_S and the output impedance Z_O as a function of R_1 and R_2.

Figure 4
AC Schematic of the Output Stage

$r_1 = 1.7 \text{ k}\Omega$
$r_2 + r_3 = 2 \text{ k}\Omega$
$r_3 = 56 \Omega$
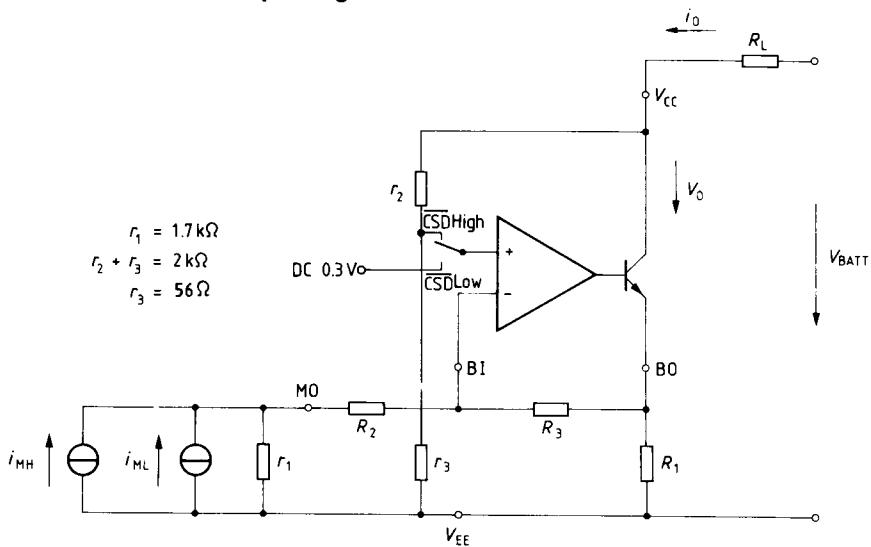
The internal feedback loop is normally closed (r_2, r_3, positive input of output amplifier).

If the current sink is disabled, the positiv input of the output amplifier is supported with a fixed voltage of about 0.3 V. This voltage is derived from the internal reference voltage.

An external RC filter network is necessary in order to meet CEPT recommendations concerning distortion and harmonics. The RC filter is easy to implement, because the pins MO, BI, BO of the output amplifier are accessible. The PSB 8591 is shown in **figure 5** with an one-pole RC filter for applications corresponding to the recommendations of the German Federal Postal Administration and in **figure 6** with a two-pole RC filter for CEPT applications. **Figure 7** shows the output spectrum for the most critical case, the frequency f_8.

The nominal output levels $P_{L, H}$ are identical for the arrangement in **figure 5** and **figure 6**, they are

$$P_L = 20 \log \left(\frac{V_{OL}}{\sqrt{2} \ \sqrt{1 \ \text{mW} \times 600 \ \Omega}} \right) = -8.12 \ \text{dBm}$$

$$P_H = 20 \log \left(\frac{V_{OH}}{\sqrt{2} \ \sqrt{1 \ \text{mW} \times 600 \ \Omega}} \right) = -6.12 \ \text{dBm}$$

The sum output level P_S is
$P_S = 10 \log (10 \ \text{EXP}(P_L/10) + 10 \ \text{EXP} (P_H/10)) = -4 \ \text{dBm}$ (with $R_1 = 56 \ \Omega$)
and the preemphasis P_D is
$P_D = P_H - P_L = 2 \ \text{dB}$

Figure 5
PSB 8591 with a 1-Pole RC Filter
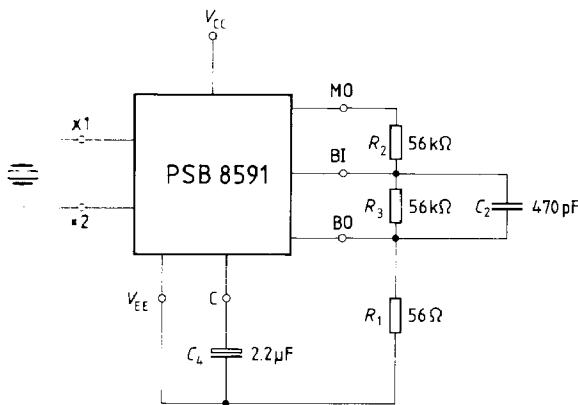
In order to keep the insertion loss for all the DTMF frequencies less than 0.2 dB the 3 dB cutoff frequency of the filter should be at least 6 kHz.

Figure 6
PSB 8591 with a 2-Pole RC Filter (Butterworth)
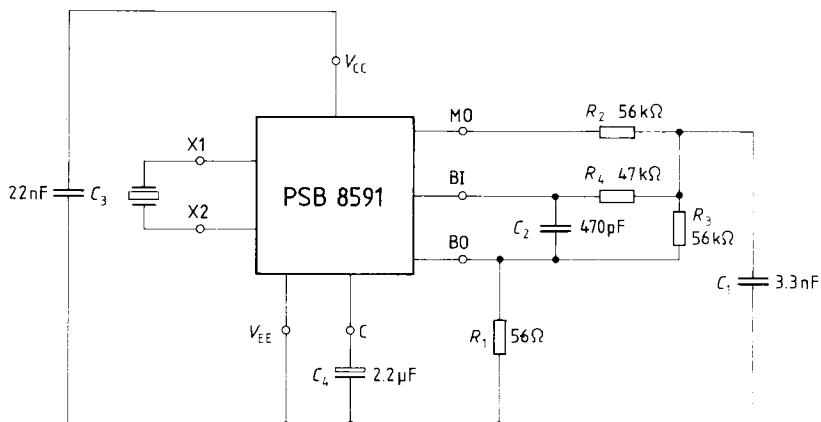
The pole is $f_p \approx 2.7$ kHz

Figure 7
**Output Spectrum for Frequency f_8 with a 2-Pole Butterworth Filter**
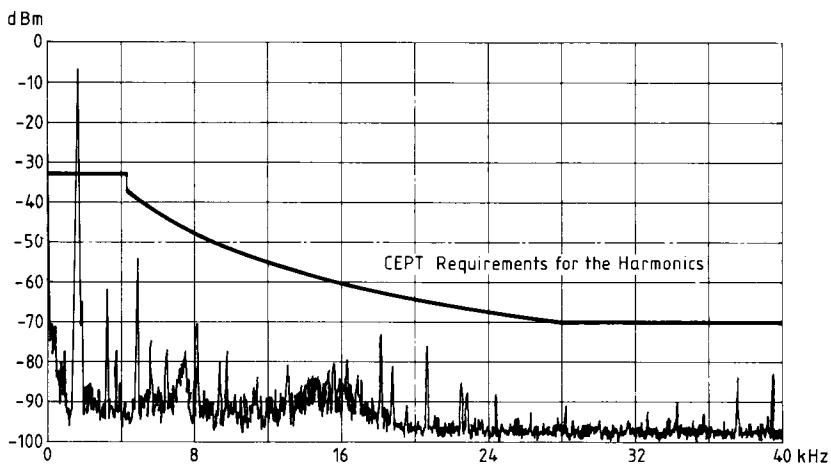
Figure 8

Sum Output Level P_S (–) and Output Impedance Z_O (---) versus Resistors R_1, R_2.
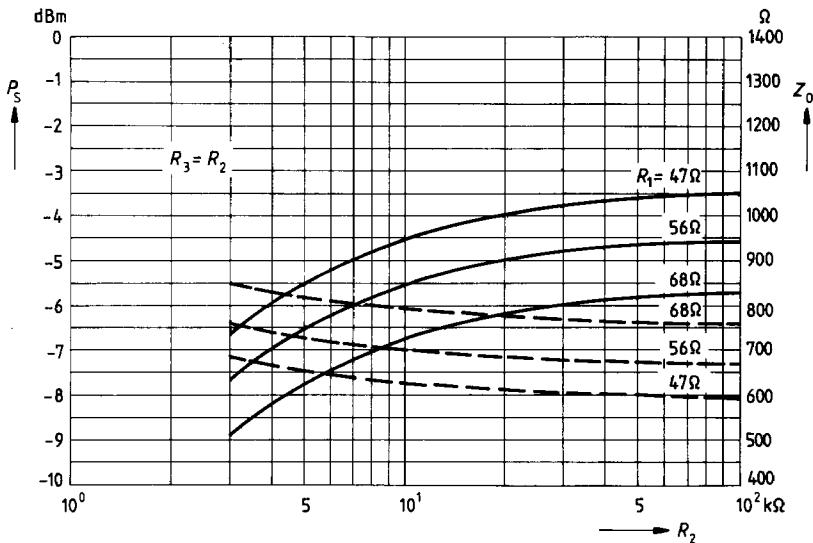
Operation Modes:

a) Single-contact or 2-out-of-8 keyboard interface
b) MPU interface

Figure 9 shows the schematic of the interface inputs F1 to F8. The inputs are divided into two groups F1 to F4 and F5 to F8. In addition, pin F8 controls the operation modes. The resistors R_F are optimized for the single-contact keyboard mode.

a) Interface to single contact or 2-out-of-8 keyboard **(figure 9)**.

The keys are debounced and electronically interlocked. If multiple keys are pushed, the frequencies of the key activated first will be generated. The requirements for the quality of the contacts are

contact open: OFF resistance $R_{OFF} > 400$ kΩ
contact closed: ON resistance $R_{ON} \leq 1$ kΩ
                                              $I = 100$ µA

Figure 9
Schematic of Keyboard Interface
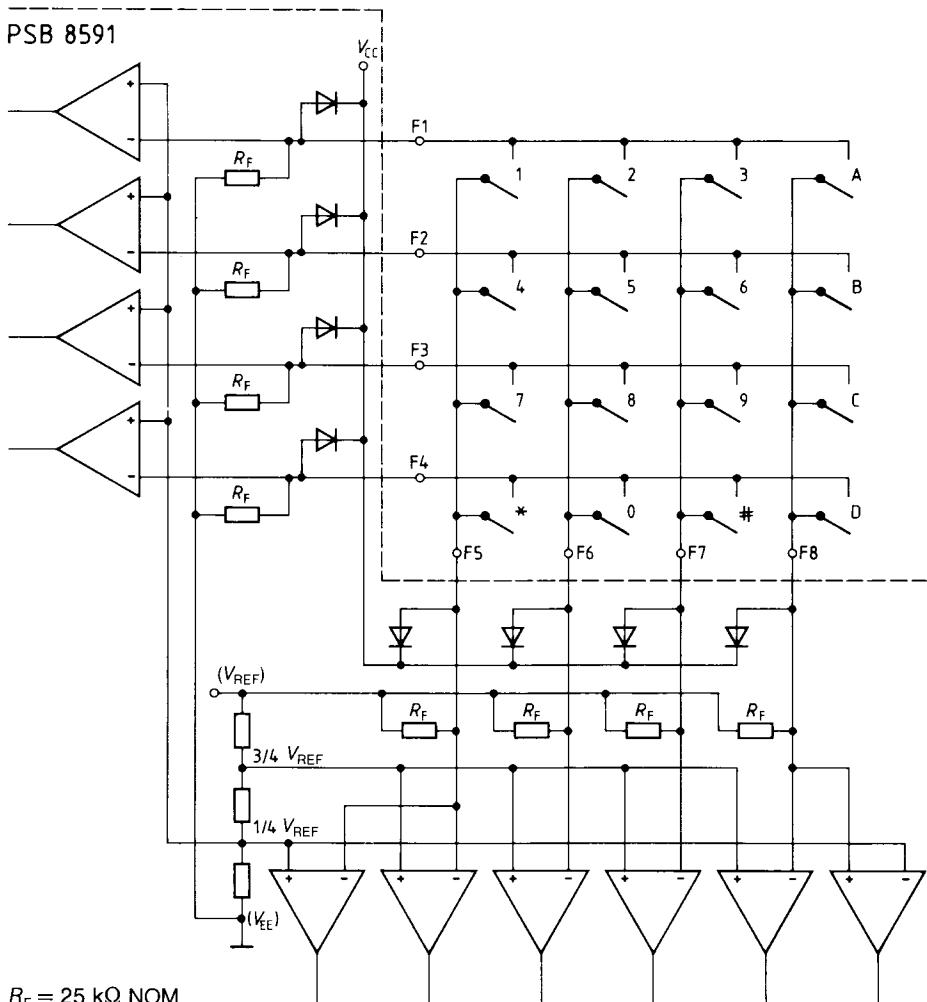
$R_F = 25\ \text{k}\Omega\ \text{NOM}$
$V_{REF} = 1.25\ \text{V} \pm 0.1\ \text{V}$

b) MPU interface **(figure 10)**

The mode control input F8 is connected to ground; pin 7 $\overline{\text{(CD)}}$ is open. Low level at pin 8 $\overline{\text{(CSD)}}$ disables the current sink. The dual tone pairs are generated according to the binary code at the inputs G1 to G4, as shown in the following table.

Information is Present at Inputs G1 to G4 in Binary Code

Digit	0	1	2	3	4	5	6	7	8	9	✳	#	A	B	C	D
G4	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
G3	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L
G2	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L
G1	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L

Figure 10

MPU Interface

I. with open collector AND-Gate

II. with Schottky – diodes
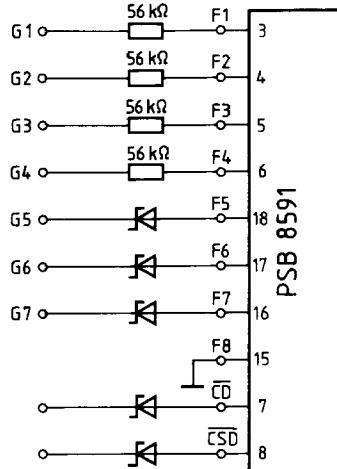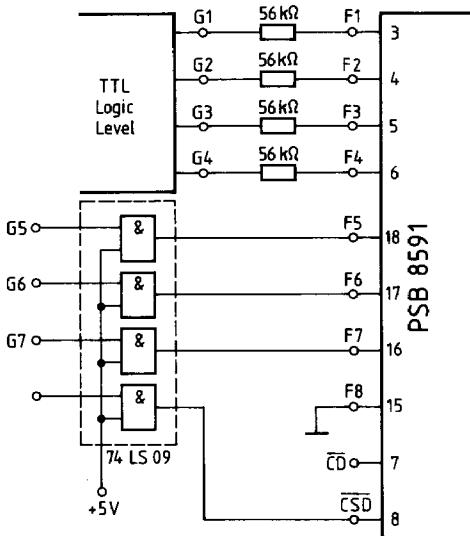
The enable inputs G5 to G7 have the following functions:

G5	G6	G7	
L	L	L	data fetch for f_L and f_H, output inhibited
L	H	L	single-tone, higher frequency group (f_H), data fetch for f_L
L	L	H	single-tone, lower frequency group (f_L), data fetch for f_H
L	H	H	sending, dual-tone

The application example shown in **figure 10** enables both, dual- and single-tone output.

Timing Diagram

Binary data input; single-tone output, F8 connected to ground.
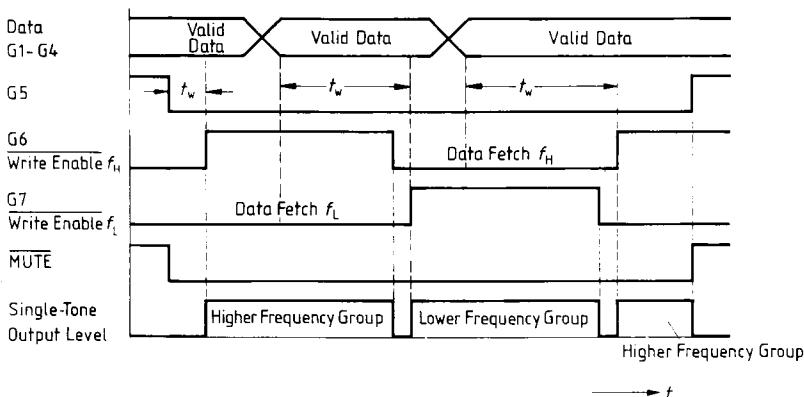
Timing Diagram

Binary data input; dual-tone output, F8 connected to ground

The valid input data is stored in clock-level-controlled flipflops

$t_w \geq 10\,\mu s$
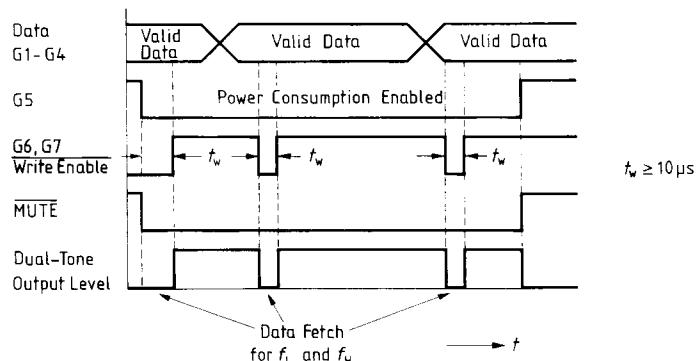
Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Voltage at any pin	V_S	$V_{EE} - 0.3$	see operating characteristics	V
Supply voltage	$V_{CC} - V_{EE}$	-0.3	22 (2 ms)	V
Storage temperature	T_{stg}	-55	125	°C

Operating Characteristics
$T_A = -25\,°C$ to $70\,°C$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
Leakage current[1]	I_{LK}		20	100	µA µA	$V_L = 18$ V $V_L = 5$ V
Standby current[2]	I_{St}		0.4	0.6	mA mA	$V_L = 18$ V $V_L = 5$ V
Line current[3]	I_L	16		120	mA	
Supply current[5]	I_S		13	17	mA	$V_L = 5$ V
Current sink voltage drop[3] (average DC value)	V_L	4.5	5	6	V	$16\ \text{mA} \leq I_L \leq 120\,\text{mA}$
Minimal peak line voltage[5] maximal peak line voltage[5]	$V_{L\,min}$ $V_{L\,max}$		3 18		V V	(see fig. 11)
Internal reference voltage[4]	V_{REF}	1.15	1.25	1.35	V	
Input resistance at pins 3–6, 13–16, F1–F8 and $\overline{CSD}$	R_F	15	25	35	kΩ	

[1] $\overline{CD}$ connected to ground, chip disabled
[2] F1–F8 open, $\overline{CD}$ open, chip enabled
[3] Current sink enabled ($\overline{CSD}$ = high level), button pressed or F5 and F8 connected to ground
[4] $\overline{CD}$ open, chip enabled
[5] Current sink disabled ($\overline{CSD}$ = low level), button pressed or F5 and F8 connected to ground
$[R_1$ (fig. 4/fig. 5) = 82 Ω)

Operating Characteristics (cont'd)
$T_A = -25\,°C$ to $70\,°C$

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Levels						
Logical L	$V_{IL\,F1\text{-}F4}$	−0.3		0.15	V	
H	$V_{IH\,F1\text{-}F4}$	0.5		V_{CC}	V	
Logical L	$V_{IL\,\overline{CSD},\,F6\text{-}F7}$	−0.3		0.7	V	
H	$V_{IH\,\overline{CSD},\,F5\text{-}F8}$	1.1		V_{REF}	V	
Logical L, key code	$V_{IL\,F5,\,F8}$	0.5		0.7	V	
Binary mode enable	$V_{IL\,F8}$	−0.3		0.1	V	
Supply current enable	$V_{IL\,F5}$	−0.3		0.1	V	
Logical L	$V_{IL\,\overline{CD}}$	−0.3		0.3	V	$I_{IL\,max} \leq -10\,\mu A$
Logical H	$V_{IH\,\overline{CD}}$	0.7		5	V	input current $I_{IH\,max} = 1\,mA$
MUTE Output Levels						
Logical L	$V_{OL\,\overline{MUTE}}$			0.5	V	$I_{OL\,max} = 1\,mA$
Logical H	$V_{OH\,\overline{MUTE}}$		V_{CC}		V	$I_{OH\,max} = 1\,mA$
	$I_{IH\,\overline{MUTE}}$			100	nA	$V_{OH\,\overline{MUTE}} = 18\,V$
Output Levels						
Low group	P_L		−8.12		dBm	
High group	P_H		−6.12		dBm	
Sum level	P_S	−5.4	−4	−2.8	dBm	$I_L = 16\,mA$ to $120\,mA$ **fig. 13**
Preemphasis	P_D	1.8	2.4	2.8	dB	$I_L = 16\,mA$ to $120\,mA$
Sum level (frequencies disabled)	P_{SO}		−80		dBm	
Output dynamic impedance	Z_{DO}	600		1000	Ω	$I_L = 120\,mA$
		660		1000	Ω	$I_L = 20\,mA$
	Z_{Dd}		9		kΩ	$\overline{CSD}$ low $V_L = 5\,V$ (current sink disabled)
Output dynamic impedance in standby mode	Z_{St}	10	20		kΩ	$V_L = 5\,V$

Operating Characteristics (cont'd)

$T_A = -25\,°C$ to $70\,°C$

| Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		

Timing Specification

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Tone frequency deviation	f/f	−7	4	7	‰	
Key debounce time	t_d	2		6	ms	
Setup time **(figure 14)**	t_s			7	ms	$I_L = 16$ mA to 20 mA
				5	ms	$I_L = 20$ mA to 120 mA
Write pulse width	t_w		2	10	µs	

**Tone Frequency Deviation (without tolerances of crystal)***

	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	
Required frequency	697	770	852	941	1209	1336	1477	1633	Hz
Generated frequency*)	697.2	771.0	851.1	943	1212.6	1337.5	1472.7	1638.4	Hz
Deviation	2.75	1.374	−1.037	2.087	3.829	1.1	−2.898	3.307	‰

Figure 11
Minimum/Maximum Peak Line Voltage
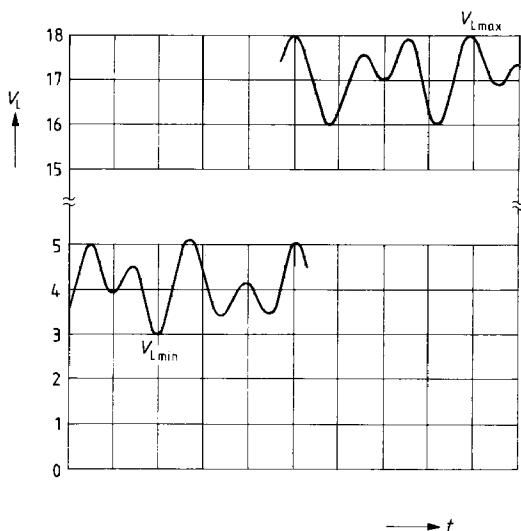
*) The low cost crystal has the following deviations (including aging and temperature range):
$\Delta f/f \leq 3.5 \times 10^{-3}$.

Figure 12

Schematic of Inputs $\overline{\text{CD}}$ (pin 7) and $\overline{\text{CSD}}$ (pin 8):

Equivalent of input $\overline{\text{CD}}$

Equivalent of input $\overline{\text{CSD}}$

$I_B = 5\,\mu A$ typ
$R_{\overline{CD}} = 5\,k\Omega$ NOM.

$R_f = 25\,k\Omega$ NOM.
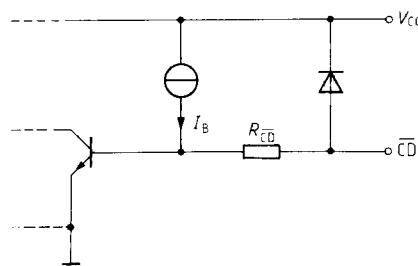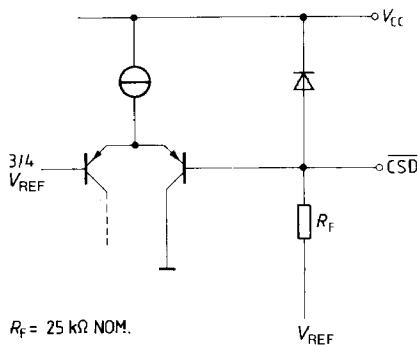
Figure 13

Test Circuit for Output Sum Level P_{so}, Power Enabled

$600\,\Omega$

V_{CC}

X1   MO

X2   BI $56\,k\Omega$

18 V   F1   **PSB 8591** $56\,k\Omega$

BO

F5

P_{SO} $15\,V < V_{BATT} < 80\,V$

V_{EE} C $56\,\Omega$

$C_4 \;\; 2.2\,\mu F$
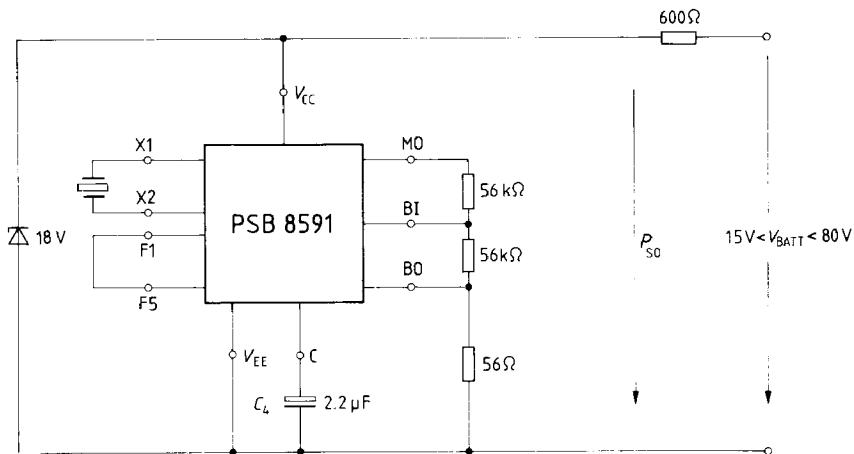
Figure 14

**a) Circuitry to Measure the Setup Time t_S, Keys Pressed or Binary Mode**
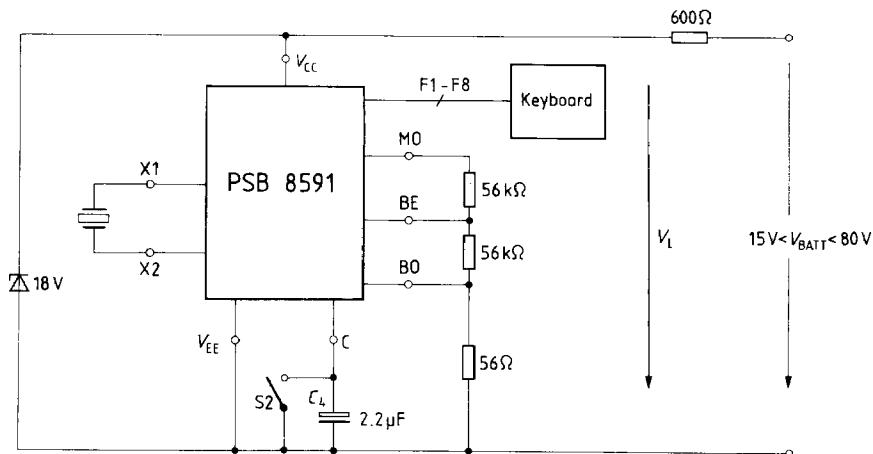
b) Timing Diagram
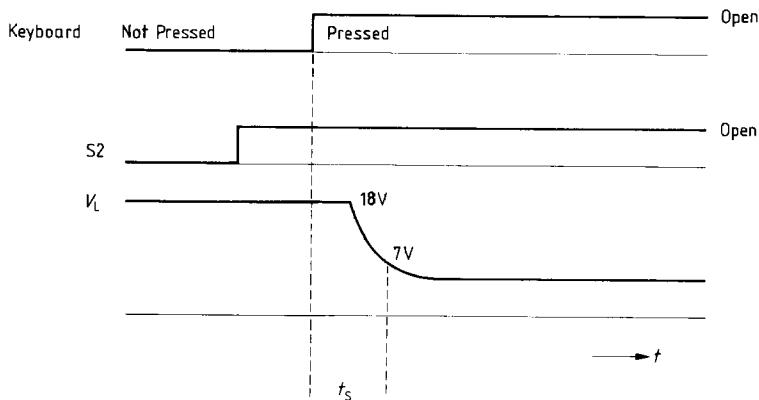
Figure 15a

Application Example

PSB 8591 Connected to a Speech Network with Hybrid Transformer
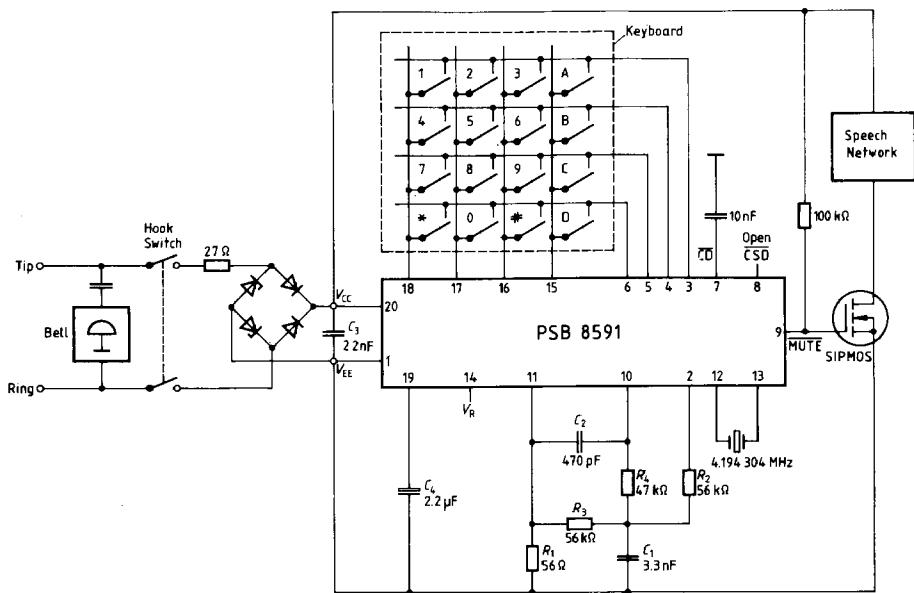
Figure 15b
Application Example
PSB 8591 Connected to an Integrated Speech Circuit
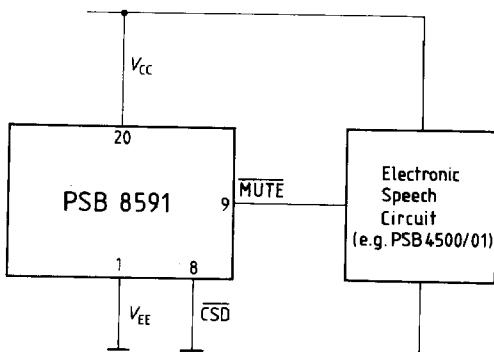
Figure 15c
Principle Block Diagram of a Pushbutton Telephone using the C̅D̅ Function

In the case of local supply failure the PSB 8591 is activated so that dialing is still possible.