

# Digital-to-Analog Converters with Serial Interface

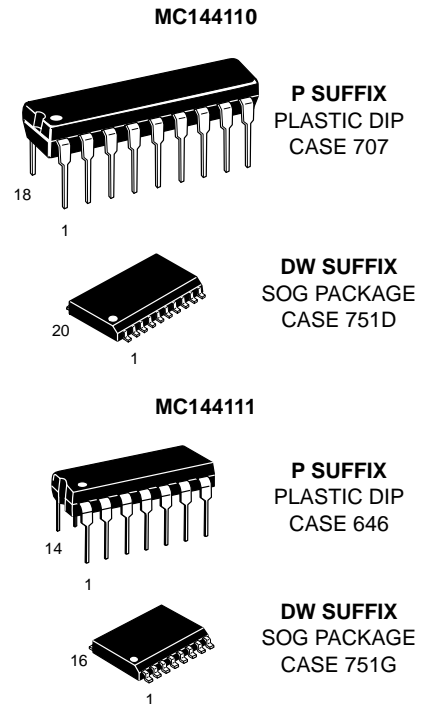
## CMOS LSI

The MC144110 and MC144111 are low-cost 6-bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

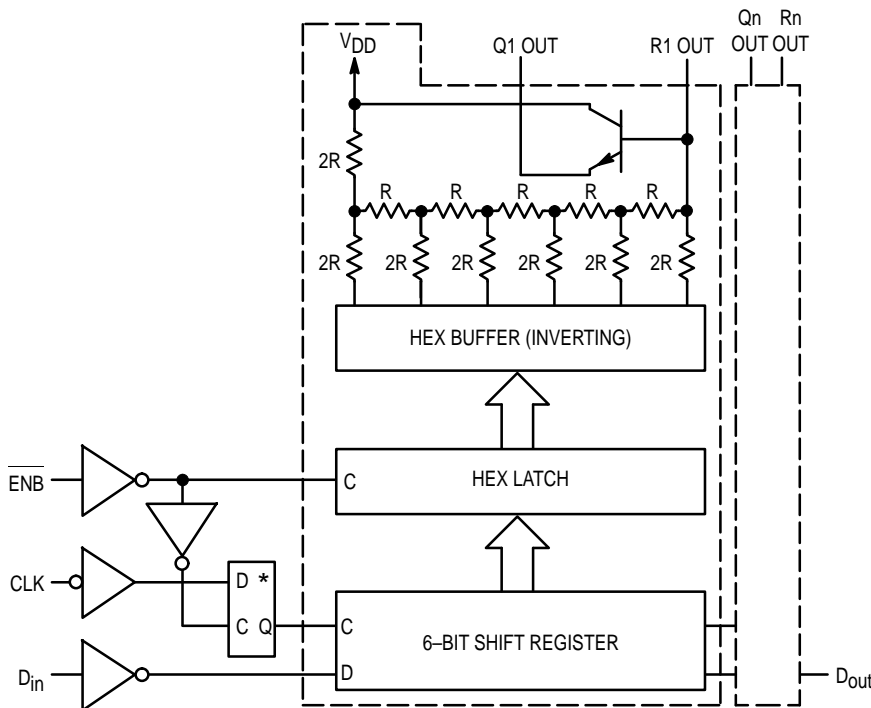
Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 V supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 V.

- Direct R-2R Network Outputs
- Buffered Emitter-Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS  $\mu$ P
- Wide Operating Voltage Range: 4.5 to 15 V
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

## MC144110 MC144111

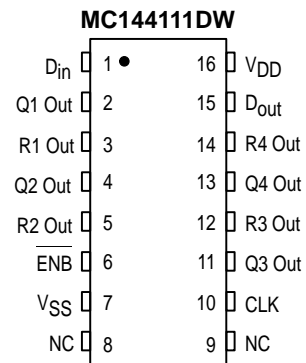
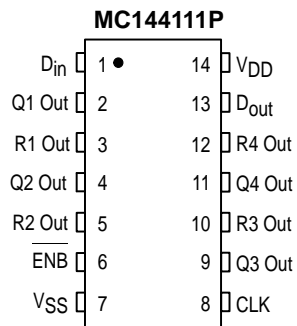
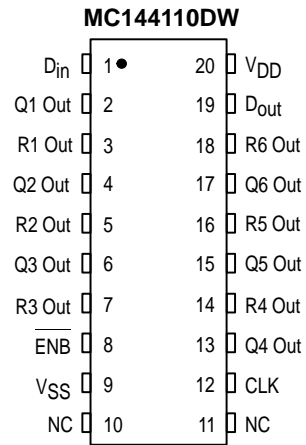
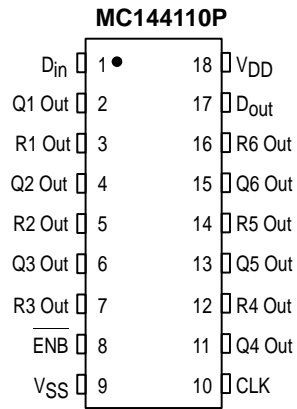


### BLOCK DIAGRAM



\* Transparent Latch

## PIN ASSIGNMENTS



NC = NO CONNECTION

**MAXIMUM RATINGS\*** (Voltages referenced to  $V_{SS}$ )

Parameter	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	- 0.5 to + 18	V
Input Voltage, All Inputs	$V_{in}$	- 0.5 to $V_{DD} + 0.5$	V
DC Input Current, per Pin	I	$\pm 10$	mA
Power Dissipation (Per Output) $T_A = 70^\circ\text{C}$ , MC144110 MC144111 $T_A = 85^\circ\text{C}$ , MC144110 MC144111	$P_{OH}$	30 50 10 20	mW
Power Dissipation (Per Package) $T_A = 70^\circ\text{C}$ , MC144110 MC144111 $T_A = 85^\circ\text{C}$ , MC144110 MC144111	$P_D$	100 150 25 50	mW
Storage Temperature Range	$T_{stg}$	- 65 to + 150	$^\circ\text{C}$

\* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that  $V_{in}$  and  $V_{out}$  be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ).

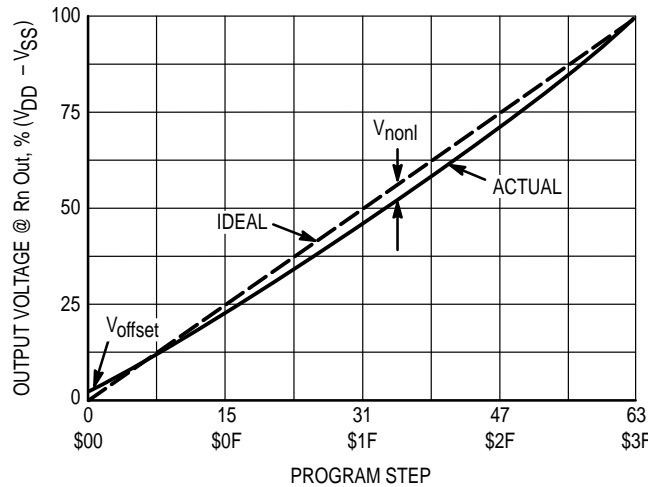
**ELECTRICAL CHARACTERISTICS** (Voltages referenced to  $V_{SS}$ ,  $T_A = 0$  to  $85^\circ\text{C}$  unless otherwise indicated)

Symbol	Parameter	Test Conditions	$V_{DD}$	Min	Max	Unit
$V_{IH}$	High-Level Input Voltage ( $D_{in}$ , ENB, CLK)		5 10 15	3.0 3.5 4	—	V
$V_{IL}$	Low-Level Input Voltage ( $D_{in}$ , ENB, CLK)		5 10 15	— — —	0.8 0.8 0.8	V
$I_{OH}$	High-Level Output Current ( $D_{out}$ )	$V_{out} = V_{DD} - 0.5 \text{ V}$	5	- 200	—	$\mu\text{A}$
$I_{OL}$	Low-Level Output Current ( $D_{out}$ )	$V_{out} = 0.5 \text{ V}$	5	200	—	$\mu\text{A}$
$I_{DD}$	Quiescent Supply Current MC144110 MC144111	$I_{out} = 0 \mu\text{A}$	15 15	— —	12 8	mA
$I_{in}$	Input Leakage Current ( $D_{in}$ , ENB, CLK)	$V_{in} = V_{DD} \text{ or } 0 \text{ V}$	15	—	$\pm 1$	$\mu\text{A}$
$V_{nonl}$	Nonlinearity Voltage ( $R_n$ Out)	See Figure 1	5 10 15	— — —	100 200 300	mV
$V_{step}$	Step Size ( $R_n$ Out)	See Figure 2	5 10 15	19 39 58	137 274 411	mV
$V_{offset}$	Offset Voltage from $V_{SS}$	$D_{in} = \$00$ , See Figure 1	—	—	1	LSB
$I_E$	Emitter Leakage Current	$V_{Rn \text{ Out}} = 0 \text{ V}$	15	—	10	$\mu\text{A}$
$h_{FE}$	DC Current Gain	$I_E = 0.1 \text{ to } 10.0 \text{ mA}$ $T_A = 25^\circ\text{C}$	—	40	—	—
$V_{BE}$	Base-to-Emitter Voltage Drop	$I_E = 1.0 \text{ mA}$	—	0.4	0.7	V

## SWITCHING CHARACTERISTICS

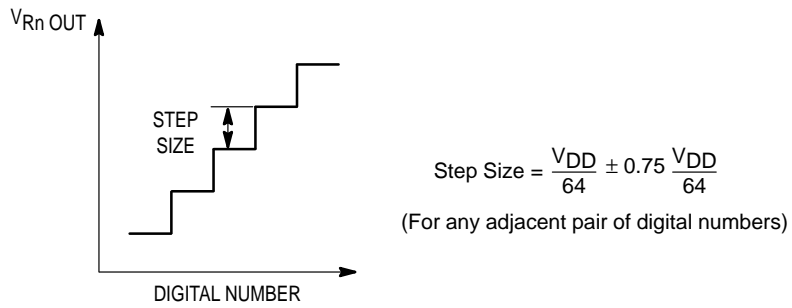
(Voltages referenced to  $V_{SS}$ ,  $T_A = 0$  to  $85^\circ\text{C}$ ,  $C_L = 50$  pF, Input  $t_r = t_f = 20$  ns unless otherwise indicated)

Symbol	Parameter	$V_{DD}$	Min	Max	Unit
$t_{wH}$	Positive Pulse Width, CLK (Figures 3 and 4)	5	2	—	$\mu\text{s}$
		10	1.5	—	
		15	1	—	
$t_{wL}$	Negative Pulse Width, CLK (Figure 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_{su}$	Setup Time, ENB to CLK (Figures 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_{su}$	Setup Time, $D_{in}$ to CLK (Figures 3 and 4)	5	1000	—	ns
		10	750	—	
		15	500	—	
$t_h$	Hold Time, CLK to ENB (Figures 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_h$	Hold Time, CLK to $D_{in}$ (Figures 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_r, t_f$	Input Rise and Fall Times	5 – 15	—	2	$\mu\text{s}$
$C_{in}$	Input Capacitance	5 – 15	—	7.5	pF

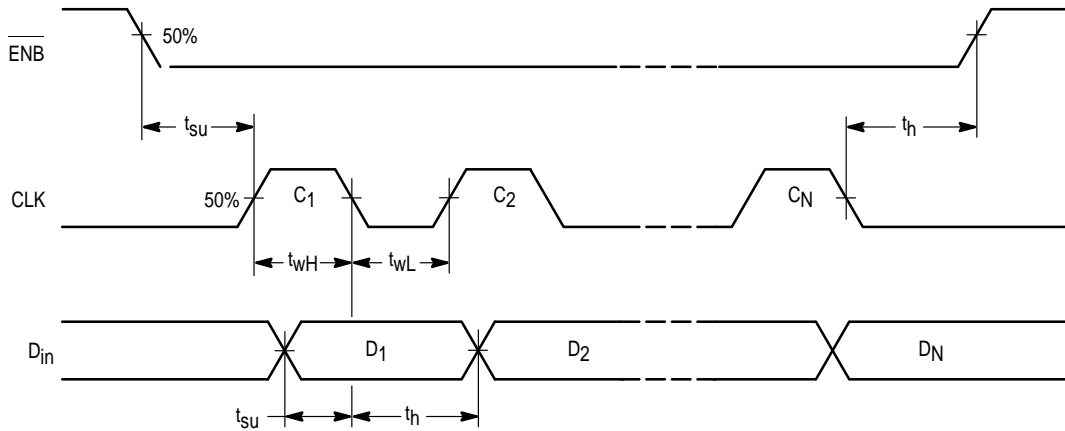


**LINEARITY ERROR** (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of linearity of the actual transfer function from the best-fit straight line. It is normally specified in parts of an LSB.

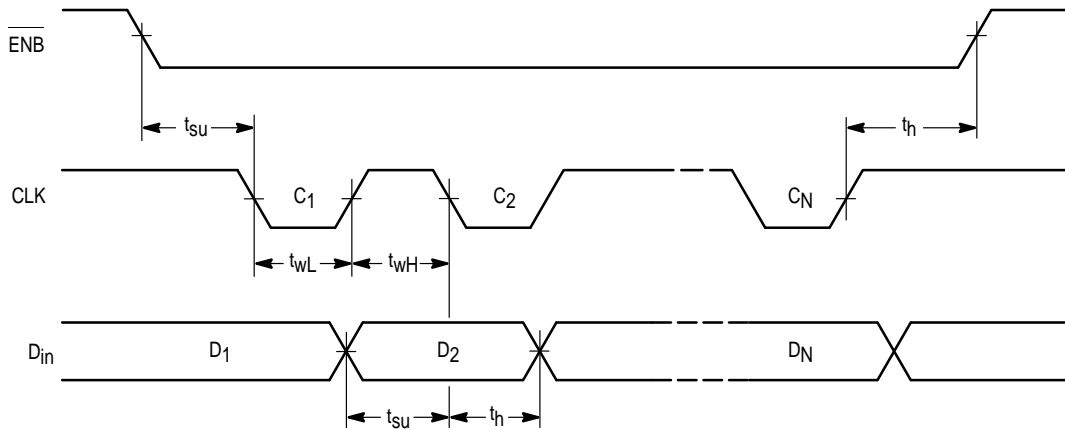
**Figure 1. D/A Transfer Function**



**Figure 2. Definition of Step Size**



**Figure 3. Serial Input, Positive Clock**



**Figure 4. Serial Input, Negative Clock**

## PIN DESCRIPTIONS

### INPUTS

#### D<sub>in</sub> Data Input

Six-bit words are entered serially, MSB first, into digital data input, D<sub>in</sub>. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

The last 6-bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next-to-last 6-bit word affects pins Q2 Out and R2 Out, etc.

#### ENB Negative Logic Enable

The ENB pin must be low (active) during the serial load. On the low-to-high transition of ENB, data contained in the shift register is loaded into the latch.

#### CLK Shift Register Clock

Data is shifted into the register on the high-to-low transition of CLK. CLK is fed into the D-input of a transparent latch, which is used for inhibiting the clocking of the shift register when ENB is high.

The number of clock cycles required for the MC144110 is usually 36. The MC144111 usually uses 24 cycles. See Table 1 for additional information.

## OUTPUTS

#### D<sub>out</sub> Data Output

The digital data output is primarily used for cascading the DACs and may be fed into D<sub>in</sub> of the next stage.

#### R1 Out through R<sub>n</sub> Out Resistor Network Outputs

These are the R-2R resistor network outputs. These outputs may be fed to high-impedance input FET op amps to bypass the on-chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

#### Q1 Out through Q<sub>n</sub> Out NPN Transistor Outputs

Buffered DAC outputs utilize an emitter-follower configuration for current-gain, thereby allowing interface to low-impedance circuits.

## SUPPLY PINS

#### V<sub>SS</sub> Negative Supply Voltage

This pin is usually ground.

#### V<sub>DD</sub> Positive Supply Voltage

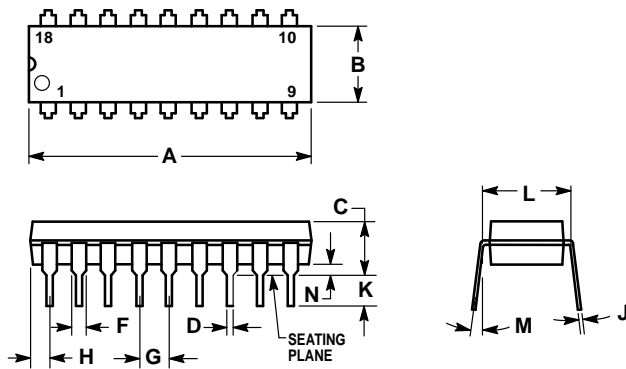
The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 V p-p.

Table 1. Number of Channels vs Clocks Required

Number of Channels Required	Number of Clock Cycles	Outputs Used on MC144110	Outputs Used on MC144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable

## PACKAGE DIMENSIONS

### P SUFFIX PLASTIC DIP CASE 707-02

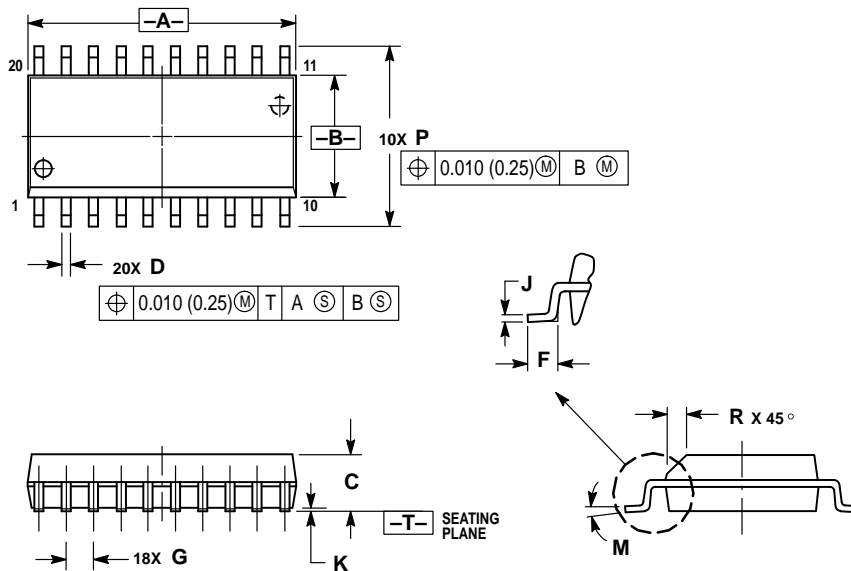


#### NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

### DW SUFFIX SOG PACKAGE CASE 751D-04

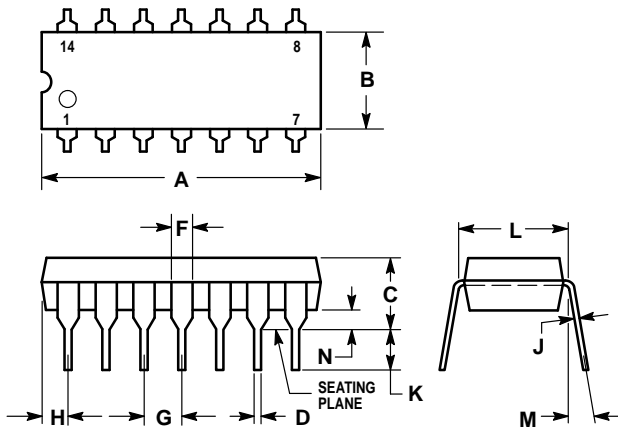


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

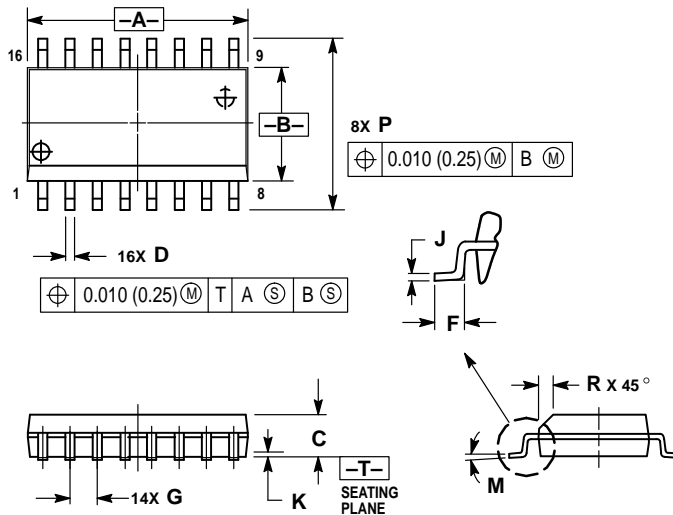
**P SUFFIX  
PLASTIC DIP  
CASE 646-06**



- NOTES:
- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  - ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

**DW SUFFIX  
SOG PACKAGE  
CASE 751G-02**



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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MC144110/D

