M51279SP/FP

NTSC/PAL DECODER

DESCRIPTION

The M51279SP/FP is a semiconductor integrated circuit designed for color signal processing, suitable for both NTSC and PAL systems. The outputs are R-Y and B-Y color difference signals, and the circuit has R-Y and B-Y output demodulation carriers. These carriers are also useful for modulating the color difference signals of another semiconductor integrated circuit, the M51272P/FP.

The M51279SP/FP consists of sync separator, ACC, tint control, APC and chroma demodulators.

Note that there is a burst signal at the ACC output in the M51279SP/FP, but not in the M51271SP/FP.

With respect to all other functions however, they are identical.

FEATURES

- Low power dissipation(Vcc=5.0V, Icc=50mA typ.)
- The demodulating angles for R-Y and B-Y are formed from a 4 fsc oscillator, so accurate that 90 deg demodulation is possible.
- Mute R-Y and B-Y output capability using external blanking pulse.
- Built-in ID pulse(for PAL)output.
- Individual burst gate pulse position and width set up capability using external constants.

APPLICATION

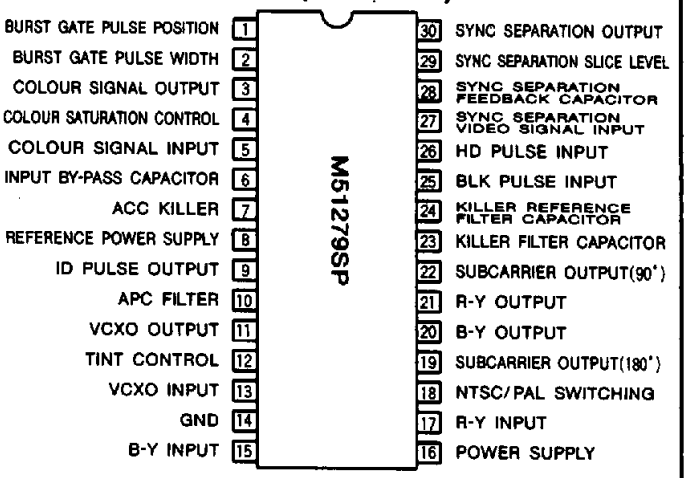
Color TV sets and VCRs.

RECOMMENDED OPERATING CONDITION

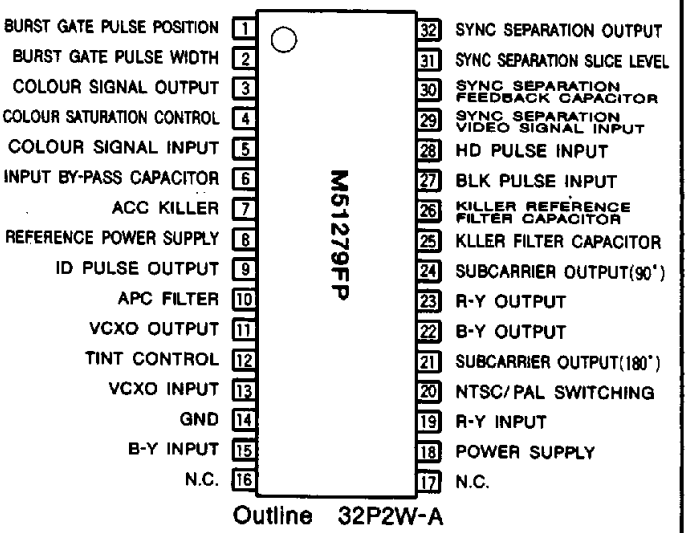
Supply voltage range.....4.0~6.0V

Rated supply voltage.....5.0V

PIN CONFIGURATION (TOP VIEW)



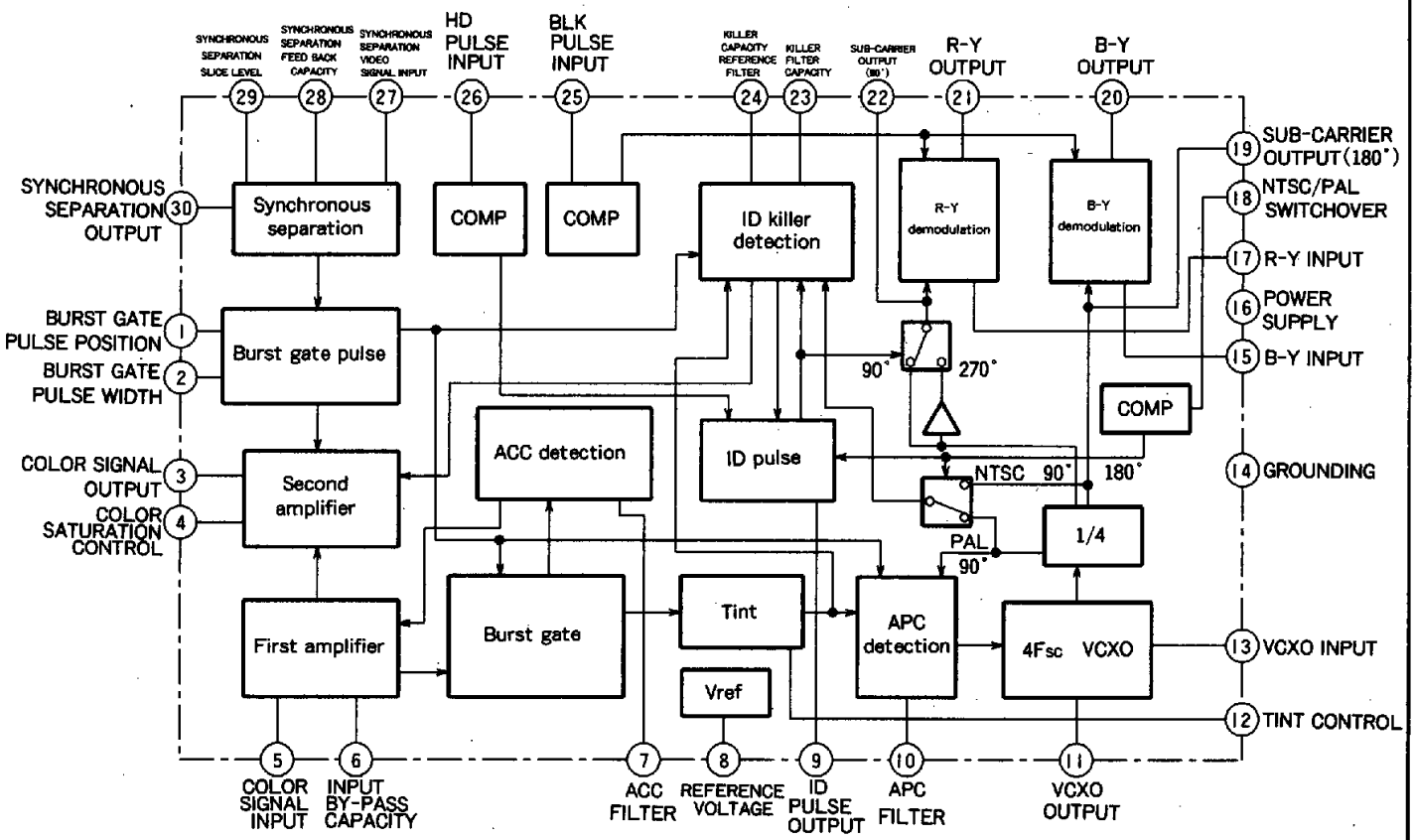
Outline 30P4B



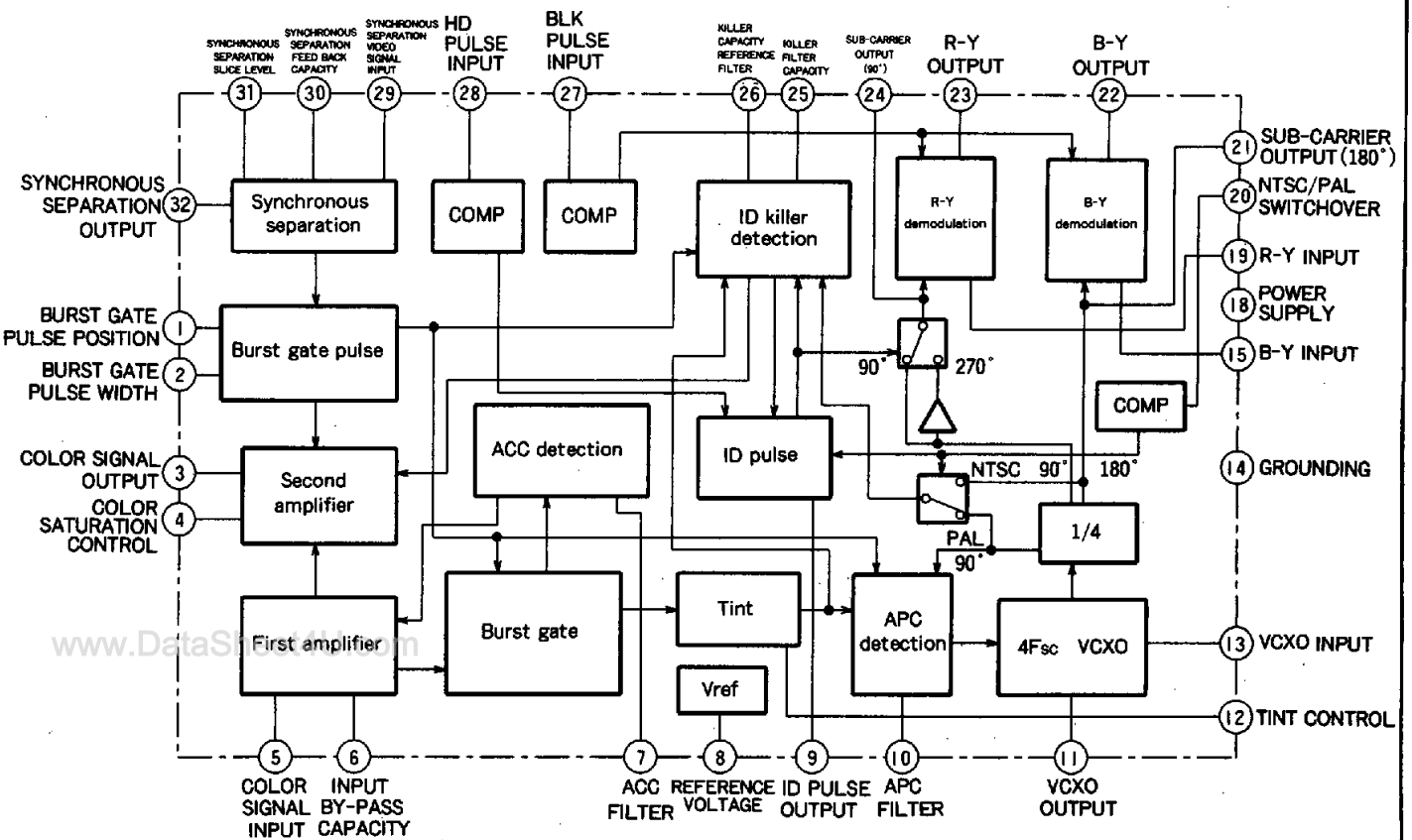
Outline 32P2W-A

NC : No connection

BLOCK DIAGRAM (M51279SP)



BLOCK DIAGRAM (M51279FP)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	6	V
Pd	Power consumption	1.25(0.5)	W
Topr	Operating temperature	−20~75	℃
Tstg	Storing ambient temperature	−40~125	℃
Kθ	Heat reduction rate	12.5(5)	mW/℃

Note;Numerical values in ( )are FP version.

ELECTRICAL CHARACTERISTICS (Ta=25℃, Vcc=5.0V, unless otherwise noted)

DC CHARACTERISTICS

(PIN No. are M51279SP)

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min.	Typ.	Max.	
Icc	Circuit current	DC bias alone	A	40	50	60	mA
V1	Voltage at terminal 1	DC bias alone		2.6	2.9	3.2	V
V3	Voltage at terminal 3	DC bias alone		1.9	2.2	2.5	V
V4	Voltage at terminal 4	DC bias alone		2.3	2.5	2.7	V
V6	Voltage at terminal 6	DC bias alone		2.8	3.0	3.2	V
V7	Voltage at terminal 7	DC bias alone		4.4	4.7	5.0	V
V8	Voltage at terminal 8	DC bias alone		2.8	3.0	3.2	V
V10	Voltage at terminal 10	DC bias alone		2.6	2.9	3.2	V
V11	Voltage at terminal 11	DC bias alone		2.4	2.7	3.0	V
V12	Voltage at terminal 12	DC bias alone		2.3	2.5	2.7	V
V13	Voltage at terminal 13	DC bias alone		3.1	3.4	3.7	V
V15	Voltage at terminal 15	DC bias alone		2.6	2.9	3.2	V
V17	Voltage at terminal 17	DC bias alone		2.6	2.9	3.2	V
V18	Voltage at terminal 18	DC bias alone		0.6	0.8	1.0	V
V20	Voltage at terminal 20	DC bias alone		1.9	2.1	2.3	V
V21	Voltage at terminal 21	DC bias alone		1.9	2.1	2.3	V
V24	Voltage at terminal 24	DC bias alone		2.5	2.8	3.1	V
V27	Voltage at terminal 27	DC bias alone		2.6	2.9	3.2	V
V28	Voltage at terminal 28	DC bias alone		2.2	2.5	2.8	V
V29	Voltage at terminal 29	DC bias alone		2.2	2.5	2.8	V

INPUT TERMINAL CHARACTERISTICS

Pin No,	Input form	Internal bias voltage (standard)	Test condftions	Input resistance or current standard value			Unit
				Min.	Typ.	Max.	
②	Open base(PNP)	Not specified	V_2=2.5V	−2.0	−1.0	—	μA
④	Resistor	2.5V	—	20.0	25.0	30.0	kΩ
⑤	Open base(NPN)	Not specified	V_5=3.0V	—	1.0	2.0	μA
⑥	Resistor	3.0V	—	9.0	12.0	15.0	kΩ
⑫	Resistor	2.5V	—	20.0	25.0	30.0	kΩ
⑬	Resistor	3.4V	—	4.0	5.0	6.0	kΩ
⑮	Resistor	2.9V	—	4.0	5.0	6.0	kΩ
⑰	Resistor	2.9V	—	4.0	5.0	6.0	kΩ
㉕	Open base(NPN)	Not specified	V_{25}=5.0V	—	0.5	1.0	μA
㉖	Open base(NPN)	Not specified	V_{26}=5.0V	—	0.5	1.0	μA
㉗	Resistor	2.9V	—	16.0	20.0	24.0	kΩ

OUTPUT TERMINAL CHARACTERISTICS

Pin No.	Output form	Test conditions	Bias current			Unit
			Min.	Typ.	Max.	
③	Emitter follower (NPN)	Ammeter between ③ pin and Vcc	0.6	0.8	1.0	mA
⑪	Emitter follower (NPN)	Ammeter between ⑪ pin and Vcc	1.5	1.8	2.1	mA
⑲	Emitter follower (NPN)	Ammeter between ⑲ pin and Vcc	230	280	330	μA
⑳	Emitter follower (NPN)	Ammeter between ⑳ pin and Vcc	0.8	1.0	1.2	mA
㉑	Emitter follower (NPN)	Ammeter between ㉑ pin and Vcc	0.8	1.0	1.2	mA
㉒	Emitter follower (NPN)	Ammeter between ㉒ pin and Vcc	230	280	330	μA

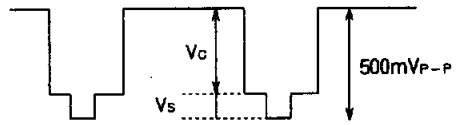
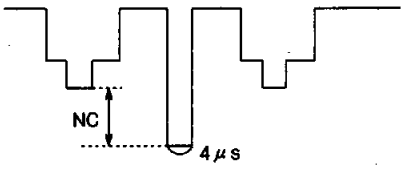
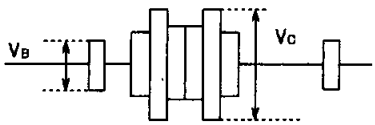
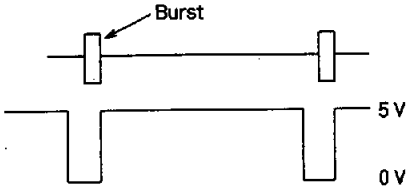
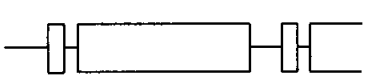
AC CHARACTERISTICS

Symbol	Parameter		Test conditions	Test ciruit	Limits			Unit
					Min.	Typ.	Max.	
V_{CCR}	Operating supply voltage range		The standard application circuit should have no abnormal operation		4.0	5.0	6.0	V
Acc I	ACC circuit	ACC characteristics I	SG1 : 200mV Reference value determined by measuring output value when inputting 100mV signal from SG1.	B	0	1.0	3.0	dB
Acc II		ACC characteristics II	SG1 : 10mV Reference value determined by measuring output value when inputting 100mV signal from SG1.		−2.0	0	2.0	dB
G_{CA}		Open-loop gain	SG1 5mV$_{P-P}$ SW 7 ON		21.0	24.0	27.0	dB
Vcmax	Color control Synchronous separation	Chroma maximum output amplitude	④pin 5V		160	200	240	mV$_{P-P}$
Vctyp		Chroma typical output amplitude	④pin open		80	100	120	mV$_{P-P}$
Vcmin		Chroma maximum attenuation	④pin GND		—	—	−35	dB
Sd_1		Synchronous output delay 1	SG2 APL100% 500mV$_{P-P}$		—	—	500	ns
Sd_2		Synchronous output delay 2	SG2 APL100% 500mV$_{P-P}$		—	—	500	ns
S_{V1}		Synchronous output amplitude 1	SG2 APL100% 500mV$_{P-P}$		4.0	4.2	4.4	V
Smin		Syncrhonous separation minimum input level	SG2 : APL100% Signal attenuation		—	—	350	mV$_{P-P}$
NC		Syncrhonous separation noise cancel	SG3 input		—	—	1.2	V
BGPp I	Burst gate pulse generator	Burst gate pulse position I	①pin 10kΩ, pull up=560kΩ ②pin 3.0V		2.0	2.5	3.0	μS
BGPp II		Burst gate pulse position II	①pin 39kΩ, pull up=2.2MΩ ②pin 3.0V		8.0	8.5	9.0	μS
BGPw II		Burst gate pulse width I	①pin 24kΩ, pull up=1.2MΩ ②pin 2.0V		3.5	4.0	4.5	μS
BGPp II		Burst gate pulse width II	①pin 24kΩ, pull up=1.2MΩ ②pin 4.0V		0.8	1.3	1.8	μS
Gdr-y	R-Y demodulator	Demodulation gain	SG5 100mV$_{P-P}$ f(beat)=10kHz	C	10	12	14	dB
ΔEr-y		Residual carrier wave	No input at 17pin		—	—	30.0	mV$_{P-P}$
Vmr-y		Demodulation maximum output	SG5 600mV$_{P-P}$ f (beat)=10kHz		2.1	2.4	2.7	V$_{P-P}$
Bwr-y		Demodulation band width	Reference : f(beat) =10kHz Measuring point : f(beat) of −3dB		1.0	—	—	MHz
BLKΔvr		Blanking DC offset	⑮pin 0V, 5V : ⑰pin DC fluctuation		—	—	50.0	mV$_{P-P}$
Gdb-y	B-Y demodulator	Demodulation gain	SG5 100mV$_{P-P}$ f (beat)=10kHz		10	12	14	dB
ΔEb-y		Residual carrier wave	No input 15pin		—	—	30.0	mV$_{P-P}$
Vmb-y		Demodulation maximum output	SG5 600mV$_{P-P}$ f (beat)=10kHz		2.1	2.4	2.7	V$_{P-P}$
BWb-y		Demodulation band width	Reference : f(beat) =10kHz f (beat) of−3dB		1.0	—	—	MHz
BLKΔvb		Blanking DC offset	⑮pin 0V, 5V;⑰pin DC fluctuation		—	—	50.0	mV
R-Y	Demodulator	R-Y, B-Y demodulation gain ratio	—		0.8	1.0	1.2	—
B-Y								
ΔV		R-Y, B-Y DC voltage offset	DC difference between output values at pin⑳ and pin㉑		—	—	50.0	mV

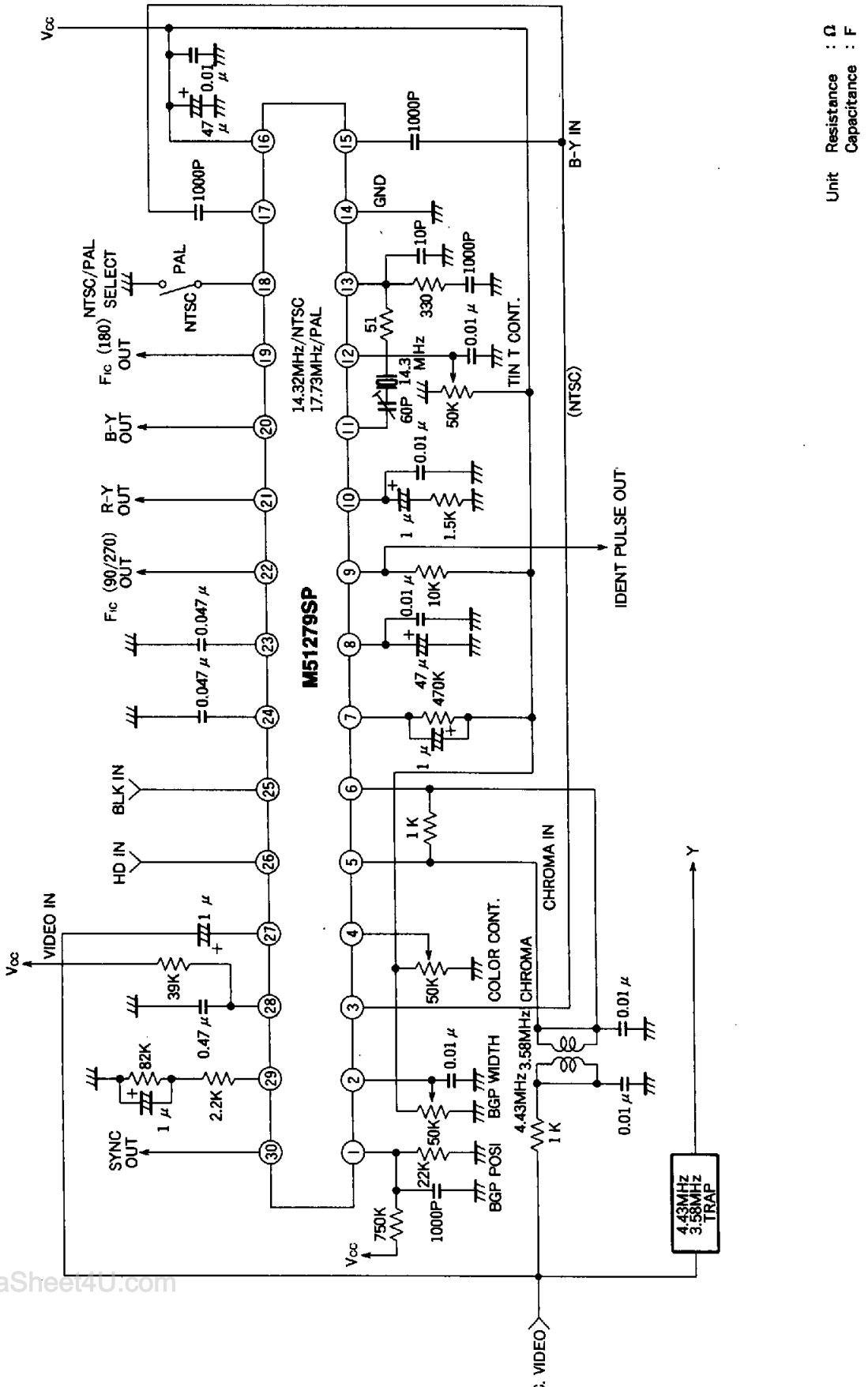
AC CHARACTERISTICS (cont.)

Symbol	Parameter			Test conditions	Test circuit	Limits			Unit
						Min.	Typ.	Max.	
T_{CP}	TINT	PAL	Center	Measure the value of V12 when output of ㉑ pin crosses 0.	C	2.30	2.35	2.40	V
T_{WP}	TINT	PAL	Variable width	Measure the amount of phase shift when voltage at ⑫ pin changes between 0V and 5V.		80	85	—	deg
T_{CN}	TINT	NTSC	Center	—		2.40	2.45	2.50	V
T_{WN}	TINT	NTSC	Variable width	—		80	85	—	deg
Kthp			Killer operation input level	Burst voltage 100mV$_{P-P}$ is 0dB.		−33	−30	−27	dB
Kth$_N$			Killer operation input level	Burst voltage 100mV$_{P-P}$ is 0dB.		−36	−33	−30	dB
ID	ID operation			Observe R-Y output (21pin).		There shall be no abnormality in operation.			
IDP	ID pulse output		ID pulse	—		There shall be no abnormality in operation.			
IDv	ID pulse output		ID vsat	SW18 : OFF open collector Vsat DC 5mA		—	250	500	mV
BLKth	Blanking pulse input threshold			㉕pin DC variable		3.3	3.5	3.7	V
HDth	HD pulse input threshold			㉖pin DC variable		3.8	4.0	4.2	V
SCob	B-Y Sub-carrier output		Output level	⑲pin output		500	550	600	mV$_{P-P}$
SCdb	B-Y Sub-carrier output		Duty	⑲pin output		45	50	55	%
SCor	R-Y Sub-carrier output		Output level	⑳pin output		500	550	600	mV$_{P-P}$
SCdr	R-Y Sub-carrier output		Duty	⑳pin output		45	50	55	%
Or-y,b-y	Sub-carrier orthogonality			Phase difference between output carrier of ⑲pin and of ⑳pin		85	90	95	deg
F_{CPP}	PAL frequency-loocking range			⑤pin input frequency variable		1.0	—	—	kHz
F_{CPN}	NTSC frequency-loocking range			⑤pin input frequency variable		1.0	—	—	kHz

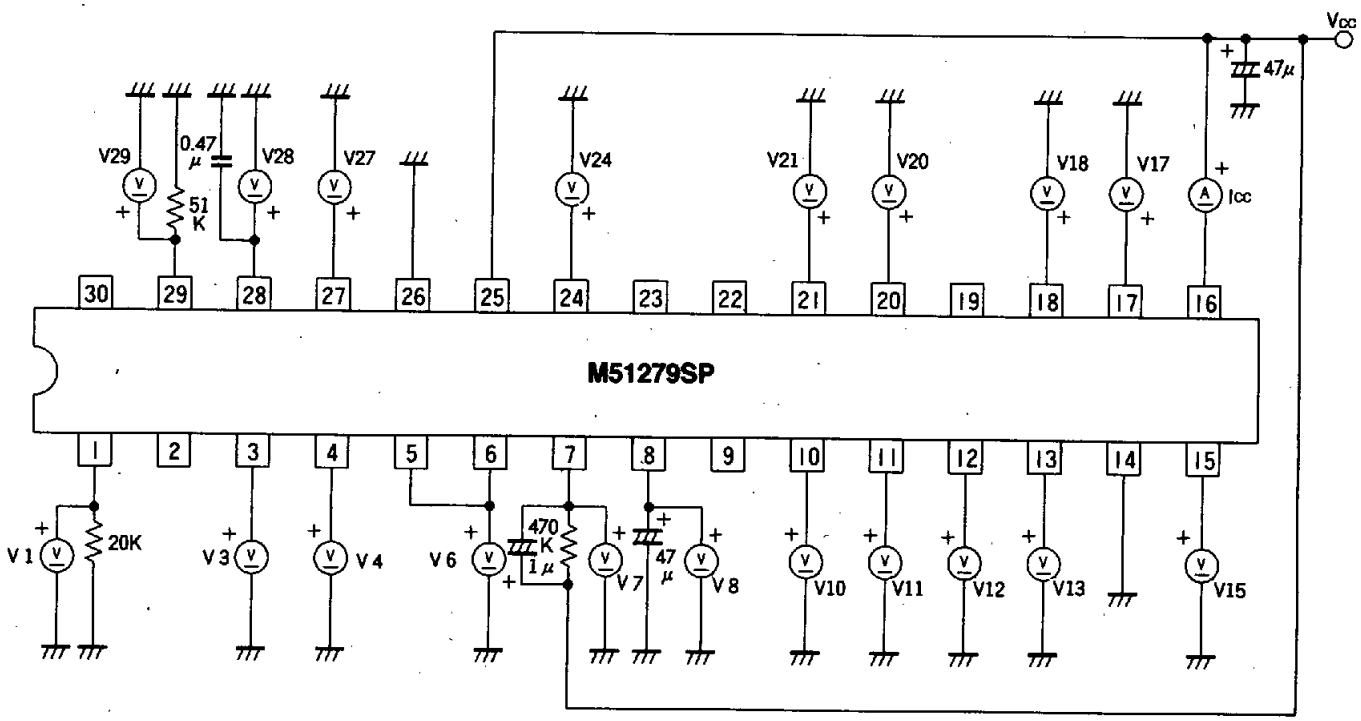
INPUT SIGNAL

SG No.	Waveform	Standard	Remarks
SG1		Sine wave CW, 100mVP-P (standard)	Frequency and output level should be variable.
SG2		APL100 signal 500mVP-P (standard), Vc : Vs=10 : 4	Level should be variable.
SG3		Mix noise to SG2 standard signal (500mVP-P).	NC should be variable (noise level alone).
SG4	 NTSC, PAL chroma standard signal	Vc : VB=2 : 1, VB=100mVP-P (standard)	Level shall be variable.
SG5		Sine wave CW	Frequency and output level should be variable.
HD pulse		Pulse should have last transition preceding the burst in horizontal blanking interval.	Vertical blanking interval should also appear with the same timing
SG6		Burst and chroma should show the same phase. Amplitude ratio of burst and chroma can take any value. Burst : 100mVP-P	Frequency : 3.579545MHz 4.433618MHz

APPLICATION EXAMPLE



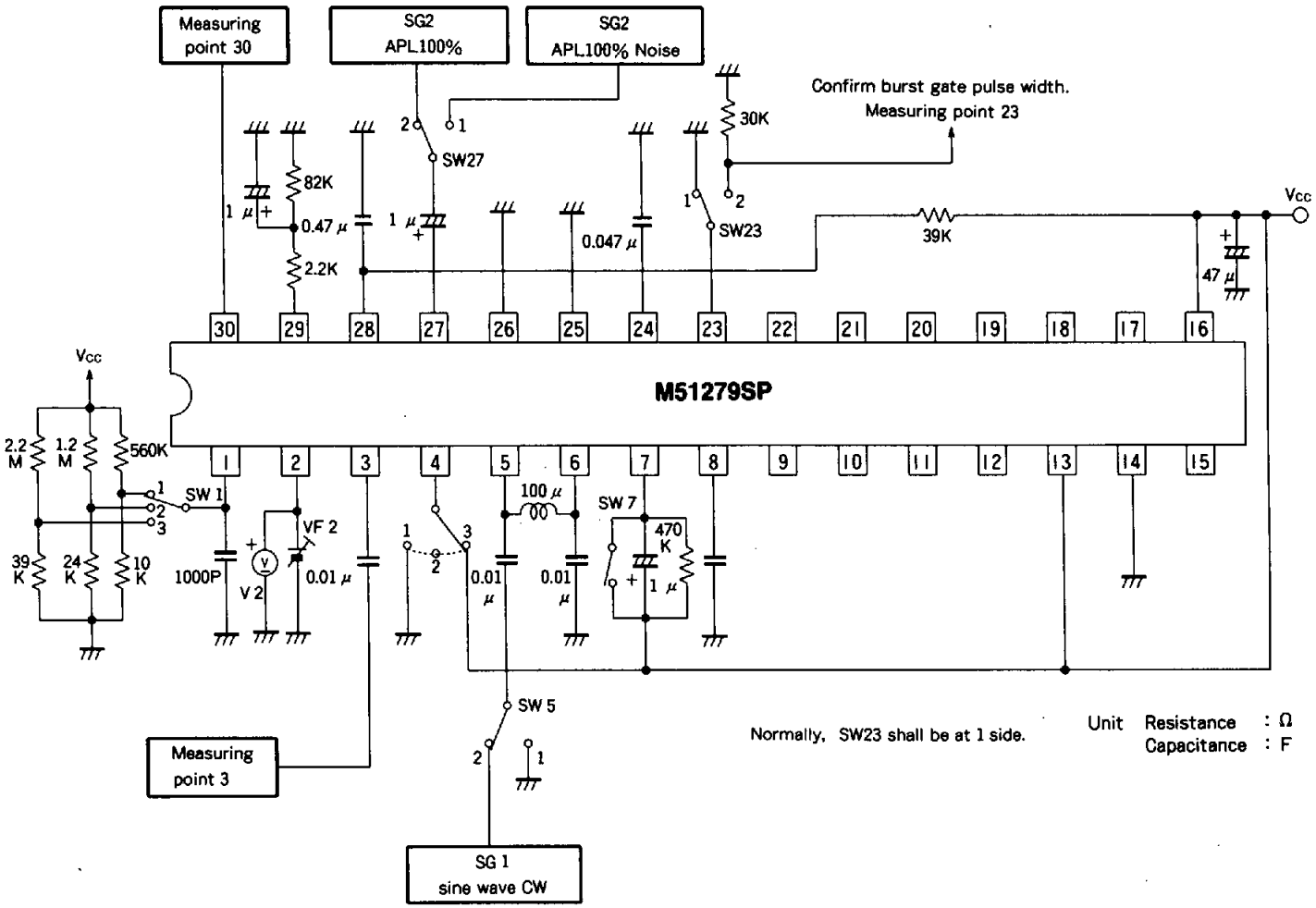
TEST CIRCUIT A



At each measuring point, the measured value is the value read from an ammeter or voltemeter.

Unit Resistance : Ω
Capacitance : F

TEST CIRCUIT B



ACCI and ACCII

Set SW1, 5 and 27 to 2; SW4 to 3, and turn off SW7.Input 3.57954MHz, 100mVp-p (odB) from SG1.Adjust VF2 (to approximately 3V) so that burst gate pulse width will be set in 2.8 μ s (burst, is approximately 10 cycles).(Check the burst gate pulse generator section to confirm burst gate pulse width).

In the following equations, V_A (mVp-p) represents the output value at the measuring point under the above conditions:V_B (mVp-p) and V_C (mVp-p) represent output values at measuring point 3: the former, when the output from SG1 is 6dB; and the latter, when the same output is -20dB.

$ACCI = 20 \log V_B/V_A$ (dB) $ACCII = 20 \log V_C/V_A$ (dB)

G_{CA}

Turn SW7 on.Set the other SWs to the same conditions specified in 1).

Set the output of SG1 to 3.579545MHz,5mVp-p.In the following equation, V_D (mVp-p) represents the output value at measuring point 3.

$G_{CA} = 20 \log V_D/5$ (dB) (Burst gate pulse 2.8 μ s)

Vcmax, Vctyp and Vcmin

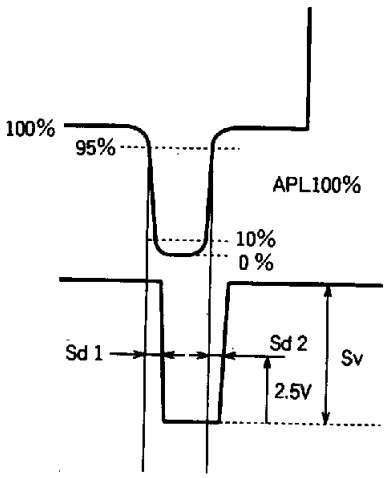
Set the SWs to the same conditions specified in 1).

Set the output of SG1 to 3.579545MHz, 100mVp-p.Vcmax, Vctyp and C (mVp-p) represent the output amplitude values at measuring point 3 when SW4 is set to 3, 2 and 1 respectively.Vcmin is obtained by the following equation.

Vcmin = 20 log C/Vcmax (dB) (Burst gate pulse 2.8 μ s)

Sd1, Sd2 and Sv

Set SW27 to 2.The other SWs can be set to any position. Input an APL 100% standard signal from SG2(500mVp-p).Determine Sd1, Sd2 and Sv, shown in the right-hand figure, by observing the input signal and synchronizing pulse output at measuring point 30.



Smin

Under the same conditions specified in 4), reduce the output of SG2.Smin (mVp-p) represents the output value of SG2 just before the output values at measuring point 30 begin to deviate from the standard values for Sd1, Sd2 and Sv

NC

Set SW27 to 1. Set other SWs to the same conditions specified in 4). Vary the noise pulse level of SG3. NC(V) represents the potential difference between the input synchronizing tip and the noise pulse tip when the noise pulse at measuring point 30 begins to fall away.

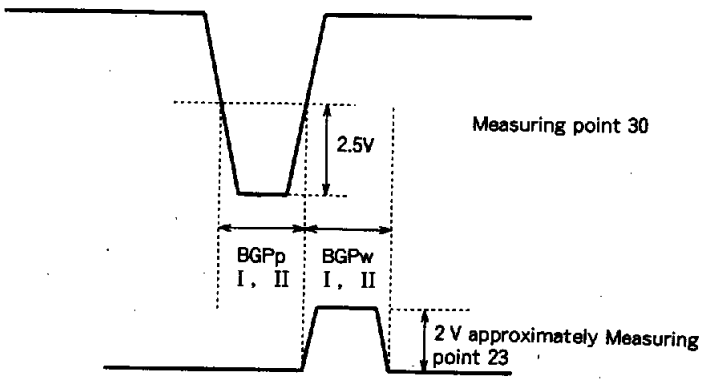
BGPp I and BGPp II

Set SW7 to 2. Input an APL 100% standard signal from SG2. Set SW23 to 2 and observe measuring point 23 and 30. Set SW1 to 1 then to 3 and measure BGPp I and BGPp II.(V2=3V)

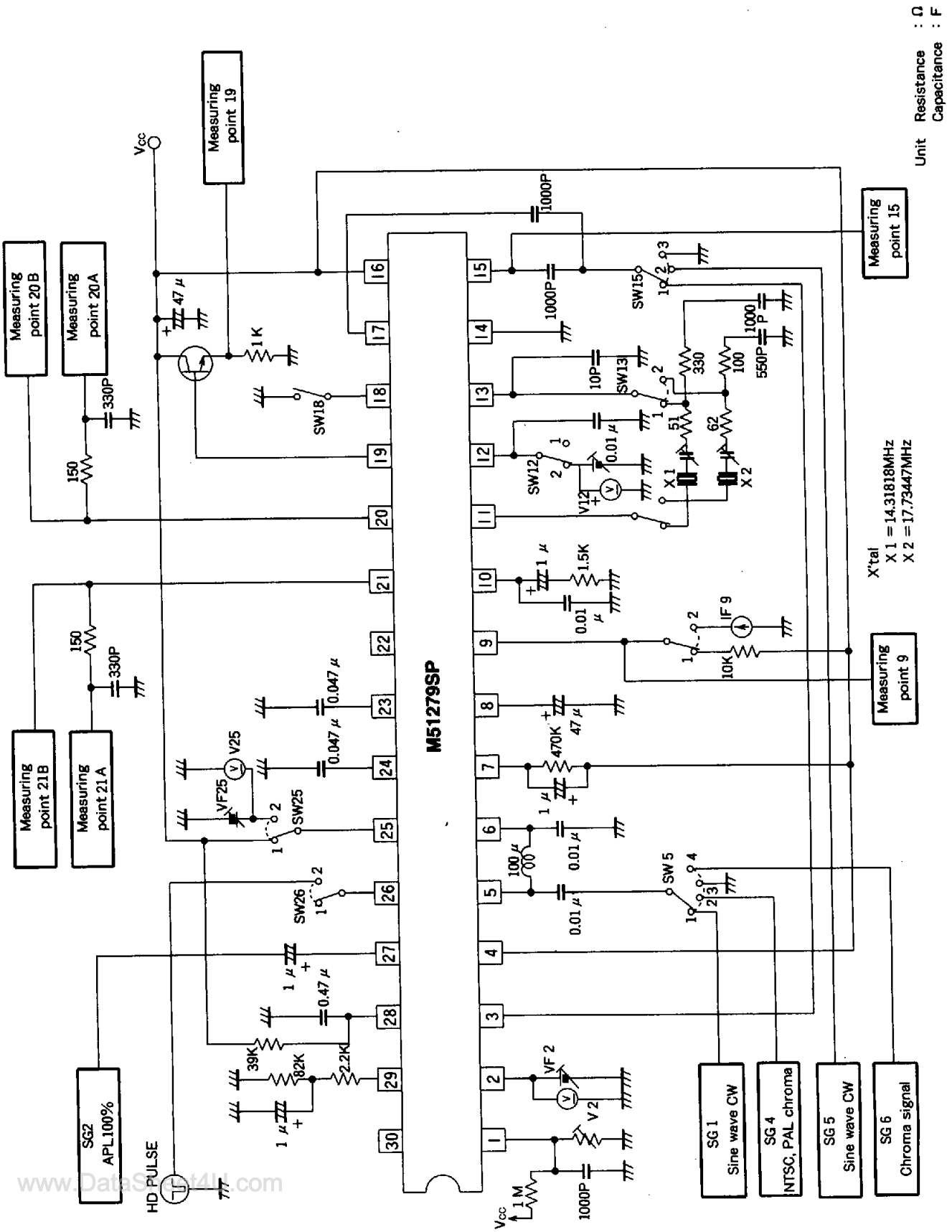
BGPw I and BGPw II

Set SW1 to 2;and the other SWs to the same conditions specified in 7).

Set V2 to 2.0V then to 4.0V and measure BGPwI and BGPw II at measuring point 23.



TEST CIRCUIT C



ADJUSTMENT OF BURST PULSE POSITION AND WIDTH

On inputting NTSC/PAL standard chroma signals, adjust the resistance value at terminal 1 and the voltage value at terminal 2 in order to locate the burst gate pulse at the burst position and observe measuring point 3.

In other cases, set the resistance value at terminal 1 to 24k Ω. Vary the burst gate width in 2.8 μs when setting conditions for NTSC, in 2.3 μs when setting conditions for PAL by adjusting the voltage at terminal 2.

(Observation has already occurred in 10-2) with SW23 set to 2).

VCXO TO ADJUSTMENT

Set SW5 to 3, SW25 and 26 to 1, and turn SW18 on (for PAL). Apply an APL100% standard signal from SG2. Adjust the VCXO external trimmer to set output frequency at measuring point 19 to :

3.579545MHz (NTSC, set SW13 to 1)

4.433618MHz (PAL, set SW13 to 2).

Gdb-y and Gdr-y

Set SW5, 12, 13, 25 and 26 to 1; SW15 to 2, and turn off SW18. Input 3.579545MHz, 100mVp-p from SG1, an APL100% standard signal from SG2, and 3.589545MHz, 100mVp-p from SG3. In the following equation, DB (mVp-p) and DR (mVp-p) represent output (f(beat)=10kHz) at measuring points 20A and 21A respectively.

$$Gdb - y = 20 \log DB / 100 \ (dB)$$
$$Gdr - y = 20 \log DR / 100 \ (dB)$$

Δ Eb-y and Δ Er-y

Set SW15 to 3, and other SWs and SG1 and 2 to the same conditions specified in 1). Δ Eb-y (mVp-p) and Δ Er-y (mVp-p) represent carrier leakage output values (3.58MHz component) at measuring points 20B and 21B respectively.

Vmb-y and Vmr-y

Set each SW, and SG1 and 2 to the same conditions specified in 1). Set the output of SG3 to 600mVp-p and measure output values (f(beat)=10kHz) at measuring points 20A and 21A. The values are represented by Vmb-y and Vmr-y (Vp-p) respectively.

BWb-y and BWr-y

Set each SW, and SG1 and 2 to the same conditions specified in 1). Vary the output frequency of SG3 from 3.58 to 5MHz with its voltage set to 100mVp-p. BWb-y and BWr-y (MHz) represent output frequency at measuring points 20A and 21A respectively when the output voltage at both measuring points is −3dB (reference is DB or DR).

BLK Δ vb and BLK Δ vr

Set SW15 to 3, SW25 to 2, and other SWs and SG1 to the same conditions specified in 1). BLK Δ vb represents DC voltage fluctuation at measuring point 20B when VF25 is set to 5.0V and then 0V. Measure BLK Δ vr similarly at measuring point 2NB.

R-Y,B-Y demodulation gain ratio

From DB and DR obtained by measurement of Gdb-y and Gdr-y, we obtain the following equation.

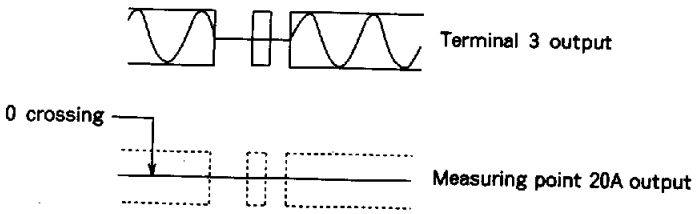
$$(R-Y) / (B-Y) = DR / DB$$

Δ V

Δ V represents the potential difference between measuring points 20A and 21A obtained by measurement of BLK△vb and BLK Δ vr when VF25 is set to 5.0V.

TCP and TCN

Set SW15, 25 and 26 to 1, SW12 and 13 to 2, SW5 to 4, and turn off SW18. Input 4.433618MHz from SG6. Vary the voltage of VF12. TCP represents the voltage of V12(V) when the output at measuring point 12A passes 0. Set SW13 to 1 and input 3.579545MHz from SG6. Measure TCN similarly.



TWP and TWN

Set SW5, 15, 25 and 26 to 1; SW12 and 13 to 2, and turn off SW18. Input 4.433618MHz, 100mVp-p from SG1. TWP (deg) represents the amount of phase shift of the output at measuring point 19 compared with that at measuring point 15 when VF12 is set at 5.0 and then 0V.

Set SW13 to 1 and input 3.579545MHz, 100mVp-p from SG1. Measure Twn (deg) similarly.

KthP and KthN

Set SW5, 13 and 26 to 2; SW12, 15 and 25 to 1, and turn SW18 on. Input the PAL chroma standard signal from SG4. Start reducing the output from SG4. In the following equation, Vkp (mVp-p) represents the burst width of the SG4 output when the color difference signal output at measuring point 20A begins to muted.

$$KthP = 20 \log VkD / 100 \ (dB)$$

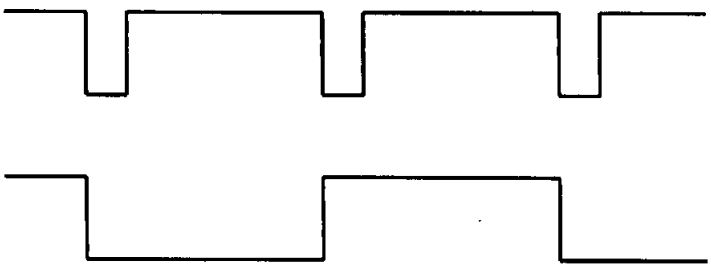
Set SW13 and 26 to 1 and turn off SW18. Input the NTSC chroma standard signal from SG4. VkN is determined similarly, and we obtain the following equation.

$$KthN = 20 \log VkN / 100 \ (dB)$$

ID operation
Under the same measuring conditions as specified for the measurement of Kthp, input the PAL chroma standard signal from SG4. Confirm that the color difference signal is not reversed every 1H at measuring point 21A for R-Y output.

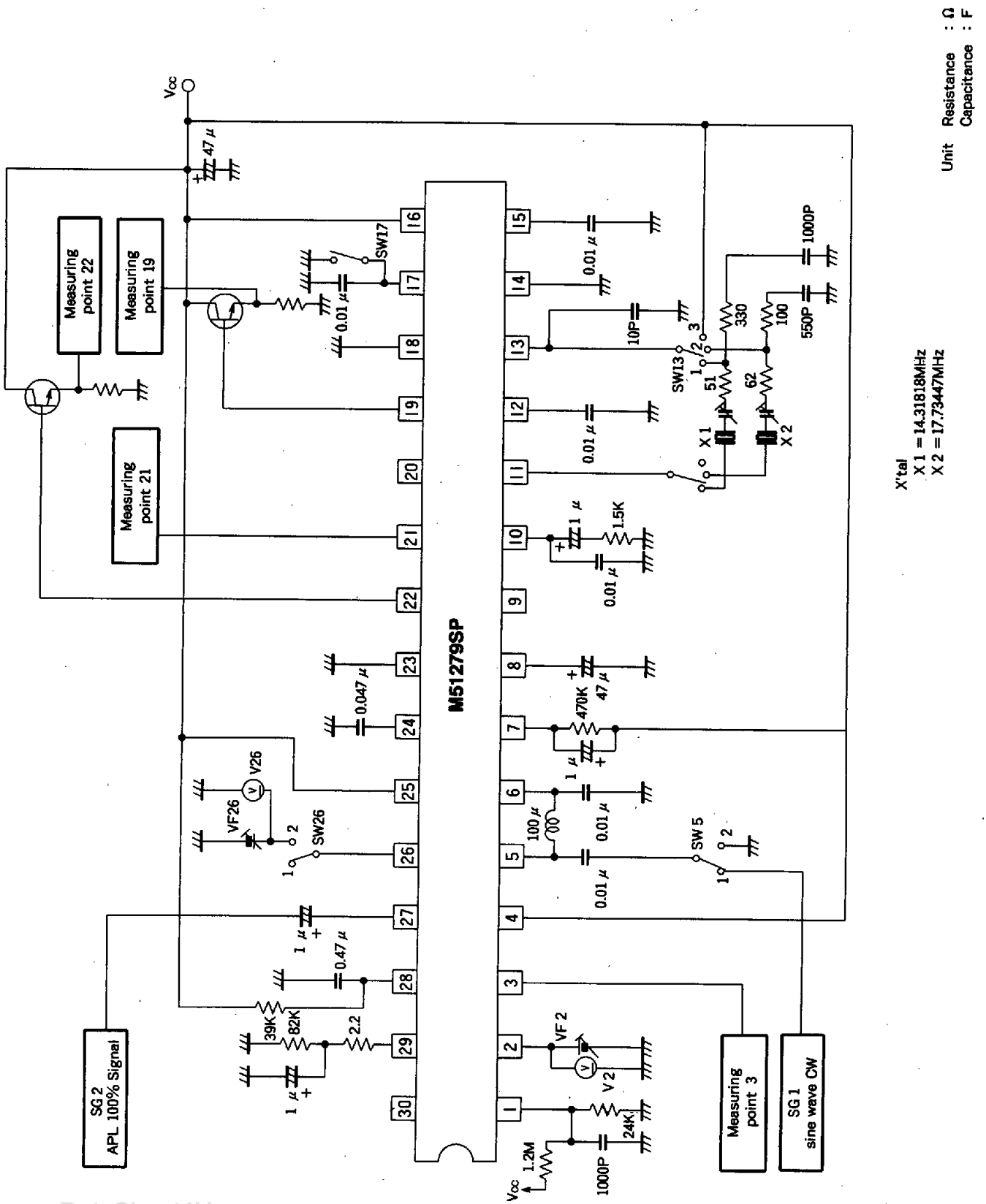
BLKth
Set SW25 to 2 and other SWs and SGs to the same conditions specified for the measurement of Kthp. Slowly reduce the VF25 voltage from 5.0V. BLKth represents the voltage of V25 (V) when color difference output at measuring points 20A and 21A begins to be muted.

ID pulse
Under the same measuring conditions specified for the measurement of Kthp, input the PAL chroma standard signal from SG4. Set SW9 to 1. Observe the pulse output at measuring point 9. Confirm that the leading edge of the HD pulse is reversed and has 1/2 dividing.



IDvsat
Under the same measuring conditions specified for the measurement of KthN, set SW9 to 2. IDvset (mV) represents the DC voltage at measuring point 9 when 5mA is applied from IF9.

TEST CIRCUIT D

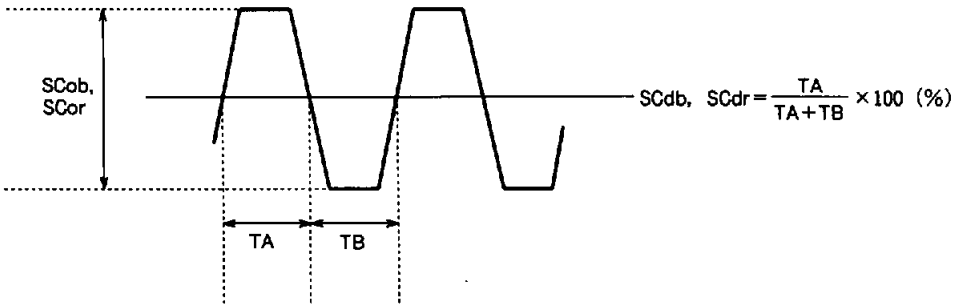


HDth
Set SW5 and 26 to 2, SW13 to 3, and turn SW17 on. Start reducing the voltage at VF25 slowly from 5.0V. HDth (V) represents VF26 voltage when DC voltage at measuring point 21 changes either from High (4V approximately) to Low (0V approximately) or similarly but in the opposite direction.

SCob and SCor
Set SW5 and 26 to 1, SW13 to 2, and turn off SW17. Input 4.433618MHz, 100mVp-p from SG1. SCob (mVp-p) represents the output voltage at measuring point 19.
SCor (mVp-p) represents the output voltage at measuring point 22 under the same conditions.

SCdb and SCdr
Under the same measuring conditions specified in 2), measure SCdb and SCdr at measuring points 19 and 22, respectively, as follows.

$$\text{SCdb, SCdr} = \frac{TA}{TA+TB} \times 100\ (\%)$$



Or-y · b-y
Under the same conditions specified in 2), measure the phase difference between the output at measuring point 19 and that at 22, which is represented by Or-y · b-y.

FcPP and FcPN
Under the same measuring conditions specified in 2), estimate the frequency of the output from SG1 by starting at 4.435MHz (asynchronous) and moving toward the center frequency (4.433618MHz), with output voltage of 100mVp-p. Determine the lock-in frequency f_1. Also,estimate the frequency by starting at 4.432MHz (asynchronous state) and moving toward the center frequency to determine the lock-in frequency f_2. We then obtain the following equation.

$$FcPP = f_1 - f_2\ (Hz)$$

Set SW13 to 1. Estimate the frequency of SG1 by starting at 3.581MHz (asynchronous state) and moving toward the center frequency (3.579545MHz).Determine the lock-in frequency f_3. Also, estimate the frequency by starting at 3.578MHz (asynchronous state) and moving toward the center frequency to determine the lock-in frequency f_4. We then obtain the following equation.

$$FcPN = f_3 - f_4\ (Hz)$$

*Please refer to Application note in M51271SP/FP