INTEGRATED CIRCUITS

DATA SHEET

NE527Voltage comparator

Product data Supersedes data of 1994 Aug 31 File under Integrated Circuits, IC11 Handbook 2001 Aug 03





Voltage comparator

NE527

DESCRIPTION

The NE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE527 is similar in design to the Philips Semiconductors NE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

- 15 ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain of 5000

PIN CONFIGURATIONS

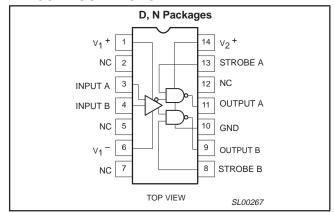


Figure 1. Pin Configuration

APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG#
14-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	NE527N	SOT27-1
14-Pin Small Outline (SO) Package	0 °C to +70 °C	NE527D	SOT108-1

EQUIVALENT SCHEMATIC

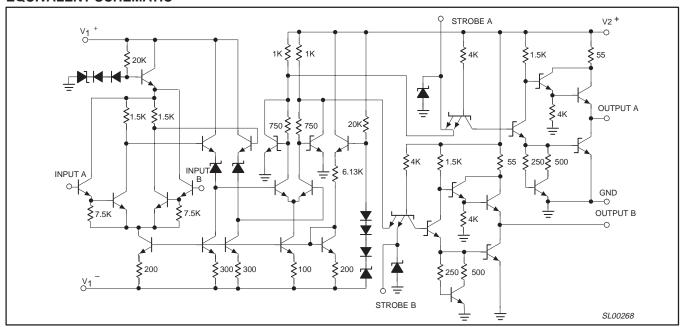


Figure 2. Equivalent Schematic

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V ₁ +	Positive supply voltage	+15	V
V ₁ -	Negative supply voltage	-15	V
V ₂ +	Gate supply voltage	+7	V
V _{OUT}	Output voltage	+7	V
V _{IN}	Differential input voltage	±5	V
V _{CM}	Input common mode voltage	±6	V
P _D	Max power dissipation ¹ 25 °C ambient (still air) N package D package	1420 1040	mW mW
T _{amb}	Operating temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C
T _{sld}	Lead soldering temperature (10sec max)	+230	°C

NOTES:

1. Derate above 25 °C, at the following rates:

N package 11.4 mW/°C

D package 8.3 mW/°C

BLOCK DIAGRAM

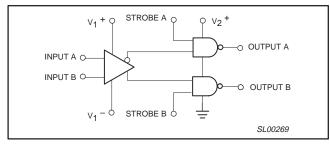


Figure 3. Block Diagram

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DC ELECTRICAL CHARACTERISTICS

 V_1 + = 10V; V_1 - = -10 V; V_2 + = +5.0 V; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		UNIT		
STMBOL	PARAMETER	TEST CONDITIONS	Min	Тур	Max	UNII
Input chara	acteristics					
\/	Input offset voltage @ 25 °C				6	mV
Vos	over temperature range				10	IIIV
	Input bias current @ 25 °C				2	
BIAS	over temperature range				4	μΑ
	Input offset current @ 25 °C				0.75	μΑ
los	over temperature range	V _{IN} = 0 V			1	μΑ
V_{CM}	Common-mode voltage range		-5		+5	V
Gate chara	acteristics					
V _{OUT}	Output Voltage "1" State "0" State	V_2 + = 4.75 V; I_{SOURCE} = -1 mA V_2 + = 4.75 V; I_{SINK} = 10 mA	2.7	3.3	0.5	V V
	Strobe inputs "0" Input current ¹ "1" Input current @ 25 °C ¹ Over temperature range "0" Input voltage "1" Input voltage	V_{2} + = 5.25 V; V_{STROBE} = 0.5 V V_{2} + = 5.25 V; V_{STROBE} = 2.7 V V_{2} + = 5.25 V; V_{STROBE} = 2.7 V V_{2} + = 4.75 V V_{2} + = 4.75 V	2.0		-2 100 200 0.8	mA μA μA V
I _{SC}	Short-circuit output current	V_2 + = 5.25 V; V_{OUT} = 0 V	-18		-70	mA
Power sup	ply requirements					
V ₁ + V ₁ - V ₂ +	Supply voltage		5 -6 4.75	5	10 -10 5.25	V V V
1	Supply current	$V_1 + = 10 \text{ V}; V_1 - = -10 \text{ V}$ $V_2 + = 5.25 \text{ V}$			_	A
l ₁ + l ₁ -		Over temp. Over temp.			5 10	mA mA
l ₂ +		Over temp.			20	mA

NOTE:

AC ELECTRICAL CHARACTERISTICS

 T_{amb} = 25 °C, unless otherwise specified. (See AC test circuit)

SYMBOL	PARAMETER	TEST CONDITIONS		UNIT		
STWIBUL	FARAMETER	TEST CONDITIONS	Min	Тур	Max	UNII
t _{PLH}	Transient response propagation delay time Low-to-High	V _{IN} = ±100 mV step		16	26 24	ns
t _{PHL}	High-to-Low Delay between output A and B			2	5	ns ns
t _{ON}	Strobe delay time Turn-on time Turn-off time			6		ns ns

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^{1.} See Logic Function Table.

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TYPICAL PERFORMANCE CHARACTERISTICS

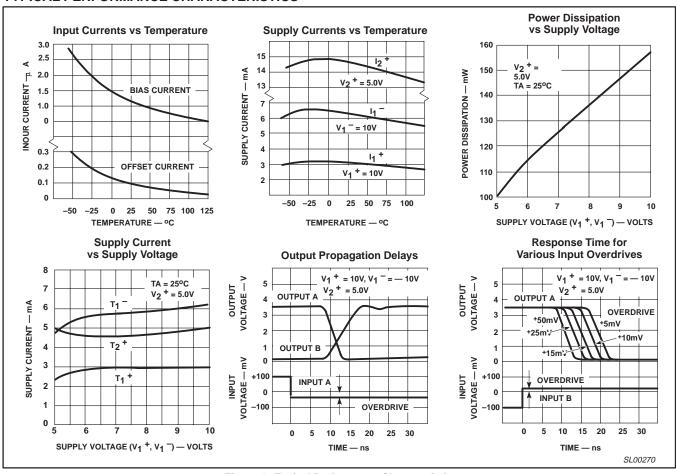


Figure 4. Typical Performance Characteristics

RESPONSE TIME TEST CIRCUIT

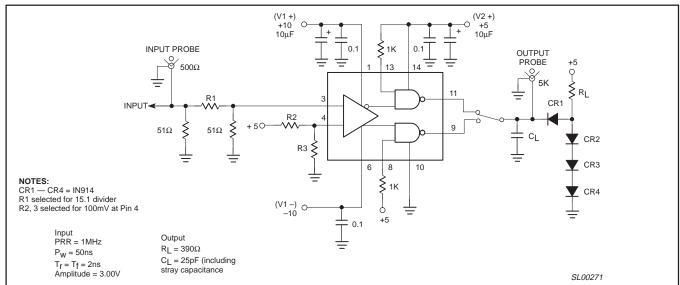


Figure 5. Response Time Test Circuit

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APPLICATIONS

One of the main features of the device is that supply voltages (V₁+, V₁–) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V₁–) should always be at least 6 V more than the ground terminal (Pin 6). Input common-mode

range should be limited to values of 2 V less than the supply voltages (V₁+ and V₁–) up to a maximum of ± 5 V as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

LOGIC FUNCTION

V _{ID} (A+, B-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \le -V_{OS}$	Н	Х	L	Н	Read I _{IHA} , I _{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	Н	Н	Undefined	Undefined	
$V_{ID} \ge V_{OS}$	Х	Н	Н	L	Read I _{ILA} , I _{IHB}
Х	L	L	Н	Н	

TYPICAL APPLICATIONS

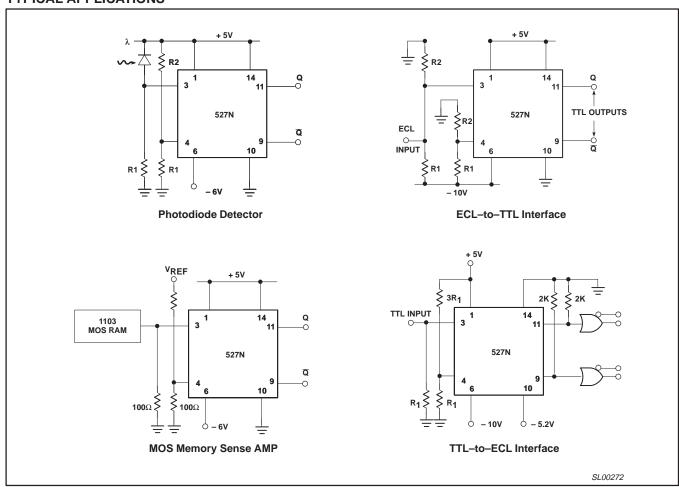


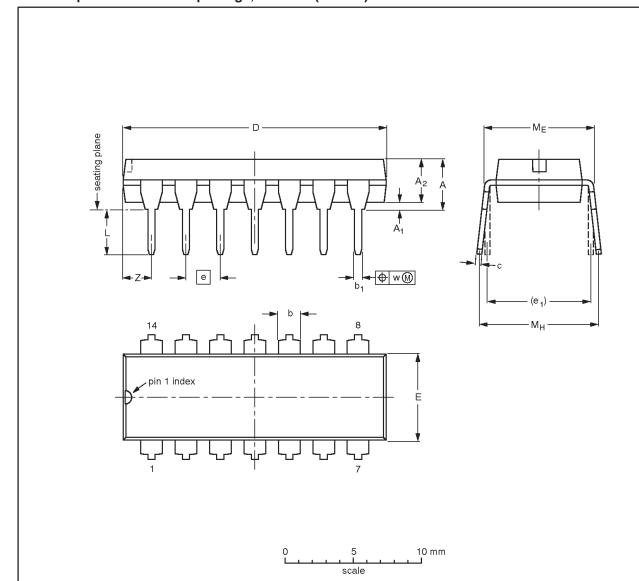
Figure 6. Typical Applications

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

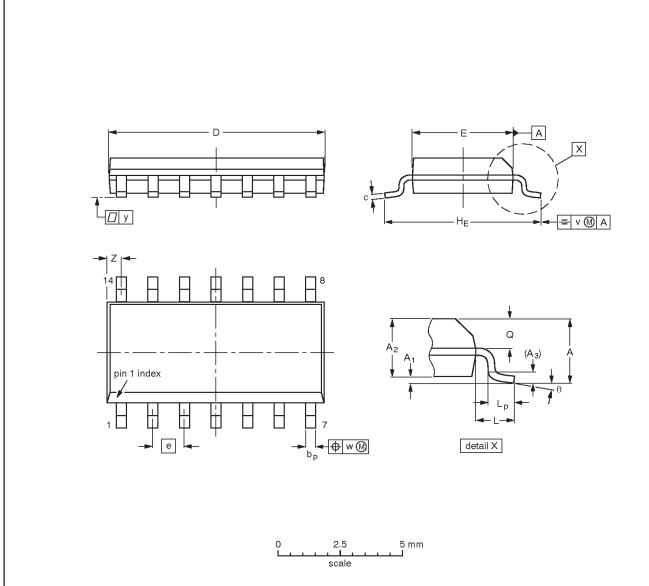
OUTLINE		REFEF	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEDEC EIAJ		PROJECTION	1330E DATE
SOT27-1	050G04	MO-001	SC-501-14			95-03-11 99-12-27

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	e	HE	L	Lp	Q	>	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN ISSUE DATE				
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE			
SOT108-1	076E06	MS-012			-97-05-22 99-12-27			

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NOTES

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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^[1] Please consult the most recently issued data sheet before initiating or completing a design.

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