

M402101BP

4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

DESCRIPTION

The M402101B is a semiconductor integrated circuit consisting of a 4×8 cross point switch capable of selecting 32 analog switches with 5 address inputs as well as 2 types of control signals.

FEATURES

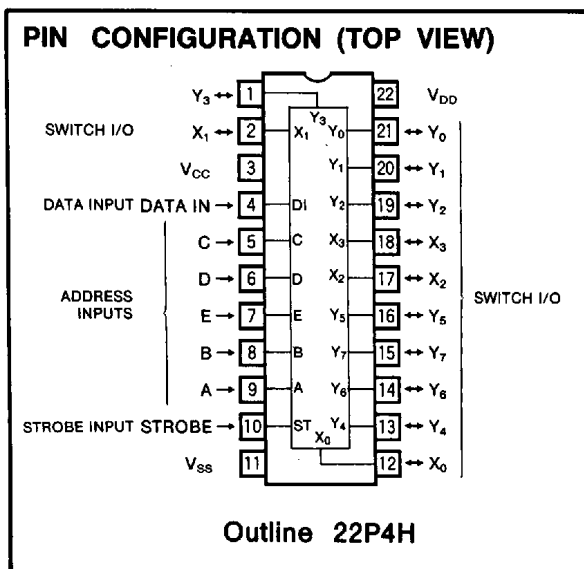
- Internal control latch circuit
- Internal level- shifter circuit
- Good crosstalk characteristics -100dB (@f=3kHz)
- Low on-state resistance 60Ω typical (@V_{DD}=15V)
- High off-state resistance more than 10⁹Ω typ.
- Excellent transfer linearity Distortion 0.05% typ. (@R_L=1kΩ, V_{DD}=5V, V_{SS}=-5V)
- 5V control logic

APPLICATION

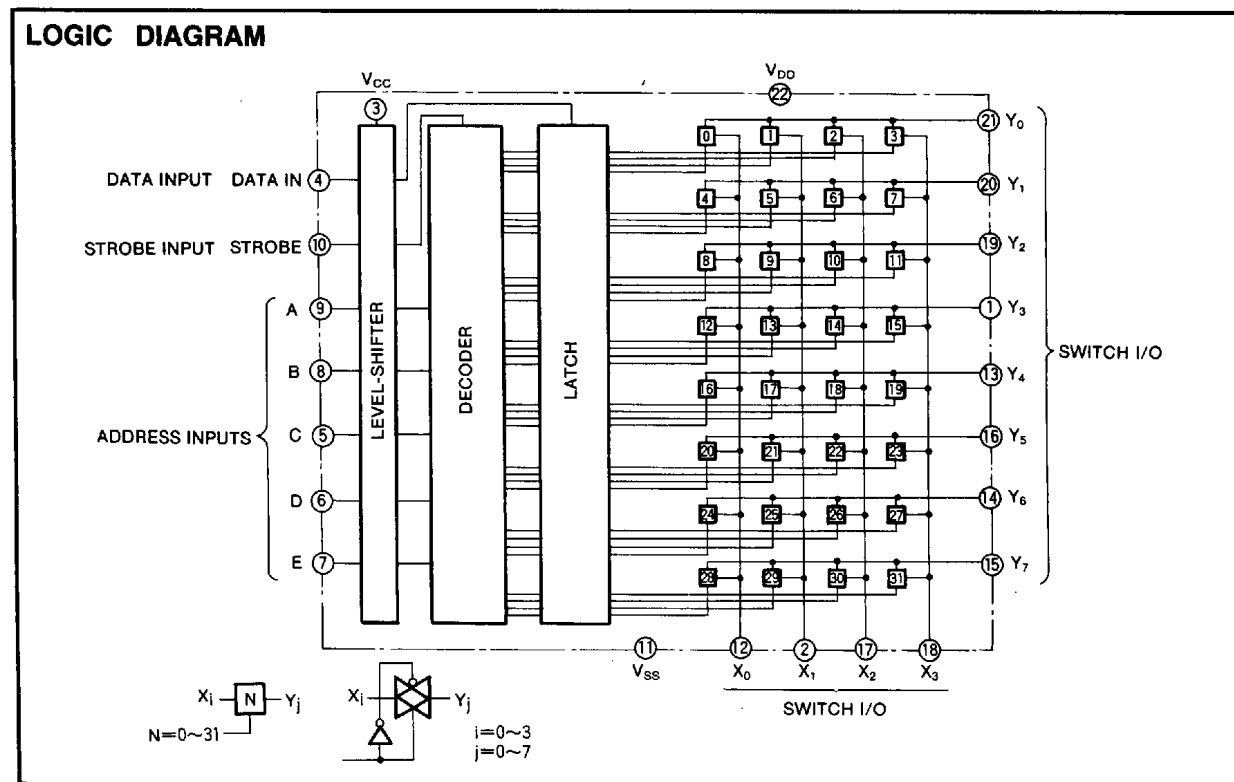
Line switching of telephone and communication equipments.

FUNCTIONAL DESCRIPTION

The input address signals (A, B, C, D, E) are five-bit binary coded. When the STROBE input is high, the switch that corresponds to the value of the input address signals is selected. If, at this time, the DATA IN input is high, the switch is turned on and until DATA IN is pulled low.



DATA IN is low, the switch is turned off and becomes in high-impedance state. When the STROBE becomes low, any of the switch conditions are not changed. The internal level-shifter makes possible to handle 15V_{p-p} analog signals by 5V control logic signals.



4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

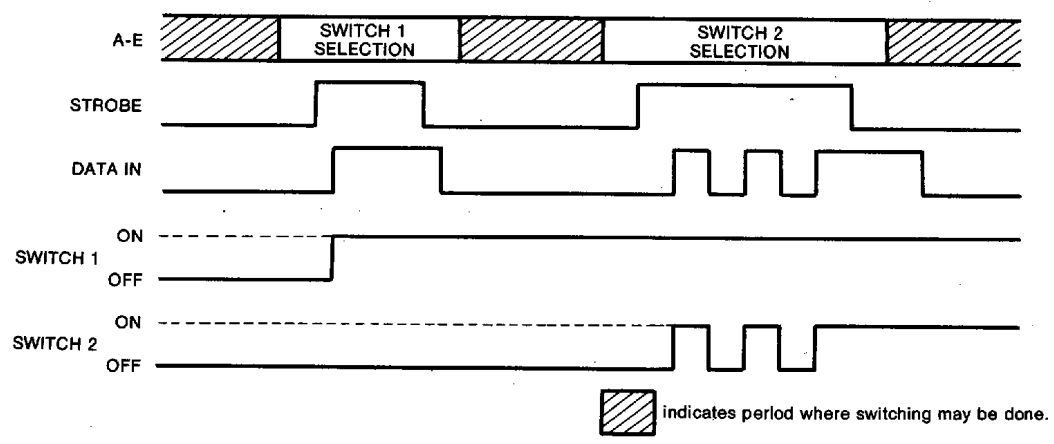
FUNCTION TABLE (Note : 1)

		0	1	2	3	4	5	6	7	8	...	30	31													
Control Input	A	X	L	L	H	H	L	L	H	H	L	L	H	H	L	L	...	L	L	H	H					
	B	X	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	...	H	H	H	H	
	C	X	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	...	H	H	H	H	
	D	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	...	H	H	H	H
	E	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	...	H	H	H	H
STROBE		L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	...	H	H	H	H	
DATA IN		X	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	...	L	H	L	H	
0	X0Y0	NC	OFF	ON																					NC	
1	X1Y0	NC	OFF ON																						NC	
2	X2Y0	NC	OFF ON																						NC	
3	X3Y0	NC	OFF ON																						NC	
4	X0Y1	NC	OFF ON																						NC	
5	X1Y1	NC	OFF ON																						NC	
6	X2Y1	NC	OFF ON																						NC	
7	X3Y1	NC	OFF ON																						NC	
8	X0Y2	NC	OFF ON																						NC	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
30	X2Y7	NC	OFF ON																						NC	
31	X3Y7	NC	OFF ON																						NC	

Note 1 : X : Irrelevant
 ON : Low impedance between X_i-Y_j ($i=0\sim3, j=0\sim7$)
 OFF : High impedance between X_i-Y_j ($i=0\sim3, j=0\sim7$)
 NC : No change and previous state is maintained.

OPERATING TIMING DIAGRAM

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4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{DD}	Supply voltage 1		−0.5~20	V
V _{CC}	Supply voltage 2		−0.5~20	V
V _{DD} −V _{CC}	Supply voltage 1−supply voltage 2		−0.5~20	V
V _I	Input voltage	A~E, STROBE, DATA IN	V _{SS} −0.5~V _{DD} +0.5	V
V _I	Input voltage	X ₀ ~X ₃ , Y ₀ ~Y ₇	V _{SS} −0.5~V _{DD} +0.5	V
V _{I/O}	On-state voltage difference between input and output	X ₀ ~X ₃ , Y ₀ ~Y ₇	+0.5	V
V _O	Output voltage	X ₀ ~X ₃ , Y ₀ ~Y ₇	−0.5~V _{CC} +0.5	V
I _I	Input current	A~E, STROBE, DATA IN	±10	mA
I _{I/O}	Input Output current	X ₀ ~X ₃ /Y ₀ ~Y ₇ (Switch off)	±10	mA
T _{stg}	Storage temperature		−65~+150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{DD}	Supply voltage 1	V _{CC}	15	18	V
V _{CC}	Supply voltage 2	4.5	5	5.5	V
V _I	Input voltage (A~E, STROBE, DATA IN)	V _{SS}		V _{CC}	V
V _I	Input voltage (X ₀ ~X ₃ , Y ₀ ~Y ₇)	V _{SS}		V _{DD}	V
V _O	Output voltage (X ₀ ~X ₃ , Y ₀ ~Y ₇)	V _{SS}		V _{DD}	V
T _{opr}	Operating free air temperature range	−40		+85	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits						Unit
			V _{DD} (V)	25°C			−40~+85°C		
				Min	Typ	Max	Min	Max	
V _{IH}	High-level input voltage (A~E, STROBE, DATA IN)	Switch on R _{ON} <R _{ON} MAX	5	4.0			4.0		V
			10	3.5			3.5		
			15	3.5			3.5		
V _{IL}	Low-level input voltage (A~E, STROBE, DATA IN)	Switch off I _L <0.2μA V _{CC} =5V	5			1.5		1.5	V
			10			1.5		1.5	
			15			1.5		1.5	
R _{ON}	On-resistance (Test circuit 1)	V _I = $\frac{V_{DD}-V_{SS}}{2}$	5		170	650		820	Ω
			10		75	150		185	
			15		60	100		130	
ΔR _{ON}	On-resistance difference (between 2 switches) (of the 32 switches)	V _I = $\frac{V_{DD}-V_{SS}}{2}$	5		16				Ω
			10		17				
			15		17				
I _O	Output off-leak current	Switch off	18			±0.3		±1.0	μA
I _{DD}	Quiescent supply current (per package)	V _I =V _{DD} , V _{SS}	5			10		150	μA
			10			20		300	
			15			40		600	
		V _I =3.5, 1.5V(Notes 2)	15		2.2				
I _{IH}	High-level input current (A~E, ST, DI)	V _{CC} =6V V _{IH} =6V	18			0.3		1.0	μA
I _{IL}	High-level input voltage (A~E, ST, DI)	V _{CC} =6V V _{IL} =0V	18			−0.3		−1.0	μA

Note 2 : Only one input is set to this value and all other inputs are tied to V_{CC} or GND.

4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

SWITCHING CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits			Unit			
			V _{SS} (V)	V _{DD} (V)	Min		Typ	Max	
f _{max} (I/O)	Maximum frequency	R _L =1kΩ Test circuit 2	-5	5		50	MHz		
f _{max}	Maximum control frequency	R _L =1kΩ C _L =50pF Test circuit 3	0	5	0.6	5	MHz		
			0	10	1.6	10			
			0	15	2.5	11			
t _{PLH}	Low- to high-level and high- to low-level output propagation time (Xn/Yn-Yn/Xn)	R _L =10kΩ C _L =50pF Test circuit 4	0	5		15	60	ns	
				0	10		7		30
				0	15		6		20
t _{PHL}			0	5		10	60	ns	
			0	10		6	30		
			0	15		5	20		
t _{PHZ}	High-level output disable time (STROBE-Yn/Xn)	R _L =1kΩ C _L =50pF Test circuit 5	0	5		200	530	ns	
			0	10		115	370		
			0	15		100	340		
t _{PZH}	High-level output enable time (STROBE-Yn/Xn)		0	5		180	800	ns	
			0	10		95	450		
			0	15		80	360		
t _{PZH}	High-level, low-level output enable time (DATA IN-Yn/Xn)	R _L =1kΩ C _L =50pF Test circuit 6	0	5		125	620	ns	
				0	10		80		440
				0	15		70		400
t _{PZL}			0	5		130	620	ns	
			0	10		80	440		
			0	15		70	400		
t _{PHZ}	High-level output disable time (A~E-Yn/Xn)	R _L =1kΩ C _L =50pF Test circuit 7	0	5		140	1070	ns	
			0	10		80	720		
			0	15		75	520		
t _{PZH}	High-level output enable time (A~E-Yn/Xn)		0	5		125	900	ns	
			0	10		65	470		
			0	15		60	380		
-	Sinewave distortion	R _L =1kΩ f _i =1kHz Test circuit 2	-5	5		0.05	%		
-	Feedthrough (switch off)	R _L =1kΩ Test circuit 8	-5	5		-80	dB		
-	Crosstalk	R _L =10kΩ Test circuit 9	0	(Note: 5) 10		150	mV		
-	Crosstalk frequency	R _L =1kΩ (Note: 3) SW(A)=on, SW(B)=off	-5	5		1.5	MHz		
		Test circuit 10 (Note: 4)	-5	5		0.1	kHz		
C _i	Input capacitance	A~E, STROBE, DATA IN, RESET			5	7.5	pF		
		Signal input	Xn		75		pF		
CX _n /Y _n	Input/output capacitance					48	pF		
					0.6		pF		

Note 3 : $20 \cdot \log \frac{V_o(B)}{V_i(A)} = -40\text{dB}$, Note 4 : $20 \cdot \log \frac{V_o(B)}{V_i(A)} = -110\text{dB}$, Note 5 : V_{CC}=10V

TIMING REQUIREMENT (V_{CC}=5V, V_{SS}=0V)

Symbol	Parameter	Test conditions	Limits			Unit
			V _{DD} (V)	Min	Typ	
t _{w(ST)}	Strobe pulse width		5	600	135	ns
			10	240	60	
			15	190	45	
t _{SU}	Data setup time before A~E, STROBE		5	280	70	ns
			10	140	35	
			15	120	25	
t _H	Data hold time after A~E, STROBE		5	420	60	ns
			10	280	35	
			15	180	25	

4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

1 On-state resistance (R_{ON})

$$R_{ON} = 10 \times \frac{(V_i - V_o)}{V_o} \text{ [k}\Omega\text{]}$$

* Only one switch is on.
See function table for conditions of address inputs A through E.

**2 Maximum frequency ($f_{max(I/O)}$)
sinewave distortion**

With an input sinewave of $+2.5V_{p-p}$, $f_{max(I/O)}$ is equal to frequency (f_1) when $20 \cdot \log_{10} V_o/V_1 = -3\text{dB}$.
See function table for conditions of address inputs A through E.

3 Maximum control frequency ($f_{max}(C_{IN})$)

Timing diagram

$f_{max}(C_{IN})$ is the value of f_1 when output amplitude reaches half the value of its original value at the time the input frequency $f_1 = 1\text{kHz}$.
See function table for conditions of address inputs A through E.

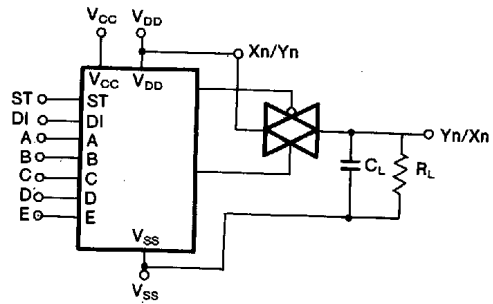
**4 Low- to high-level and high- to low-level
output propagation time ($X_n/Y_n - Y_n/X_n$)**

Timing diagram

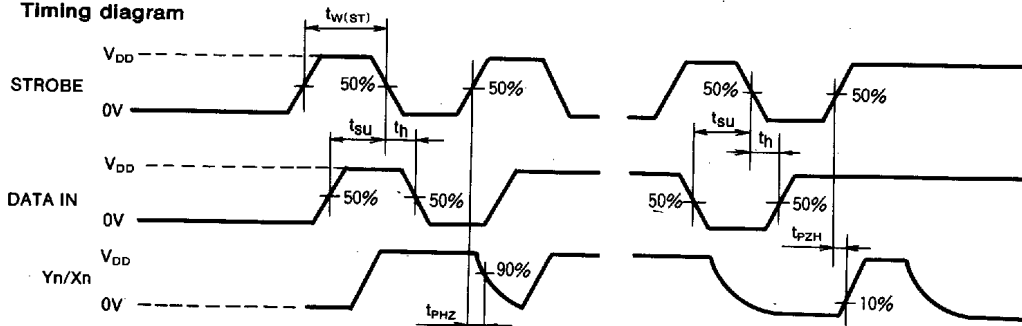
See function table for conditions of address inputs A through E.

4x8 CROSSPOINT SWITCH WITH CONTROL MEMORY

**5 High-level output disable/enable time
 (STROBE—Yn/Xn)**



Timing diagram



See function table for conditions of address inputs A through E.

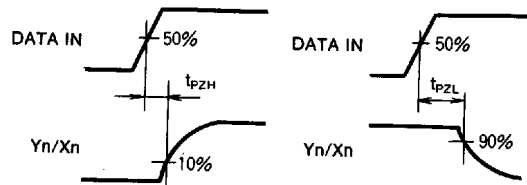
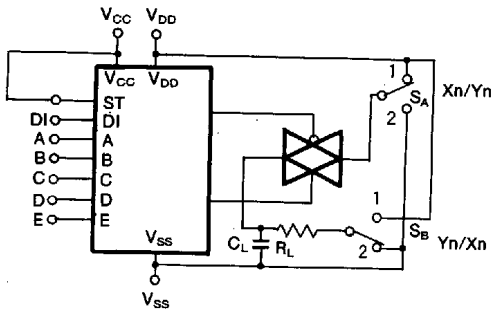
**6 High-level, low-level enable time
 (DATA IN—Yn/Xn)**

Timing diagram

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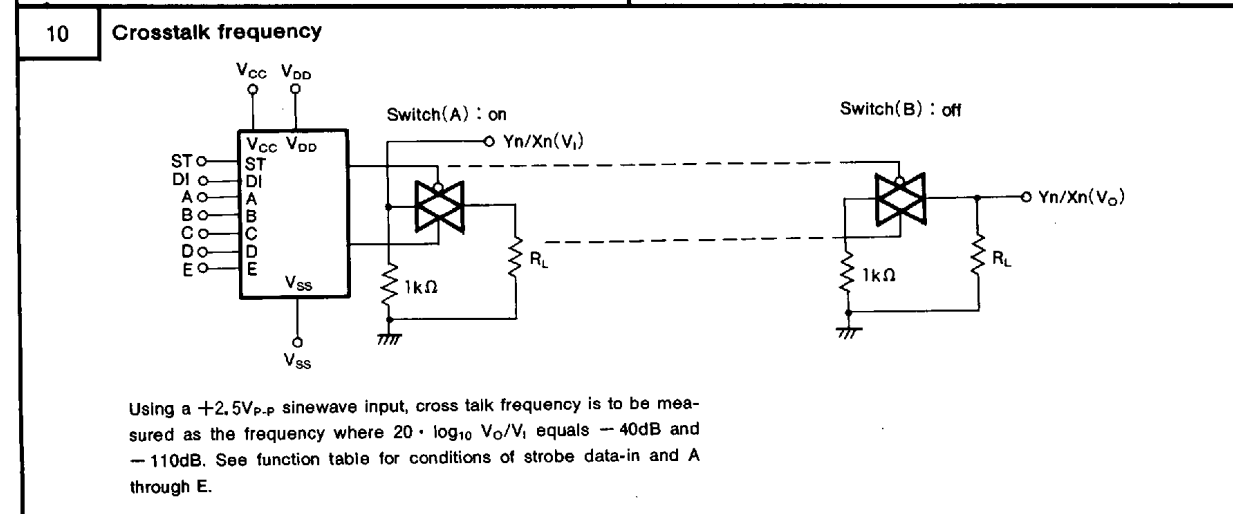
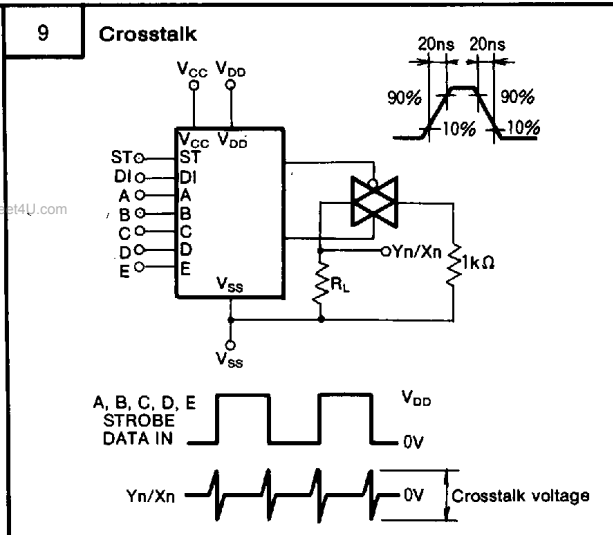
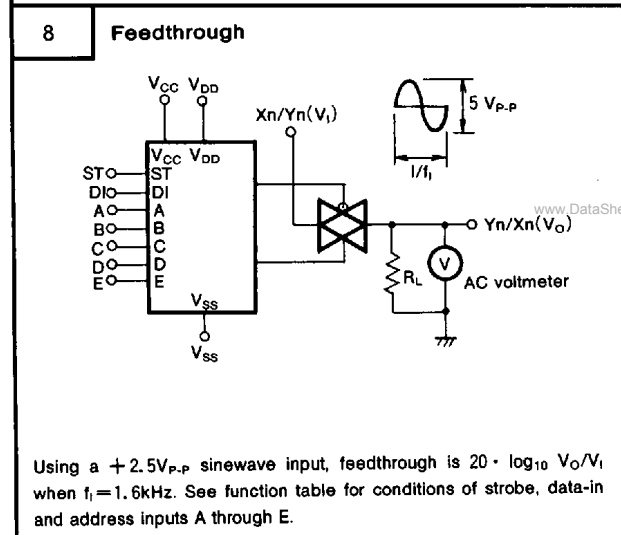
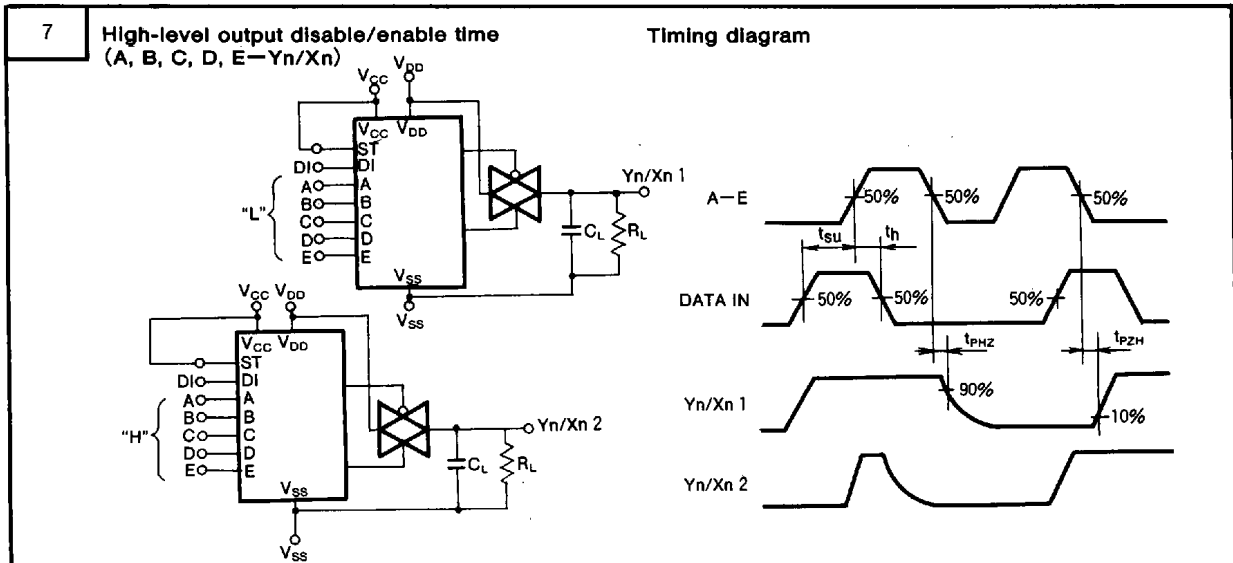
$S_A = 1, S_B = 2$

$S_A = 2, S_B = 1$



See function table for conditions of address inputs A through E.

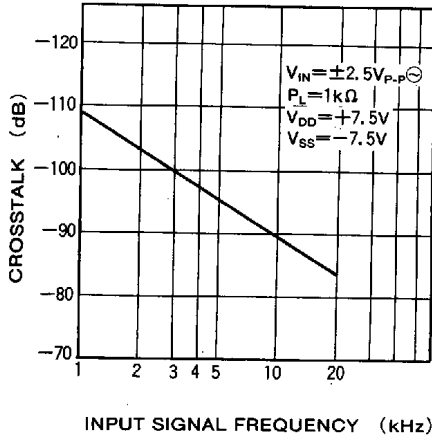
4x8 CROSSPOINT SWITCH WITH CONTROL MEMORY



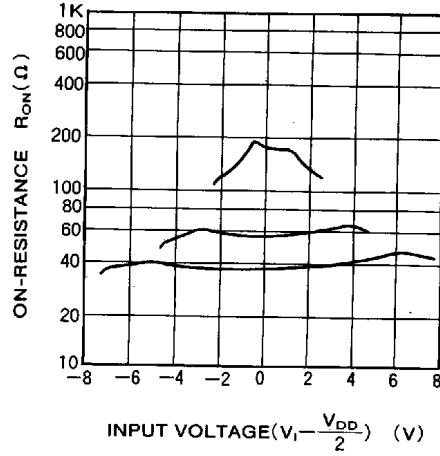
4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

TYPICAL CHARACTERISTICS

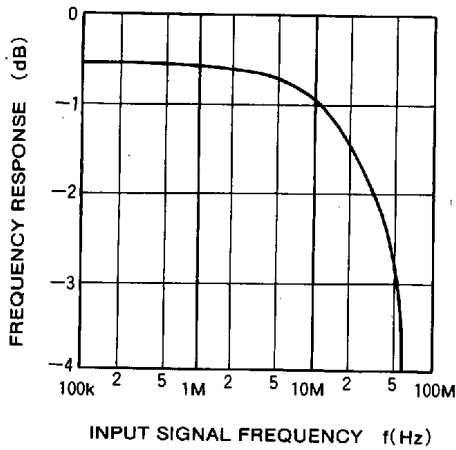
CROSSTALK—INPUT SIGNAL FREQUENCY



R_{ON}—INPUT VOLTAGE ($V_I - \frac{V_{DD}}{2}$)



FREQUENCY RESPONSE



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