

# TC5064BP, TC5065BP

C<sup>2</sup>MOS DIGITAL INTEGRATED CIRCUIT  
SILICON MONOLITHIC

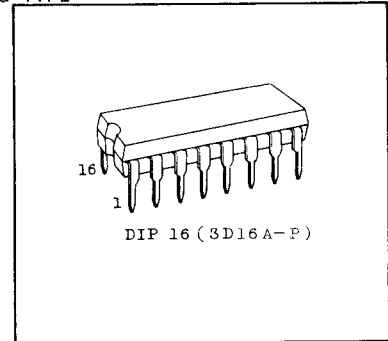
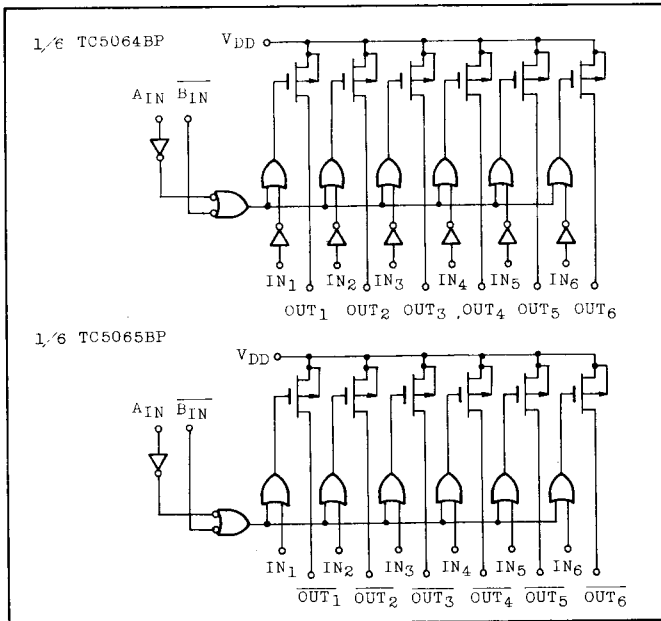
TC5064BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/NON INVERTING TYPE  
TC5065BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/INVERTING TYPE

TC5064BP and TC5065BP contain six circuits of buffers having two common INHIBIT inputs ( $A_{IN}$ ,  $\overline{B}_{IN}$ ). As both have the output of open drain structure with high breakdown voltage P-channel MOS FET (-50 volts... Maximum Rating), these are suitable for driving fluorescent display tubes and for interfacing with high voltage MOS LSI's. TC5064BP is non-inverting type and TC5065BP is inverting type.

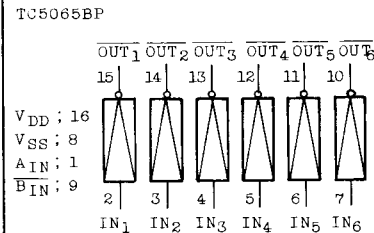
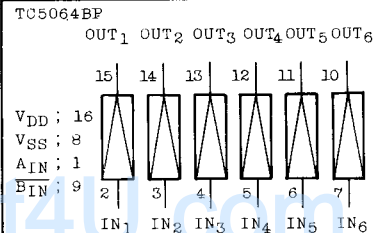
## ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.5 ~ V <sub>SS</sub> +20	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>DD</sub> -50 ~ V <sub>DD</sub> +0.5	V
Power Dissipation	PD	300	mW
DC Input Current	I <sub>IN</sub>	±10	mA
Storage Temperature Range	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C · 10sec	

## LOGIC DIAGRAM



## PIN ASSIGNMENT



## TRUTH TABLE

INPUT			OUTPUT	
A <sub>IN</sub>	$\overline{B}_{IN}$	IN	TC5064BP	TC5065BP
L	H	L	HZ	H
L	H	H	H	HZ
*	L	*	HZ	HZ
H	*	*	HZ	HZ

HZ; High Impedance  
\*; Don't care

RECOMMENDED OPERATING CONDITIONS (VSS=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	3		18	V
Input Voltage	VIN	0		VDD	V
Operating Temp.	Topr	-40		85	°C

ELECTRICAL CHARACTERISTICS (VSS=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VDD (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	VOH	IOUT < 1μA VIN=VSS or VDD	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
High Level Output Current	IOH	VOH=3V (VDD-2V)	5	-6	-	-5	-10	-	-4	-	mA
		VOH=2V (VDD-3V)	5	-9	-	-8	-13	-	-6	-	
		VOH=7V (VDD-3V)	10	-12	-	-10	-25	-	-8	-	
		VOH=12V (VDD-3V)	15	-17	-	-15	-35	-	-12	-	
High Level Input Voltage	* VIH	VOUT=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		VOUT=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		VOUT=1.5V, 13.5V	15	11.0	-	11.0	8.25	-	11.5	-	
Low Level Input Voltage	* VIL	VOUT=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	V
		VOUT=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		VOUT=1.5V, 13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
Output OFF Current	IOFF	VOUT = 0V	15	-	-3	-	-0.01	-3	-	-10	μA
		VOUT = VDD-45V	15	-	-10	-	-1	-10	-	-20	
Input Current	IIH	VIH = 18V	18	-	0.3	-	10 <sup>-5</sup>	0.3	-	1.0	μA
	IIIL	VIL = 0V	18	-	-0.3	-	-10 <sup>-5</sup>	-0.3	-	-1.0	
Quiescent Supply Current	IDD	VIN=VSS, VDD, OUTPUTS OPEN	5	-	4.0	-	0.005	4.0	-	30	μA
			10	-	8.0	-	0.010	8.0	-	60	
			15	-	16.0	-	0.015	16.0	-	120	

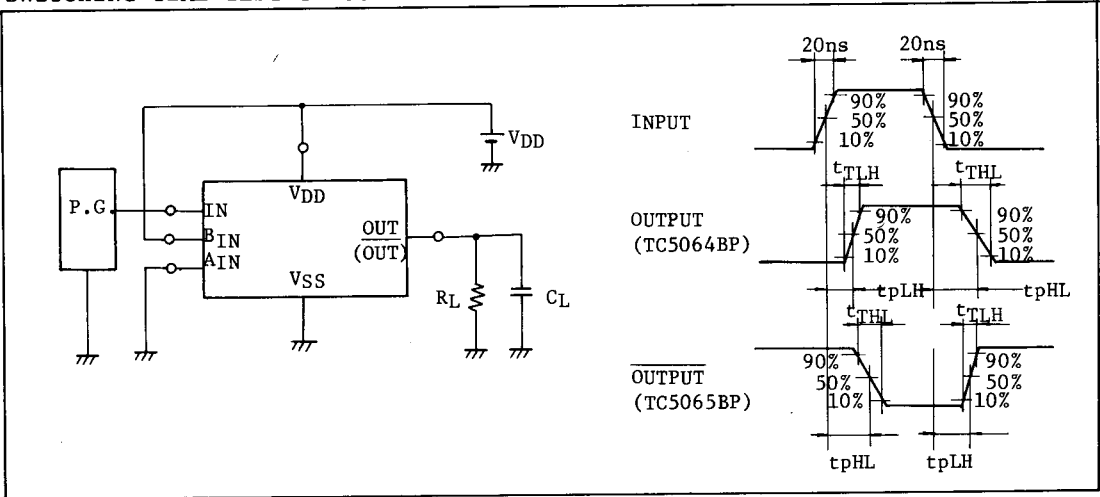
\* RL = 20 kΩ

SWITCHING CHARACTERISTICS (Ta=25°C, VSS=0V, CL=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VDD (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	tTLH	RL = 20 kΩ	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Fall Time	tTHL	RL = 20 kΩ	5	-	5.0	8.0	μs
			10	-	5.0	8.0	
			15	-	5.0	8.0	
(LOW-HIGH) Propagation Delay Time	tpLH	RL = 20 kΩ	5	-	200	500	ns
			10	-	100	250	
			15	-	80	200	
(HIGH-LOW) Propagation Delay Time	tpHL	RL = 20 kΩ	5	-	2.0	4.0	μs
			10	-	2.0	4.0	
			15	-	2.0	4.0	
Input Capacity	CIN			5	7.5	pF	

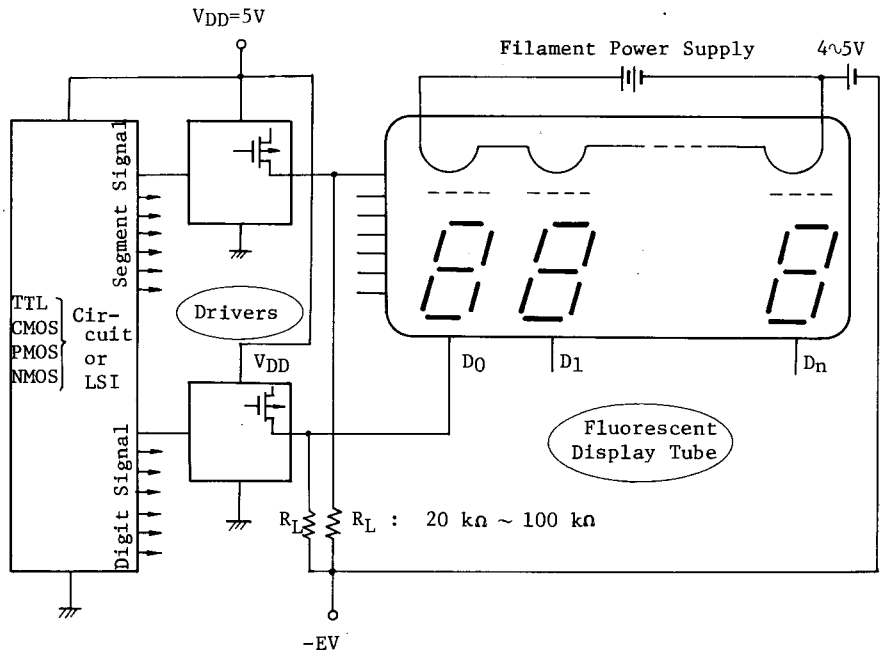
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SWITCHING TIME TEST CIRCUIT AND WAVEFORM



EXAMPLES OF APPLICABLE CIRCUITS

(1) Fluorescent Display Tube Driving Circuit



(2) Interface between CMOS and PMOS

