

Integrated Device Technology, Inc.

# HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841A/B/C

## FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT841A equivalent to FAST™ speed
- **IDT54/74FCT841B 25% faster than FAST**
- **IDT54/74FCT841C 40% faster than FAST**
- Buffered common latch enable, clear and preset inputs
- IOL = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

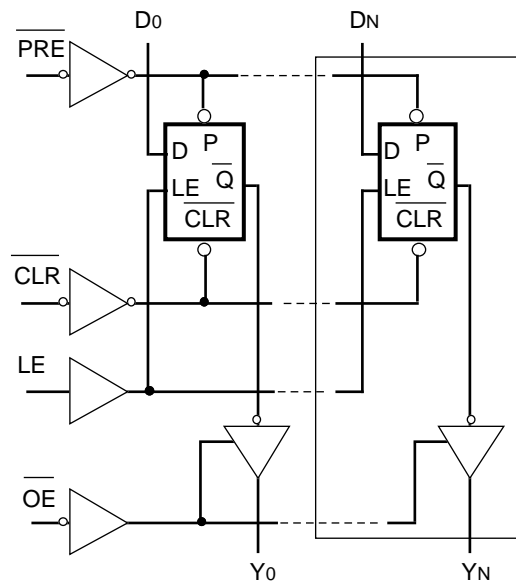
## DESCRIPTION:

The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 is a buffered, 10-bit wide version of the popular '373 function.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

## FUNCTIONAL BLOCK DIAGRAM



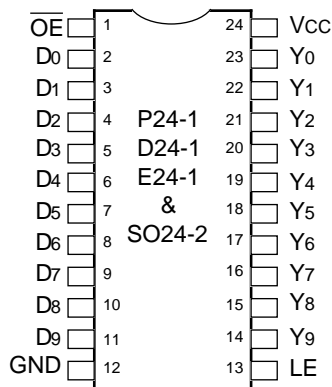
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FAST is a trademark of National Semiconductor Co.

**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

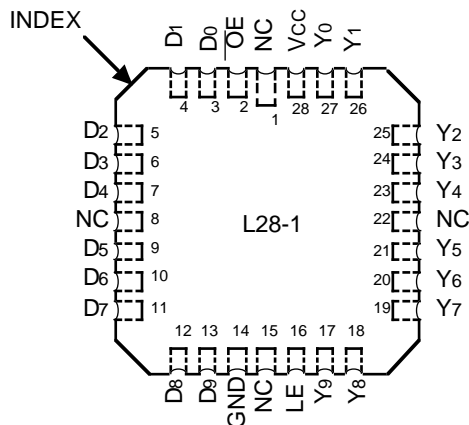
**APRIL 1994**

## PIN CONFIGURATIONS



DIP/CERPACK/SOIC  
TOP VIEW

2607 drw 02



LCC  
TOP VIEW

2607 drw 03

## PIN DESCRIPTION

Name	I/O	Description
$\overline{\text{CLR}}$	I	When $\overline{\text{CLR}}$ is LOW, the outputs are LOW if $\overline{\text{OE}}$ is LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the latch.
$\text{Di}$	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
$\text{Yi}$	O	The 3-state latch outputs.
$\overline{\text{OE}}$	I	The output enable control. When $\overline{\text{OE}}$ is LOW, the outputs are enabled. When $\overline{\text{OE}}$ is HIGH, the outputs ( $\text{Yi}$ ) are in the high-impedance (off) state.
$\overline{\text{PRE}}$	I	Preset line. When $\overline{\text{PRE}}$ is LOW, the outputs are HIGH if $\overline{\text{OE}}$ is LOW. Preset overrides $\overline{\text{CLR}}$ .

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## FUNCTION TABLE<sup>(1)</sup>

Inputs					Inter- nal	Out- puts	Function
$\overline{\text{CLR}}$	$\overline{\text{PRE}}$	$\overline{\text{OE}}$	LE	$\text{Di}$	$\text{Qi}$	$\text{Yi}$	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

**NOTE:**

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

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### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub>	-0.5 to V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

- NOTE:** 2607 tbl 03
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
  - Input and V<sub>CC</sub> terminals only.
  - Outputs and I/O terminals only.

### CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

- NOTE:** 2607 tbl 04
- This parameter is measured at characterization but not tested.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V  
 Commercial: T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5.0V ± 5%; Military: T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max.	V <sub>I</sub> = V <sub>CC</sub>	—	—	5	μA
I <sub>IL</sub>	Input LOW Current		V <sub>I</sub> = 2.7V	—	—	5 <sup>(4)</sup>	
			V <sub>I</sub> = 0.5V	—	—	-5 <sup>(4)</sup>	
			V <sub>I</sub> = GND	—	—	-5	
I <sub>OZH</sub>	Off State (High Impedance) Output Current	V <sub>CC</sub> = Max.	V <sub>O</sub> = V <sub>CC</sub>	—	—	10	μA
I <sub>OZL</sub>			V <sub>O</sub> = 2.7V	—	—	10 <sup>(4)</sup>	
			V <sub>O</sub> = 0.5V	—	—	-10 <sup>(4)</sup>	
			V <sub>O</sub> = GND	—	—	-10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>N</sub> = -18mA	—	-0.7	-1.2	V	
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>O</sub> = GND	-75	-120	—	mA	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OH</sub> = -32μA	V <sub>HC</sub>	V <sub>CC</sub>	—	V	
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -300μA	V <sub>HC</sub>	V <sub>CC</sub>		—
			I <sub>OH</sub> = -15mA MIL.	2.4	4.3		—
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OL</sub> = 300μA	—	GND	V <sub>LC</sub>	V	
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 300μA	—	GND		V <sub>LC</sub> <sup>(4)</sup>
			I <sub>OL</sub> = 32mA MIL.	—	0.3		0.5
		I <sub>OL</sub> = 48mA COM'L.	—	0.3	0.5		

- NOTES:** 2607 tbl 05
- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
  - Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
  - Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
  - This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{OE} = GND$ LE = V <sub>CC</sub> One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle $\overline{OE} = GND$ LE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.0	5.0	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle $\overline{OE} = GND$ LE = V <sub>CC</sub> Eight Bits Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	3.2	6.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	5.2	14.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

2607 tbl 06

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT841A				FCT841B				FCT841C				Unit	
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.			
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.		
tPLH tPHL	Propagation Delay DI to Yi (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns	
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0		
tPLH tPHL	Propagation Delay LE to Yi	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	1.5	6.4	1.5	6.8	ns	
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	1.5	15.0	1.5	16.0		
tPLH tPHL	Propagation Delay, $\overline{\text{PRE}}$ to Yi	CL = 50pF RL = 500Ω	1.5	12.0	1.5	14.0	1.5	8.0	1.5	10.0	1.5	7.0	1.5	9.0	ns	
tPHL	Propagation Delay, $\overline{\text{CLR}}$ to Yi		1.5	14.0	1.5	17.0	1.5	10.0	1.5	13.0	1.5	9.0	1.5	12.0		
tPHL	Propagation Delay, $\overline{\text{CLR}}$ to Yi		1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	1.5	9.0	1.5	10.0	ns	
tPLH	Propagation Delay, $\overline{\text{CLR}}$ to Yi		1.5	14.0	1.5	17.0	1.5	10.0	1.5	10.0	1.5	9.0	1.5	9.0		
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to Yi	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	6.5	1.5	7.3	ns	
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	1.5	12.0	1.5	13.0		
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to Yi	CL = 5pF <sup>(4)</sup> RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	5.7	1.5	6.0	ns	
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.3		
tSU	Data to LE Set-up Time	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
tH	Data to LE Hold Time		2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
tW	LE Pulse Width <sup>(3)</sup>		HIGH	4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{\text{PRE}}$ Pulse Width <sup>(3)</sup>		LOW	5.0	—	7.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{\text{CLR}}$ Pulse Width <sup>(3)</sup>		LOW	4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{\text{PRE}}$ to LE		4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns	
tREM	Recovery Time $\overline{\text{CLR}}$ to LE		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	

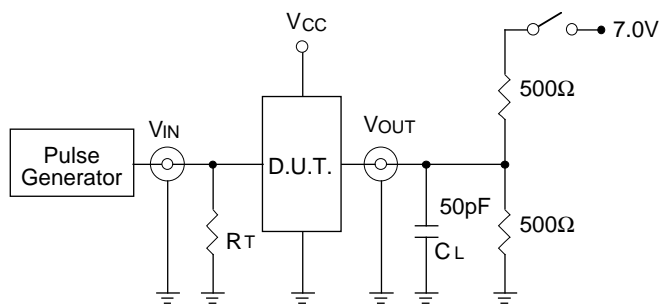
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2607 tbl 07

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

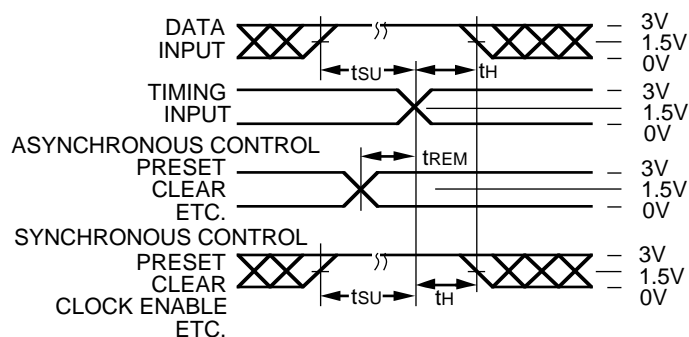
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

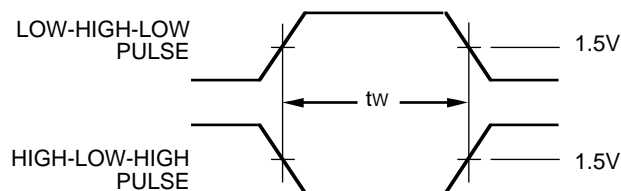
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2607 tbl 08

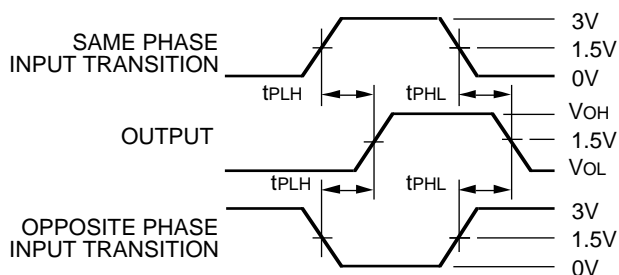
### SET-UP, HOLD AND RELEASE TIMES



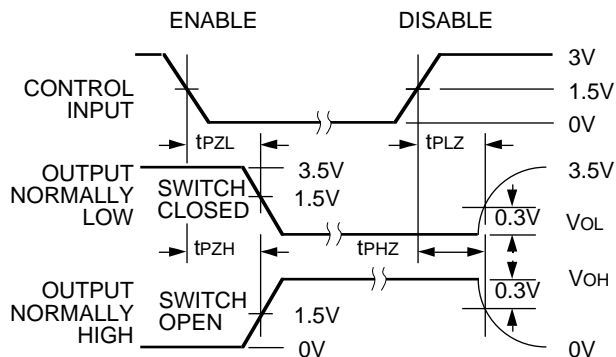
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

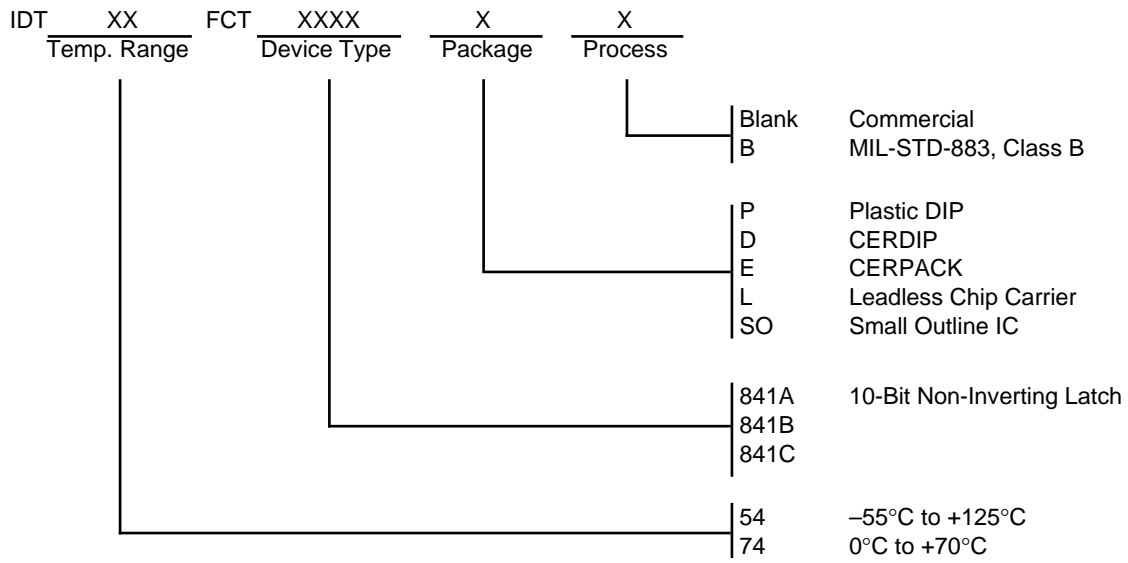


#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$

2607 drw 04

**ORDERING INFORMATION**



2607 drw 05