CS4281

Product Data Sheet

FEATURES

- **Full DOS Games Compatibility via PC/PCI, DDMA, and CrystalClear Legacy Support**
- **PCI Version 2.1 Bus Master**
- **PC '98 and PC '99 Compliance**
- **MPU-401 interface, FM Synthesizer, and Game Port**
- **Full Duplex Operation**
- **Hardware Volume Control**
- **Win 95®, 98 (WDM), Win NT® 4.0, Win NT 5.0 (WDM) Drivers**
- **Advanced Power Management (PPMI)**
- **Digital Docking Solution with AC '97 2.0 Codec**
- **Support for Multi-Channel Audio Output**
- **Hardware Sample Rate Converters**
- **Pin-Compatible with CS4614 and CS4280-CM**

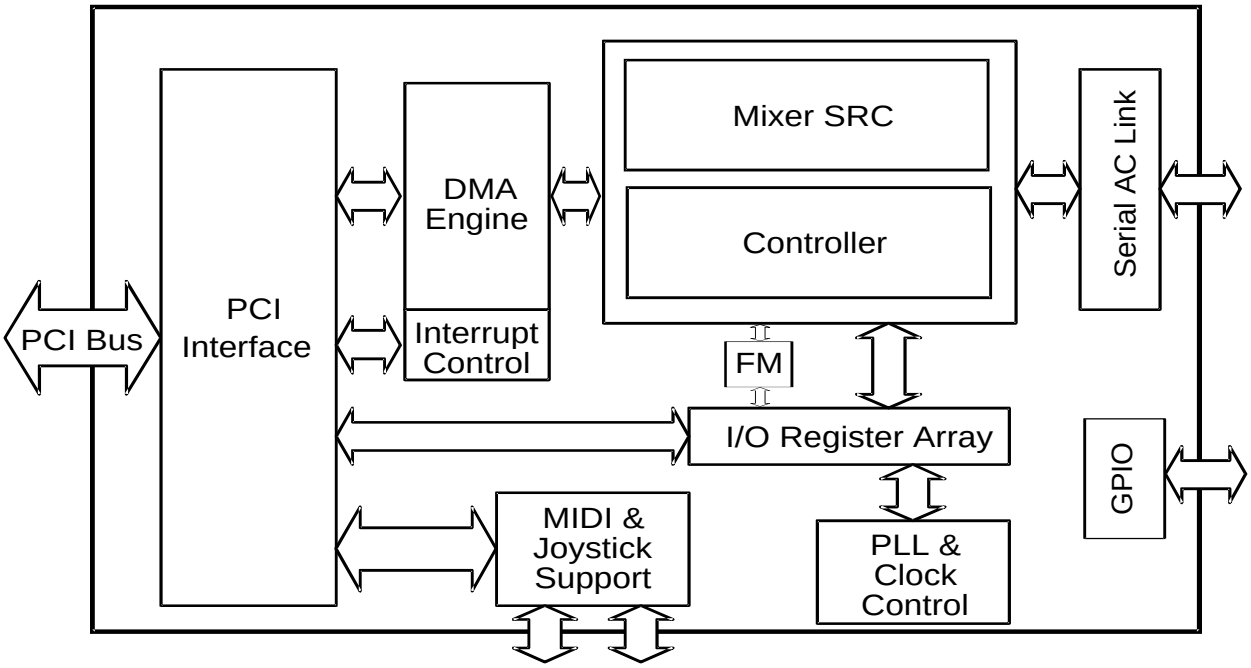
CrystalClear™ PCI Audio Interface

DESCRIPTION

The CS4281 is a PCI audio controller with integrated legacy games support suitable for desktop and notebook PC designs. When combined with driver software and an AC '97 codec such as the CS4297A, this device provides a complete high quality audio solution. Legacy compatibility is achieved via PC-PCI, DDMA, and CrystalClear Legacy Support. The product includes an integrated FM synthesizer and Plug-and-Play interface. In addition, the CS4281 offers hardware volume control and power management features. WDM drivers provide support for Windows 98® and Windows NT®. When used with the CS4297A, the CS4281 is fully compliant with Microsoft's PC '98 and PC '99 audio requirements. In the 100-pin MQFP package, the CS4281 is pin-compatible with the CS4614 and CS4280-CM.

ORDERING INFORMATION

CS4281-CM	100-pin MQFP	14x20x2.72mm
CS4281-CQ	100-pin TQFP	14x14x1.4mm



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Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

CHARACTERISTICS/SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(PCIGND = CGND = CRYGND = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies		PCIVDD	-	-	4.6	V
		VAUX	-	-	4.6	V
		CVDD	-	-	4.6	V
		CRYVDD	-	-	4.6	V
		VDD5REF	-	-	5.5	V
Total Power Dissipation	(Note 1)		-	-	1.0	W
Input Current per Pin, DC (Except supply pins)			-	-	±10	mA
Output current per pin, DC			-	-	±50	mA
Digital Input voltage	(Note 2)		-0.3	-	Vdd+ 0.3	V
Ambient temperature (power applied)	(Note 3)		-55	-	125	°C
Storage temperature			-65	-	150	°C

Notes: 1. Includes all power generated by AC and/or DC output loading.
2. The power supply pins are at recommended maximum values.
3. At ambient temperatures above 70° C, t otal power dissipation must be limited to less than 0.4 Watts.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(PCIGND = CGND = CRYGND = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	PCIVDD	3	3.3	3.6	V
	VAUX	3.135	3.3	3.465	V
	CVDD	3	3.3	3.6	V
	CRYVDD	3	3.3	3.6	V
	VDD5REF	4.75	5	5.25	V
Operating Ambient Temperature	T_A	0	25	70	°C

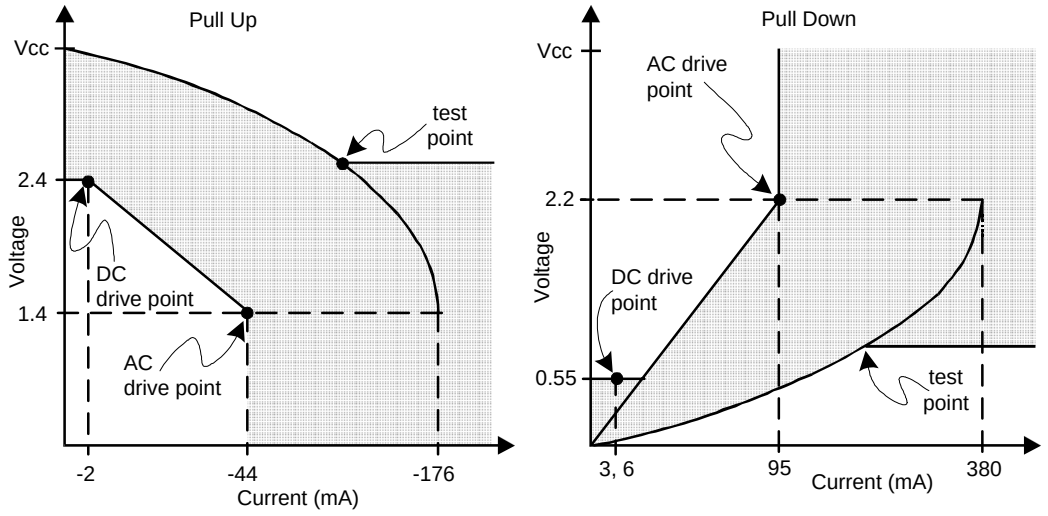
Specifications are subject to change without notice.

AC CHARACTERISTICS (PCI SIGNAL PINS ONLY)

(T_A = 70° C; PCIVDD = CVDD = VAUX = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Reference levels = 1.4 V; unless otherwise noted; (Note 4))

Parameter			Symbol	Min	Max	Unit
Switching Current High		(Note 5)	I_{OH}			
		0 < Vout ≤ 1.4		-44	-	mA
		1.4 < Vout < 2.4		$-44 + \frac{Vout - 1.4}{0.024}$	-	mA
		3.1 < Vout < 3.3		-	(Note 7)	
Switching Current Low		(Note 5)	I_{OL}			
		Vout ≥ 2.2		95	-	mA
		2.2 > Vout > 0.55		Vout/0.023	-	mA
		0.71 > Vout > 0		-	(Note 8)	
Low Clamp Current		-5 < Vin ≤ -1	I_{CL}	$-25 + \frac{Vin + 1}{0.015}$	-	mA
Output rise slew rate	0.4 V - 2.4 V load	(Note 6)	$slew_r$	1	5	V/ns
Output fall slew rate	2.4 V - 0.4 V load	(Note 6)	$slew_f$	1	5	V/ns

Notes:
4. Specifications guaranteed by characterization and not production testing.
5. Refer to V/I curves in Figure 1. Specification does not apply to PCICLK and RST# signals. Switching Current High specification does not apply to PME#, CLKRUN#, and INTA# which are open drain outputs.
6. Cumulative edge rate across specified range. Rise slew rates do not apply to open drain outputs.
7. Use Equation A in Figure below.
8. Use Equation B in Figure below.



Equation A:

$I_{OH} = 11.9 \times (Vout - 5.25) \times (Vout + 2.45)$
for 3.3 V > Vout > 3.1 V

Equation B:

$I_{OL} = 78.5 \times Vout \times (4.4 - Vout)$
for 0 V < Vout < 0.71 V

Figure 1. AC Characteristics

DC CHARACTERISTICS (T_A = 70° C; PCIVDD = VAUX = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Typ	Max	Unit
PCI Interface Signal Pins							
High level input voltage			V_{IH}	2	-	5.75	V
Low level input voltage			V_{IL}	-0.5	-	0.8	V
High level output voltage	Iout = -2 mA		V_{OH}	2.4	-	-	V
Low level output voltage	Iout = 3 mA, 6 mA	(Note 9)	V_{OL}	-	-	0.55	V
High level leakage current	Vin = 2.7 V	(Note 10)	I_{IH}	-	-	70	µA
Low level leakage current	Vin = 0.5 V		I_{IL}	-	-	-70	µA
PME# power off input leakage	Vin = 5.25 V	(Note 11)	I_{OFF}	-	-	1	µA
Non-PCI Interface Signal Pins		(Note 12)					
High level output voltage	Iout = -5 mA	(Note 13)	V_{oh}	0.9×Vdd		-	V
Low level output voltage	Iout = 5 mA		V_{ol}	-		0.1×Vdd	V
High level input voltage		(Note 14)	V_{ih}	0.65×Vdd		Vdd+0.3	V
Low level input voltage		(Note 14)	V_{il}	-0.3		0.35×Vdd	V
High level leakage current	Vin = 3.6 V	(Note 14)	I_{ih}	-		10	µA
Low level leakage current	Vin = 0	(Note 14)	I_{il}	-		-10	µA

Parameter			Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded)						
Power Supply Current:	VDD5REF		-	0.6	-	mA
	VAUX		-	TBD	20	mA
PCIVDD/CVDD/CRYVDD Total		(Note 4)	-	TBD	TBD	mA
Low Power Mode Supply Current			-	TBD	-	mA

Notes:
9. The following signals are tested to 6 mA: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, PERR#, and INTA#. All other PCI interface signals are tested to 3 mA.
10. Input leakage currents include hi-Z output leakage for all bi-directional buffers with three-state outputs.
11. Maximum allowable leakage into the PME# open-drain pin when power is removed from VAUX. Assumes no event occurred to drive PME# (idle state).
12. For AC-Link and VOLUP/DN pins, Vdd is VAUX. For all others Vdd is the core supply.
13. For open drain pins, high level output voltage is dependent on external pull-up used and number of attached gates.
14. All inputs that do not include internal pull-ups or pull-downs, must be externally driven for proper operation. If an input is not driven, it should be tied to power or ground, depending on the particular function. If an I/O pin is not driven and programmed as an input, it should be tied to power or ground through its own resistor.

PCI INTERFACE PINS

(T_A = 0 to 70° C ; PCIVDD = CVDD = VAUX = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V)

Parameter	Symbol	Min	Max	Unit
PCICLK cycle time	t_{cyc}	30	-	ns
PCICLK high time	t_{high}	11	-	ns
PCICLK low time	t_{low}	11	-	ns
PCICLK to signal valid delay - bused signals	t_{val}	2	11	ns
PCICLK to signal valid delay - point to point	$t_{val(p+p)}$	2	12	ns
Float to active delay (Note 15)	t_{on}	2	-	ns
Active to Float delay (Note 15)	t_{off}	-	28	ns
Input Set up Time to PCICLK - bused signals	t_{su}	7	-	ns
Input Set up Time to PCICLK - point to point	$t_{su(p+p)}$	10, 12	-	ns
Input hold time for PCICLK	t_h	0	-	ns
Reset active to output float delay (Notes 15, 16, 17)	$t_{rst-off}$	-	30	ns

Notes: 15. For Active/Float measurements, the Hi-Z or “off” state is when the total current delivered is less than or equal to the leakage current. Specification is guaranteed by design, not production tested.
16. RST# is asserted and de-asserted asynchronously with respect to PCICLK.
17. All PCI output drivers are asynchronously floated when RST# is active. Note ASDOUT and ASYNC are not affected by RST#.

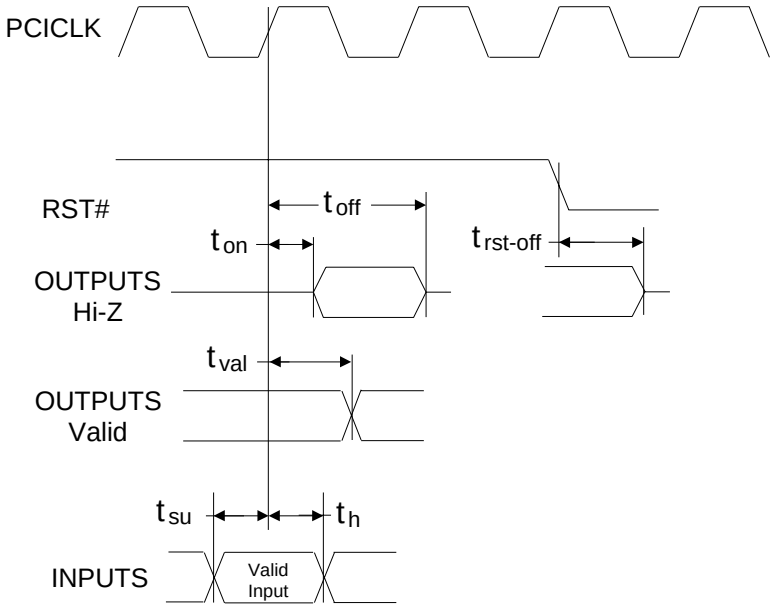


Figure 2. PCI Timing Measurement Conditions

AC-LINK SERIAL INTERFACE (T_A = 0 to 70° C; PCIVDD = CVDD = VAUX = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = V_{ol},V_{il}, Logic 1 = V_{oh},V_{ih}; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK input cycle time	t_{clk_period}		81.4	-	ns
ABITCLK input high time	t_{clk_high}	36	40.7	45	ns
ABITCLK input low time	t_{clk_low}	36	40.7	45	ns
ABITCLK input rise/fall time	t_{rfclk}	2	-	6	ns
ASDIN/ASDIN2 valid to ABITCLK falling	t_{setup}	10	-	-	ns
ASDIN/ASDIN2 hold after ABITCLK falling	t_{hold}	10	-	-	ns
ASDIN/ASDIN2 input rise/fall time	t_{rfin}	2	-	6	ns
ABITCLK rising to ASDOUT/ASYNC valid, C_L = 55 pF	t_{co}	2	-	15	ns
ASYNC/ASDOUT rise/fall time, C_L = 55 pF	t_{rfout}	2	-	6	ns

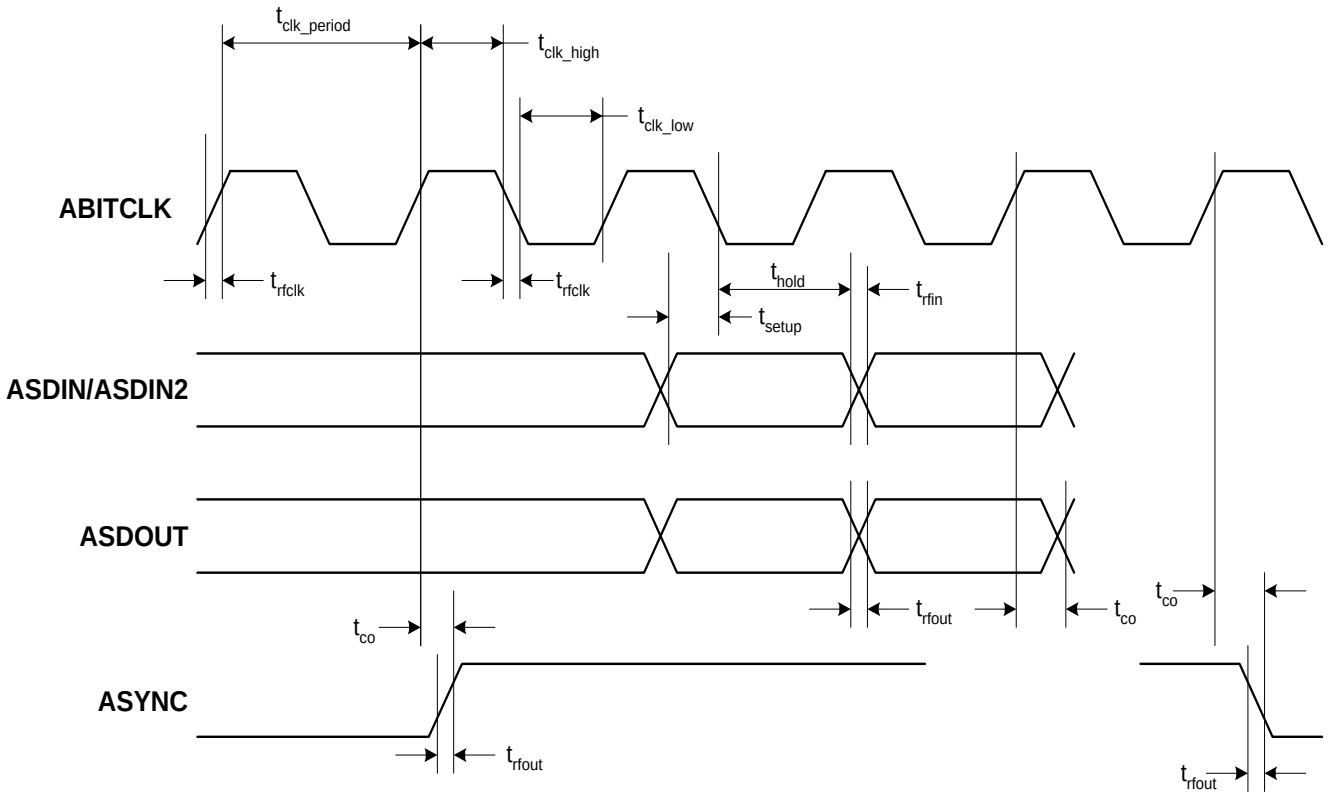


Figure 3. AC '97 Configuration Timing Diagram

EEPROM TIMING CHARACTERISTICS

Note 4. (T_A = 0 to 70 °C, PCIVDD = CVDD = VAUX = CRYVDD = 3.3 V; VDD5REF = 5 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V; PCI clock frequency = 33 MHz; unless otherwise noted)

Parameter	Symbol	Min	Max	Units
EECLK Low to EEDAT Data Out Valid	t_{AA}	0	7.0	µs
Start Condition Hold Time	$t_{HD:STA}$	5.0	-	µs
EECLK Low	t_{LEECLK}	10	-	µs
EECLK High	t_{HEECLK}	10	-	µs
Start Condition Setup Time (for a Repeated Start Condition)	$t_{SU:STA}$	5.0	-	µs
EEDAT In Hold Time	$t_{HD:DAT}$	0	-	µs
EEDAT In Setup Time	$t_{SU:DAT}$	250	-	ns
EEDAT/EECLK Rise Time (Note 18)	t_R	-	1	µs
EEDAT/EECLK Fall Time	t_F	-	300	ns
Stop Condition Setup Time	$t_{SU:STO}$	5.0	-	µs
EEDAT Out Hold Time	t_{DH}	0	-	µs

Notes: 18. Rise time on EEDAT is determined by the capacitance on the EEDAT line with all connected gates and the required external pull-up resistor.

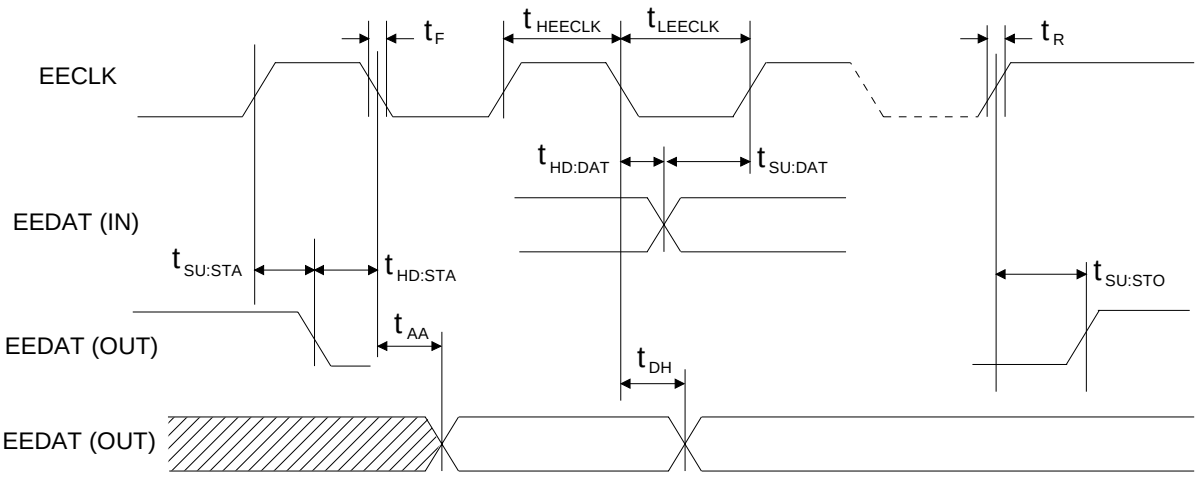


Figure 4. EEPROM Timing

OVERVIEW

The CS4281 provides a low-cost PCI audio solution with Legacy Game compatibility for the PC environment. The CS4281 is compatible with the CS4614 and CS4280-CM. The CS4281 is divided into several functional blocks.

- PCI Interface
- Sound System Interface
- FM Synthesis
- Peripheral Devices (MIDI & Gameport)

The PCI Interface is the physical connection to the bus. It is subdivided into several smaller functional groups such as: PCI configuration and interface, DMA controller, interrupt control, and chip control. The PCI interface serves as a Master/Target PCI device and its two-base address registers provide access to the chip operation registers and internal memory blocks. The Sound System Interface provides all the registers and controls to operate the entire sound system. The FM Synthesis provides full compatibility with market standard FM-based music synthesis used in DOS games and educational software. The CS4281's flexibility is further enhanced by the inclusion of peripheral devices such as Hardware Volume Control, Clock Generation, General Purpose I/O (GPIO), MIDI UART Port, Game (Joystick) Port, and the AC Link.

The DMA Engine provides dedicated hardware to manage transfer of up to 4 concurrent audio/data streams to and from host memory buffers. Four Bus Mastering DMA controllers support simultaneous capture, play, modem transmit, and modem receive.

The CS4281 supports a variety of audio I/O configurations including a single CS4297A CrystalClear AC '97 Codec or dual CS4297A codecs where the second codec is used as a portable's docking station solution. The combination of a CS4281 with a CS4298 AMC '97 codec, provides a cost-effective, superior quality, two-chip audio/modem solution.

Legacy Support

Legacy games are supported by CrystalClear Legacy Support CCLS™, DDMA, or by the PC/PCI interface. In both motherboard and add-in card designs, CCLS and DDMA provide support for legacy games by providing a hardware interface that supports a Sound Blaster Pro™ compatible interface, as well as support for FM, and joystick interfaces. These hardware interfaces provide PCI-only games compatibility for real-mode DOS and Windows DOS box support.

For motherboard designs, PC/PCI is used by connecting the PCGNT# and PCREQ# pins to the appropriate pins on the south bridge motherboard chip. The PC/PCI interface is compliant with Intel's PC/PCI spec. (version 1.2).

SYSTEM ARCHITECTURES

A typical system diagram depicting connection of the CS4281 to the CrystalClear CS4297A AC '97 Codec is given in Figure 5. All analog audio inputs and outputs are connected to the CS4297A. Audio data is passed between the CS4297A and the CS4281 over the serial AC-Link. The CS4281 provides a hardware interface for connection of a joystick and MIDI devices.

Figure 6 depicts the CS4281 using both AC '97 codec interfaces in a portable design. The primary AC '97 interface is connected to a CS4297A used for all audio I/O inside and connected to the portable. The second AC '97 interface is sent across to the docking station which contains a second CS4297A. The second codec

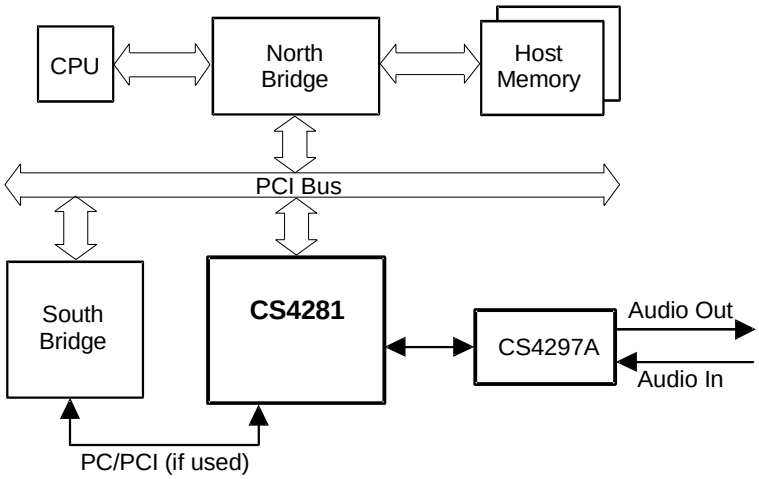


Figure 5. AC '97 Codec Interface

is activated when the portable is in the docking station. Software can disable the audio I/O paths on the portable that are superseded by docking station I/O and enable the paths needed in the docking station. Note that both interfaces are needed in systems where the CD-ROM analog input is in the portable and the Line In/Out jacks on the docking stations are used. Using the AC '97 digital link across the dock maintains the absolute highest audio quality along with a standard well-defined non-proprietary interface that will last through many system generations.

Figure 7 depicts the CS4281 using an AC '97 codec in an audio/modem design. The primary AC '97 interface is connected to a CS4298 and is used for audio/modem I/O such as Mic In, Line In, Line Out and the Analog Front End (AFE) for Modem features. The CS4298 analog interface is connected to the DAA via the EGPIO pins. The EGPIO supports the PCI Power Management Event system wake-up feature allowing a powerdown system to be powered up by an incoming call on the modem.

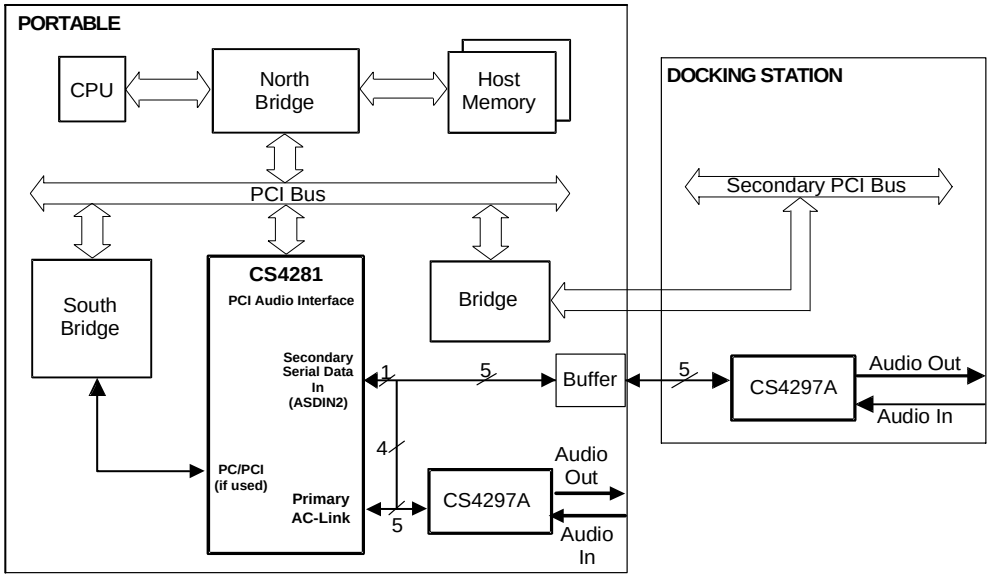


Figure 6. Portable Docking Station Scenario

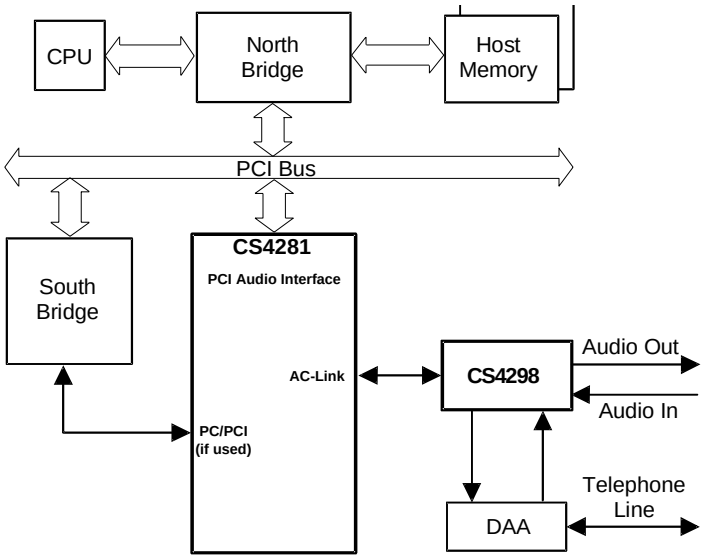


Figure 7. Modem Scenario

HOST INTERFACE

The CS4281 host interface is comprised of two separate interface blocks which are memory mapped into host address space. The interface blocks can be located anywhere in the host 32-bit physical address space. The interface block locations are defined by the addresses programmed into the two Base Address Registers in the PCI Configuration Space. These base addresses are normally set up by the system's Plug and Play BIOS. The first interface block (Base Address 0) contains the general purpose configuration, control, and status registers for the device. The second interface block (Base Address 1) maps the FIFO RAMs into host memory space. The relationship between the Base Address Registers in the CS4281 PCI Configuration Space and the host memory map is depicted in Figure 8. The bus mastering PCI bus interface complies with the PCI Local Bus Specification (version 2.1).

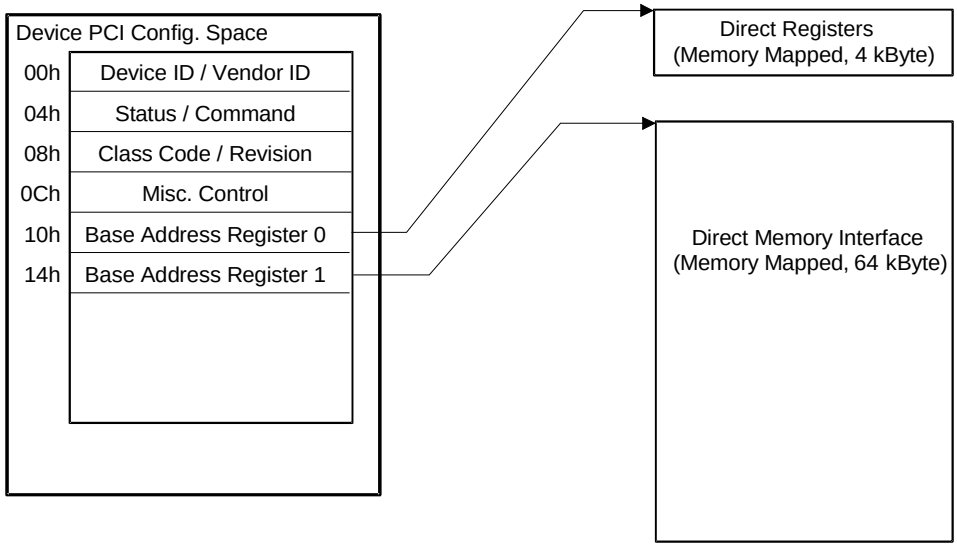


Figure 8. Host Interface Base Address Registers

PCI Bus Transactions

As a target of a PCI bus transaction, the CS4281 supports the Memory Read (from internal registers or memory), Memory Write (to internal registers or memory), Configuration Read (from CS4281 configuration registers), Configuration Write (to CS4281 configuration registers), Memory Read Multiple (aliased to Memory Read), Memory Read Line (aliased to Memory Read), and the Memory Write and Invalidate (aliased to Memory Write) transfer cycles. The I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not supported.

As a Bus Master, the CS4281 generates the Memory Read and Memory Write transactions. The Memory Read, Configuration Read, Configuration Write, Memory Read Line, Memory Write and Invalidate, I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not generated.

The PCI bus transactions supported by the CS4281 device are summarized in Table 1. Note that no Target Abort conditions are signalled by the device. Byte, word, and doubleword transfers are supported for Configuration Space accesses. Only doubleword transfers are supported for Register and Memory area accesses. Bursting is not supported for host-initiated transfers to/from the CS4281 internal register space, RAM memory space, or PCI configuration space (disconnect after first phase of transaction is completed).

Initiator	Target	Type	PCI Dir
Host	Registers (BA0)	Mem Write	In
Host	Registers (BA0)	Mem Read	Out
Host	Memories (BA1)	Mem Write	In
Host	Memories (BA1)	Mem Read	Out
Host	Config Space 1	Config Write	In
Host	Config Space 1	Config Read	Out
DMA	Host System	Mem Write	Out
DMA	Host System	Mem Read	In

Table 1. PCI Interface Transaction Summary

Configuration Space

The content and format of the PCI Configuration Space is given in Table 2. The registers from 00 to 44h are standard PCI configuration registers. The registers from E0h to FFh are Cirrus-Logic specific and are read-only by default. For protection from inadvertent writes, the Configuration Space registers from E4h to FFh are read-only unless the CWPR register at E0h is loaded with 4281h. Once CWPR contains 4281h, the registers are writable.

Subsystem Vendor ID Fields

The Subsystem ID and Subsystem Vendor ID fields can be loaded in two ways. Typically add-in cards use an external EEPROM where the CS4281 loads the data from EEPROM on power-up. For mother-board systems the BIOS typically loads the Configuration Space at offset FCh (see Table 2). Once these values are loaded they will appear in the Configuration Space offset 2Ch. The Subsystem ID and Subsystem Vendor ID fields in the PCI Configuration Space default to value 0000h. The CWPR register at E0h must be loaded with 4281h on order to write the Subsystem IDs at FCh.

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID: R/O, 6005h for CS4281		Vendor ID: R/O, 1013h		00h
Status Register, bits 15-0: Bit 15: Detected Parity Error: Error Bit Bit 14: Signalled SERR: R/O: 0 Bit 13: Received Master Abort: Error Bit Bit 12: Received Target Abort: Error Bit Bit 11: Signalled Target Abort: R/O 0 Bit 10-9: DEVSEL Timing: R/O, 01b (medium) Bit 8: Data Parity Error Detected: Error Bit Bit 7: Fast Back to Back Capable: R/O 0 Bit 6: User Definable Features: R/O 0 Bit 5: 66MHz Bus: R/O 0 Bit 4: New Capabilities: R/O 1 Bit 3-0: Reserved R/O 000 Reset Status State: 0210h Write of 1 to any error bit position clears it.		Command Register, bits 15-0: Bit 15-10: Reserved, R/O 0 Bit 9: Fast B2B Enable: R/O 0 Bit 8: SERR Enable: R/O, 0 Bit 7: Wait Control: R/O 0 Bit 6: Parity Error Response: R/W, default 0 Bit 5: VGA Palette Snoop: R/O 0 Bit 4: MWI Enable: R/O 0 Bit 3: Special Cycles: R/O 0 Bit 2: Bus Master Enable: R/W, default 0 Bit 1: Memory Space Enable: R/W, default 0 Bit 0: IO Space Enable: R/O 0		04h
Class Code: R/O 040100h Class 04h (multimedia device), Sub-class 01h (audio), Interface 00h			Revision ID: R/O 01h	08h
BIST: R/O 0	Header Type: Bit 7: R/O 0 Bit 6-0: R/O 0 (type 0)	Latency Timer: Bit 7-3: R/W,default 0 Bit 2-0: R/O 0	Cache Line Size: R/O 0	0Ch
Base Address Register 0 Device Control Register space, memory mapped. 4kByte size Bit 31-12: R/W, default 0. Compare address for register space accesses Bit 11 - 4: R/O 0, specifies 4kByte size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				10h
Base Address Register 1 Device Memory Array mapped into host system memory space, 64kByte size Bit 31-16: R/W, default 0. Compare address for memory array accesses Bit 15-4: R/O 0, specifies 64kByte size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				14h
Base Address Register 2: R/O 00000000h, Unused				18h
Base Address Register 3: R/O 00000000h, Unused				1Ch
Base Address Register 4: R/O 00000000h, Unused				20h
Base Address Register 5: R/O 00000000h, Unused				24h
Cardbus CIS Pointer: R/O 00000000h, Unused				28h

Table 2. PCI Configuration Space

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Subsystem ID R/O 0000h default, see *Subsystem ID* section		Subsystem Vendor ID R/O 0000h default, see *Subsystem ID* section		2Ch
Expansion ROM Base Address: R/O 00000000h, Unused				30h
Reserved: R/O 000000h			Cap_Ptr: R/O, 40h	34h
Reserved: R/O 00000000h				38h
Max_Lat: R/O 18h 24 × 0.25 µS = 6 µS	Min_Gnt: R/O 04h 4 × 0.25 µS = 1 µS	Interrupt Pin: R/O 01h, INTA used	Interrupt Line: R/W, default 0	3Ch
PMC Bit 15: PME# from D3cold: R/O 0 default Bit 14: PME# from D3hot: R/O 1 Bit 13: PME# from D2: R/O 1 Bit 12: PME# from D1: R/O 1 Bit 11: PME# from D0: R/O 1 Bit 10: D2 support: R/O 1 Bit 9: D1 support: R/O 1 Bit 8-6: Vaux Power: R/O 000 default Bit 5: Device Specific Init: R/O 1 Bit 4: Auxiliary Power: R/O 0 default Bit 3: PME# clock: R/O 0 Bit 2-0: Version: R/O 001		Next Item Pointer: R/O 00h	Capability ID: R/O 01h	40h
Data: R/O 0	PMCSR_BSE: R/O 0	PMCSR Bit 15: PME# status: R/W 0 Bit 14-13: Data scale: R/O 00 Bit 12-9: Data select: R/O 0000 Bit 8: PME_En: R/W 0 Bit 7-2: Reserved: R/O 000000 Bit 1-0: Power state: R/W 00		44h
Configuration Write Protect (CWPR): R/W 00000000h				E0h
Reserved				E4h
GPIO Pin Interface (GPIOR): R/W* 00000000h				E8h
Serial Port Power Management & Control (SPMC): R/W* 00000000h				ECh
Configuration Load Register (CFLR): R/W* 00000000h default†				F0h
BIOS Flags: R/W* 00h	ISA IRQC: R/W* 00h	ISA IRQB: R/W* 00h	ISA IRQA: R/W* 00h	F4h
Reserved				F8h
Subsystem ID: R/W* 0000h default†, see *Subsystem ID* section		Subsystem Vendor ID: R/W* 0000h default†, see *Subsystem ID* section		FCh

* Write capability controlled by CWPR setting.

† Power-up values could be loaded from external EEPROM.

Table 2. PCI Configuration Space *(cont.)*

Cirrus-Specific Configuration Registers

Configuration Space locations E0h through FFh are Cirrus-specific registers and are only listed in the PCI specification as *vendor-defined*. E0h is the *Configuration Write Protect* register (CWPR) and blocks registers E4h through FFh from being written (they are read-only), when the CWPR register is anything but 4281h. When CWPR is programmed for 4281h, registers E4h through FFh are writable. This section will describe the Cirrus-specific Configuration registers with the exception of the Subsystem ID register at FCh which was described in the last section.

The Cirrus-specific registers provide the BIOS with access to general setup and configuration options of the CS4281. Placing these registers in the Configuration Space lets the BIOS configure the CS4281 before any operating system has assigned memory base addresses. Some general-purpose bits are also available to allow the BOIS to communicate with the CS4281 driver software. Cirrus Logic must be contacted before using any of these general-purpose bits when using Cirrus-supplied software drivers.

General Purpose I/O Register (GPIOR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GP3W	GP3ST	GP3PT	GP3OE	GP1W	GP1ST	GP1PT	GP1OE	VUPW	VUPST	VUPPO	VUPLT	VDNW	VDNST	VDNPO	VDNLT
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				GP3D	GP1D					GPPS	GPSS	GP3S	GP1S	VUPS	VDNS

Address: PCI CFG: E8h, Read-Write if CWPR configured, otherwise Read-Only

Definition: The General Purpose I/O register provides a host port for accessing extended general-purpose I/O pins.

Bit Descriptions:

VDNS — VOLDN input Status: This bit reflects the status of the VOLDN input pin. If configured as sticky (VDNST=1), VDNS reads one when the VOLDN pin goes active (edge sensitive - edge defined by polarity bit VDNPO), and is cleared by writing a 0 to VDNS.
If configured as level sensitive (VDNST=0), this bit reflects the current state of the VOLDN pin qualified by the polarity bit VDNPO.

VUPS — VOLUP input Status: This bit reflects the status of the VOLUP input pin. If configured as sticky (VUPST=1), VUPS reads one when the VOLUP pin goes active (edge sensitive - edge defined by polarity bit VUPPO), and is cleared by writing a 0 to VUPS.
If configured as level sensitive (VUPST=0), this bit reflects the current state of the VOLUP pin qualified by the polarity bit VUPPO.

GP1S — ASDIN2/GPIO1 input Status: Assuming this pin is not configured for ASDIN2, this bit reflects the status of the ASDIN2/GPIO1 pin. If ASDIN2/GPIO1 is an output, this bit reflects the actual state of the pin. If ASDIN2/GPIO1 is an input:
If configured as sticky (GP1ST=1), this bit reads one when the ASDIN2/GPIO1 pin goes active (edge sensitive - edge defined by polarity bit GP1PT), and is cleared by writing a 0 to GP1S.
If configured as level sensitive (GP1ST=0), this bit reflects the current state of the ASDIN2/GPIO1 pin qualified by the polarity bit GP1PT.
See the *Serial Port Power Management Control* (SPMC) register description of ASDI2E bit.

GP3S — GPIO3 input Status: This bit reflects the status of the GPIO3 pin itself. If GPIO3 is an output, this bit reflects the actual state of the pin. If GPIO3 is an input:
If configured as sticky (GP3ST=1), this bit reads one when the GPIO3 pin goes active (edge sensitive - edge defined by polarity bit GP3PT), and is cleared by writing a 0 to GP3S.
If configured as level sensitive (GP3ST=0), this bit reflects the current state of the GPIO3 pin qualified by the polarity bit GP3PT.

GPSS GP_INT input Secondary Status. A general purpose input pin on the Secondary Codec (ASDIN2) caused AC-Link slot 12, GP_INT to set. Writing GPSS = 0 clears the locally stored copy; however, since the interrupt condition occurred in the Secondary Codec, the condition must be removed through the Secondary Codec GPIO Pin Sticky register, Index 54h.

GPPS GP_INT input Primary Status. A general purpose input pin on the Primary Codec caused AC-Link slot 12, GP_INT to set. Writing GPPS = 0 clears the locally stored copy; however, since the interrupt condition occurred in the Primary codec, the condition must be removed through the Primary Codec GPIO Pin Sticky register, Index 54h.

GP1D GPIO1 output data. When ASDIN2/GPIO1 is not ASDIN2 and is configured as an output (GP1OE = 1), writes to this bit are presented on the ASDIN2/GPIO1 pin.

GP3D GPIO3 output data. When configured as an output (GP3OE = 1), writes to this bit are presented on the GPIO3 pin. Note that in backward-compatible sockets, this pin is a PCI power supply pin.

VDNLT Volume Down Load/Type. Function dependent on whether hardware volume is enabled.
Hardware Volume Control Enabled:
0 - GPIO logic input reflects the pin status directly
1 - GPIO logic input is pulse from Down hardware volume control logic. When a hardware volume change is generated from VOLDN, a pulse is sent to this GPIO input.
Hardware Volume Control Disabled:
0 - Enable VOLDN pin pullup
1 - Disable VOLDN pin pullup

VDNPO Volume Down input Polarity.
0 - active low
1 - active high

VDNST Volume Down input Sticky.
1 - VOLDN input pin is latched, for edge sensitive inputs, and presented on the VNDS bit. The VDNS bit is cleared by writing a 0 to VDNS.
0 - VOLDN input pin (after VNDPO) is presented on VDNS bit for level sensitive inputs.

VDNW Volume Down Wake. When set, VOLDN can cause a wake-up event (asserts PME#). VDNST must be set sticky for this bit to be effective.

VUPLT Volume Up Load/Type. Function dependent on whether hardware volume is enabled.
Hardware Volume Control Enabled:
0 - GPIO logic input reflects the pin status directly
1 - GPIO logic input is pulse from Up hardware volume control logic. When a hardware volume change is generated from VOLUP, a pulse is sent to this GPIO input.
Hardware Volume Control Disabled:
0 - Enable VOLUP pin pullup
1 - Disable VOLUP pin pullup

VUPPO Volume Up input Polarity.
0 - active low
1 - active high

VUPST Volume Up input Sticky.
1 - VOLUP input pin is latched, for edge sensitive inputs, and presented on the VUPS bit. The VUPS bit is cleared by writing a 0 to VUPS.
0 - VOLUP input pin (after VUPPO) is presented on VUPS bit for level sensitive inputs.

VUPW Volume Up Wake-up. When set, VOLUP can cause a wake-up event (asserts PME#). VUPST must be set sticky for this bit to be effective.

GP1OE Output Enable ASDIN2/GPIO1. When this pin is not configured as ASDIN2, setting this bit enables the output buffer allowing writes to the GP1D bit to be presented on the pin.
0 - Output disabled, pin is configured as an input (reset default)
1 - Output enabled

GP1PT GPIO1 input Polarity/output Type. When ASDIN2/GPIO1 is not configured as ASDIN2:
When ASDIN2/GPIO1 pin is configured as an input (GP1OE = 0), this bit sets the polarity.
0 - active low input
1 - active high input
When ASDIN2/GPIO1 pin is configured as an output (GP1OE = 1), this bit sets the type
0 - CMOS output
1 - open drain output

GP1ST GPIO1 input Sticky. Assumes GP1OE = 0 and pin not configured for ASDIN2.
1 - GPIO1 input pin is latched, for edge sensitive inputs, and presented on the GP1S bit. The GP1S bit is cleared by writing a 0 to GP1S.
0 - GPIO1 input pin (after GP1PT) is presented on GP1S bit for level sensitive inputs.

GP1W GPIO1 Wake. When set, GPIO1 can cause a wake-up event (asserts PME#). GP1ST must be set sticky for this bit to be effective and the pin must not be configured for ASDIN2.

GP3OE Output Enable GPIO3: Setting this bit enables the output buffer allowing writes to the GP3D bit to be presented on the GPIO3 pin. Note that in backwards-compatible sockets, this pin is a PCI power supply pin.
0 - Output disabled, pin is configured as an input (reset default)
1 - Output enabled

GP3PT GPIO3 input Polarity/output Type.
When the GPIO3 pin is configured as an input (GP3OE = 0), this bit sets the polarity.
0 - active low input
1 - active high input
When the GPIO3 pin is configured as an output (GP3OE = 1), this bit sets the type
0 - CMOS output
1 - open drain output

GP3ST GPIO3 input Sticky. Assumes GP3OE = 0.
1 - GPIO3 input pin is latched, for edge sensitive inputs, and presented on the GP3S bit. The GP3S bit is cleared by writing a 0 to GP3S.
0 - GPIO3 input pin (after GP3PT) is presented on GP3S bit for level sensitive inputs.

GP3W GPIO3 Wake. When set, GPIO3 can cause a wake-up event (asserts PME#). GP3ST must be set sticky for this bit to be effective.

Serial Port Power Management Control (SPMC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GIPPEN	GISPEN					EESPD	ASDI2E	res				WUP2	WUP1	ASYN	RSTN

Address: PCI CFG: ECh, Read-Write if CWPR configured, otherwise Read-Only

Definition: Supports power management of the AC Link and the enable for ASDIN2. This register is unaffected by the PCI RST# signal.

Bit Descriptions:

RSTN Reset NOT!: This bit controls the ARST# pin. Note the negative sense of the bit, which matches the active low output pin definition. The ARST# pin is a logical OR of RSTN with the PCI reset pin RST#.
0 = ARST# active, AC-Link and Codec reset (reset default)
1 = ARST# inactive, AC-Link and Codec not reset (normal operation).

ASYN Asynchronous ASYNC Assertion: This bit allows the unclocked assertion of the ASYNC pin for AC-Link management protocol requirements.
0 = Normal ASYNC generation (reset default)
1 = Force ASYNC high

WUP1 Wakeup for primary input: This bit indicates that a Codec attached to the ASDIN pin signaled a wake-up event by forcing a low-to-high transition on ASDIN while the AC-Link is down. This bit remains set until host driver software issues a warm reset of the AC-Link by setting the ASYN bit; specifically, the falling edge of the ASYNC warm reset pulse clears this bit.
0 = No wake-up event signaled by ASDIN
1 = Wake-up event signaled by ASDIN

WUP2 Wakeup for secondary input: This bit indicates that a Codec attached to the ASDIN2 pin signaled a wake-up event by forcing a low-to-high transition on ASDIN2 while the AC-Link is down. This bit remains set until host driver software issues a warm reset of the AC-Link by setting the ASYN bit; specifically, the falling edge of the ASYNC warm reset pulse clears this bit.
0 = No wake-up event signaled ASDIN2
1 = Wake-up event signaled by ASDIN2

GIPPEN GP_INT Primary PME# Enable for primary ASDIN2 Slot 12 data. When set, allows Primary Codec's slot 12 to generate a PME event when GP_INT goes from 0 to a 1.

GISPEN GP_INT Secondary PME# Enable for secondary ASDIN2 Slot 12 data. When set, allows the Secondary Codec to generate a PME event when GP_INT goes from 0 to a 1.

EESPD EEPROM Serial Port Disable. When set, the EEPROM engine is disabled and does NOT try and read the EERPOM on a power-on reset. The two EEPROM pins are also disconnected from the EEPROM engine. When clear, the EEPROM engine is enabled and goes out on the EEPROM port and tries to read the EEPROM after a power-on reset.

ASDI2E ASDIN2 Enable.
0 = ASDIN2 function disabled (reset default) (converts to extended GPIO1).
1 = ASDIN2 function enabled (implies a Secondary Codec is attached)

Configuration Load Register (CFLR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CB37	CB36	CB35	CB34	CB33	CB32	CB31	CB30	CB27	CB26	CB25	CB24	CB23	CB22	CB21	CB20
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB17	CB16	CB15	CB14	CB13	CB12	CB11	CB10	CB07	CB06	CB05	CB04	CB03	CB02	CB01	CB00

Address: PCI CFG: F0h, Read-Write if CWPR configured, otherwise Read-Only

Definition: The Configuration Load Register provides a host port for reading of four bytes of device configuration options from EEPROM. The BIOS can pre-load this register by writing to it in configuration space. The following bit descriptions are for driver information only as these bits have no direct hardware affect. When using the Cirrus software drivers, contact Cirrus before using any of these bits as they may have pre-defined meanings.

Bit Descriptions:

CB0[7:0] This bit field returns the first configuration byte.

CB1[7:0] This bit field returns the second configuration byte.

CB2[7:0] This bit field returns the third configuration byte

CB3[7:0] This bit field returns the fourth configuration byte.

ISA Interrupt Select Register (IISR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAUXS	VAC2	VAC1	VAC0	AUXP	BCF2	BCF1	BCF0	GTD				IRQC3	IRQC2	IRQC1	IRQC0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				IRQB3	IRQB2	IRQB1	IRQB0					IRQA3	IRQA2	IRQA1	IRQA0

Address: PCI CFG: F4h, Read-Write if CWPR configured, otherwise Read-Only

Definition: Defines the ISA interrupt associated with a particular pin and relays flags from BIOS to the OS and host software. This register is unaffected by the PCI RST# signal.

Bit Descriptions:

VAUXS Vaux Support. This bit is reflected into the $D3_{cold}$ support bit, PMC.PMD3C. BIOS code would generally set this bit if VAUX is supported.

VAC[2:0] Vaux Current. These bits are reflected in the PMC.VAC[2:0] bits and must be initialized by the BIOS to indicate how much current Vaux pulls. Note this is total current and is the combined CS4281 and any attached Codecs and external logic using Vaux.
000 - 0 mA (self powered/don't support Vaux)
001 - 55 mA
010 - 100 mA
011 - 160 mA
100 - 220 mA
101 - 270 mA
110 - 320 mA
111 - 375 mA (spec maximum)

AUXP Auxiliary Power. This bit is reflected in the PMC.AUXP bit.

BCF[2:0] BIOS Configuration Flags. These bits have no direct affect on the operation of the CS4281 and may be used by host software when communicating with the BIOS.

GTD Global Trapping Disable. When set, disables all I/O trapping. When GTD is clear, I/O trapping is allowed (must be configured through other registers).

IRQA[3:0] IRQA pin interrupt mapping. A 0 disables (high impedance) the corresponding ISA interrupt pin. A non-zero value (preferably the actual ISA interrupt connected to the pin) allows the pin to be enabled through software drivers.

IRQB[3:0] IRQB pin interrupt mapping. A 0 disables (high impedance) the corresponding ISA interrupt pin. A non-zero value (preferably the actual ISA interrupt connected to the pin) allows the pin to be enabled through software drivers.

IRQC[3:0] IRQC pin interrupt mapping. A 0 disables (high impedance) the corresponding ISA interrupt pin. A non-zero value (preferably the actual ISA interrupt connected to the pin) allows the pin to be enabled through software drivers.

Interrupt Signal

The CS4281 PCI Interface includes an interrupt controller function which receives interrupt requests from multiple sources within the CS4281 device, and presents a single interrupt line (INTA) to the host system. Interrupt control registers in the CS4281 provide the host interrupt service routine with the ability to identify the source of the interrupt and to clear the interrupt sources.

ISA interrupts are provided for real-mode DOS support. The three ISA interrupt pins are high-impedance when the CS4281 powers up. The output enables for a particular ISA interrupt are a combination of bits set by the BIOS and an interrupt enable bit controlled by start-up configuration software.

AC '97 LINK

The CrystalClear solution includes a CS4281 plus a CS4297A. The CS4281 communicates with the CS4297A over the AC-Link as specified in the Intel® Audio Codec '97 Specification (version 2.1). A block diagram for the AC '97 Controller configuration is given in Figure 5. The signal connections between the CS4281 and the AC '97 Codec are indicated in Figure 9.

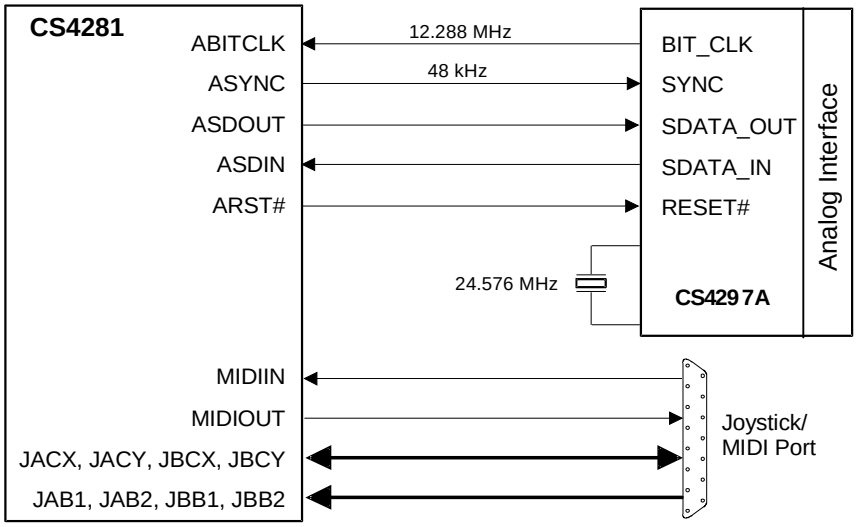


Figure 9. Single AC '97 Codec Connection Diagram

The dual codec architecture of AC '97, version 2.1, is supported wherein the second codec uses the same pins from the primary, with the exception of a separate serial data-in line (ASDIN2) illustrated in Figure 10. The Primary Codec is the timing master for the digital audio link and the CS4281. The ASDOUT output supports data transmission on nine of the output sample slots (output slots 3 - 11). The ASDIN and ASDIN2 inputs support receiving of audio sample data on nine of the input sample slots (input slots 3 - 11).

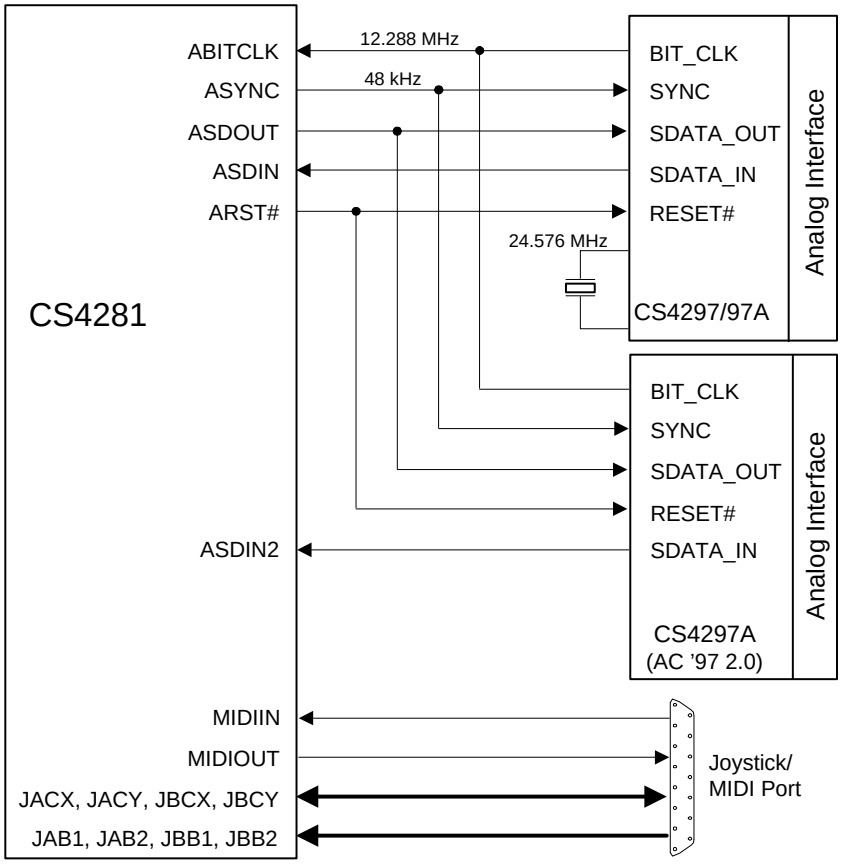


Figure 10. Dual AC '97 Codec Connection Diagram

MIDI PORT

A bi-directional MIDI interface allows connection of external MIDI devices. The MIDI interface includes a 16-byte FIFO for the MIDI receive path. A MIDI buffer (see Figure 11) is recommended due to some joystick manufactures grounding the MIDIOUT pin.

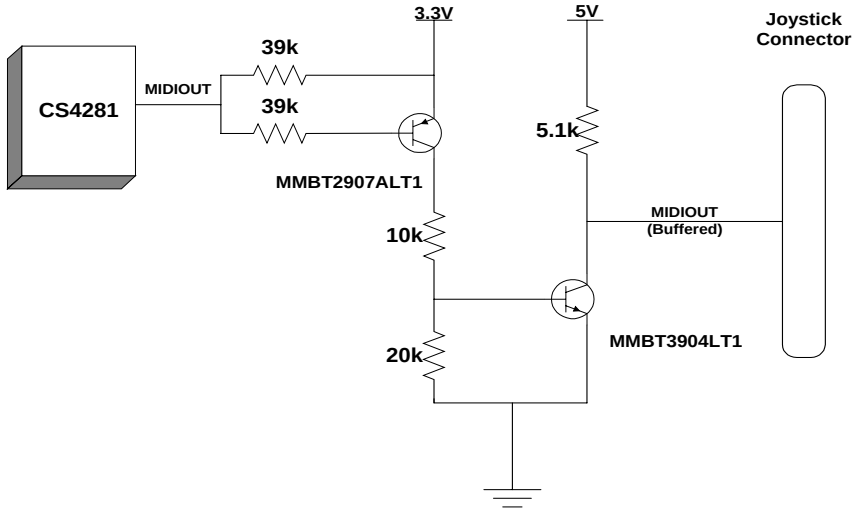


Figure 11. MIDIOUT Buffer

JOYSTICK PORT

The joystick port supports four "coordinate" channels and four "button" channels. The coordinate channels provide joystick positional information to the host, and the button channels provide user button event information. The Joystick schematic is illustrated in Figure 12.

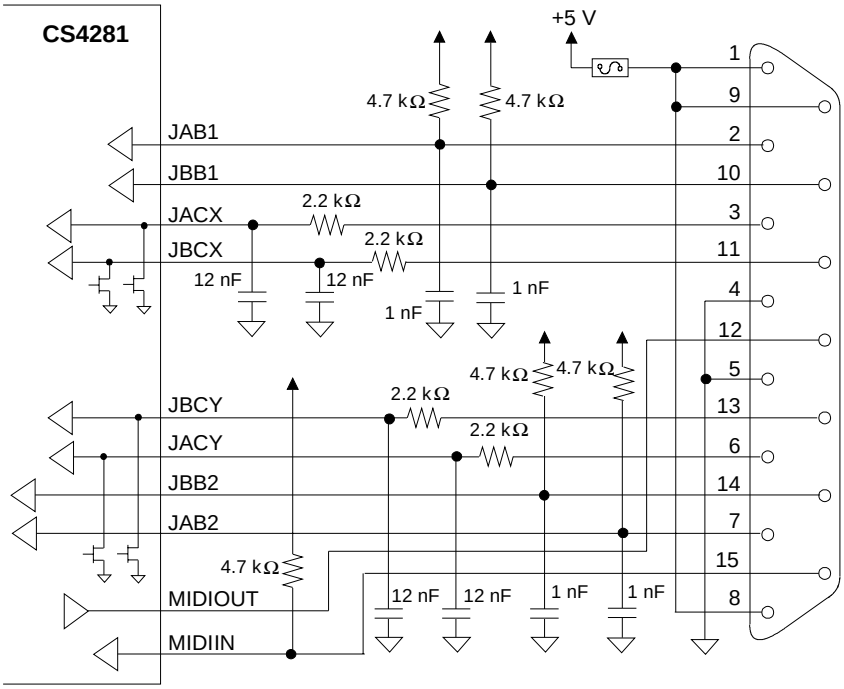


Figure 12. Joystick Logic

EEPROM INTERFACE

The EEPROM configuration interface allows the connection of an optional external EEPROM device to provide power-up configuration information. The external EEPROM is not required for proper operation; however, in some applications power-up configuration settings other than the default values may be required to support specific Operating System compatibility requirements.

After a hardware reset, an internal state machine in the CS4281 will automatically detect the presence of an external EEPROM device. If the EEPROM header is correct, then EEPROM data is loaded into the Subsystem ID and Subsystem Vendor ID fields at FCh in Configuration Space, along with four bytes of general configuration information loaded into the CFLR register in Configuration Space. If the header data is invalid, the data transfer is aborted. After power-up, the host can read or write from/to the EEPROM device by accessing specific registers in the CS4281. Cirrus Logic provides software to read and write the EEPROM.

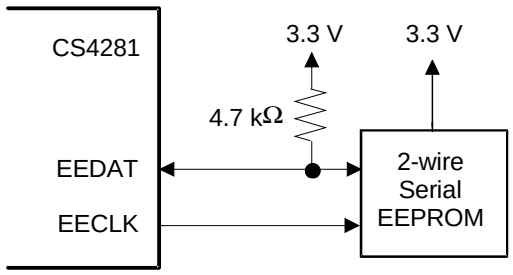


Figure 13. External EEPROM Connection

The two-wire interface for the optional external EEPROM device is depicted in Figure 13. During data transfers, the data line (EEDAT) can change state only while the clock signal (EECLK) is low. A state change of the data line while the clock signal is high indicates a start or stop condition to the EEPROM device.

The EEPROM device read access sequence is shown in the Figure 14. The timing follows that of a random read sequence. The CS4281 first performs a "dummy" write operation, then generates a start condition followed by the slave device address and the byte address of zero. The CS4281 always begins access at byte address zero and continues access a byte at a time, using a sequential read, until all needed bytes in the EEPROM are read. Since only 9 bytes are needed, the smallest EEPROM available will suffice.

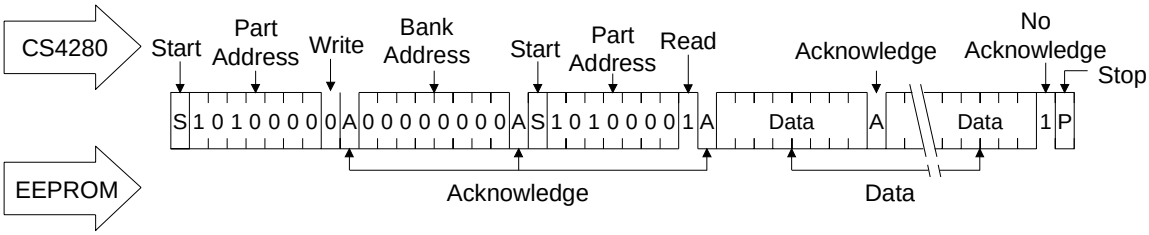
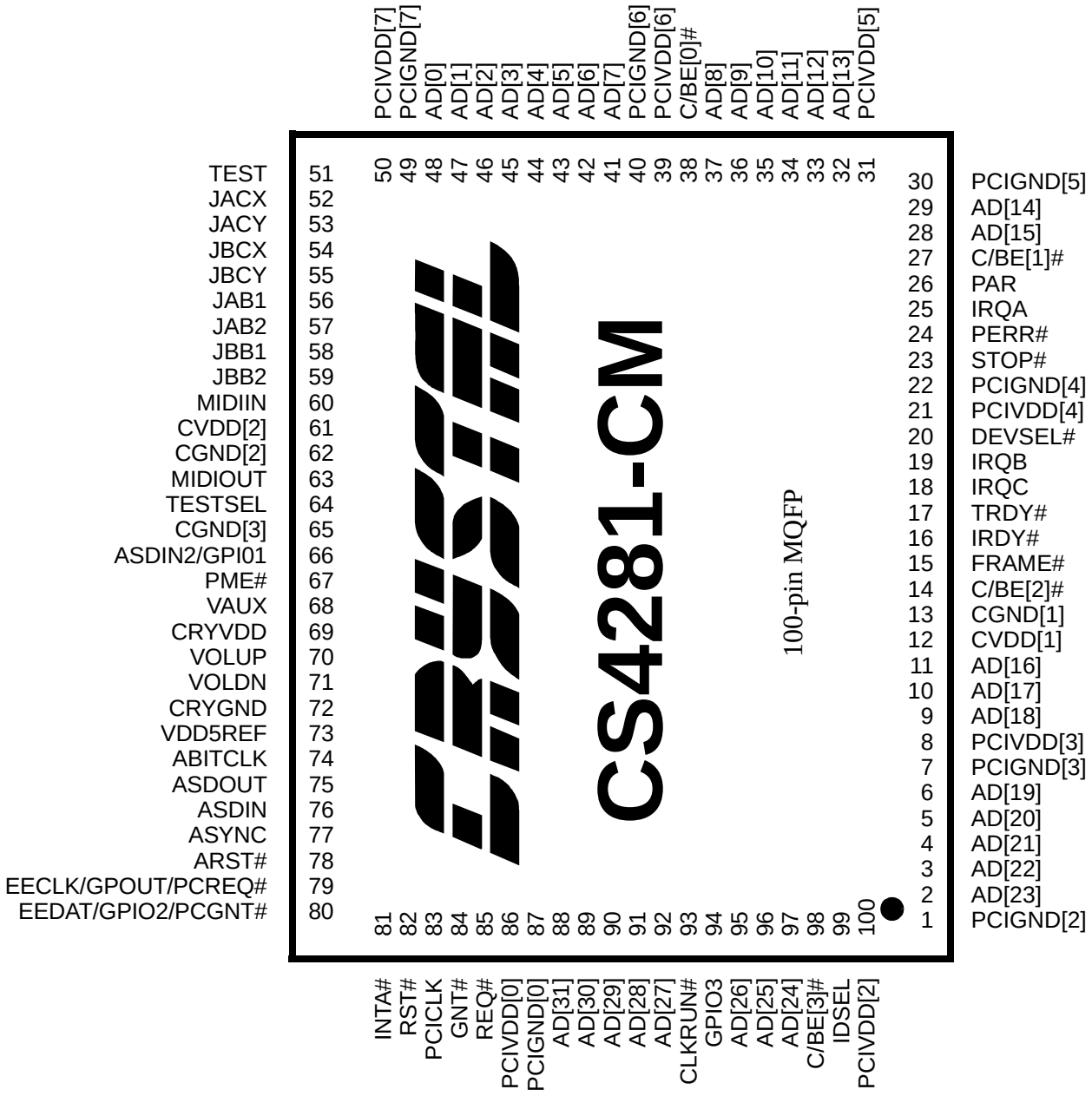


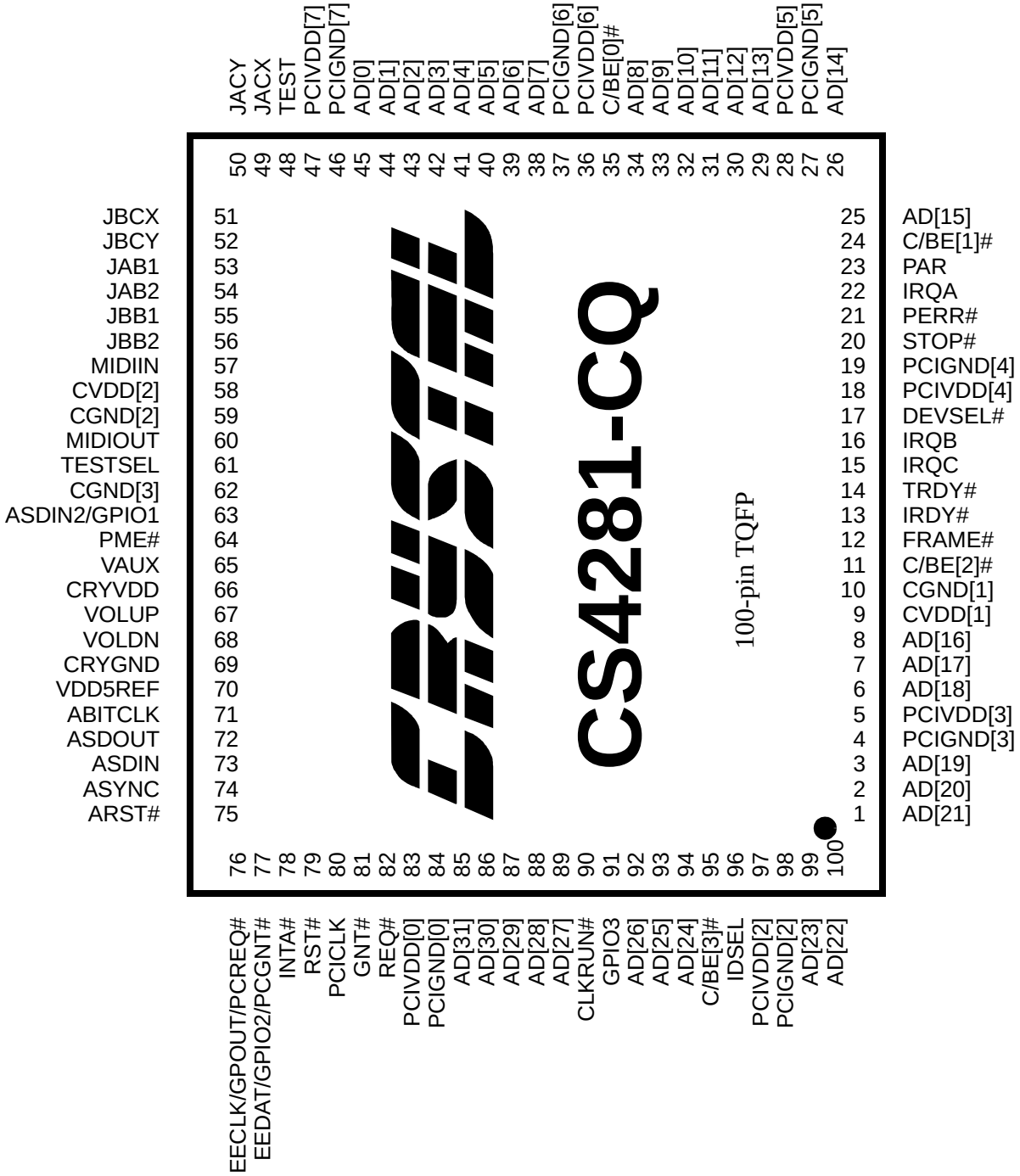
Figure 14. EEPROM Read Sequence

GENERAL PURPOSE I/O PINS

Some CS4281 pins are internally multiplexed to serve different functions depending on the CS4281 driver. The CS4281 general purpose functionality includes PME# assertion and interrupt functionality. Please contact Cirrus Logic's PC Audio support group for more information on the flexibility of the CS4281 GPIO pins.

PIN DESCRIPTION





A '#' sign suffix on a pin names indicates an active-low signal.

PCI Interface

AD[31:0] - Address/Data Bus, I/O

These pins form the multiplexed address / data bus for the PCI interface.

C/BE[3:0]# - Command Type / Byte Enables, I/O

These four pins are the multiplexed command / byte enables for the PCI interface. During the address phase of a transaction, these pins indicate cycle type. During the data phases of a transaction, active low byte enable information for the current data phase is indicated. These pins are inputs during slave operation and they are outputs during bus mastering operation.

PAR - Parity, I/O

The Parity pin indicates even parity across AD[31:0] and C/BE[3:0] for both address and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.

FRAME# - Cycle Frame, I/O

FRAME# is driven by the current PCI bus master to indicate the beginning and duration of a transaction.

IRDY# - Initiator Ready, I/O

IRDY# is driven by the current PCI bus master to indicate that the initiator is ready to transmit or receive data (complete the current data phase).

TRDY# - Target Ready, I/O

TRDY# is driven by the current PCI bus target to indicate that the target device is ready to transmit or receive data (complete the current data phase).

STOP# - Transition Stop, I/O

STOP# is driven active by the current PCI bus target to indicate a request to the master to stop the current transaction.

IDSEL - Initialize Device Select, Input

IDSEL is used as a chip select during PCI Configuration Space read and write cycles.

DEVSEL# - Device Select, I/O

DEVSEL# is driven by the PCI bus target device to indicate that it has decoded the address of the current transaction as its own chip select range.

REQ# - Master Request, Three-State Output

REQ# indicates to the system arbiter that the CS4281 is requesting access to the PCI bus. This pin is high-impedance when RST# is active.

GNT# - Master Grant, Input

GNT# is driven by the system arbiter to indicate that CS4281 owns the PCI Bus.

PERR# - Parity Error, I/O

PERR# is used for reporting data parity errors on the PCI bus.

INTA# - Host Interrupt A, Open Drain Output

INTA# is the level triggered interrupt pin dedicated to servicing internal device interrupt sources.

PCICLK - PCI Bus Clock, Input

PCICLK is the PCI bus clock for timing all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.

RST# - PCI Device Reset, Input

RST# is the PCI bus master reset.

VDD5REF - Clean 5 V Power Supply

VDD5REF is the power connection pin for the 5 V PCI pseudo supply for the PCI bus drivers. The internal core logic runs on 3.3 Volts. This pin enables the PCI interface to support and be tolerant of 5 Volt signals. For a 5 Volt PCI Bus, VDD5REF must be connected to +5 Volts.

PCIVDD[7:2,0] - PCI Bus Driver Power Supply

PCIVDD pins are the PCI driver power supply pins. These pins must have a nominal +3.3 Volts.

PCIGND[7:2,0] - PCI Bus Driver Ground Pins

PCIGND pins are the PCI driver ground reference pins.

PME# - PCI Power Management Event, Open Drain, Output

PME# signals a PCI Power Management event. This pin powers up high impedance for backwards compatibility. It is also backwards compatible since the previous function was a ground pin. PME# functionality is powered from the VAUX power supply to support $D3_{cold}$ wake-up from the AC Link.

CLKRUN# - Optional System Clock Control, I/O, Open Drain

CLKRUN# is an optional PCI signal defined for mobile operations. As an input, high indicates that the PCICLK is active. The bus controller drives CLKRUN# low when it wants to stop the PCICLK. As an output, driven low to request that the PCICLK be activated or not stopped. If not used, this pin must have a weak pull-down attached to keep low. This pin is backwards compatible since the previous function was a ground pin.

VAUX - PCI Auxiliary Power Supply, Power

Auxiliary 3.3 Volt VDD pin used to maintain limited device funcitonality when the normal VDD is turned off. This pin is backwards compatible since the previous function was a core power supply pin with the same voltage.

External Interface Pins

TEST - Test Mode, Input

This pin must be tied to ground.

TESTSEL - Test Mode Select, Input with Pullup

This pin must be left floating or tied to a core power supply pin for normal operation.

EEDAT/GPIO2/PCGNT# - EEPROM Data Line / PC/PCI Grant, I/O

For expansion card designs, this is the data line for external serial EEPROM containing device configuration data. When used with an external EEPROM, a 4.7 kΩ pullup resistor is required. In motherboard designs using PC/PCI, this pin is the PC/PCI serialized grant input. In designs with neither of the above requirements, this pin can be used as a general purpose input or open drain output (GPIO2).

EECLK/GPOUT/PCREQ# - EEPROM Clock Line / PC/PCI Request, Output

For expansion card designs, this is the clock line for external serial EEPROM containing device configuration data. In motherboard designs using PC/PCI, this pin is the PC/PCI serialized request output. In designs with neither of the above requirements, this pin can be used as a general purpose output pin (GPOUT).

GPIO3 - General Purpose Input/Output 3, I/O

A general purpose I/O pin that is powered off the PCI power supply. Therefore, this pin does not support PME# control from the AC link during $D3_{cold}$. This pin powers up in a high impedance state providing backward compatibility. All general purpose I/O left unused must be tied high through its own 10 kΩ resistor.

VOLUP - Volume-Up Button, Input

This pin is the volume-up button control input. This pin may also be used as a general purpose input if its primary function is not needed. Due to the internal 20 kΩ pull-up resistor, if VOLUP is unconnected, it will be pulled to its inactive state.

VOLDN - Volume-Down Button, Input

This pin is the volume-down button control input. This pin may also be used as a general purpose input if its primary function is not needed. Due to the internal 20 kΩ pull-up resistor, if VOLDN is unconnected, it will be pulled to its inactive state.

Clock / Miscellaneous

IRQ[A:C] - ISA interrupt pins, Outputs

These pins can be used in DOS legacy-compatibility mode to bypass the PCI interrupt and use an ISA interrupt directly. Using these pins can preserve the multi-drop capability of the PCI interrupt at the expense of another interrupt line. These pins power up high impedance for backwards compatibility.

CRYVDD - DLL Power Supply

Power pin for internal delay-locked loop. This pin must be connected to a nominal +3.3 Volts.

CRYGND - DLL Ground Supply

Ground pin for internal delay-locked loop.

JACX, JACY, JBCX, JBCY - Joystick A and B X/Y Coordinates, I/O

These pins are the 4 axis coordinates for the joystick port.

JAB1, JAB2, JBB1, JBB2 - Joystick A and B Button Inputs, Input

These pins are the 4 button switch inputs for the joystick port.

MIDIIN - MIDI Data Input

This is the serial input pin for the internal MIDI port. An internal 20 kΩ pull-up resistor will pull MIDIIN to CVDD.

MIDIOUT - MIDI Data Output

This is the serial output pin for the internal MIDI port.

CVDD[2:1] - Core Power Supply

Core power pins. These pins must be connected to a nominal +3.3 Volts.

CGND[3:1] - Core Ground Supply

Core digital ground reference pins.

Serial Codec Interface

ABITCLK - AC-Link Bit Clock, Input

Master timing clock for serial audio data. This pin is an input which drives the timing for the AC-Link interface, along with providing the source clock for the CS4281.

ASYNC - AC-Link Frame Sync, Output

Framing clock for serial audio data. This pin is an output which indicates the 48 kHz framing for the AC-Link. High during slot 0 and low for slots 1 through 12. Also used to induce a warm reset of the AC-Link when its down.

ASDOUT - AC-Link Data Out, Output

CS4281 serial data out. Provides a register interface and playback audio data path to both the Primary and Secondary Codecs.

ARST# - AC-Link Reset, Output, Active Low

AC-Link and Codec reset pin. This pin is the logical OR of the PCI reset pin RST# and the software controlled RSTN bit in the SPMC register. When low, forces all Codecs attached to the AC Link into a cold reset state.

ASDIN - Primary Codec Data In, Input

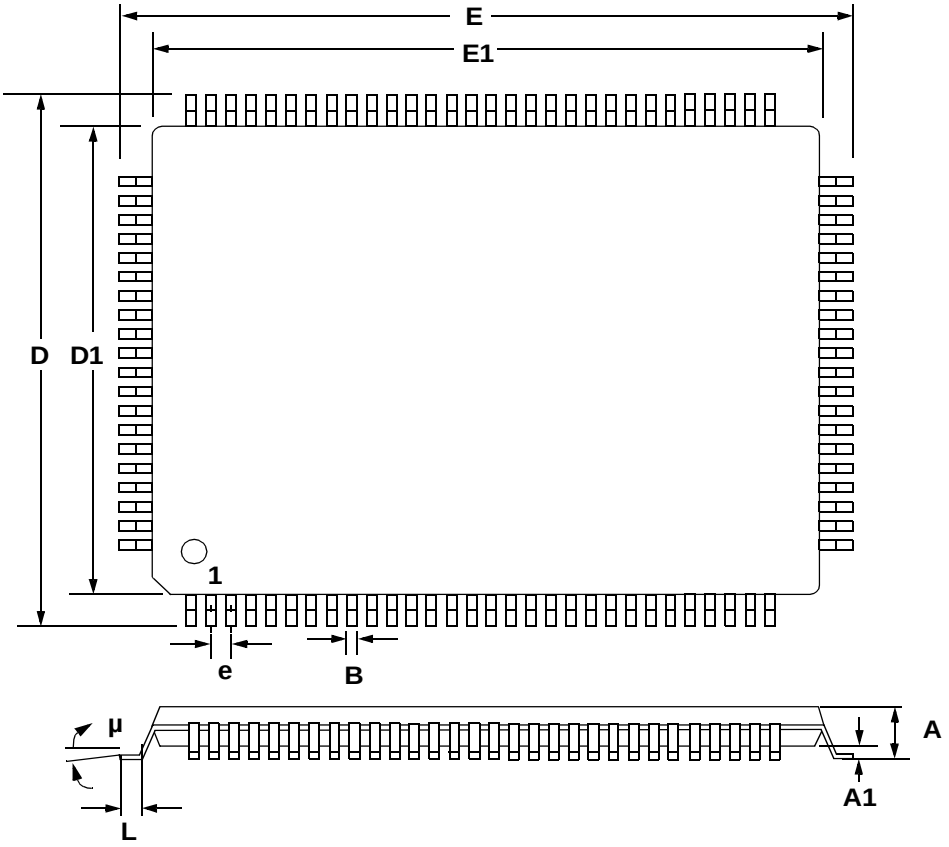
Primary Codec's serial data input to the CS4281 for register reads and capture audio data streams. This pin is powered from the VAUX power pin to support wake-up events that drive PME#.

ASDIN2/GPIO1 - Secondary Codec Data In, Input / General Purpose I/O Pin 1

Secondary Codec's serial data input to the CS4281 or general purpose input, selected via the *Serial Power Management Control* (SPMC) register. This pin is powered from the VAUX power pin to support wake-up events that drive PME#. As a general purpose I/O pin, it supports extended capability and PME# (powered from VAUX). If this pin is not used, it should have an external resistor of 50 kΩ or greater attached to ground (not power).

PACKAGE OUTLINE

100-PIN MQFP PACKAGE DRAWING

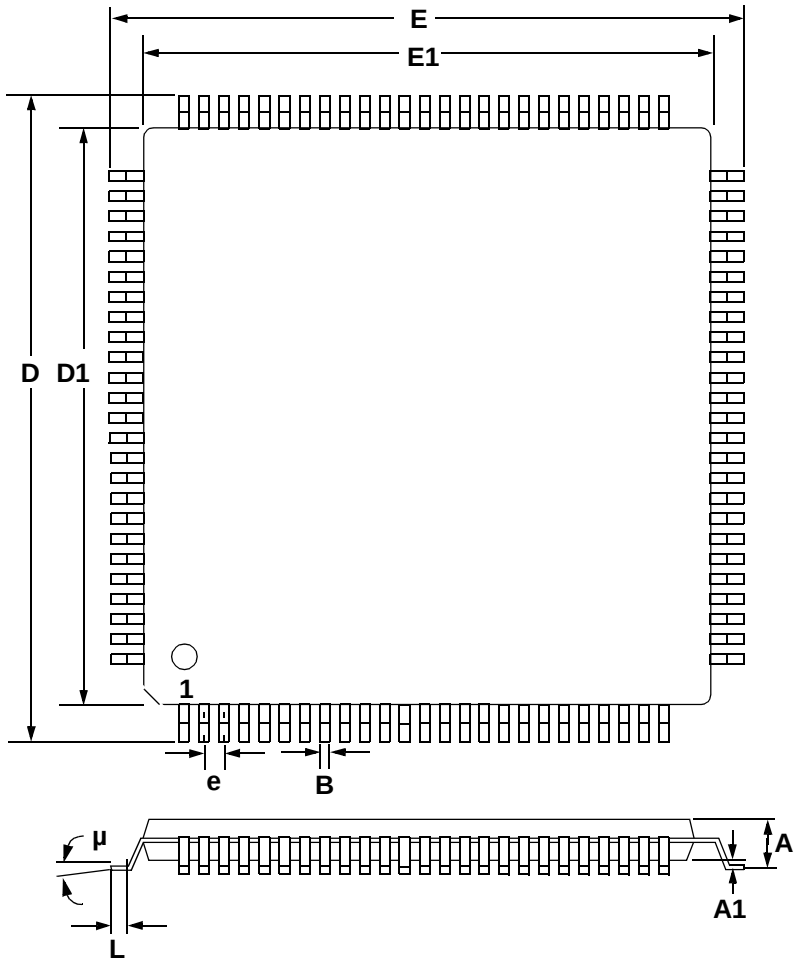


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.134	----	3.400
A1	0.010	0.014	0.250	0.350
B	0.009	0.015	0.220	0.380
D	0.667	0.687	16.950	17.450
D1	0.547	0.555	13.900	14.100
E	0.904	0.923	22.950	23.450
E1	0.783	0.791	19.900	20.100
e*	0.022	0.030	0.550	0.750
μ	0.000°	7.000°	0.000°	7.000°
L	0.018	0.030	0.450	0.750

* Nominal pin pitch is 0.65 mm

Controlling dimension is mm.
JEDEC Designation: MS022

100-PIN TQFP PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.063	----	1.600
A1	0.002	0.006	0.050	0.150
B	0.007	0.011	0.170	0.270
D	0.618	0.642	15.700	16.300
D1	0.547	0.555	13.900	14.100
E	0.618	0.642	15.700	16.300
E1	0.547	0.555	13.900	14.100
e*	0.016	0.024	0.400	0.600
L	0.018	0.030	0.450	0.750
μ	0.000°	7.000°	0.000°	7.000°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS026

APPENDIX A. MIGRATION FROM A CS4280 DESIGN TO A CS4281 DESIGN

The CS4281-CM is designed to be backward compatible with the CS4280-CM PWB footprint. When the CS4281 is placed in a CS4280-designed board, the CS4281 will provide the same level of functionality as the CS4280-CM. The CS4281 is not be available in the 128-pin TQFP package; however, a 100-pin TQFP package is available for notebook designs. The following descriptions apply only to the 100-pin MQFP package.

Several supply pins have been redefined on the CS4281. The functionality of two additional pins has been modified to support additional features. Modified pin definitions default to CS4280 functionality.

Upgraded Pins

- IRQC (pin 18) – replaced CGND[0]
- IRQB (pin 19) – replaced CVDD[0]
- IRQA (pin 25) – replaced SERR#
- TESTSEL (pin 64) – replaced CVDD[3]
- ASDIN2/GPIO1 (pin 66) – replaced GPIO
- PME# (pin 67) – replaced CGND[4]
- VAUX (pin 68) – replaced CVDD[4]
- CLKRUN# (pin 93) – replaced PCIGND[1]
- GPIO3 (pin 94) – replaced PCIVDD[1]

IRQ[A:C] - ISA interrupt pins

Three pins have been redefined as ISA IRQ signals for DOS legacy game support. For backward compatibility, these pins default to high impedance. Pin 18 will be connected to ground, pin 19 will be connected to VDD, and Pin 25 will be connected SERR#. High impedance pins connected to the supply rail results in no damage or excess current being drawn by that pin. The SERR# pin (25) on the CS4280 has no useful functionality. An audio device has no condition whereby it must generate a system error. The SERR# pin on the CS4281 has been eliminated. Pin 25 is held in a high impedance state by power-on default.

TESTSEL - Test Mode Select pin

Pin 64 was formerly a supply pin (CVDD[4]). This pin is designated for selecting test modes for production testing. This pin must be left floating or tied to a core power supply pin for normal operation. This pin is tied to CVDD on the CS4280 PWB layout.

ASDIN2/GPIO1 - Secondary Codec Data In / General Purpose I/O Pin

The ASDIN2 function is added to the GPIO pin. The function is determined by the AC-Link configuration setup. The power-up default is the GPIO functionality.

PME# - PCI Power Management Event

The PME# is a new function added to the CS4281. It is an open drained output used to indicate a power management event. For the CS4280 layout, this pin will be grounded.

VAUX - PCI Auxiliary Power Supply

VAUX maintains limited device functionality when the normal VDD is turned off in the CS4281. When the CS4281 is used on the CS4280 layout, this pin will be tied to normal VDD.

CLKRUN# - Optional System Clock Control

CLKRUN# is an optional PCI signal defined for mobile operations and is only available on the CS4280-CQ (128-pin package). This pin is redefined from supply ground to an input with an open drained output. If maintained at a logic 0, the open drained output is never required to drive the CLKRUN# signal. In the CS4280 layout, this pin will be tied to ground. Note: CLKRUN# is not available on the add-in card connector

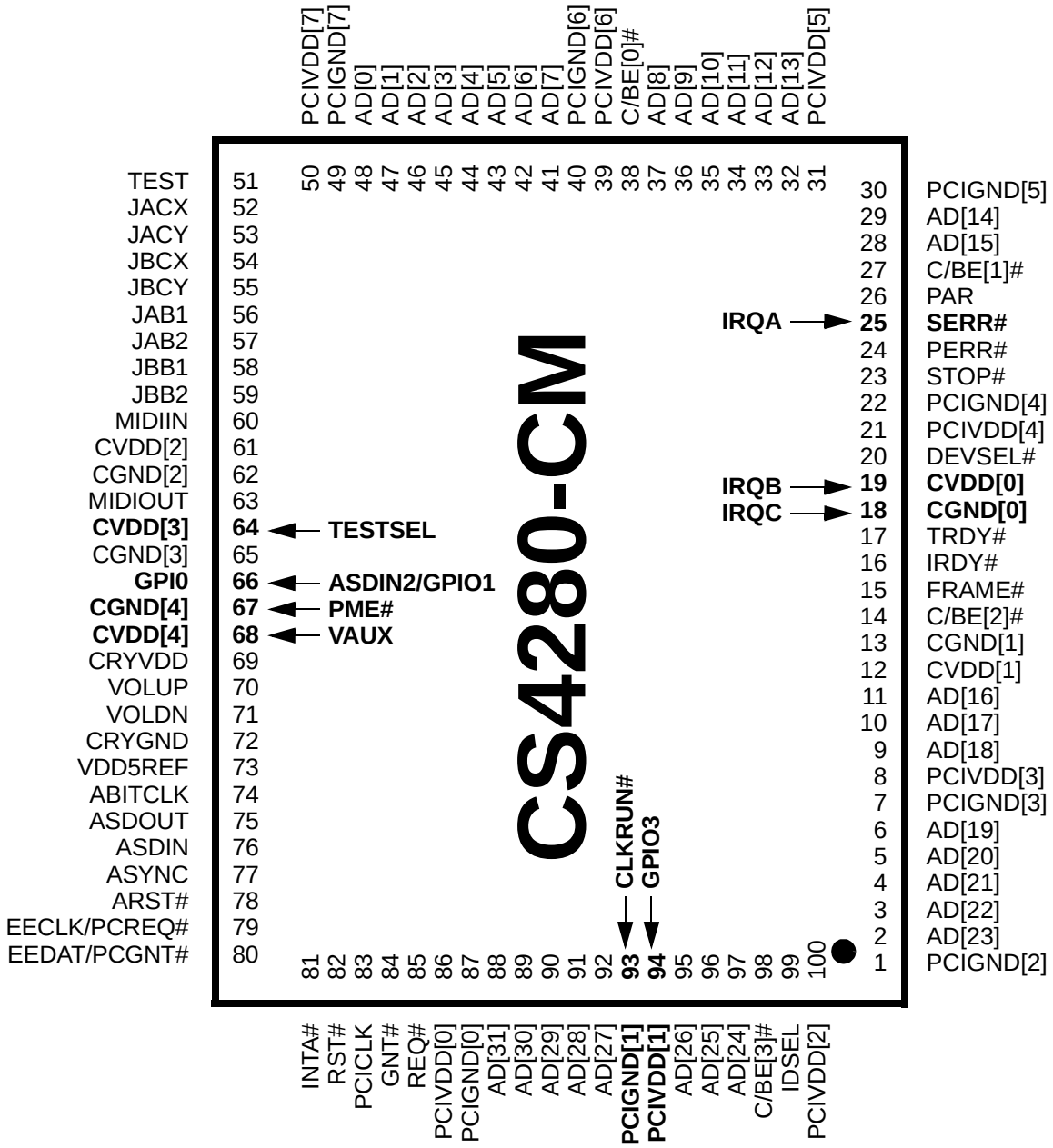
GPIO3 - General Purpose Input/Output 3

GPIO3 pin of the CS4281 powers up high impedance. High impedance pins connected to the supply rail results in no damage or excess current being drawn by that pin.

Summary

The new features included in the CS4281 (CLKRUN#, VAUX, TESTSEL, and ISA IRQs) are not usable when the CS4281 is placed in a CS4280 PWB footprint. The CS4281 maintains the same functionality as the CS4280 from a user perspective. The CS4281 is NOT backward compatible with the CS4280 software drivers. A driver upgrade is required to use the CS4281. The upgraded driver will contain support for both the CS4280 and the CS4281 for those customers that have both devices in their product lines.

For new applications migrating from the CS4280 to the CS4281, several design considerations need attention. Joystick coordinate capacitor values should change from 5.6 nF to 12 nF to more closely approximate legacy game port timing; however, the CS4281 does approximate the CS4280 timing. The CS4281 does not support ZV-Port found on the 128-pin version of the CS4280. Full PME capabilities are available on the CS4281 with the support of Vaux and the PME# functions. CLKRUN# only available on the 128-pin version of the CS4280 is now available on either the 100-pin MQFP or 100-pin TQFP CS4281. The CS4281 also supports up to two AC ‘97 Codecs that support the Audio Codec Specification 2.1 extensions.



• Notes •